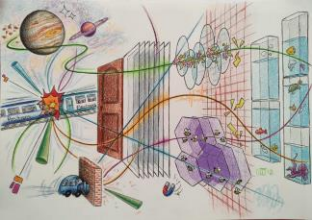


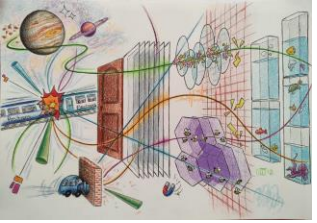
DRD3

DRD3 collaboration
(R&D on Silicon Detector Technologies)

Gregor Kramberger on behalf of the collaboration

Jožef Stefan Institute, Slovenia

JSI
Ljubljana
Slovenia
Slovenian Research Agency



Motivation

非常感謝您的邀請
...以及更多款待

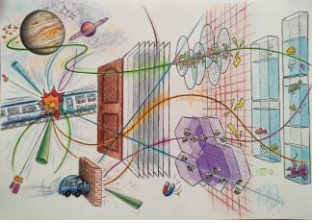
Presentation of the DRD3 as a platform for collaborative R&D on semiconductor sensors for future experiments

A flash-review of where we are, what we do, (no real details) and where future R&D will likely go.

Much more details can be found in the presentations from:

- Status of DRD3 WG1/WP1 – monolithic - was presented by Eva Villea (Thursday session)
- Status of DRD3 WG2/WP2 – hybrid - was presented by Alessandro Tricoli (Thursday session)
- Many presentations dedicated to specific topics included also collaborative efforts (Thursday and Friday Si-Det sessions)

The whole DRD framework was presented by Thomas Bergauer on Wednesday.

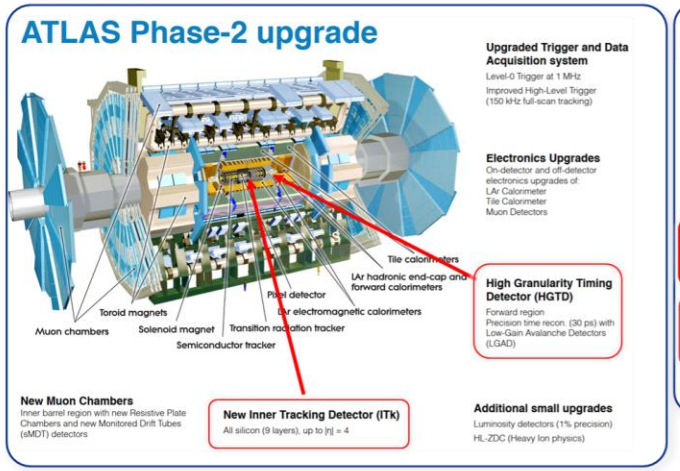


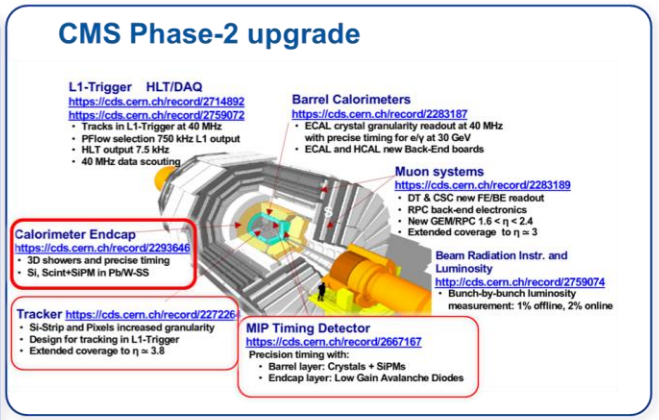
Silicon detectors

Remarkable challenges were over come in the last decade for the LHC upgrade!

- **Radiation hardness** at levels not imagined decades ago (few 10^{16} n cm^{-2}, tens of MGy) - 25x100, 50x50 μm^2 cells
- Not only the position but precise timing (~30 ps) resolution should be measured for the particle collisions **Endcap Timing detectors** for ATLAS and CMS (4D tracking)
- **Superb resolution at low mass** (ALICE ITS)

Coming after the accelerator upgrade in 2029





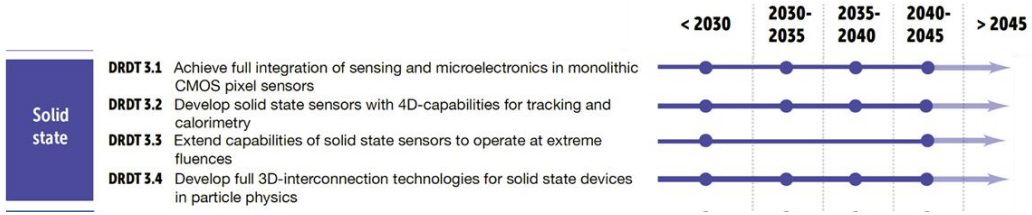
…also very close collaboration with LHCb!

New Major Challenges for the future:

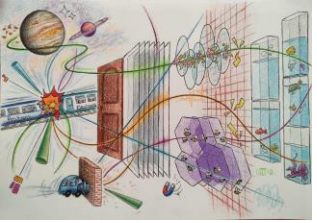
- FCC-ee/CEPC: Vertex detectors with low mass, high resolution (Target per layer spatial resolution of ≤ 3 µm and x/x0≤ 0.05%),
- FCC-hh/SppC: low power and high radiation hardness (up to $8 \cdot 10^{17}$ $n_{eq} cm^{-2}$). Resolving many pp hits in a bunch by ultra-fast timing in O(10-100ps)
- Full integration with electronics, mechanics, services

Large area sensors at low cost for calorimetry

European Commission for Future Accelerators
Road map document on sensors

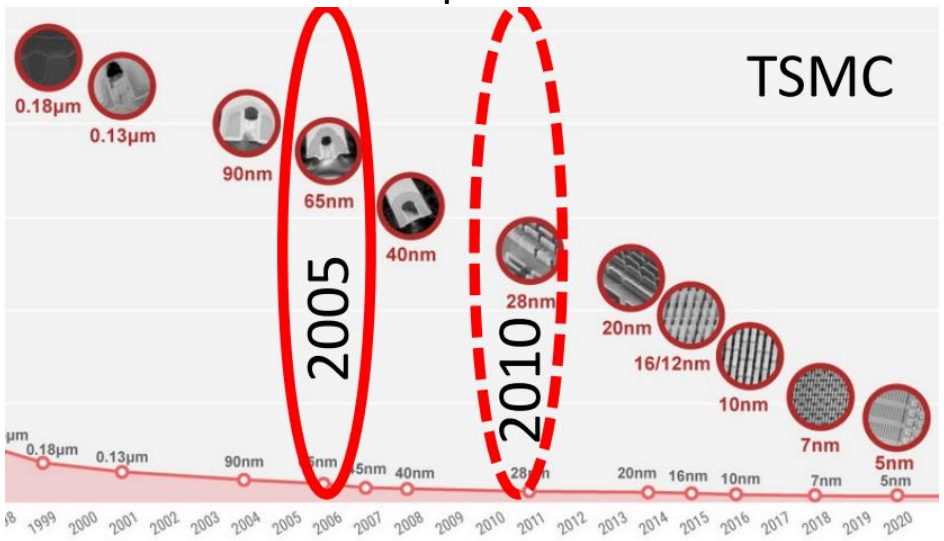


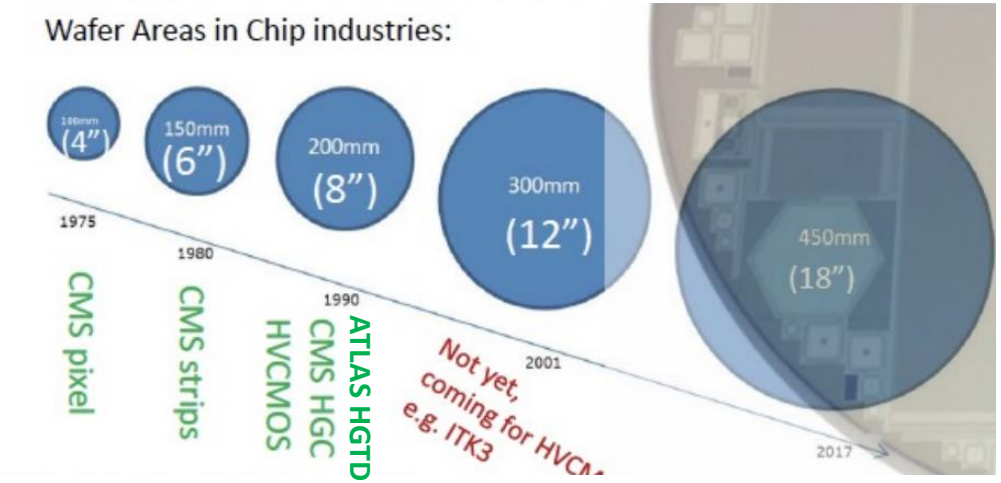
ECFA Detector R&D roadmap [CERN CDS]



Evolution of Si particle sensors

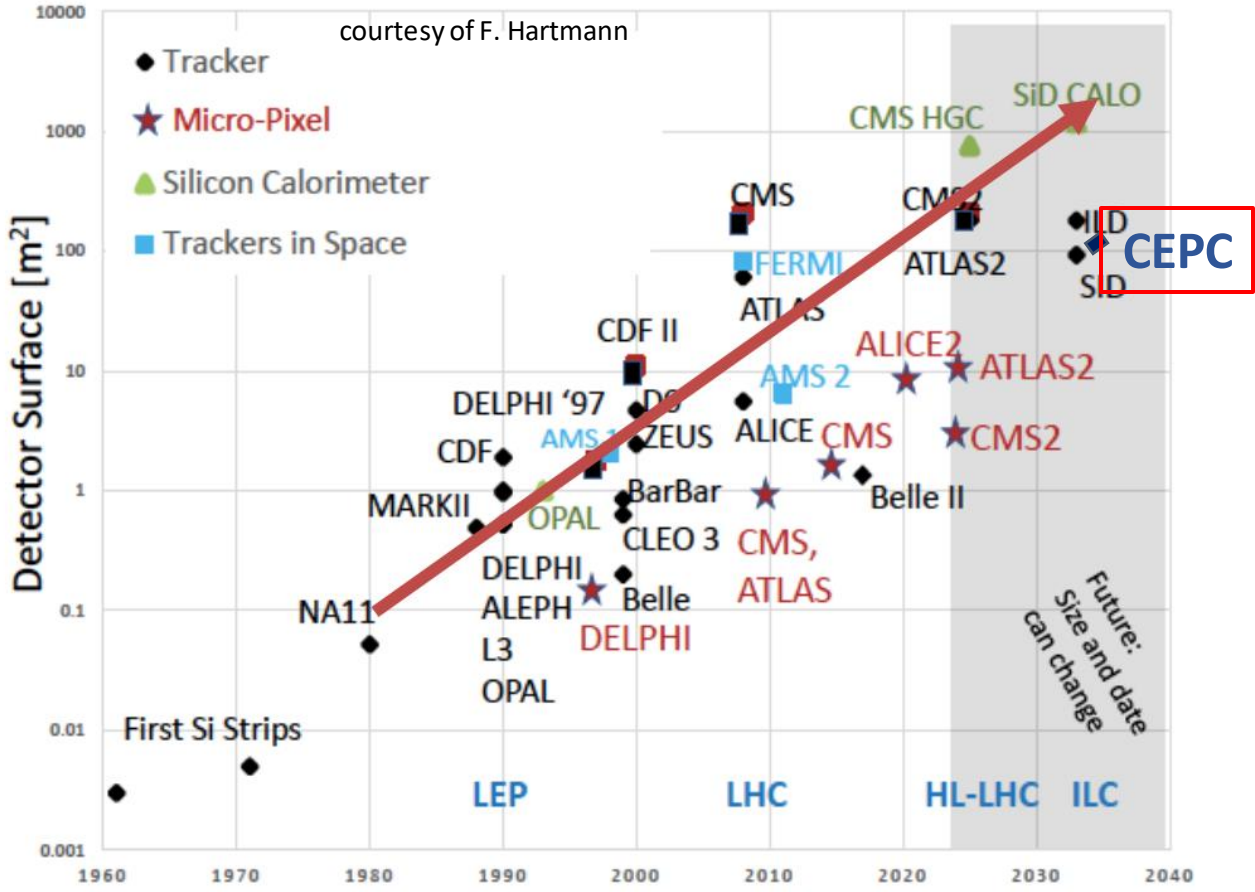
Remarkable success in HEP enabled by significant advancements in chip industries.

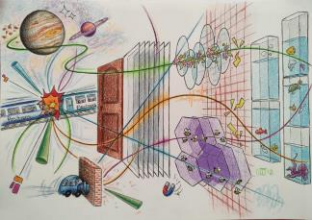




Huge growth of semiconductor particle detectors in various fields

Detector area increased by one order of magnitude each decade (1 m^2 → 10 m^2 → 200 m^2 → 600m^2)

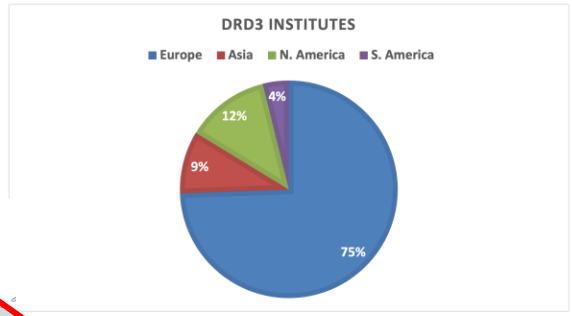


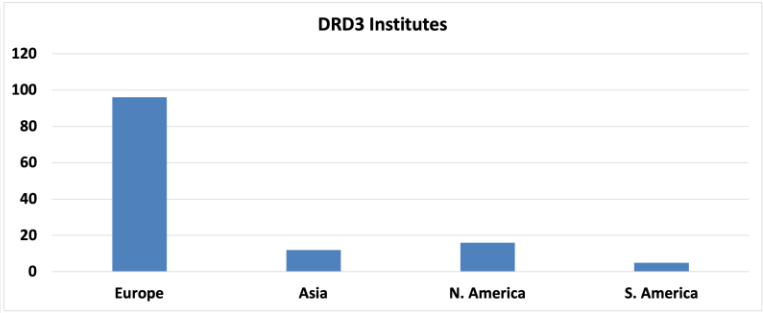


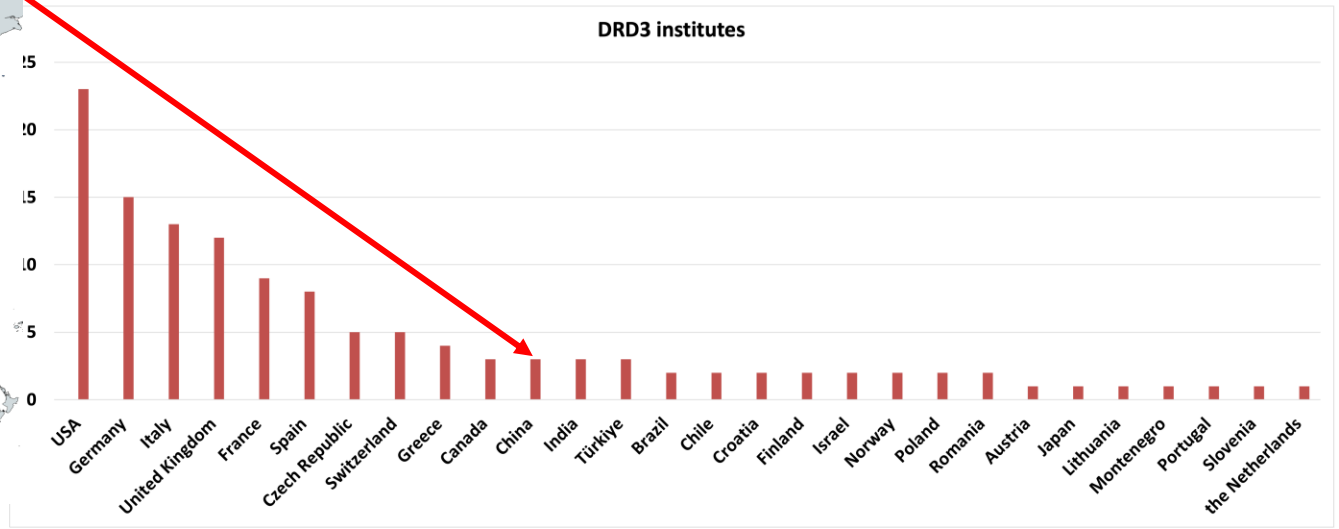
The DRD3 collaboration

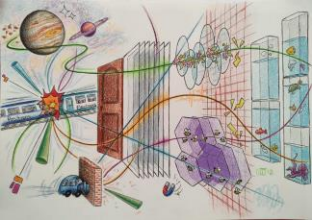
A large collaboration on semiconductor has been formed at CERN to guide and steer the developments of semiconductor sensor developments in the next decades. **143 Institutes currently involved with 700+ people**

Institute of High Energy Physics, CAS, IHEP
Ludong University
Jilin University
University of Science and Technology of China
Institute of Microelectronics, Chinese Academy of Sciences (IMECAS)
Dalian University of Technology



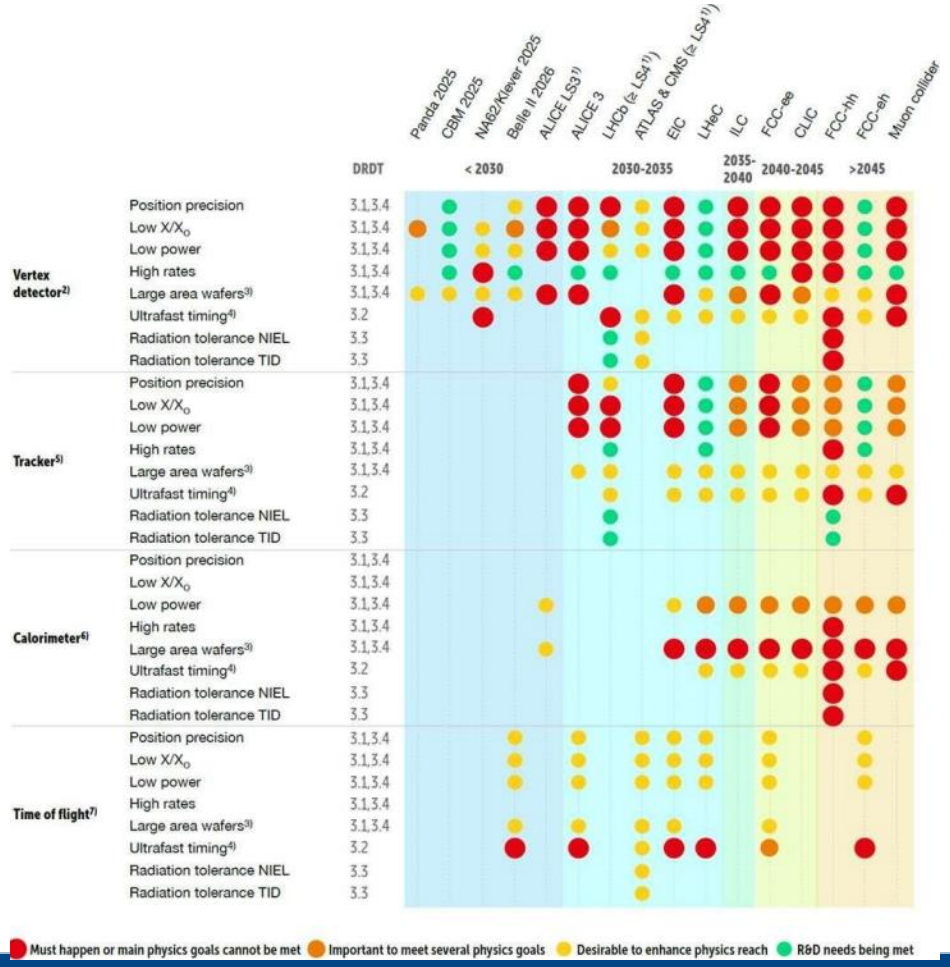


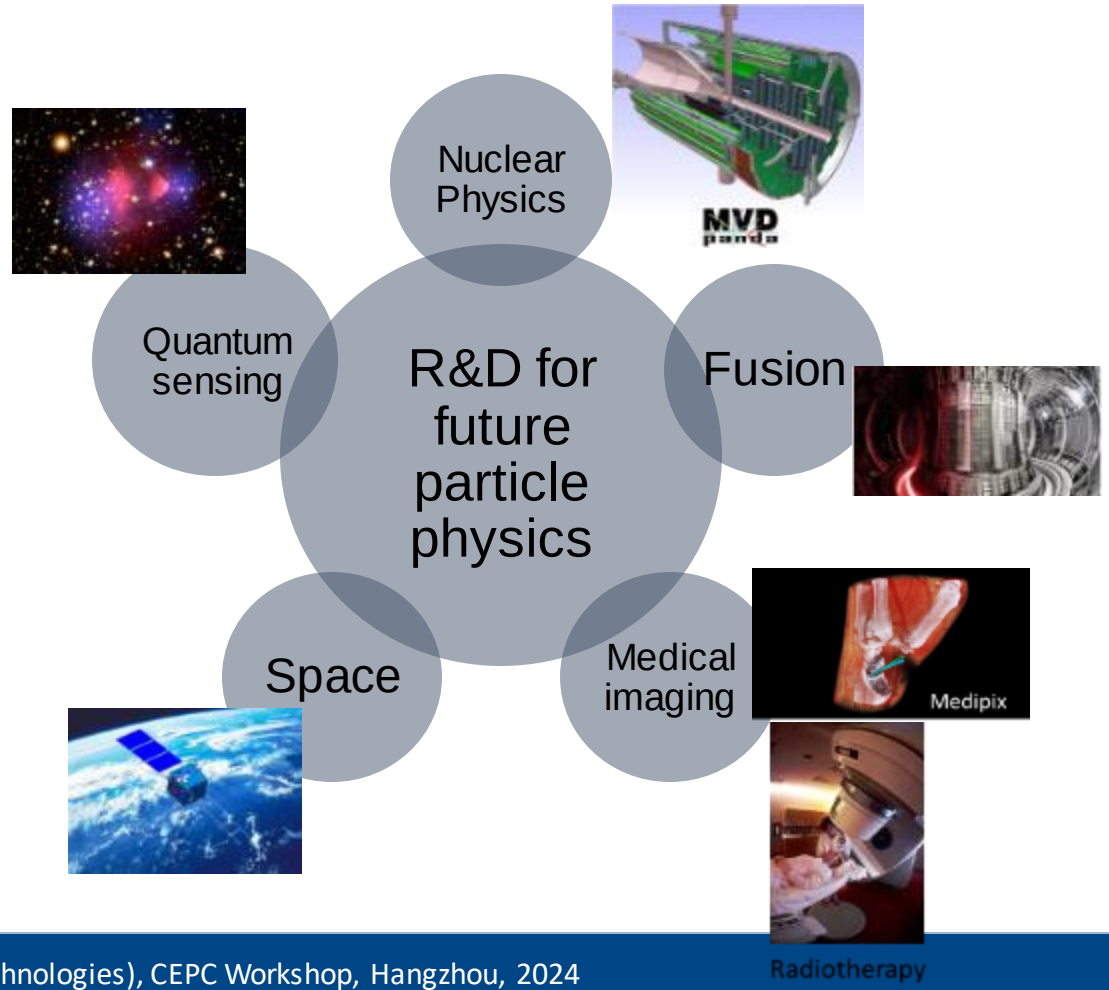


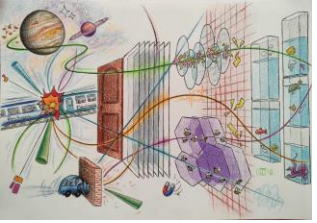


Objectives of the collaboration

The DRD3 collaboration has the dual purpose of pursuing the realization of the **strategic developments** outlined in the ECFA road map and **promoting blue-sky R&D** in the field of solid-state detectors including the synergies with other fields of science where charged particle detection is a key ingredient.







Organizational structure

DRD3

Collaboration board
CB Chair: G. Pellegrini (CNM)
Deputy: R. Arcidiacono (INFN-TO)

DRD3 management
G. Kramberger (JSI) - SP
M. Moll (CERN)-DSP
I. Gregor (DESY)-DSP
S. Seidel (UNM)-DSP

Steering committee:
DRD3 management + CB Chair + WG conveners

DRD3 bodies
- Secretariat/administration
- Resource coordinator /Project office (D. Muensterman, HRM/Lancaster)
- Cross-DRD coordination
  CPAD coordination
- Speakers committee (U. Parzefall - Freiburg)

R&D activities

WG 1	WG 2	WG 3	WG 4	WG 5	WG 6	WG7	WG 8
Convener(s)	Convener(s)	Convener(s)	Convener(s)	Convener(s)	Convener(s)	Convener(s)	Convener(s)
Monolithic silicon technologies	Hybrid silicon technologies	Radiation damage & extreme fluences	Simulations	Characterization techniques and facilities	Wide band-gap and innovative sensor materials	Interconnections and device fabrication	Dissemination & outreach
H. Pernegger (CERN) E. Vilella (Liverpool) J. Baudot (Strasbourg)	A. Macchiolo (UZH) M.v.Beuzekom (NIKHEF) A. Tricoli (BNL)	Ioana Pintilie (NIMP) J. Schwandt (Uni. HH) TBD	*H. Wennloef (DESY)* M. Mandurrino (INFN-TO)	I. Vila (IFCA) B. Hiti (JSI)	A. Oh (Manchester) X. Shi (IHEP) + TBD	G. Calderini (LPNHE) D. Dannheim (CERN) F. Huegging (Bonn)	C. Nellist (NIKHEF) TBD

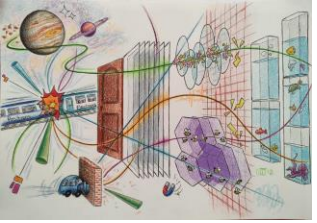
WP1	WP2	WP3	WP4
Leader(s)	Leader(s)	Leader(s)	Leader(s)
Monolithic CMOS sensors	Sensors for 4D-tracking	Sensors for extreme fluences	3D-integration& Interconnections

Strategic/Targeted R&D projects

Scientific proposal
10/2023
Provisional approval
01/2024
Elections of CB chair and SP
02/2024
Nominations of WG leaders
04/2024
Approval by CERN DRDC/RB
06/2024
1st DRD3 week
06/2024

The Work Package preparation for **strategic funding of the R&D**

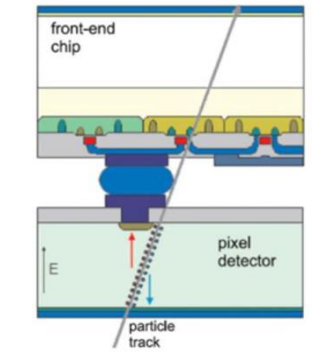
Work Package (WP) = strategic R&D activity and is linked to DRD Tasks. It should pursue the goals listed there.
- o WPs gather a subset of DRD3 institutions, are resource loaded with clear milestones and deliverables and funded
- o WPs reviewed/approved by DRD3 and appended to MoU annex
- o WPs will be shaped and optimized (synergies with similar projects, sharing runs…)



WG2/WP2: Hybrid silicon technologies and 4D tracking

DRD3

By “4D tracking” we mean the process of assigning a space and a time coordinate to a hit - ~10-30 μm position **and ~10-30 ps time resolution** – simultaneously (many benefits in dense particle environment for tracking and PID)

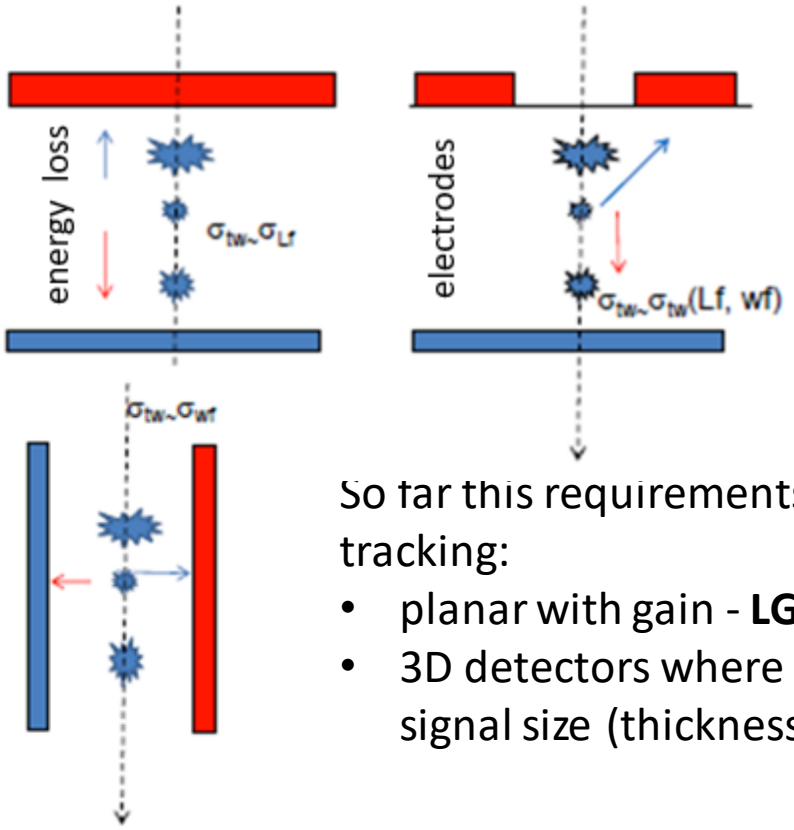


HYBRID

Readout ASIC chip

The sensor

Contributions to the timing for planar and 3D + jitter:

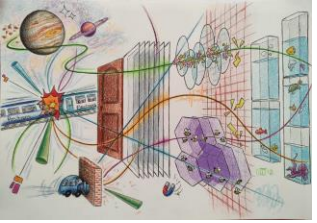


Not possible to achieve goals in planar technology without gain!

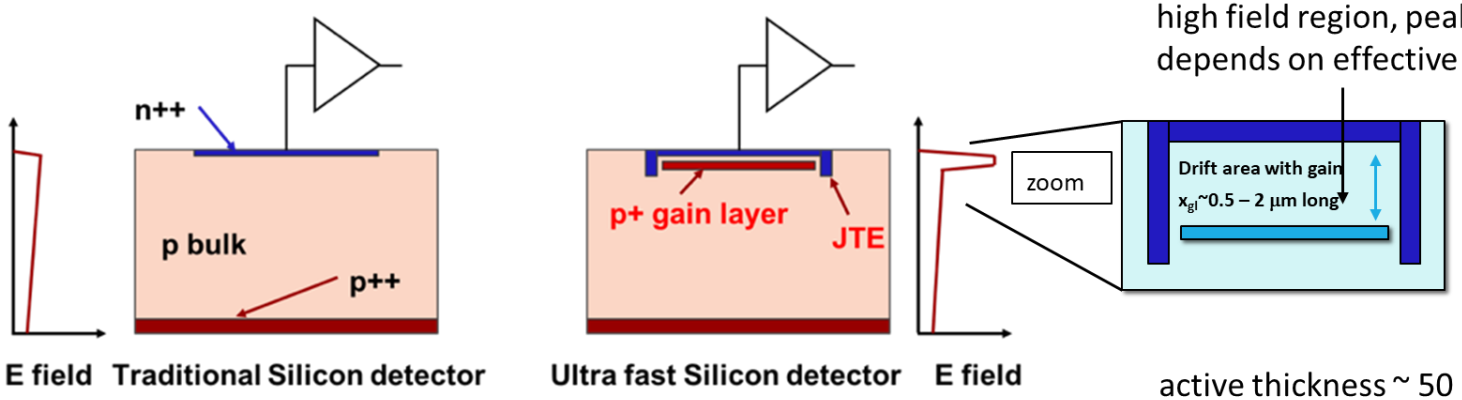
So far this requirements lead to two solutions for 4D tracking:

- planar with gain - **LGAD detectors**
- 3D detectors where drift time/rise time and signal size (thickness) are decoupled

WG2 research goals <2027	
	Description
RG 2.1	Reduction of pixel cell size for 3D sensors
RG 2.2	3D sensors for timing (50 × 50 μm, < 50 ps)
RG 2.3	LGAD for 4D tracking < 10 μm, < 30 ps, wafer 6” and 8”
RG 2.4	RSD for ToF (Large area, < 30 μm, < 30 ps)



WG2/WP2: LGADs



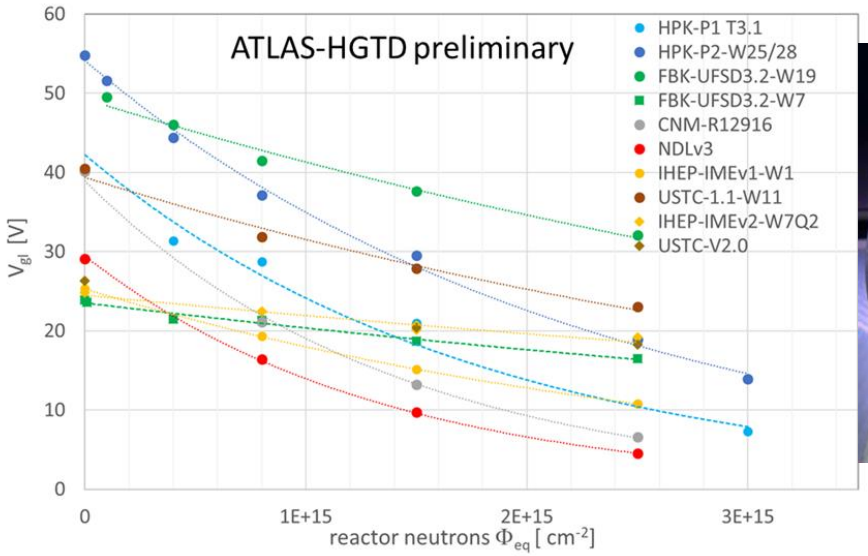
Typically 25-50 µm thick with signals of 20fC (G~40)

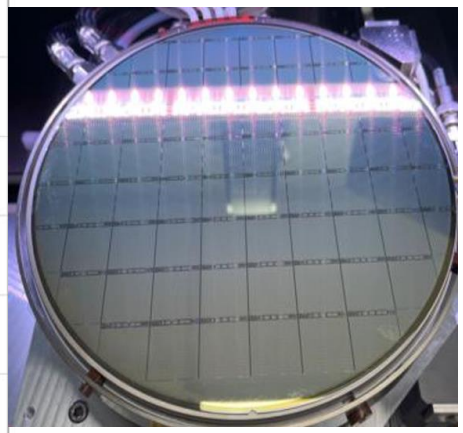
Limitations for conventional LGADs:

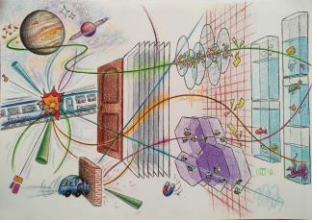
- Fill factor (large cell devices) due to JTE
- Radiation harness – **currently to ~3e15 cm^{-2}**

Radiation hardness:

- C-enrichment of the gain layer (prevention of B removal – reduction of the field) - IME (USTC&IHEP) mastered the C-enrichment and has so far produced most radiation hard sensors for ATLAS-HGTD – is there still room for improvement?
- Compensated LGADs – use of compensated p+ silicon in gain layer which if carefully tuned would not suffer from reduction of negative space charge with irradiation (both P and B are removed)
- Thermal treatment >200°C reactivation of space charge







WG2: LGADs different flavors

Several technologies were proposed and are investigated to overcome fill factor problem:

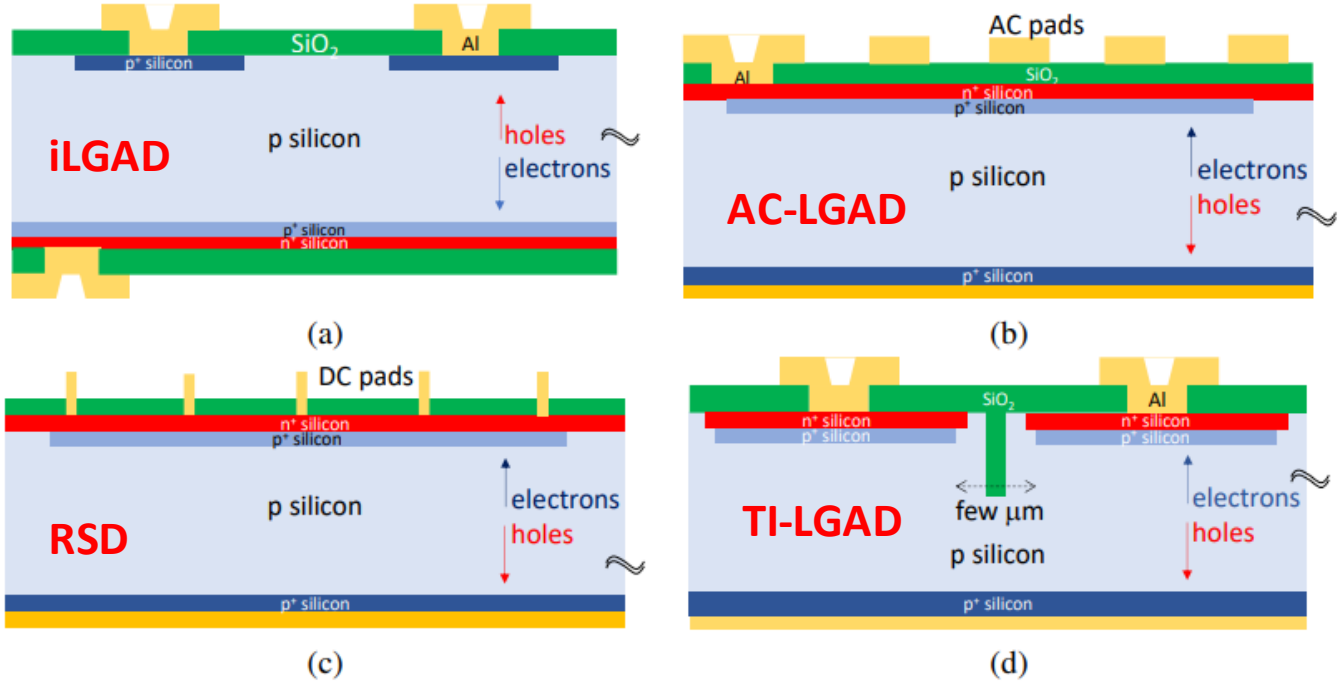
iLGAD – segment the side without multiplication no p-stop, JTE at the bottom (**complex processing, radiation hardness, hole collection**, ideal for high rate)

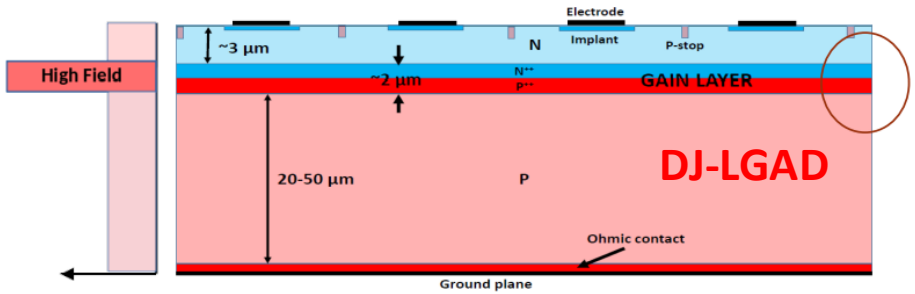
TI-LGAD – use SiO_2 trenches to isolate the pads, reducing the gap by an order of magnitude (C-enriched produced)

AC-LGAD / RSD– use AC coupling – bipolar signals:

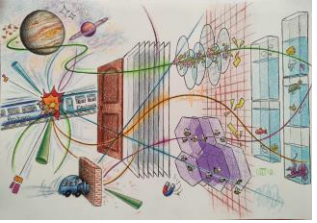
- superb spatial and time resolution (order of magnitude better than pitch)
- **rate limited, radiation hardness**

DJ-LGAD





LGADs are the only planar technology good enough for precise timing (<50ps), but excellent electronics is needed. **(marriage of LGAD + CMOS looks promising – DJ-LGAD, MONOLITH)**



WG2/WP2: 3D detectors

3D technology as timing detectors:

- They have fill factor ~100% (inclined tracks)
- The radiation tolerance of small cell size devices is large (for signal) and allows operation at higher bias voltages – shown up to ~1e17 cm^{-2}
- Technology is already mature-latest 3D detectors are done in single sided processing!

Challenges:

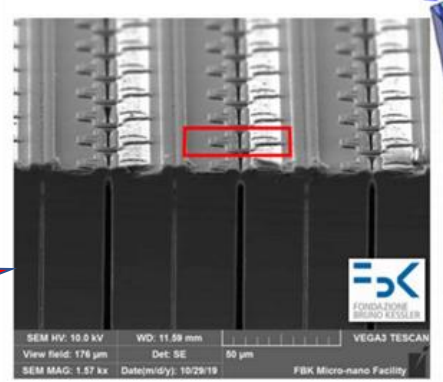
- the capacitance will be much larger (hence noise and the jitter) particularly for thick sensors with large signals (very narrow columns/trenches -> 100:1 at IME) – noise and jitter
- scalability of the processing -> 8”
- clustering issues for small cells
- marriage of LGAD and 3D - complex filling of the holes?

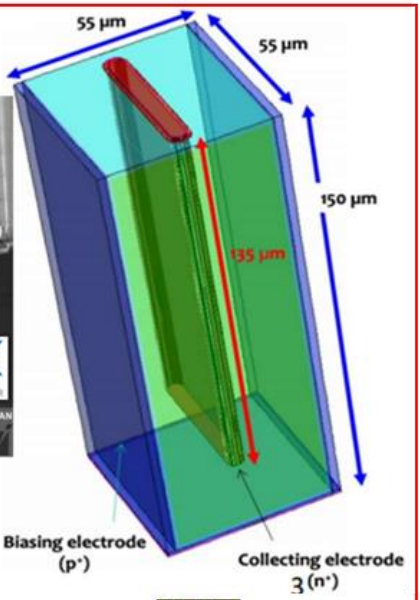
Trench 3D

(INFN – FBK)

3D silicon detectors

<30 ps mips

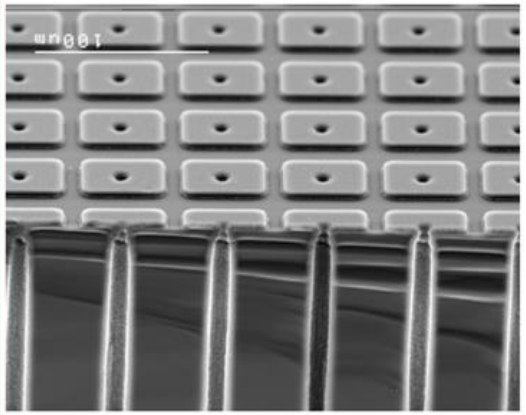


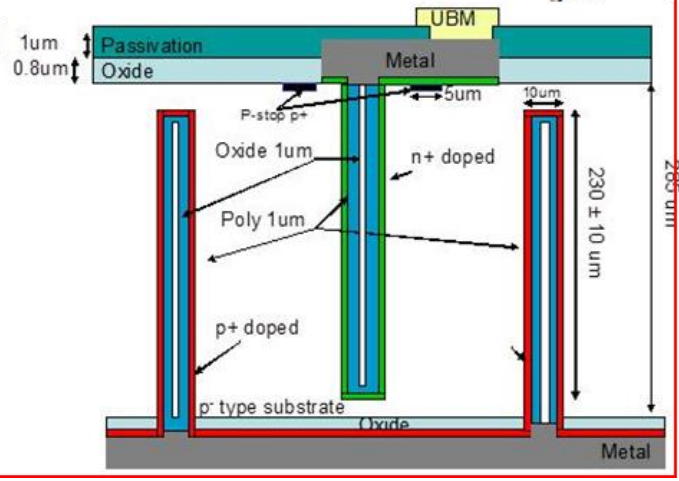


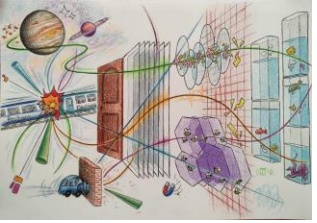
TimeSPOT

Column 3D

(CNM/FBK/Sintef/IME…)





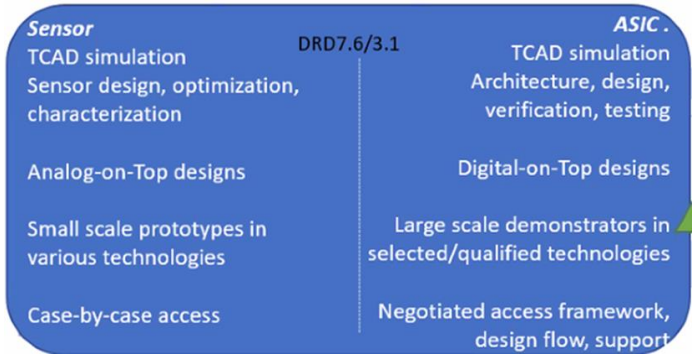


WG1/WP1 Monolithic silicon sensors

<u>Aim</u> is to advance the performance of monolithic CMOS, combining sensing and readout elements, for future tracking applications, tackling the challenges of:

- very high spatial resolution;
- high data rate;
- high radiation tolerance;
- low mass;
- covering large areas;
- reducing power;
- keeping an affordable cost;
- **and ultimately combining these requirements in one single sensor device.**

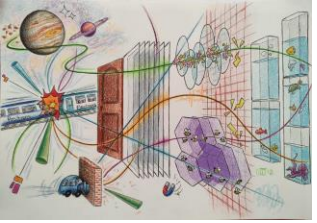
Program shared between DRD3/7



WG1 research goals <2027	
	Description
RG 1.1	Spatial resolution: ≤3 µm position resolution
RG 2.2	Timing resolution: towards 20 ps timing precision
RG 1.3	Readout architectures: towards 100 MHz/cm^2, 1 GHz/cm^2 with 3D stacked monolithic sensors, and on-chip reconfigurability
RG 1.4	Radiation tolerance: towards 10^{16} n_{eq}/cm^2 NIEL and 500 MRad
RG 1.5	Low-cost large-area CMOS sensors

We will have several MPW and engineering runs in 65-180 nm technologies (LF, Tower, AMS, TPSCo)

Maurice Garcia-Sciveres and Norbert Wermes 2018 Rep. Prog. Phys. 81 066101
Peric I 2007 , Nucl. Instrum. Methods A 582 876–85



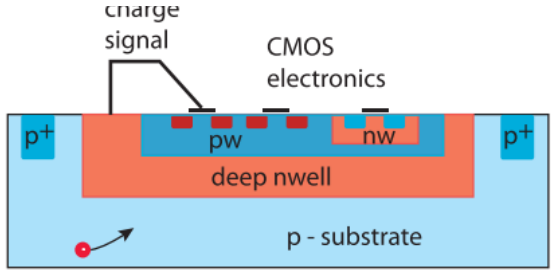
WG1/WP1 – main challenges

DRD3

taken from N. Wermes

LARGE ELECTRODE DESIGN

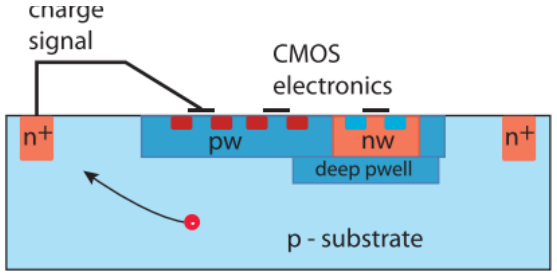
$\tau \propto \frac{C}{g_m}$, $ENC_{thermal} \propto \frac{kTC}{g_m}$ compensated by power (g_m)



- Large electrode: $C \approx 300$ fF
- Strong drift field, short drift paths, large depletion depth
- Higher power, slower
- Threshold $\sim 2000\ e^-$

Timing: large jitter and small distortion component - ~100 ps

SMALL ELECTRODE DESIGN

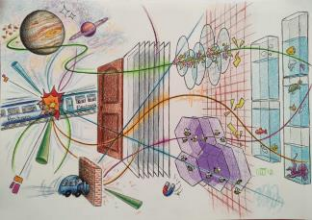


- Small electrode: $C \approx 3$ fF
- Low analogue power
- Faster at given power
- Difficult lateral depletion, process modifications for radiation hardness
- Threshold $\sim 300\ e^-$

Timing: small jitter and large distortion/landau component ~ 1ns

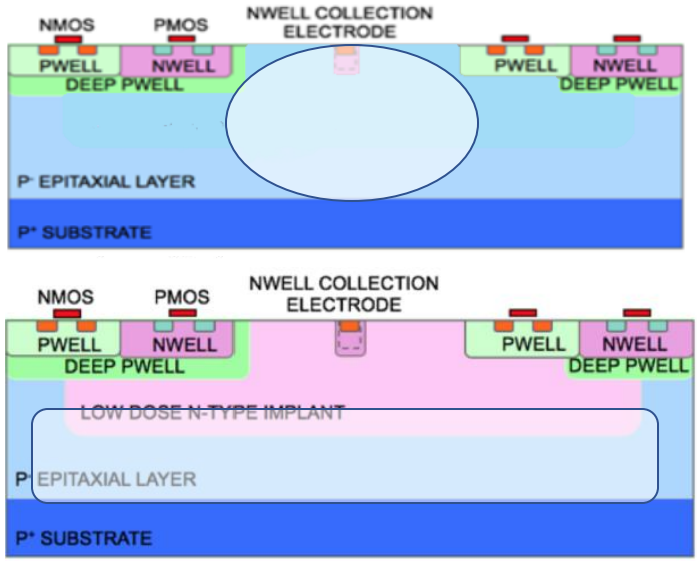
Main challenges (from DRD3 point):

- availability of the active volume (60-80 e-h/μm)
  - epitaxial layer decreases with smaller node processes (350 nm->28 nm). Also, the lateral drift becomes even bigger problem for thin epitaxial layers.
  - few foundries are/will be open to use high resistivity substrate wafer
- costs increase rapidly with the smaller node (MPW runs may not be available)
- allocating the vendors that are open to our needs
  - minimum information about the process which allows for simulation of particle detection in the devices.
  - adaptation of the process
- accessibility to the processes – licensing (process development kits - PDK)
- requirements of additional processing (back side processing), back side metallization …



An example of advances in the design MALTA (Tower Jazz 180 nm process)

W. Snoeys et al., Nucl. Instrum. Meth. A 871 (2017) 90.
H. Pernegger et al 2023 JINST 18 P09018



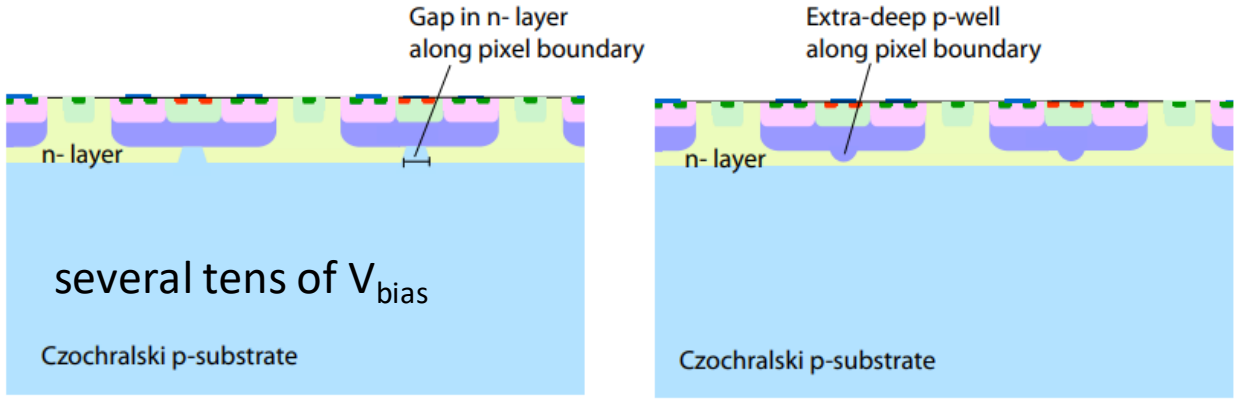
Standard (few V)

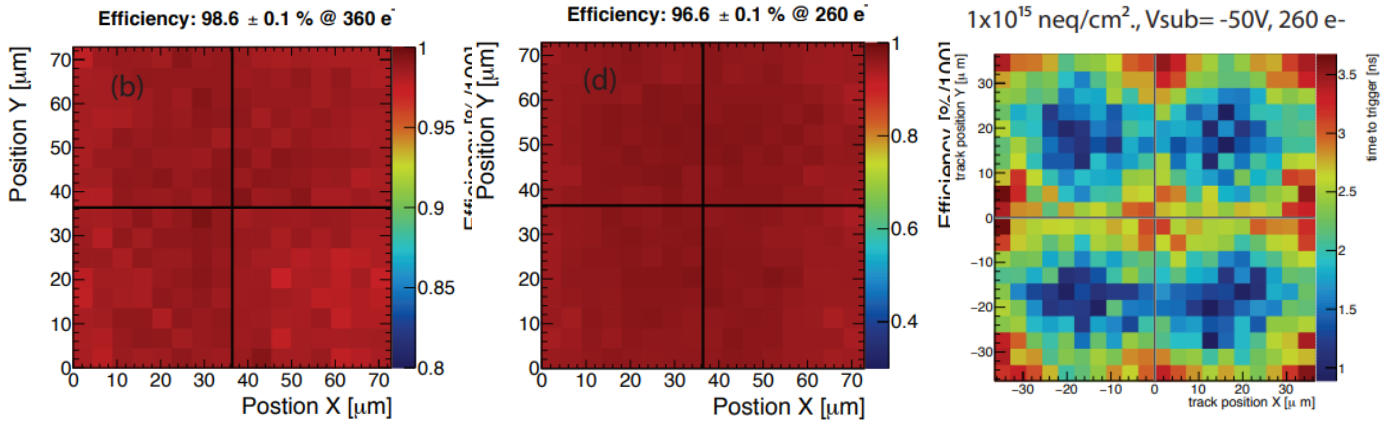
Modified implant (lateral collection)

Figure 1. Improved pixel design with n-gap [8]

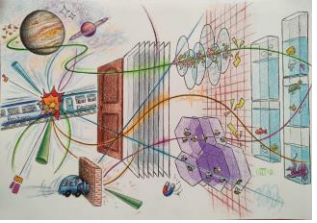
Modified implant – additional notch

MALTA-Cz – high resistivity substrate





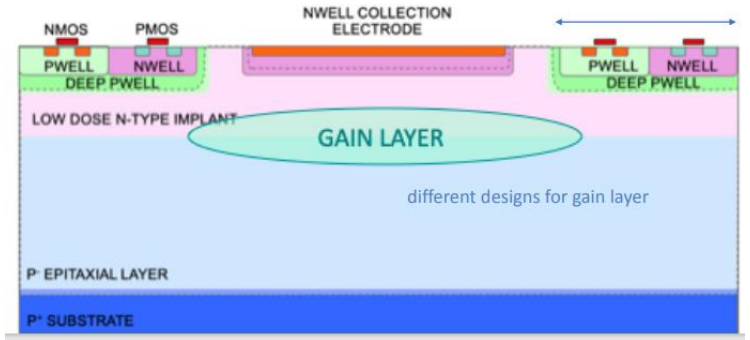
- good efficiency over the pixels even after 3e15 cm^{-2}
- ToA distribution shows differences in signal speed ~2 ns resolution



Future advances – CMOS with gain

- CMOS sensor with gain – can the process be modified in the way that you create an internal gain structure
  - faster rise time and better S/N - better timing
  - better position resolution
  - less power consumption
- Examples of different approaches to reach gain layer multiplication (small electrode design seems more suitable)

Cassia (DRD3 WP1 project)

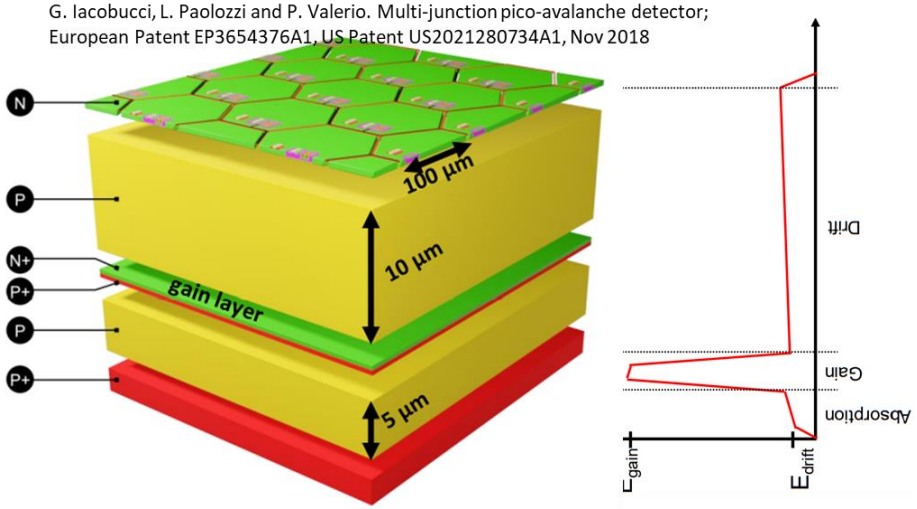


"deep junction" gain layer design

- TJ180 conventional LGAD

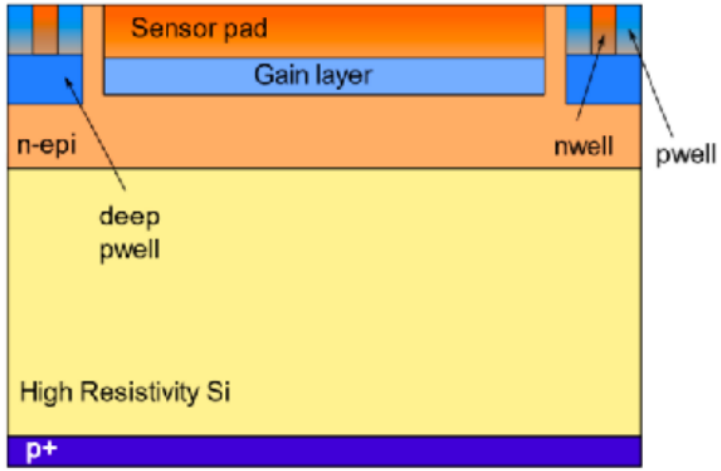
PicoAdd SiGe130 nm (Uni-Geneve)

G. Iacobucci, L. Paolozzi and P. Valerio. Multi-junction pico-avalanche detector; European Patent EP3654376A1, US Patent US2021280734A1, Nov 2018

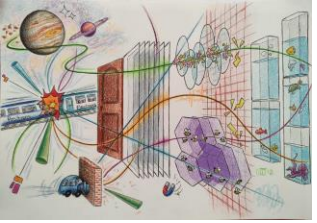


- SiGe bipolar amplifiers – fast (good timing)
- CMOS for digital electronics (monolithic)
- Gain-layer removed from the surface allowing very good spatial resolution without dead area

ARCADIA LF110 nm (DRD7.6)

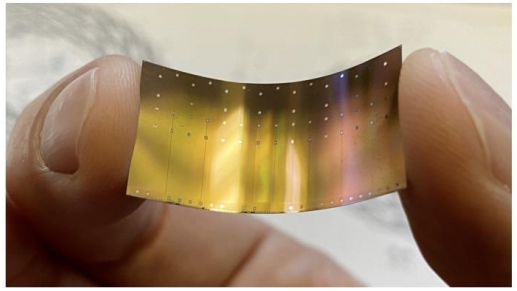


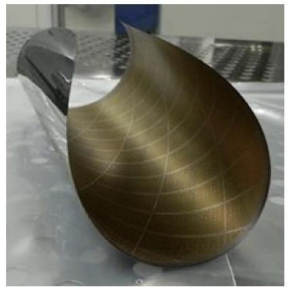
- Back side processing
- High-field grows from the back side

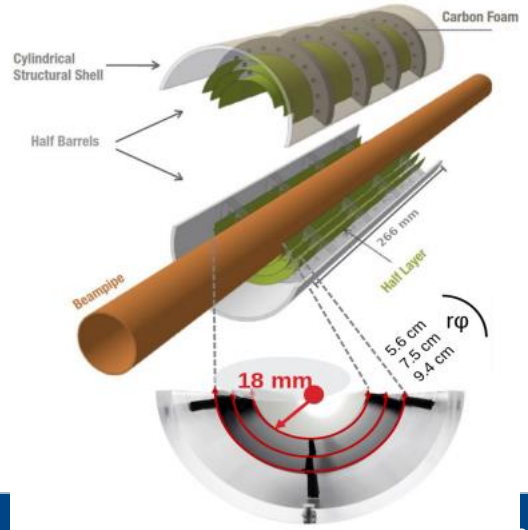


Future advances – scaling up

- Chip-Chip transmission and serial powering
- Stacking up the wafers – better electronics
- **Large-scale reticle stitching of thinned foldable MAPS**

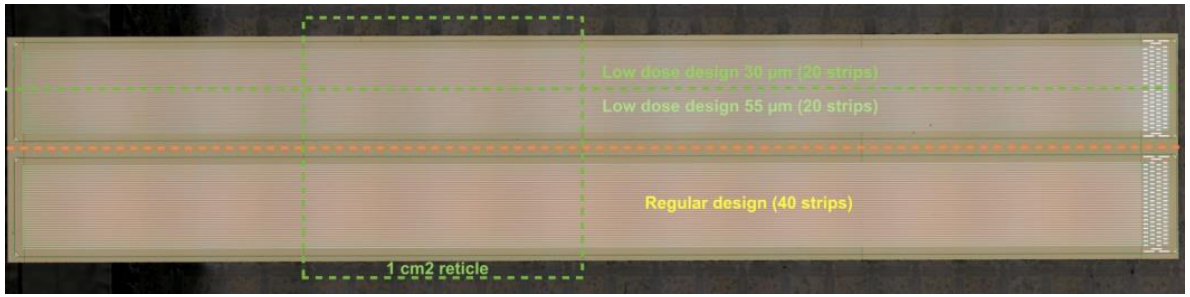




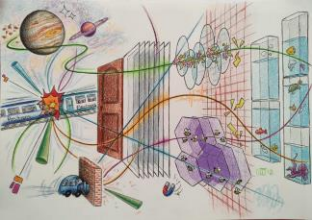


- **Large area strip sensors**
  - Reduced material budget
  - Easier integration
  - Potentially low cost and availability

Monolithic CMOS Strip Sensors for large area detectors
(Dortmund, Freiburg, DESY, Bonn)
LFA150 nm - Resistivity of wafer: >2000 Ω·cm



Next step is implementation of the FEI4 like readout per strip



WG3/WP3: Radiation damage characterization and sensor operation at extreme fluences

DRD3

- WG covers 3 main areas around radiation hardening (see below)
- WG closely related to all other WGs

WG4: Simulations

Need for simulations in all areas

- on the material level
  Geant4, TRIM, NIEL, DFT, KMC, …
- on the device & system level
  TCAD, AP2, Signal & MC simulators, generic sensor parameter simulations (e.g. Hamburg model)
- extrapolation to extreme fluences
  do models still deliver reliable results?

WG5: Characterization techniques

Need for tools in all areas

- on the material level
  EPR, FTIR, PL, DLTS, TSC, …
- on the device & system level
  TCT, CV, IV, IBIC, test-beams, ….
- extrapolation to extreme fluences
  which tools still deliver reliable results?
  radiation facilities,…

WG3: Radiation Hardening

Radiation hardening of material
understand fundamental damage process, defect formation, impact of defects on device performance (also non-silicon!), material and defect engineering

Radiation hardening of devices and systems
understand device operation with radiation damage, device engineering

Extreme fluences
understand physics, possibilities for operation of detectors

WG6: Non-silicon based detectors

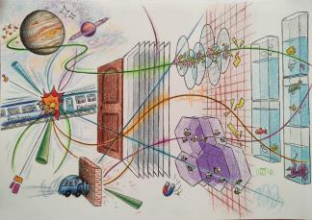
- Material & devices to be studied and understood as silicon in terms of radiation damage in all areas (simulations, material/sensor characterization, tool development)
- Developments for extreme fluence

WG1 & WG2: Silicon based detectors

- Radiation hardness evaluation of all sensors with exposure to radiation (existing and newly developed sensors/sensor concepts)
- Developments for extreme fluence

Synergies with other application areas in radiation fields

- Detectors for nuclear physics, space applications, fusion, medical applications, …



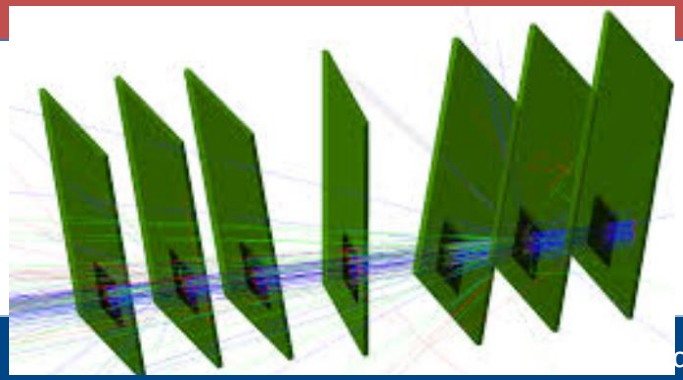
WG 4: Simulations

- Simulations are essential for planning, understanding the performance and designing of devices.
- Simulations WG will provide the tools that could be (easily) implemented to simulate any specific detector or measurement.

"Monte Carlo"
(predicting the performance of complex detector assemblies)

AllPix2 / Garfield++ as the main tool
complement by other ones (also RASER)

GOALS:
- Implementation of improved semiconductor models (e.g. mobility, impact ionization, trapping …)
- Adaptation of WBS sensors
- Adaptation of dynamic /adaptive E, E_w
- Implementation of common electronics/digitization



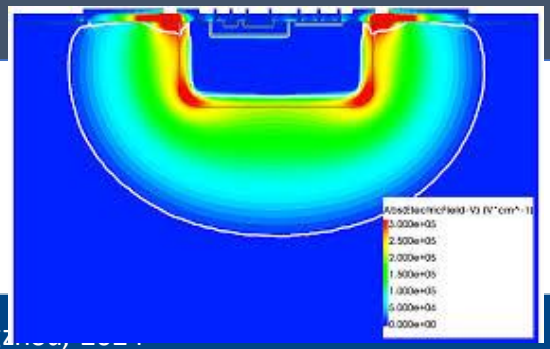
GEANT4

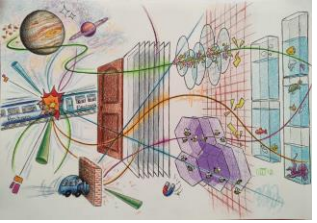
E, E_w

TCAD
(understanding the sensors)

Synopsis, Silvaco …

GOALS:
- Developing and verification of damage models (effective and defect based)
- Establish how to benchmark/evaluate the models against the measured properties (important milestone)
- Improving the TCAD with new findings (WBS, extreme fluences)
- Develop a flexible framework to simulate performance of different processes (CMOS)



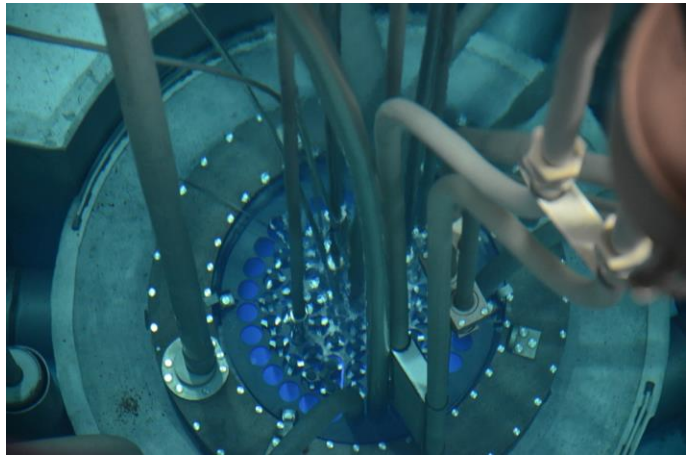


WG5: R&D on new techniques, common infrastructures, and characterization facilities

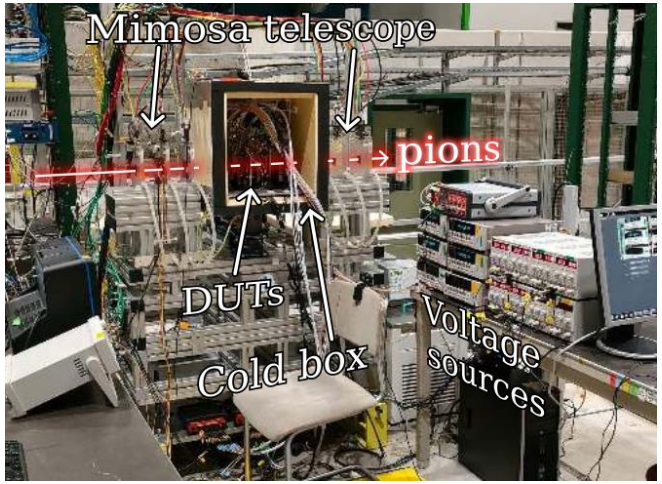
DRD3

- **WG lines of actions:**
  - Development/improvement/diffusion of **methods and techniques for characterizing sensors** (those for defects spectroscopy DLTS,TSC, EPR…. as well those for characterization TCT, Beta-scope…)
  - Joint research activities for the **delivery of common infrastructures for sensor testing** (common sensor readers, jigs, test fixtures,…)
  - Promoting the **use of unique characterization facilities.**

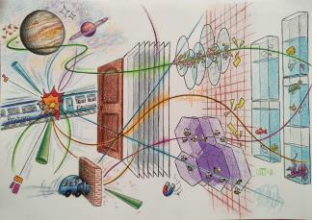
Irradiation facilities (e.g. JSI reactor)



Test beam activities (CERN/DESY)



fs high intensity laser facilities (ELI Prague, SGIKER Bilbao…)



WG7/WP4: Interconnections

WG conveners: G. Calderini, D. Dannheim, F. Hügging

WG Scope: Sensor mechanical and electrical integration to **low-mass tracking + vertexing systems:**

- **Post-processing** (plating/UBM)
- Sensor to frontend **hybridisation**
  - **In-house single-die**
  - **3d integration (wafer-to-wafer)**
- **low-mass flex PCBs / module integration**

Groups with ongoing work / interest in the different domains

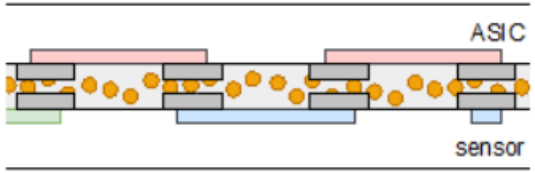
Group	Contact	Ongoing work / topics of interest	Maskless	classical processes	2.5D integr. / modules	3D integration
ANL	Jessica Metcalfe	technologies for large-scale tracking devices	☐	☐	☐	☐
Bonn University*	Fabian Hügging, Jochen Dingfelder	fine-pitch (<50 um) bonding; W2W bonding; in-house hybridisation	☑	☑	☐	☑
CERN*	Dominik Dannheim	In-house plating and hybridisation; compact module studies (including silicon photonics integration)	☑	☐	☑	☐
FBK	Giovanni Paternoster	3d-integration and interconnection of BSI-SiPMs for NUV/VUV; mask and mask-less UBM; W2W temporary bonding; chip-level solder-ball bonding >50 um; wafer-level micro bumps/pillars <50 um; in-house maskless interconnects	☑	☑	☑	☑
Fraunhofer IZM*	Thomas Fritzsch	hybridisation with <=25 um pitch; W2W bonding; wafer-level packaging; single-chip bump bonding for R&D	☐	☑	☐	☑
Geneva University*	Mateus Vicente	In-house flip-chip bonding: gold studs, ACP/ACF, Cu pillars; chip-to-flex	☑	☐	☑	☐
IMB-CNM-CSIC	Miguel Ullán	RDL, TSV, interposers	☐	☑	☑	☐
INFN Bari	Giovanni Francesco Ciani	interconnection between bent sensors; stacking of several CMOS sensors for full 3d tracking	☐	☐	☑	☐
INFN Cagliari	Adriano Lai	in-house single-die hybridisation with innovative bonding techniques such as ACF/ACP	☑	☐	☐	☐
INFN Firenze	Giacomo Sguazzoni, Giovanni Passaleva	Novel interconnection techniques for future applications	☑	☐	☑	☐
INFN Milano	Gianluca Alimonti	Indium bump bonding; in-house die-to-die and die-to-PCB bonding; hybridisation of RSD; multi-chip systems on PCB/bus tape	☑	☑	☑	☐
INFN Trieste	Giacomo Contin	interconnects for bent and ultrathin chips (ALICE ITS3); aerosol jet printing for RDL and contactless interconnects; TSV and wafer-to-wafer for 3D stacking	☐	☐	☐	☑
IPHC Strasbourg	Maciej Kachel	3D integration; small pitch (<10 um) interconnection	☐	☑	☐	☑
IP2I Lyon	Didier Contardo	wafer-to-wafer interconnect demonstrator	☐	☐	☐	☑
KIT Karlsruhe	Michele Caselle	in-house flip chip, gold studs, TSV processing, RDL	☑	☐	☑	☐
LPNHE Paris	Giovanni Calderini	interconnects: ACF, ACP, gold studs; characterisation techniques and devices; reliability testing; new interconnection techniques / scalability	☑	☐	☐	☐
MPG Halbleiterlabor*	Ladislav Andricek, Jelena Ninkovic	direct wafer bonding; 3D/2.5D systems with micro-channel cooling; W2W/C2W bonding	☐	☑	☑	☑
NIKHEF	Martin Fransen	high-frequency ASIC to module integration (RDL, TSV), wire bonding	☐	☐	☑	☐
ORNL	Mathieu Benoit	in-house interconnect for hybridisation and module building: single-chip bumping, UBM, bonding; gold studs, ACP/ACF, Cu pillars; chip-to-flex, chip-to-interposer; interposer fabrication	☑	☐	☑	☐

*groups presenting at DRD3 workshop June 2024

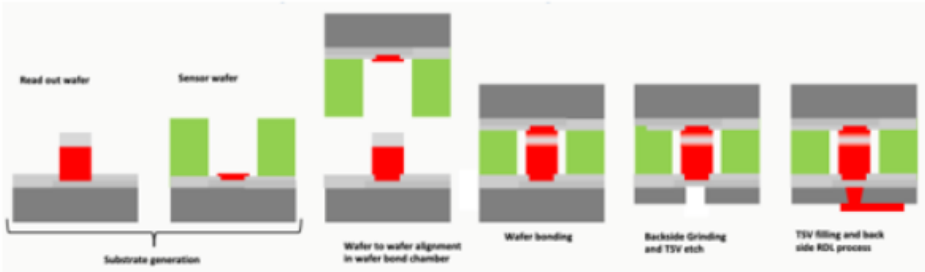
https://indico.cern.ch/event/1402825/sessions/543129

Plating

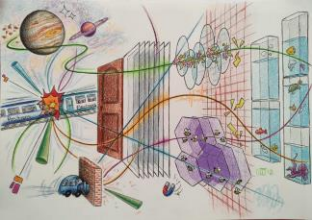
In-house hybridisation



Wafer-to-wafer bonding



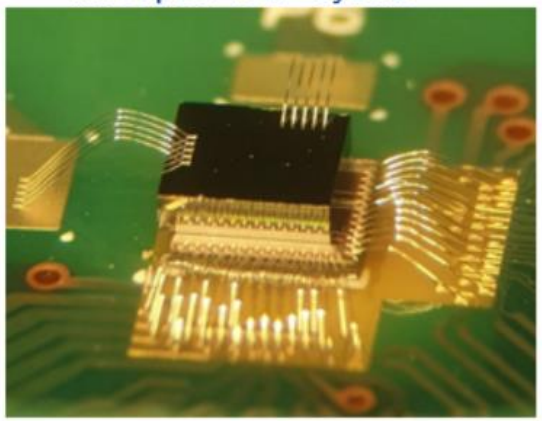
Module integration



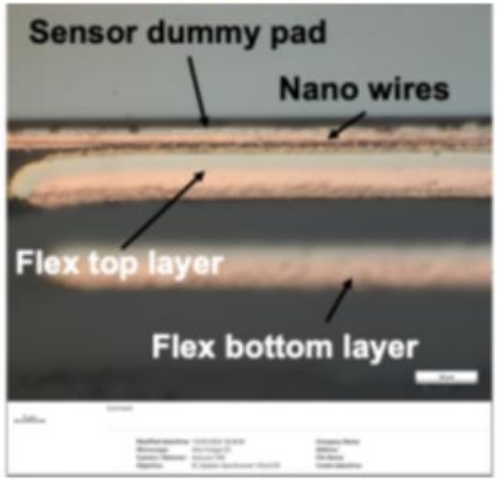
WG7/WP4: In house bonding and wafer-wafer

DRD3

Timespot1 ACF hybrid



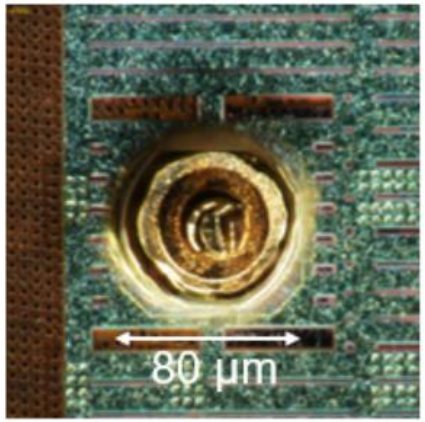
Nanowires on flex



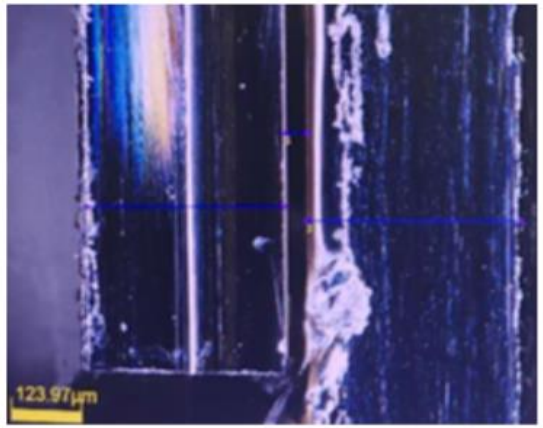
In-house hybridization, module integration

- Exploring innovative **bonding** methods, adapted to the requirements of various projects
  - **Conductive adhesives (ACF / ACP)**
    → good results for <1cm^2 devices and >~50 µm pitch
  - **Nano wires**
    → successful bonding of MALTA2 to flex
  - **Gold studs** + epoxy
    → successfully used for large (>100 µm) pitch
    → developed **low-temperature bonding process** suitable for **irradiated samples**

Gold-stud on ALTIROCA



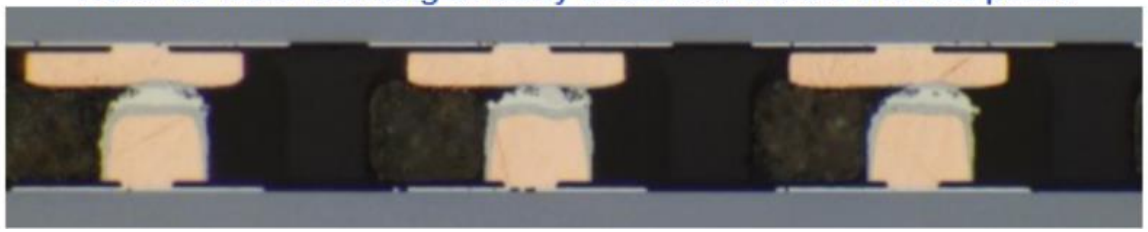
ALTIROCA + irradiated LGAD

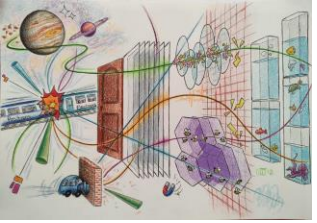


Wafer-to-wafer bonding

- Target: ultra-thin hybrid detectors with TSV
- Pilot project U Bonn / IZM: passive CMOS sensors + Timepix3

Wafer-to-wafer bonding of daisy-chain test wafers with Cu pillars





WG8- Dissemination and outreach activities

Disseminating knowledge on solid-state detectors:

Organize DRD3 schools for young post-doc and Ph.D. in:

- TCAD, FPGA, GEANT
- Laboratory measurements, TCT

Participation to instrumentation schools

- In specific locations (CERN, FNAL…)
- On specific topics (Allpix2, TCAD, setups..)

Share knowledge of measurement techniques

- Device characterizations, such as IV, CV
- Transient studies using TCT, beta telescopes
- Handling and measurements of irradiated sensors
- Intra-DRD3 groups training

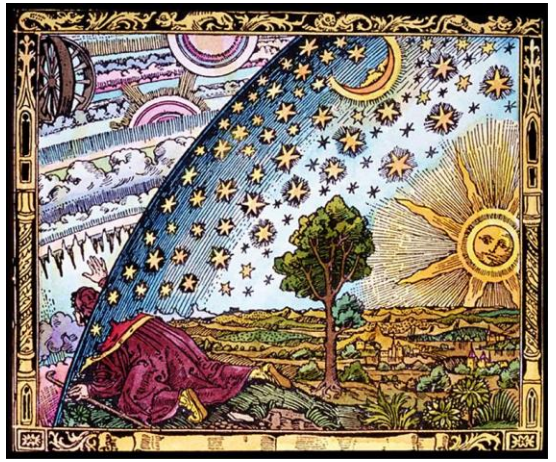
Dissemination of the DRD3 activities:

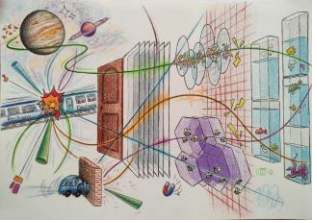
Organize the DRD3 website (drd3.web.cern.ch)

- Point of entry to DRD3
- Link to results, meeting, etc
- Opportunities: conferences, stages
- Documentation (how to do XYZ…)

Present DRD3 work at conferences

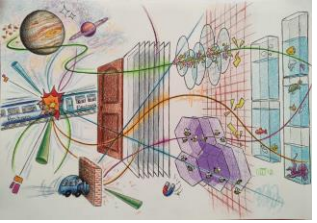
- Opportunity for young researchers
- DRD3 activities documented in printed papers





Conclusions

- DRD3 is a large collaboration under which umbrella future R&D on semiconductor particle detectors will take place.
  - The **strategic funding of the activities (HEP detector R&D)** will be supported by funding agencies
  - WP project proposals are being formed and shaped - in the Annexes of MoU presented to FA (please have a look and join or propose – template available)
  - We are in quite far with MoU preparation – expected to be ready for signing in the following months
  - The collaboration will have common fund from which many smaller R&D projects will be supported also for synergies with other fields and Blu-Sky R&D
- Coming events:
  - The 2nd DRD3 week in going to happen soon (2-6.12.2024 at CERN) – online is free and open.
  - 1st DRD3 TCT School (beginning in Feb. 2025 at CERN – 3 days practical work)
- More information can be found on drd3.web.cern.ch



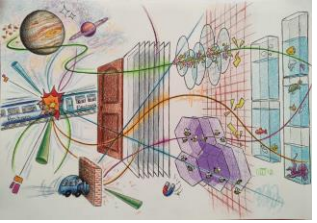
DRD3

I hope that CEPC, if built, will profit from DRD3 as HL-LHC experiments have from the previous R&D programs

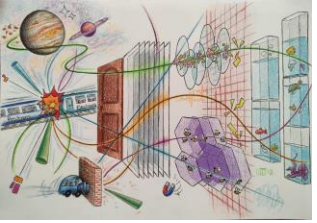
GOOD LUCK!

Nothing is **impossible**, even the word itself says "**I'm possible**"

A. Hepburn

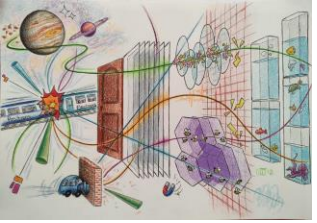


Backup/additional slides



WG2/WP2: 3D sensors

- Small cell size 25x25 μm^2 /25x50 μm^2 required for position resolution and high rates would allow also hit time resolutions **~10-20 ps**.
  - the column width reduction ~10 μm to <5 μm (reduction of capacitance, improvement of S/N, reduction of the jitter/power and increase of fill factor) – in the future column widths as low as ~1-2 μm may be possible allowing possible multi-cell configurations.
  - improved aspect ratio of Deep Reactive Ion Etching (DRIE) is crucial -> current aspect ratio of 25 should be improved, particularly for thicker detectors that may be required to improve the signal required in severe radiation hard environment - larger clusters become the problem.
  - The choice of design (Trench/Column) will be a matter of optimization time resolution vs. fill factor and there is no clear answer to which is better (it depends on application)
- New ideas will be important and may become possible and/or mature over the years:
  - "Marriage" of LGADs and 3D (either by trench filling, careful substrate selection with small interelectrode distance allowing charge multiplication without special processing of gain layer)
  - "Marriage" of CMOS and 3D.
- The scalability is a question for the producers:
  - single sided processing is a major step forward, the next is move to >=8" wafers, where thicker wafers are required
  - Yield improvement , robustness of the designs are key
- Operation conditions: cooling down as low as possible improves the performance in all respects not only power dissipation/leakage current, but also in speed and possible charge multiplication

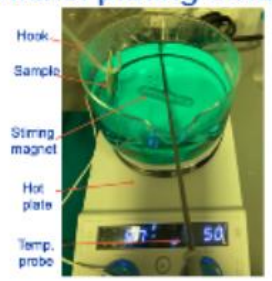


WG7/WP4 post processing and bonding

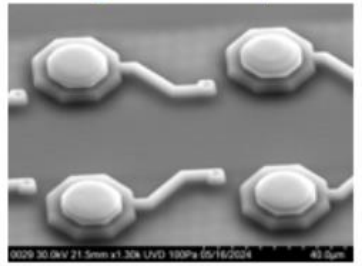
DRD3

Plating:
Well-controlled plating process is required for most interconnect methods
- Consolidated and documented process flow for in-house Ni/Au plating
- **Consistent plating results** for a variety of devices and pixel-pitches (20 µm to 1.3 mm)

Nickel plating setup

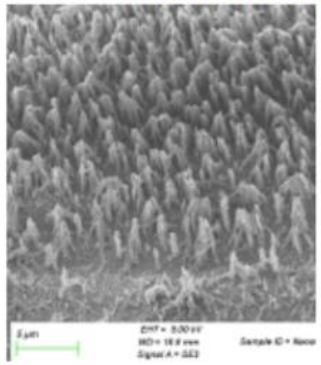


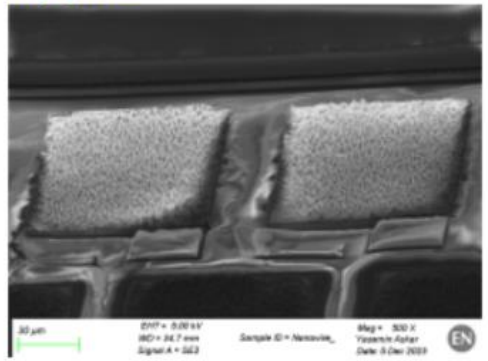
Plating on Timespot ASIC



Nano wires:
Low-resistance interconnects, suitable for chip- and wafer-level integration
- Developed process with MALTA2 as test vehicle (with Nanowired, Gernsheim)

Nano wires on chip pads

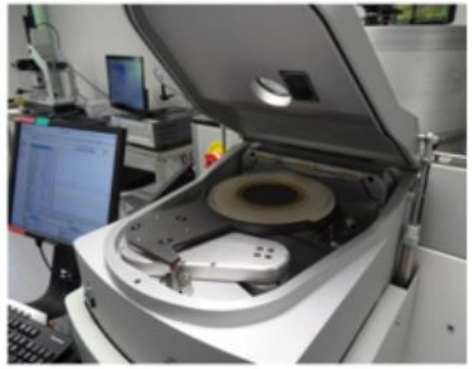




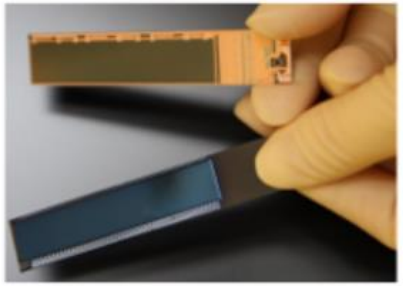
Flex PCB / modules developments:

Module concepts target low mass and large active area
- Custom **flex-PCB** process under development with FCBG (Geneva)
- DEPFET all-silicon modules (MPG-HLL)

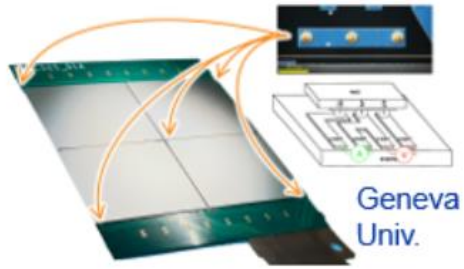
Dry-etching of dummy flex

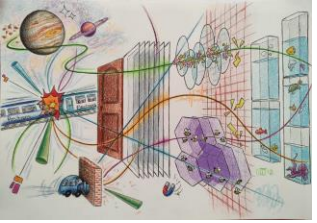


DEPFET all-silicon modules



100µPET module with Au studs

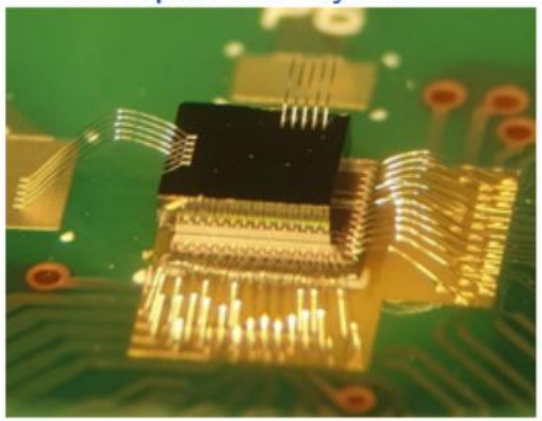




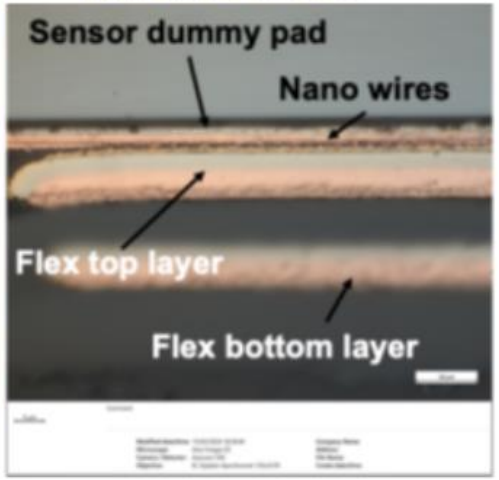
WG7/WP4: In house bonding and wafer-wafer

DRD3

Timespot1 ACF hybrid



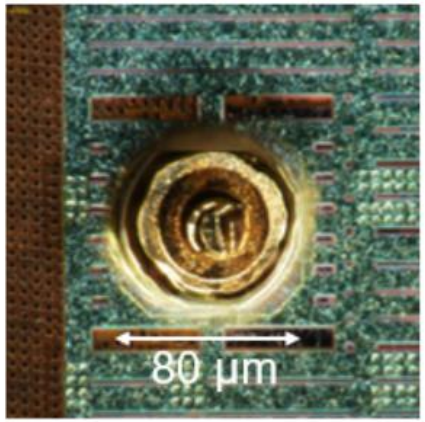
Nanowires on flex



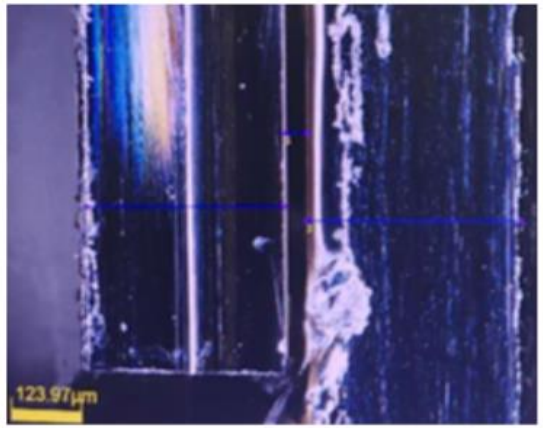
In-house hybridization, module integration

- Exploring innovative **bonding** methods, adapted to the requirements of various projects
  - **Conductive adhesives (ACF / ACP)**
    → good results for <1cm^2 devices and >~50 µm pitch
  - **Nano wires**
    → successful bonding of MALTA2 to flex
  - **Gold studs** + epoxy
    → successfully used for large (>100 µm) pitch
    → developed **low-temperature bonding process** suitable for **irradiated samples**

Gold-stud on ALTIROCA



ALTIROCA + irradiated LGAD



Wafer-to-wafer bonding

- Target: ultra-thin hybrid detectors with TSV
- Pilot project U Bonn / IZM: passive CMOS sensors + Timepix3

Wafer-to-wafer bonding of daisy-chain test wafers with Cu pillars