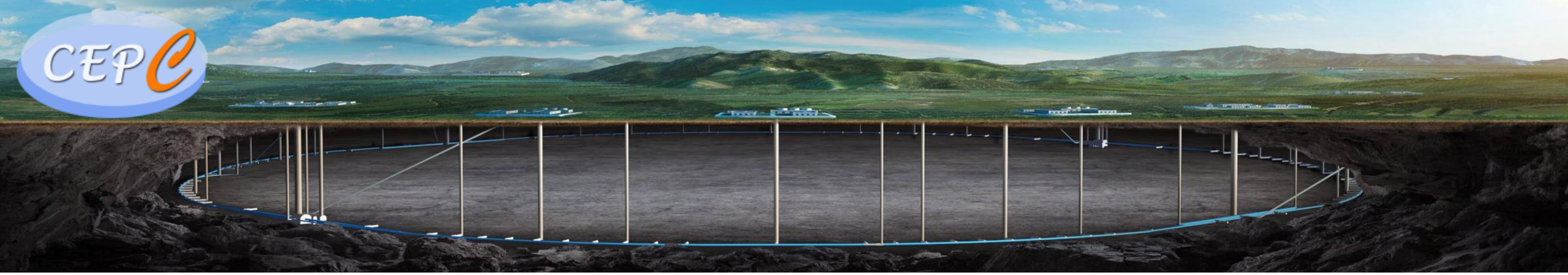

CEPC Hardware Trigger design for ref-TDR

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- Introduction
- Requirements
- TDAQ structure
- Preliminary trigger design
- Detailed design scheme
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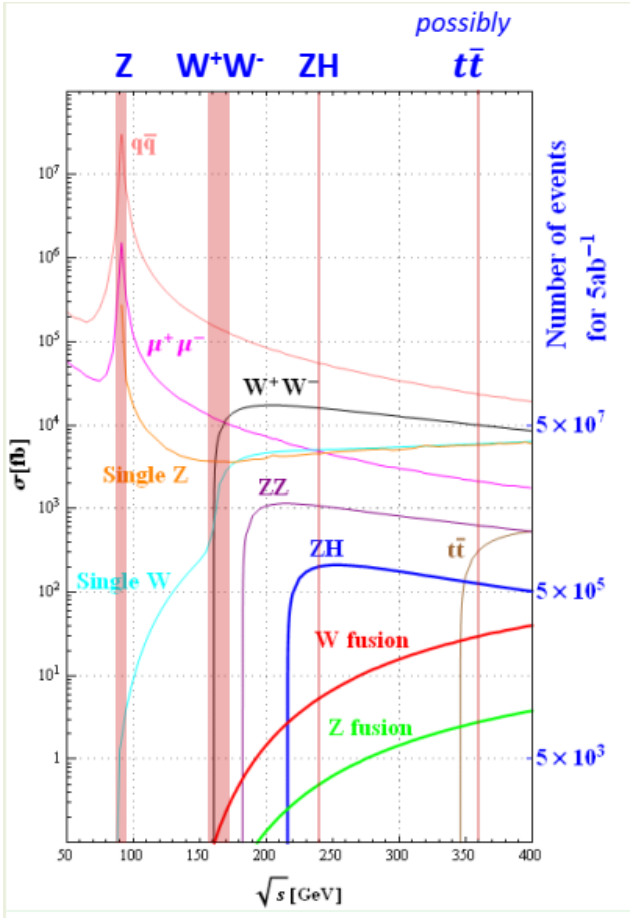
Introduction

- CEPC is designed to operate at around 91.2 GeV as a *Z* factory, at around 160 GeV of the *W W* production, at 240 GeV as a Higgs factory.

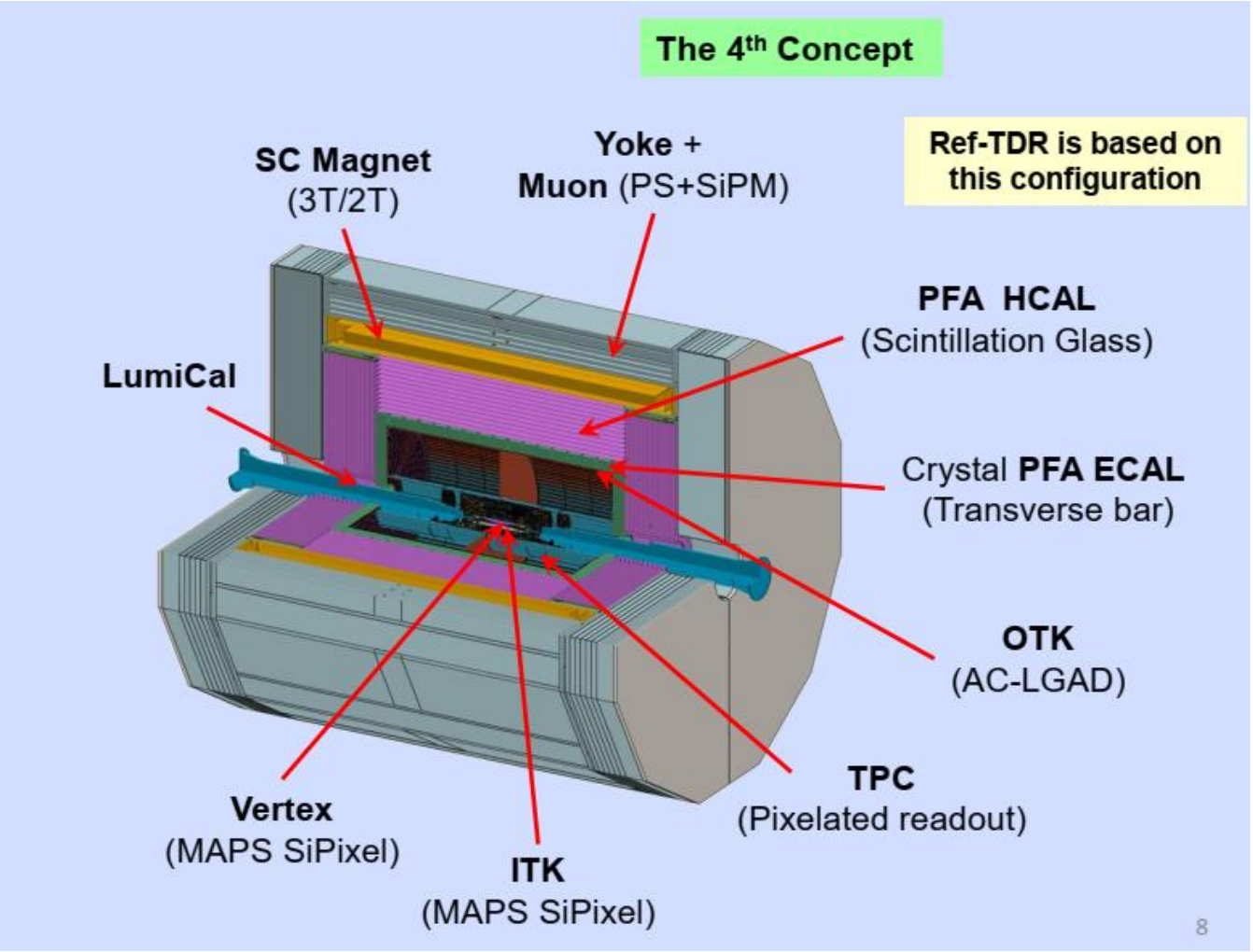


Operation mode		ZH	Z	W⁺W⁻	$t\bar{t}$
$\sqrt{s}$ [GeV]		~240	~91	~160	~360
Run Time [years]		10	2	1	5
30 MW	L / IP [$\times 10^{34}$ cm^{-2}s^{-1}]	**5.0**	**115**	**16**	**0.5**
	$\int L\,dt$ [ab^{-1}, 2 IPs]	13	60	4.2	0.65
	Event yields [2 IPs]	2.6×10^{6}	2.5×10^{12}	1.3×10^{8}	4×10^{5}
50 MW	L / IP [$\times 10^{34}$ cm^{-2}s^{-1}]	**8.3**	**192**	**26.7**	**0.8**
	$\int L\,dt$ [ab^{-1}, 2 IPs]	21.6	100	6.9	1
	Event yields [2 IPs]	4.3×10^{6}	4.1×10^{12}	2.1×10^{8}	6×10^{5}

CEPC accelerator TDR (Xiv:2312.14363)

Detector introduction

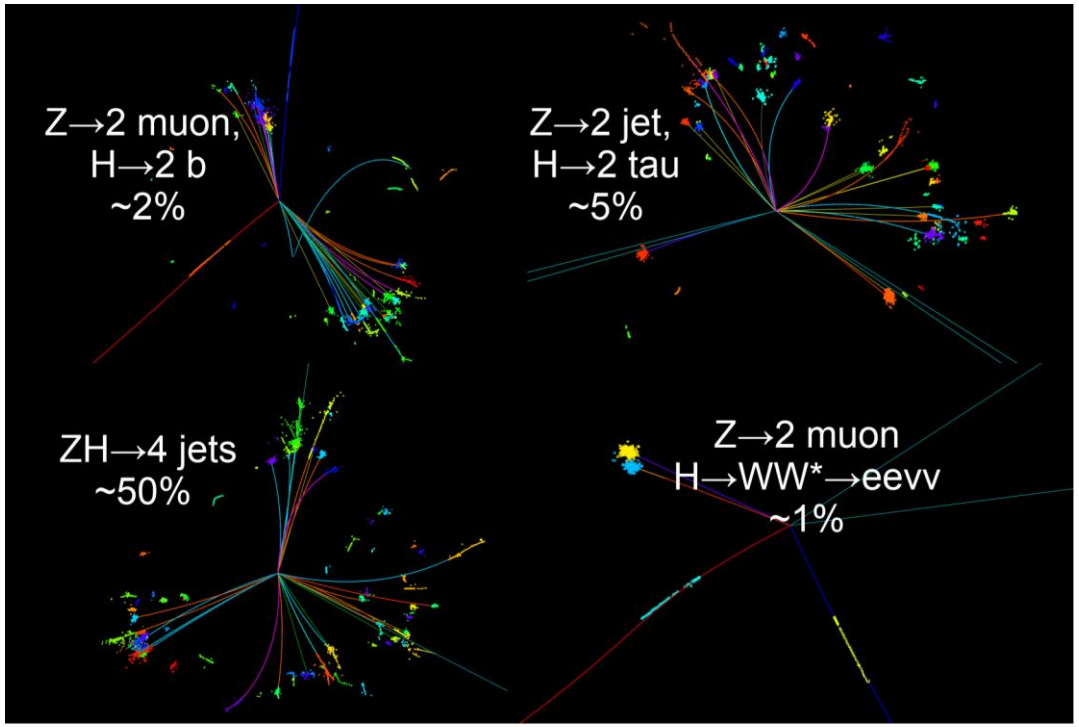
- From innermost to outer (ref-TDR baseline option)
  - Vertex
    - 4 signal layers + 1 double layer ladder
  - ITK
    - ITKB 3 layers，
    - ITKE 4 layers
  - TPC
    - Maximum drift time: 34us
  - OTK with TOF
    - 50 ps
  - ECAL
    - 480 modules, 28 layers,
  - HCAL
    - Barrel: 16 sector,48 layers,
  - Muon
    - 6 super layers



Requirements: Physical Event Rate

- 8 Hz @ Higgs 240GeV(50MW)
  - Bunch crossing rate: 2.9 MHz
  - Higgs: ~0.02Hz
- 82 kHz @ Z pole 91GeV(50MW)
  - Bunch crossing rate: 43.3 MHz
- Physical event rates are sufficiently low relative to the bunch crossing rate.
- Keep physical events as more as possible
  - By a rough selection of the relevant objects (jet, e, muon, tau,v, ...) and their combinations.
  - Required detailed signal feature extraction and simulation studies.

	Higgs	Z	W	$t\bar{t}$
SR power per beam (MW)	50			
Bunch number	446	13104	2162	58
Bunch spacing (ns)	346.2 (×15)	23.1 (×1)	138.5 (×6)	2700.0 (×117)
Train gap (%)	54	9	10	53
Luminosity per IP (10^{34} cm^{-2} s^{-1})	8.3	192	26.7	0.8



Ref: CEPC Physics at a glance, Lomonosov Conference 2021, by Manqi Ruan

Requirements: Data Rate estimation

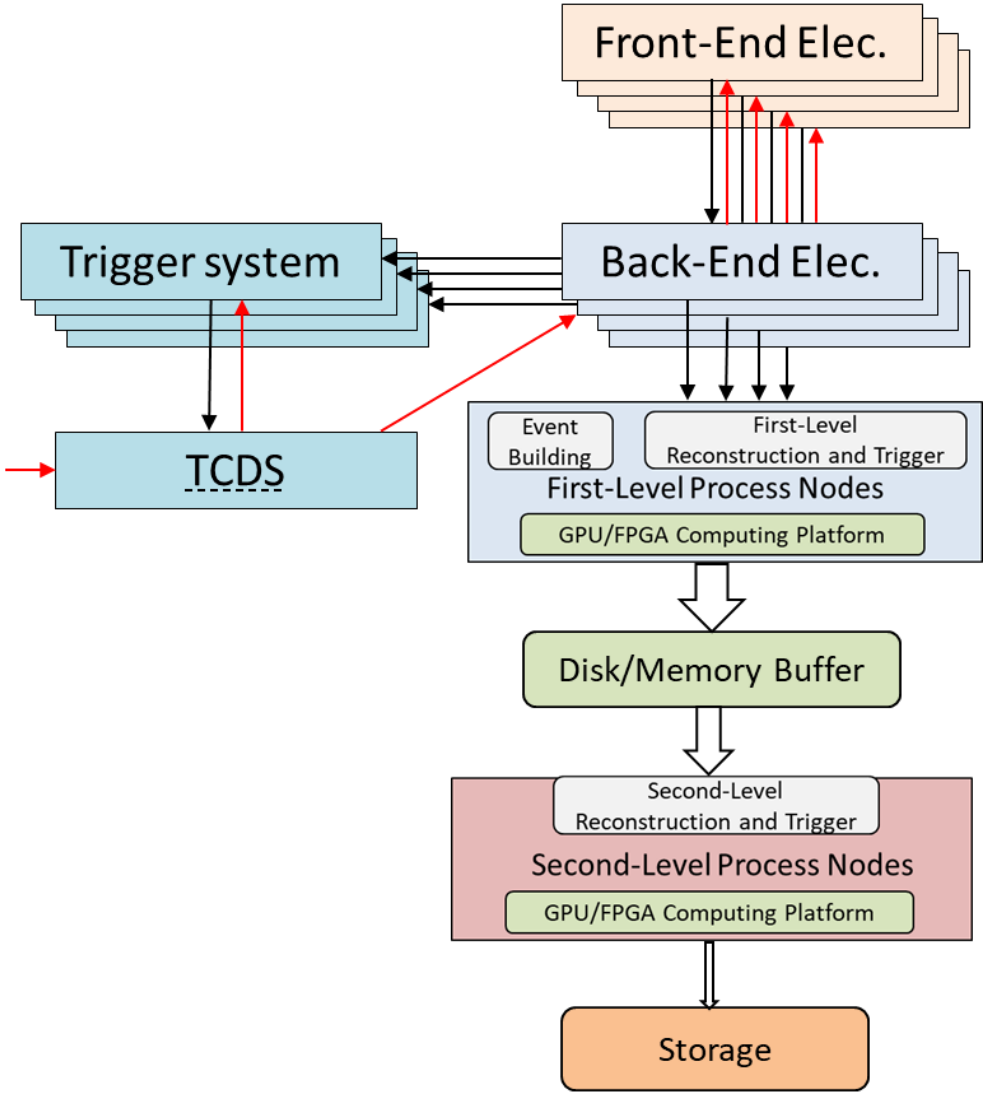
- Data rate before trigger
  - <1 TB/s @ Higgs
  - Several TB/s @Z
- L1 trigger rate
  - O(1k) Hz @ Higgs
  - O(100k) Hz @ Z
- Event size < 2 MB
  - Related to occupancy and read out window
- Storage rate after HLT
  - <100 Hz(200 MB/s) @Higgs
  - 100 kHz (200 GB/s) @Z

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024	512*128	1024	128		128	8~16				
Data Width /hit	32bit	42bit	32bit	48bit		48bit	48bit				
Avg. data rate / chip	0.18Gbps/chip, 1Gbps/chip inner	3.53Mbps/chip	21.5Mbps/chip	2.9Mbps/chip	38.8Mbps/chip	~70Mbps/module Inmost	10kHz/ch	10kHz/ch	5kHz/channel	5kHz/channel	10kHz/channel, 20kHz/iner endcap
Detector Channel/module	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	0.39 M chn	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	43,176 chn(iner end-cap 6912), 288 modules
Avg Data Vol before trigger	474.2Gbps	101.7Gbps	298.8Gbps	249.1 Gbps	27.9Gbps	34.4Gbps	460.8Gbps	187Gbps	811.2Gbps	537.6Gbps	24Gbps
Occupancy	0.22e-4	2.5e-4				2.8e-4	58e-4			19.5e-4	
Sum	3.2 Tbps = 400GB/s @Higgs										

Preliminary background and data rate estimation

TDAQ structure

- Electronics framework schema
  - Transmit full raw data from Front-End Elec. to Back-End Elec.(BEE)
  - Connect trigger with Back-End Elec.
- Trigger solutions
  - Hardware trigger(L1) + high level trigger(HLT)
    - A single type of common hardware trigger board
      - Collect trigger primitives from BEE common boards
      - Send back trigger accept signal to BEE
    - Provide fast and normal trigger menu
    - Network readout

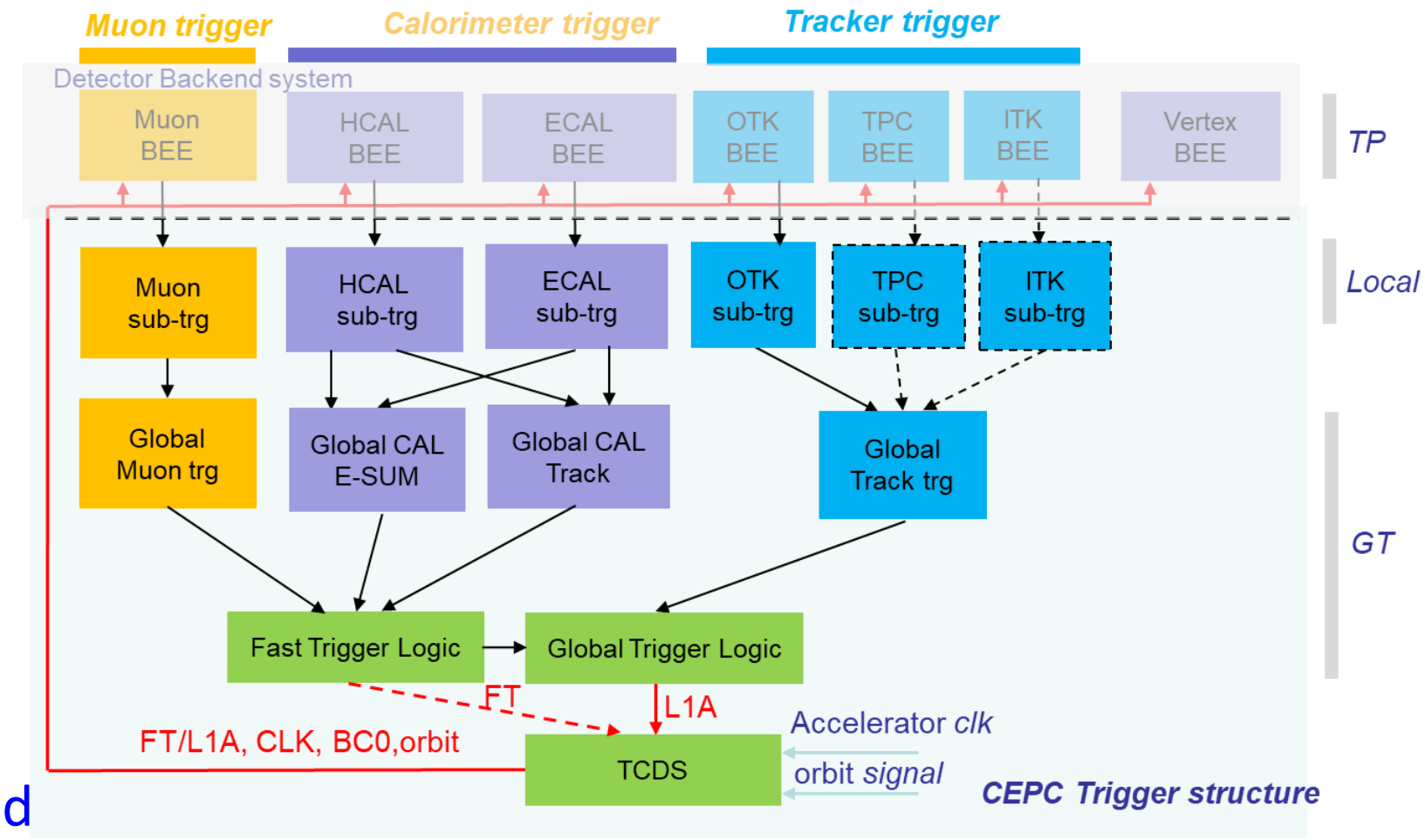


Main Technical Challenges

- High efficiency algorithms in trigger and background compression
  - 2.9MHz->O(1k)Hz @Higgs
  - 43.3MHz->O(100k)Hz @Z
- Trigger primitive synchronization control with asynchronous data readout from electronics
  - Manage data disorder due to data transfer queuing and delay
  - Align sub-detector data of each bunch crossing within limited time and resource

Preliminary Hardware Trigger Structure

- Trigger primitive(TP)
  - Extracted by BEE
- Local detector trigger
  - Sub energy and tracking…
- Global trigger
  - E-sum and tracking
  - Fast trigger(FT) and L1A generation on demand
- TCDS (Trigger Clock Distribution System)
  - Distribute clock and fast control signals to BEE
- Which detectors participate in trigger needs to be studied

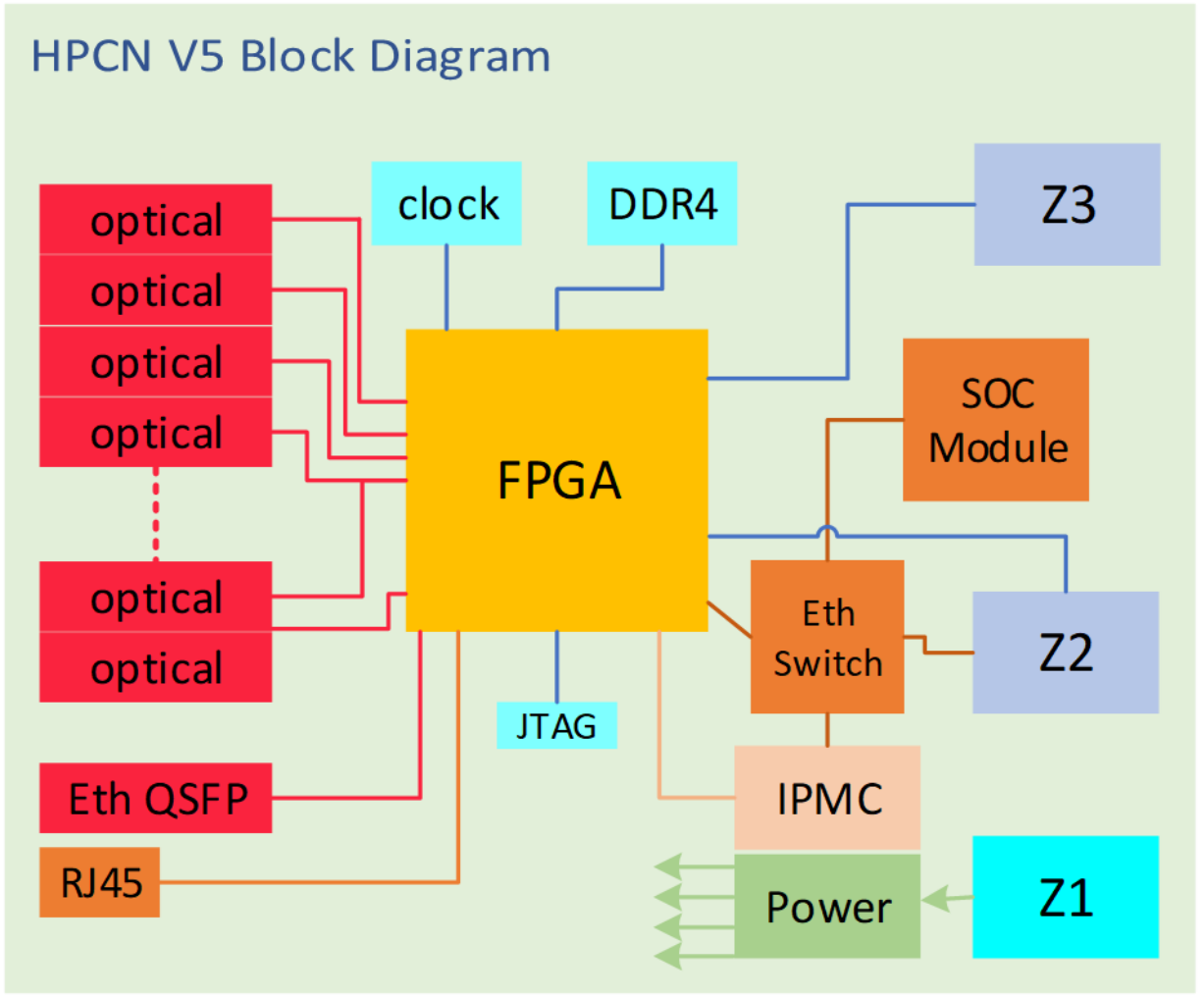


Trigger Prilimilary and alogrithm

- Trigger simulation is ongoing
- Much more things need to be study
  - Whether ITK short track can reduce background or not? Join trigger or not?
  - ECAL cluster size or energy threshold?
  - HCAL cluster size or energy threshold?
  - Muon tracks or hits, which can be used?
  - How long trigger latency is acceptable for FEE/BEE?
  - ……
- Neural network, ML will be used for cluster finding ,tracking,...

Preliminary design of the common Trigger Board

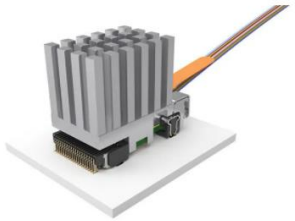
- Common Trigger board function list
  - ATCA standard
  - Xilinx Virtex Ultrascale Plus FPGA
  - Optical channel: 10-25 Gbps/ch
  - Channel number:36-80 channels
  - Optical Ethernet port: 40-100GbE
  - DDR4 for mass data buffering
  - SoC module for board management
  - IPMC module for Power management



Key components for Trigger board design

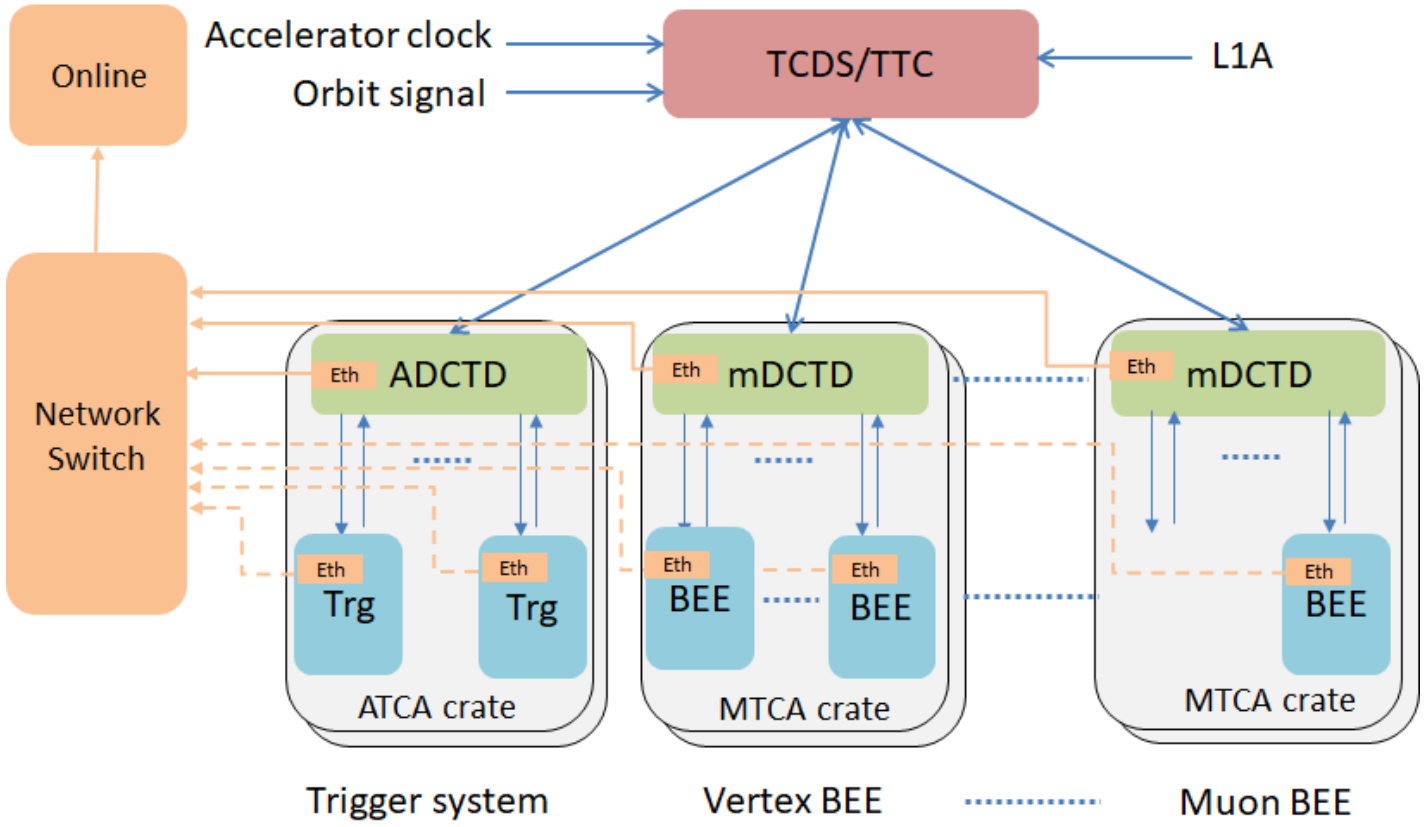
- FPGA: AMD/XILINX VU7P
  - system logic cells: 1,724K
  - CLB Flip-Flops: 1,576K
  - CLB LUTs: 788K
  - DRAM(Mb): 24.1
  - BRAM(Mb): 50.6
  - GTY(32.75Gb/s): 76
  - Footpin: B2104, pin compatable with VU9P, VU11P and VU13P for FPGA resuorce upgrade
  - Pin2pin compatable with Fudan Micro chip

- optics: Samtec Firefly
  - High desity
  - 12ch TX/RX /module
  - MPO optics fiber port
  - 14-25Gbps/ch



Preliminary design of TCDS and Readout

- TCDS/TTC
  - Clock, BC0, Trigger, orbit start signal distribution
  - Full, ERR signal feed back to TCDS/TTC and mask or stop L1A
- Data readout from BEE
  - Read out directly or concentrated by DCTD board
  - Depending on the size of the data volume



- TCDS-Trigger Clock Distribution System
- TTC- Trigger, Timing and Control
- ADCTD- ATCA Data Concentrator and Timing Distribution
- mDCTD-mTCA DCTD
- BEE-BackEnd Electronic

TCDS/TTC

- Function list of TCDS/TTC -preliminary
  - system clock generation from accelerator clock or local high-precision clock for test.
  - orbit signal receive from accelerator and generate orbit number and Bunch Crossing Zero(BC0) signal for Bunch counting.
  - Fast trigger or L1A received from trigger system, fanout trigger signal or mask trigger signal to all sub-system according sub-system status.
  - sub-system status receive from feedback link.
  - Downlink signal to BEE(fan out to all BEE and trigger system)
    - Clock, FT, FT_chk, L1T, L1T_chk, BC0, orbit number?,.....
  - Uplink signal information(Feedback to TCDS):
    - Busy, Fiber ERR, ...

DCTD

- DCTD is the xTCA based Data Concentrator and Timing Distribution for trigger insert in trigger ATCA/MTCA crate.
- Data concentrate
  - receive data from each ATCA trigger board
  - package the ATCA crate data based on trigger
  - packaged data send to online via TCP or RDMA
- Timing Distribution
  - system clock/Fast control receive from TCDS or generate locally for test
  - system clock fan-out to ATCA trigger board within ATCA crate
  - Fast control signals fan-out(FT/L1A, BC0, orbit number,...)
  - collect ATCA status information and send back to TCDS

Low latency data transmission link

- uniform data transmission link between BEE to trigger sub-system and within trigger system
  - 10Gbps/ch or 16Gbps/ch
  - low latency for time alignment between different channels
  - uniform data frame format with BX number, delay number, trigger primitive(such as cluster, energy, track, hit) information

Summary

- For ref-TDR, CEPC hardware trigger has a preliminary structure design.

- But much more need to study further.
  - trigger strategy
    - trigger primitive
    - trigger algorithm
  - trigger latency
  - ……

Thank you.

Backup

Previous experience with TDAQ Hardware

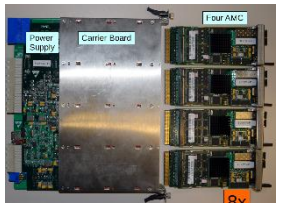
- Designed and constructed BESIII trigger system
  - Comprehensive trigger simulation/hardware design/core trigger firmware development
- GSI PANDA TDAQ R&D
  - High performance computing node (HPCN) board
- Designed and constructed for Belle II DAQ
  - Belle2Link and HPCN V3 as ONSEN
- Constructed CPPF system for CMS Phase-I trigger
  - MTCA board, Cluster finding for Muon/RPC
- Designing for CMS Phase-II backend and trigger
  - ATCA common board for iRPC/RPC

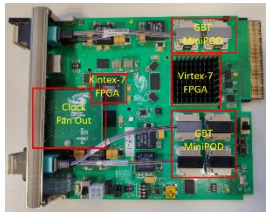
Extensive experience in TDAQ system design, algorithm and hardware development

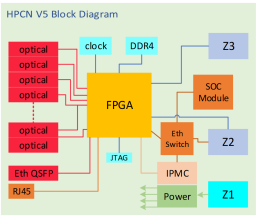
R&D efforts and results

- xTCA for physics standard(ATCA/MTCA extension)
  - IHEP is a founding and development lab together with DESY, FNAL and SLAC
- Developed a series of xTCA boards
  - Started the design of an ATCA common trigger board for CEPC







Version	HPCN V1	HPCN V2	HPCN V3	CPPF	HPCN V4	Serenity	HPCN V5
Line rate	3Gbps	3Gbps	6Gbps	10Gbps	10Gbps	25Gbps	>=16Gbps
Num. of ch	8 ch	8ch	8-16ch	36ch	48ch	124ch	36-80 ch
Buffer	2GB	2GB	4GB	—	48GB	—	TBD
Ethernet	1GbE			1/10GbE	10GbE	100GbE	40-100GbE
Aplication	PANDA		Belle II/PXD	CMS Phase-I	CMS Phase-II		CEPC R&D
Time	2006-		2009-	2013-	2017-		2024-