

# A Low-Level Radio Frequency (LLRF) Control System for Multiple Superconducting Cavities Based on MicroTCA.4\*



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In modern particle accelerators, multiple superconducting cavities are often driven simultaneously by one high-power klystron, thereby reducing the cost of the power sources. The CEPC RF system contains 96 cryomodules for 650 MHz 2-cell cavities. Each cryomodule contains six 650 MHz 2-cell cavities. In the CEPC EDR horizontal test, it is planned to use a single power source to drive a superconducting module (6×2-cell cavities), set up a testing platform, and verify its feasibility. This approach significantly reduces the cost of the power source but introduces several challenges for high-precision control of superconducting cavities, such as gradient differences due to individual cavity variations, frequency offsets caused by Lorentz force detuning, and the calibration of vector sum of amplitudes and phases for multiple cavities. This paper introduces the design of a MicroTCA.4 based Low-Level Radio Frequency (LLRF) control system for multi-cavity control, which will be used for the horizontal testing of the CEPC 650MHz superconducting cavities. Based on the vector-sum control principle, the system utilizes IQ sampling, feedforward-feedback control, and other techniques, eventually achieved high-precision amplitude and phase control and frequency tuning of six superconducting cavities.

## BACKGROUND & INTRODUCTION

The control of multiple superconducting cavities is based on vector sum control principles, where the energy gain of the beam results from the integration of the accelerating voltage along the acceleration path. The calibrated amplitude and phase vectors of multiple cavities are summed to form a single equivalent amplitude and phase signal, which is applied to all control loops. Individual cavities undergo separate coupling adjustments and tuning without individual feedback control. This approach reduces the number of feedback control loops, and consequently, the number of LLRF systems, thereby lowering costs and simplifying the system.

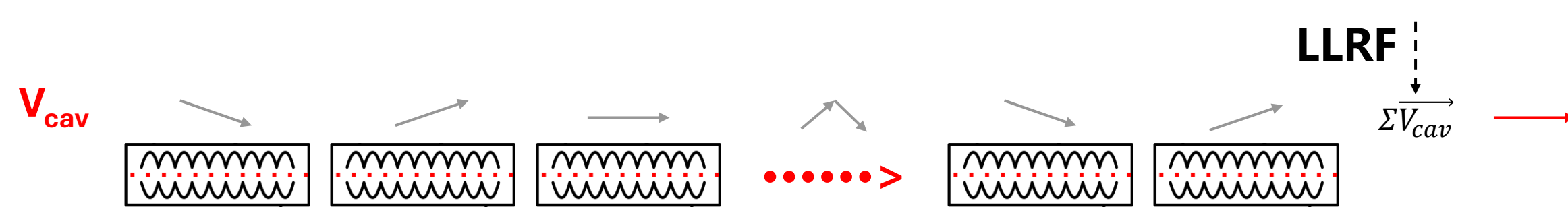


Figure 1: The Vector Sum Control Principle

The key focus of vector sum control lies in calibrating the measurement signals. Small measurement errors in each cavity can be negligible when controlled individually, but when the measurement signals from multiple cavities are summed, the error in the vector sum can significantly increase to an unacceptable level. If the measurement signals are not corrected, even perfect control of the vector sum would still result in substantial errors. Therefore, the prerequisite for everything is the calibration of the vector sum.

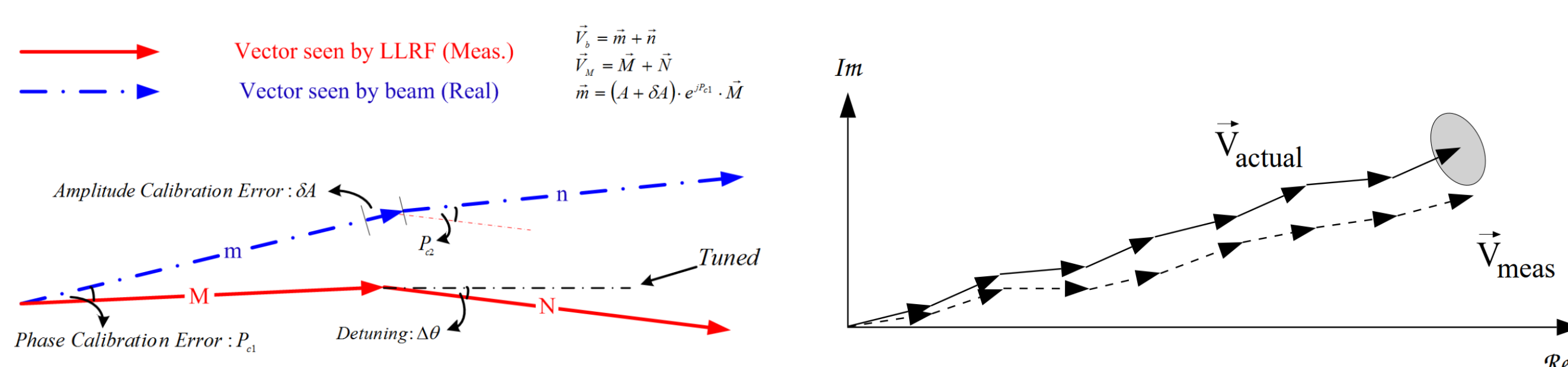


Figure 2: The actual vector seen by the beam and the uncalibrated measurement vector

## DESIGN OF THE LLRF FOR MULTI-CAVITY

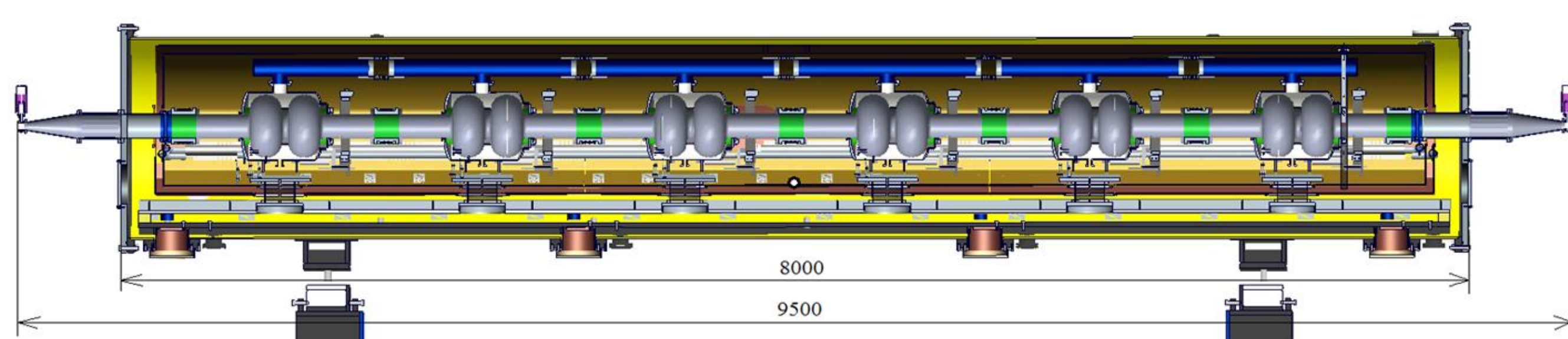


Figure 3: CEPC 650 MHz 6×2-cell superconducting module

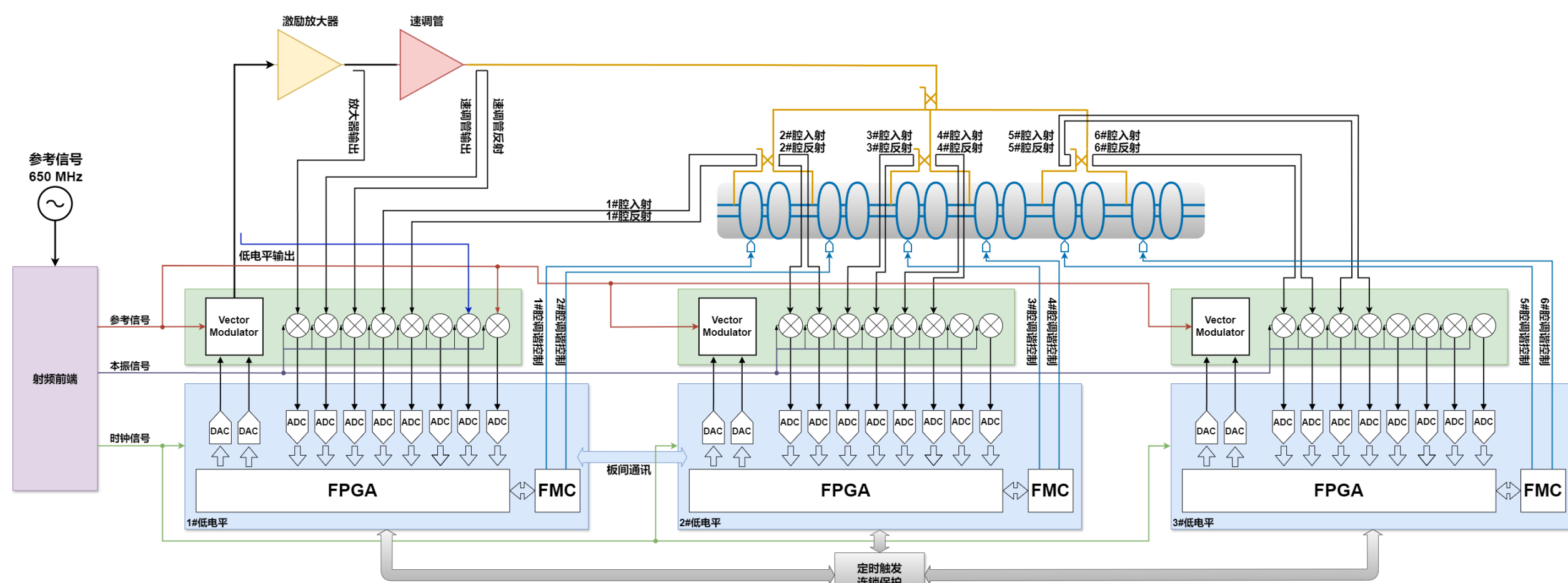


Figure 4: CEPC 650 MHz 6×2-cell superconducting module LLRF system design scheme

- Six 2-cell superconducting cavities are driven by a **klystron power source** system
- The LLRF adopts the domestic MicroTCA platform, including **3** sets of control boards
- A multi-cavity control algorithm based on **vector sum** is used to achieve synchronous control of the amplitude, phase and frequency of six superconducting cavities driven by a set of power source.

## DESIGN PROGRESS

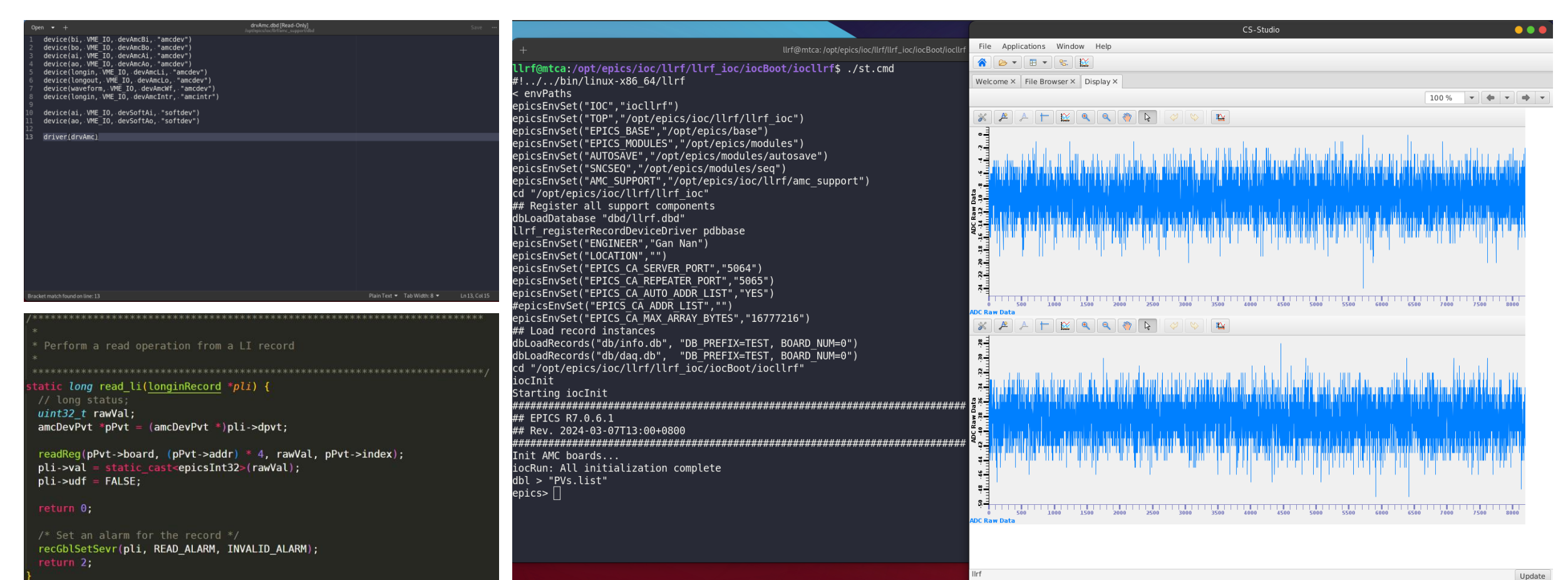


Figure 5: A portion of the firmware and IOC programs

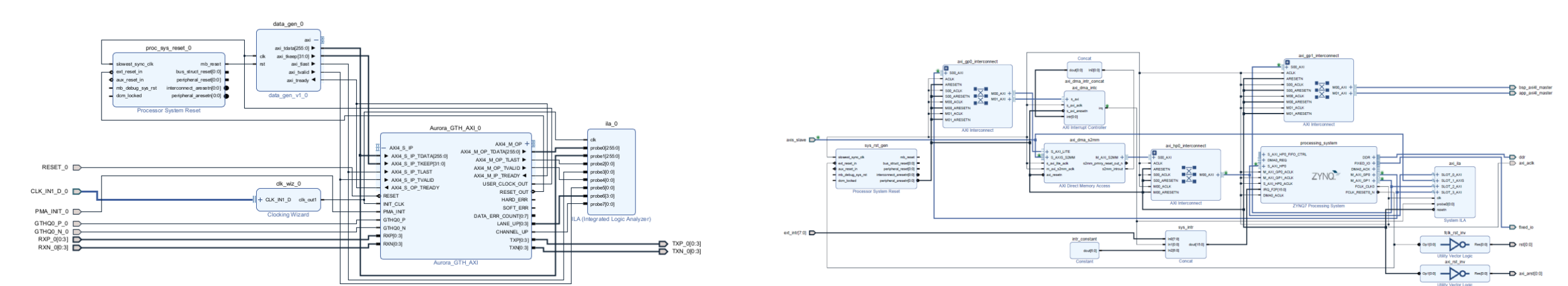


Figure 6: Inter-board communication module and processing system block design



Figure 7: tuning control board and partial domestic hardware resources

## CONCLUSION

Currently, the project team has completed the development of the LLRF firmware for the domestically produced MicroTCA control board and the development of the upper-layer EPICS application, as well as successfully finished the development and debugging of the inter-board communication program. Moving forward, it is planned to complete the migration of the LLRF algorithms by the end of March 2025. This includes the research and development of multi-cavity control algorithms and the transplantation of firmware and upper-layer applications. At the same time, the procurement of domestically produced MicroTCA hardware, including chassis power sources, CPU boards, and FPGA control boards, will be completed by the same deadline. Additionally, the team plans to set up a horizontal test platform in Huairou in June 2025 for the installation and debugging of the low-level control system. These advancements indicate that the project is steadily progressing according to the scheduled timeline, laying a solid foundation for subsequent testing and practical application.

## REFERENCES

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