Poster ID: 15

Installation and operation of LHCb Upstream Tracker

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Abstract

The Large Hadron Collider (LHC) began its third run, known as Run 3, in 2023. During this phase, the LHCb detector operates at a higher instantaneous luminosity ($\mathcal{L}_{inst} = 2 \times 10^{33} cm^{-2} s^{-1}$), which is five times increase from Run2, and use a separate sentence for software trigger. The increase in luminosity is very demanding on the detectors. To address these challenges, LHCb has undergone a major upgrade, replacing nearly all of its subsystems. The all-software trigger relies on real-time readout, reconstruction and selection of events. Fast and efficient track reconstruction is particularly crucial. The Upstream Tracker (UT), a new silicon microstrip detector located upstream of the dipole magnet, replaces the old tracker TT and is a critical component of LHCb tracking system. The UT consists of four silicon microstrip planes and read out with 128-channel SALT ASICs. Installed in LHCb in 2023, the UT has recently started physics data-taking globally after a few months of commissioning. This poster will cover the installation and commissioning of the UT and will also include the operation during data-taking.

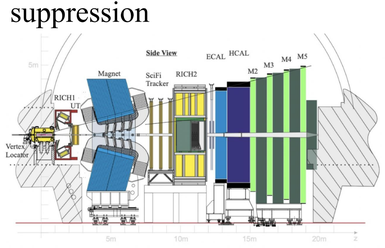
Introduction

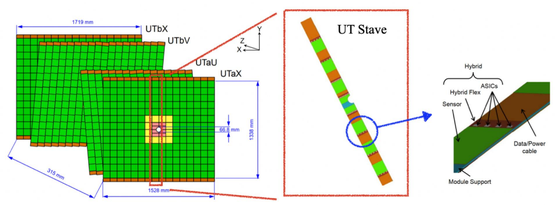
The Upstream Tracker (UT)

- A silicon strip detector with four layers, located upstream of the LHCb bending magnet
- Full angular coverage
- Higher segmentation sensors in the region surrounding the beam pipes[1]
- An important component of LHCb track system

UT front-end readout, SALT (Silicon ASIC for LHCb Tracker)

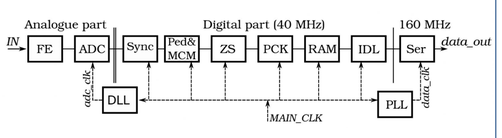
- 128 Channels with 6-bit ADC, 40MHz readout
- CMOS 130nm technology
- Fast shaping time: Tpeak < 25ns
- Digital signal processing providing pedestal & common mode noise subtraction, zero-suppression





UT Commissioning

UT was the last detector to be installed in the LHCb, leaving very limited time for commissioning

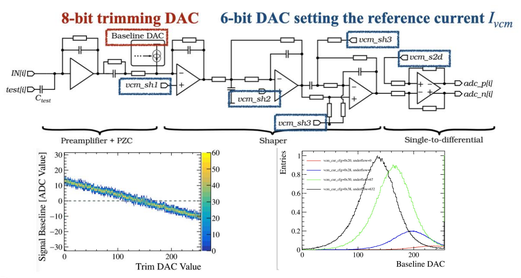


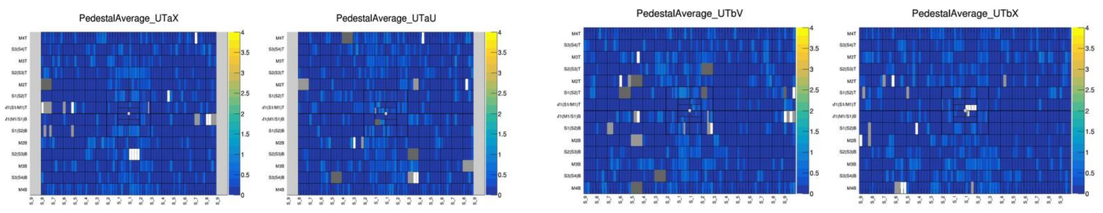
UT Calibration steps:

Tune DLL/PLL, Scan serializer delay, Tune e-link phase on GBTx, Tune ADC, Tune deserializer, TrimDAC scan, Pedestals, Tune ZS threshold, Tune MCM thresholds, Gain scan, Run DAQ with random triggers @ 30MHz

TrimDAC Scan

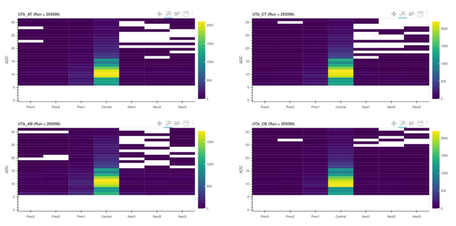
- Each ASIC channel contains an 8-bit trimming DAC for a precise baseline setting[2]
- The single common mode voltage setting couldn't cover all cases: apply 4 different setting for all ASICs
- 99.97% channels work properly at the TrimDAC scan stage

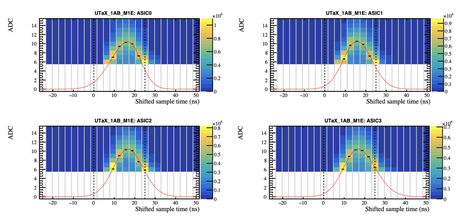




Time Alignment

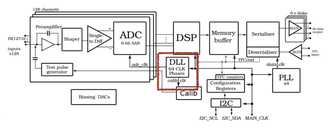
- Time alignment was done using the TAE events produced by the LHC during its 2024 luminosity ramp-up
- Coarse time alignment was done per DCB (Data Control Boards). It makes sure that all ASICs correctly identify a bunch crossing with its corresponding bunch crossing ID within the LHC orbit
- Fine time alignment was done by scanning the ADC sampling phase, which adjusting the delay for each ASIC by fitting a known signal shape to the actual detector signals, resulting in precise time synchronization across the detector

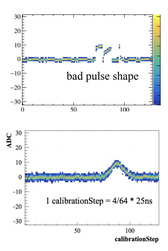




Pulse Scan

- Check the whole processing chain in the SALT chip
- SALT contains a dedicated internal Delay Locked-Loop (DLL) block to provide 64 independent clock phases selection
- Generate test pulse and take data with different clock phase (adc_clk_sel)
- Most of ASICs have the correct pulse shape
  - Recorrected adc_sync_sel bit setting for ASICs with bad pulse shape (32 out of 4048 ASICs)



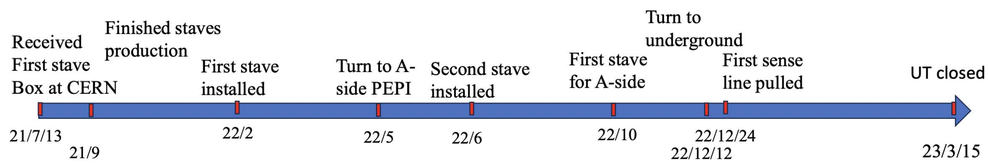


adc_clk_sel	adc_sync_sel	time shift [ns]
0 – 7	1 (falling edge)	$adc\_clk\_sel \cdot \frac{25}{64} + 25$
8 – 39	0 (rising edge)	$adc\_clk\_sel \cdot \frac{25}{64}$
40 – 63	1 (falling edge)	$adc\_clk\_sel \cdot \frac{25}{64}$

Default setting

UT installation

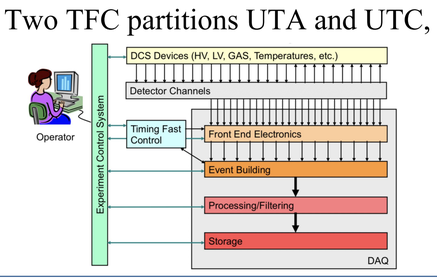
- The Installation started in July 2021 and completed in March 2023
- Chinese groups have significant contributions in design validation, detector installation, and system commissioning
  - HV patch panel, LV splitter, PEPI patch panel, HV cable designed and produced by HNU & IHEP
  - IHEP/HNU/CCNU/LZU/THU/UCAS/SCNU all participated in installation

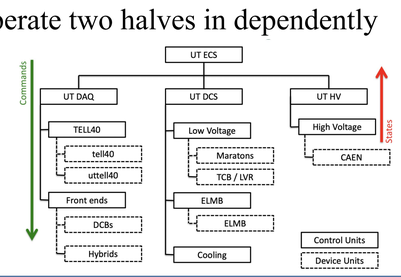


UT Control System

LHCb Experiment Control System (ECS)

- Supervisory Control and Data Acquisition System (SCADA) based on WinCC-OA
- Each tree is a Finite State Machine (FSM)
- UT ECS implemented following LHCb rules
  - Two TFC partitions UTA and UTC, operate two halves in dependently





Working in global

The UT is already taking data smoothly at nominal rates with the rest of LHCb

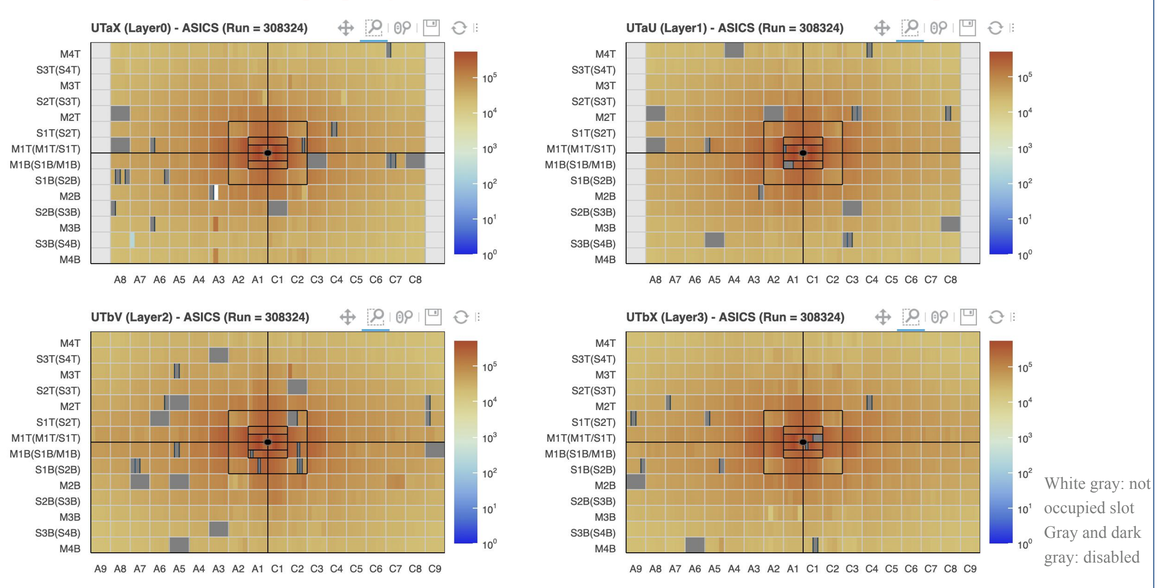
The UT features 4192 ASICs of 128 channels each, with a total of 536,576 strips in 4 layers

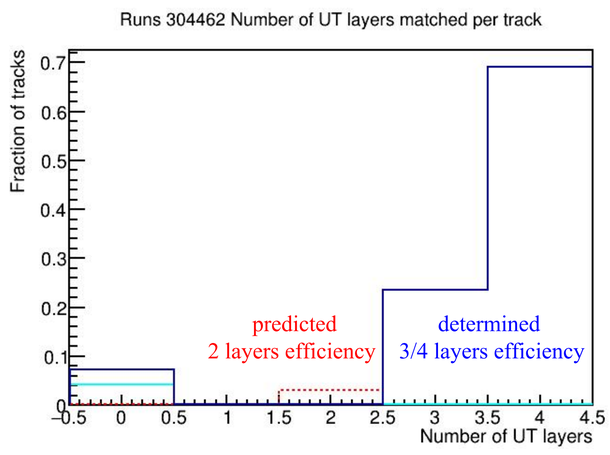
A typical fill of proton-proton collisions at nominal luminosity

The 2D plot for 4 UT layers shows number of hits in each UT chip

Those plots are computed in real time during data taking, so it can timely reflect whether the detector is working properly

Most of the ASICs work properly, and the hit distribution is consistent with expectations!





- The determined efficiency of UT layers (3+4) that match the long track ~ 96.9%
- The predicted UT layers (2+3+4) efficiency ~ 99.8%

Reference and links:
[1]Jianchun Wang et al., The upstream tracker for the LHCb upgrade, https://www.sciencedirect.com/science/article/pii/S0168900216300407
[2] M. Firlej et al., SALT3 chip documentation, https://twiki.cern.ch/twiki/pub/LHCb/StripAsic/salt_v5_spec.pdf

The 2024 International Workshop on the High Energy Circular Electron Positron Collider
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