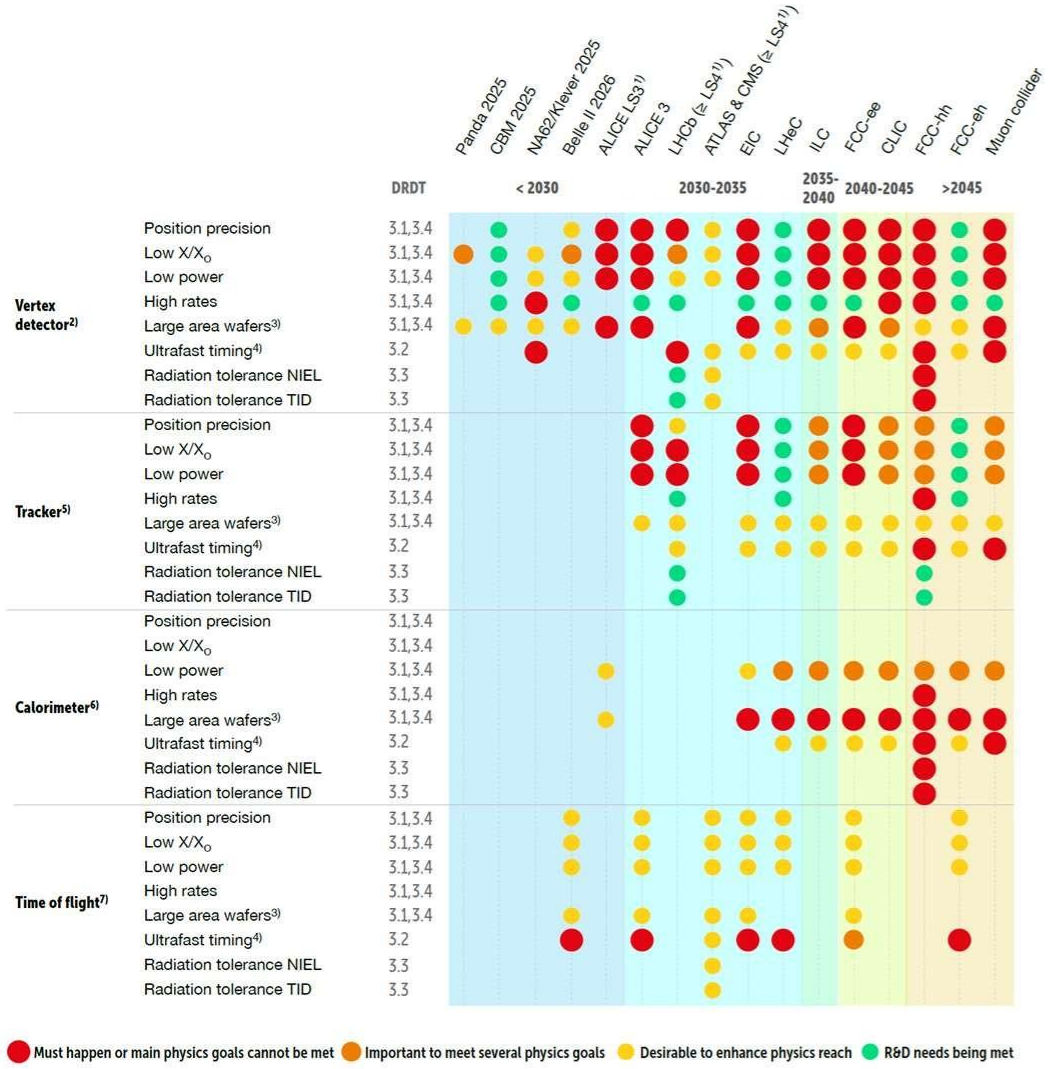
MAPS development in DRD3

Eva Vilella
[on behalf of DRD3.1]
University of Liverpool
vilella@hep.ph.liv.ac.uk

Overview

- DRD3 collaboration on solid state detectors
- DRD3.1 monolithic CMOS sensors
- Research proposal document
- DRD3.1 WP projects
- First DRD3 collaboration week
- Zoom meetings for project proposals

ECFA R&D Roadmap and DRD3



Solid state detectors chapter 3

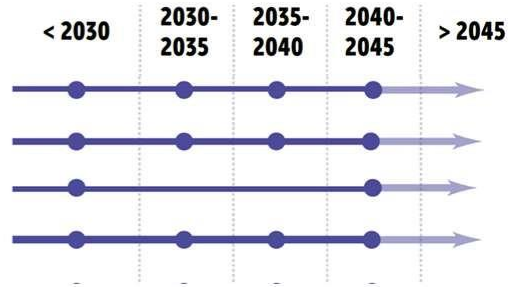
Solid state

DRDT 3.1 Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors

DRDT 3.2 Develop solid state sensors with 4D-capabilities for tracking and calorimetry

DRDT 3.3 Extend capabilities of solid state sensors to operate at extreme fluences

DRDT 3.4 Develop full 3D-interconnection technologies for solid state devices in particle physics



DRD3 Research topics	
WG1	Monolithic silicon sensors
WG2	Hybrid silicon technologies
WG3	Extreme fluence
WG4	Simulation
WG5	Characterisation techniques
WG6	Wide bandgap and innovative sensors materials (diamond, SiC, GaN)
WG7	Interconnections and device fabrication

DRD3.1 Monolithic silicon sensors

- **Aim is to advance the performance of monolithic CMOS, combining sensing and readout elements, tackling the challenges of:**
  - Very high spatial resolution
  - Good timing performance
  - High data rate
  - High radiation tolerance
  - Keeping an affordable cost
  - Low mass
  - Covering large areas
  - Reducing power
  - And ultimately combining all these in one single device

DRD3.1 research goals <2027	
1.1	Position resolution: ≤3 µm
1.2	Timing resolution: towards 20 ps
1.3	Readout architectures: towards 100 MHz/cm^2, 1 GHz/cm^2 with 3D stacked monolithic sensors, and on-chip reconfigurability
1.4	Radiation tolerance: towards e16 n_{eq}/cm^2 NIEL and 500 Mrad TID
1.5	Low-cost large-area CMOS sensors

WG1 Programme and technologies

- **R&D programme divided into three phases:**
  - Initial stepping stones developments for ALICE-3, LHCb-2, EIC, Belle-3, ATLAS, CMS and HGCAL (DRD6);
  - the subsequent further developments for e+e− colliders;
  - and lastly the R&D for MC and FCC-hh.
- **Several complementary technology processes with features that are attractive for HEP detectors:**
  - Accessible to the HEP community;
  - Wafer sizes of 200 mm and 300 mm;
  - High resistivity bulk (through high resistivity epitaxial and Czochralski substrates of p- and n-type);
  - Processes with node sizes ranging from 65 nm to 180 nm, and potential to optimise implant designs for charged particle detection;
  - Availability of MPWs and/or dedicated engineering run with large reticles (with options for reticle stitching or 3D stacking to logic wafers).

WG1 Planning

- **Identified technologies:**
  - TPSCo 65 nm, LFoundry 110 nm, IHP 130 nm, LFoundry 150 nm, AMS/TSI 180 nm, TJ 180 nm, low-cost large-area CMOS and 3D stacking.
    - TSI discontinued its technology in 2023, and efforts focus now on the AMS technology;
    - low-cost large-area refers to large-area monolithic CMOS sensors aimed at instrumenting hundreds of m2 in central tracking applications in future collider experiments.
- **Submissions:**
  - The programme foresees several submissions in approximately 18 months cycles (design, submission and evaluation) until 2027.
    - Proposed submissions in TPSCo 65 nm will take advantage of the runs currently proposed by CERN to be shared with the community;
    - proposed submissions in the other technologies will be as offered by the foundry and/or Europractice.

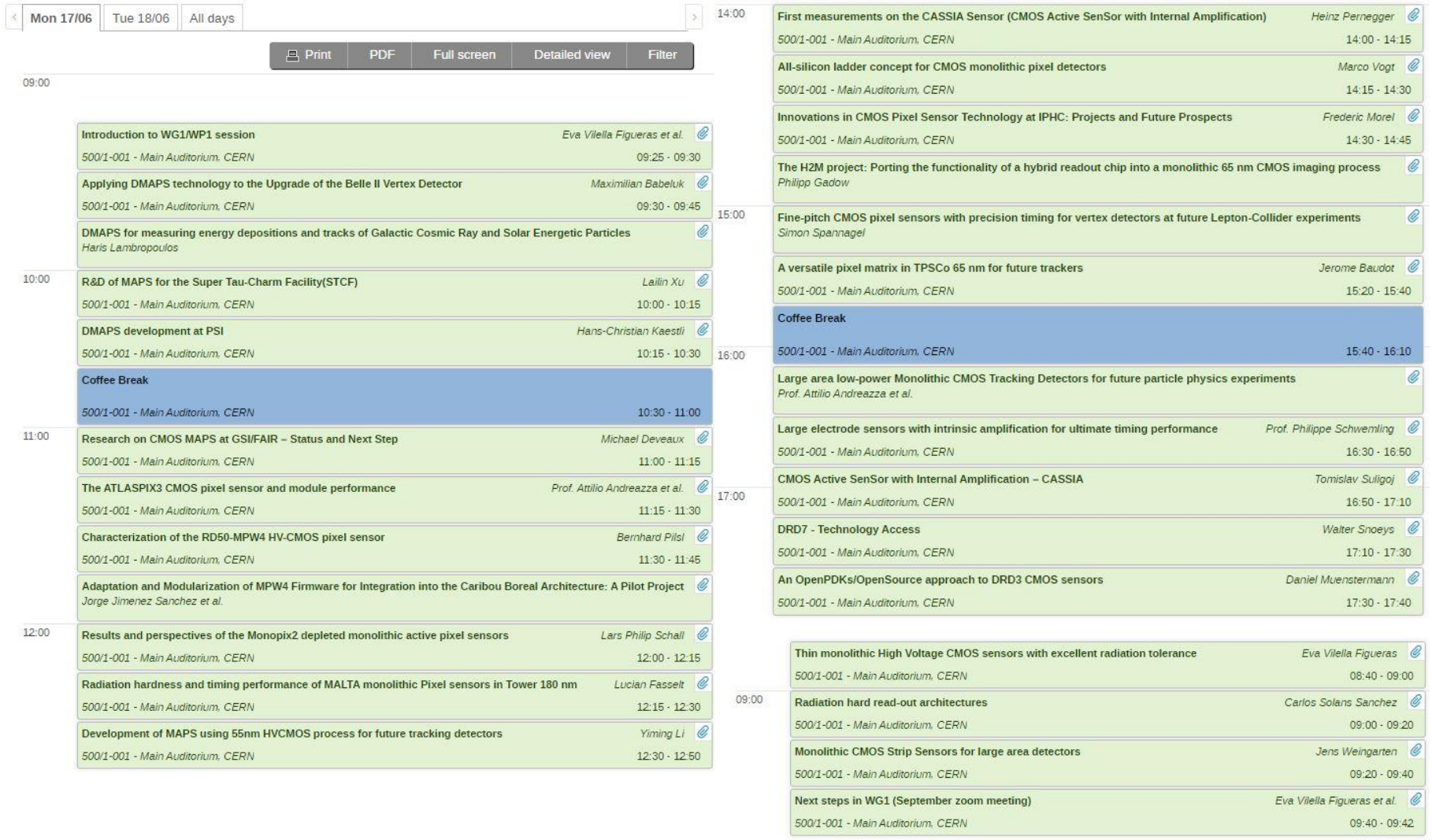
WG1 Planning

- **Technologies and research goals:**
  - The programme does not exclude any of the identified technologies for any of the research goals initially, but it assumes that some technologies might be more suited to achieve certain research goals.
  - As the programme progresses, it is anticipated that perhaps the research focus will shift from all to a sub-set of the identified technologies.
  - It will be possible to add WP projects to achieve the combination of multiple research goals in one single device, which is an important challenge that needs to be met for strategic applications, as the collaboration develops
    - e.g. to achieve devices with high spatial granularity and fast timing while consuming little power;
    - e.g. to achieve devices with fast data rate and high radiation tolerance while consuming little power.

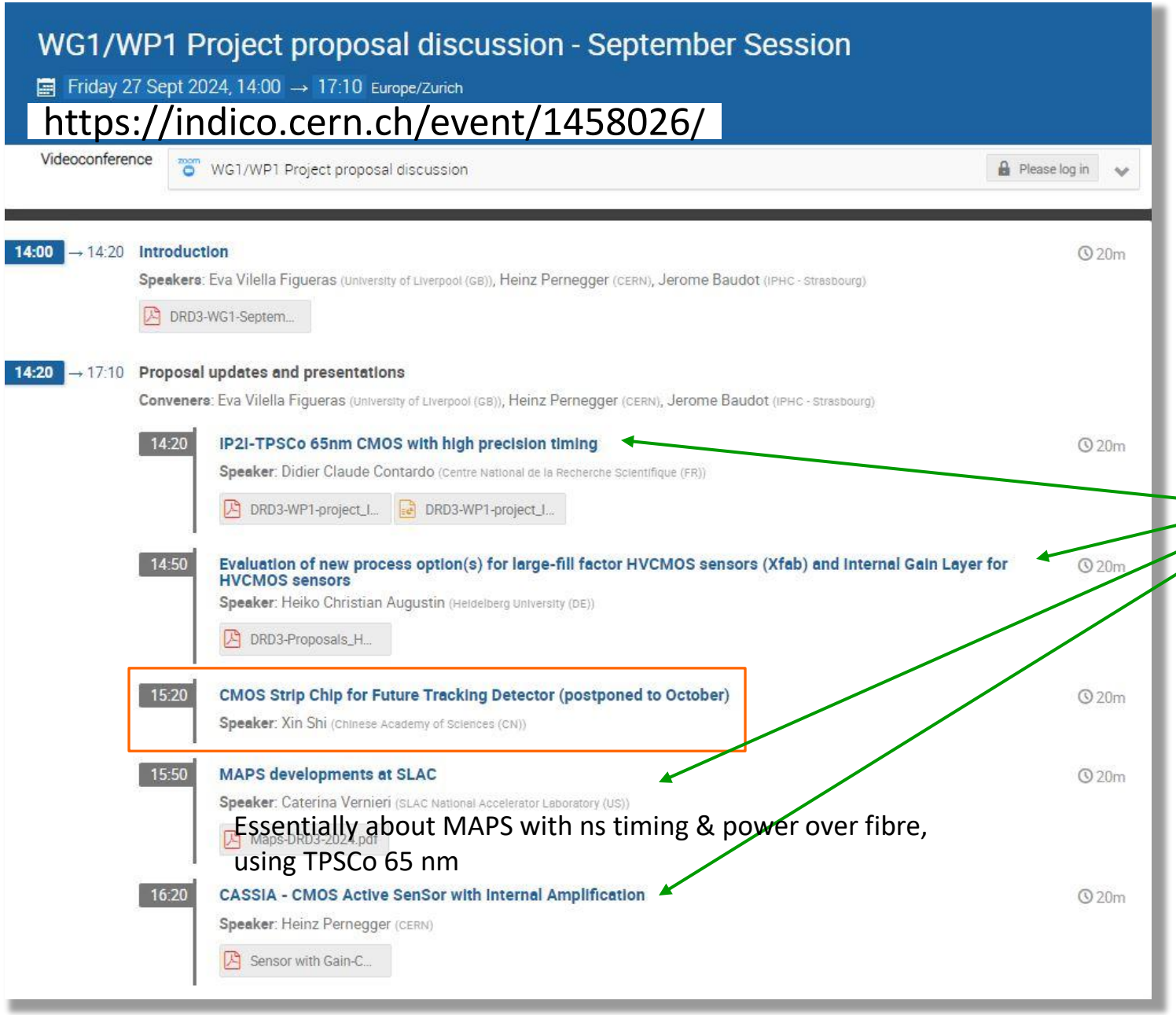
Work Package projects

- **Work Package projects proposed by groups of institutes interested in specific questions within the DRD3 research goals.**
- **Projects will investigate research goals by:**
  - Designing and simulating the sensor;
  - Submitting the design for fabrication;
  - Developing specific data acquisition systems (e.g. chip carrier boards, firmware, etc.)
  - Characterising the fabricated devices in lab measurements, irradiations, and test beams as appropriate.

1st DRD3 week – WG1/WP1 CMOS technologies session



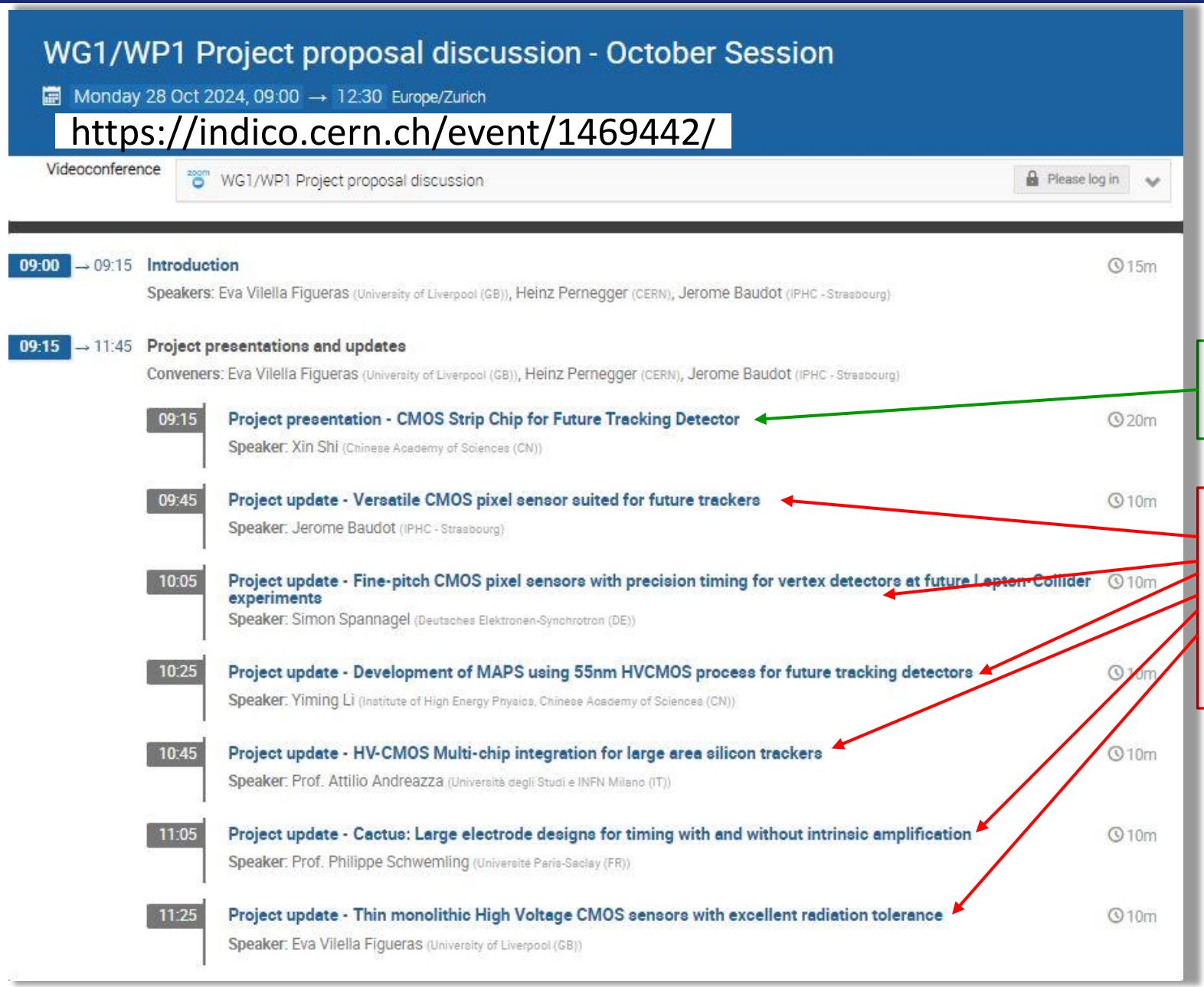
- 3 reports from experiment-oriented developments
- 12 reports from “generic” R&D
- 8 project proposals (+ further project proposals in zoom meetings)



Essentially about MAPS with ns timing & power over fibre, using TPSCo 65 nm

Four new project proposals on different interesting topics

Positive meeting and discussions with many interesting questions about science



One new project proposal

Six updates (projects presented at the first DRD3 week already)

Project proposals

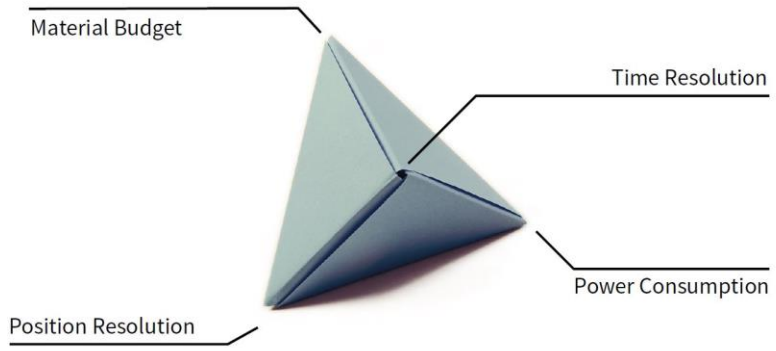
Fine-Pitch CMOS Sensors with Precision Timing for Lepton Collider Experiments

M. Backhaus, T. Bergauer, A. Besson, M. Bomben, D. Dannheim, M. Deveaux, M. Deveaux, J. Dingfelder, A. Macchiolo, **S. Spannagel**, P. Svihra

Project Goals & Scope

- Simulation, development and evaluation of MAPS
- Development in 65nm TPSCo CIS process
- Targeting the **vertex-detector requirements of future Lepton Colliders**:
  - **3 µm single-point resolution**
  - down to 5 ns time resolution (depending on chosen Lepton-Collider technology)
  - average power consumption below 50 mW/cm^2
  - thinning to 50 µm, minimal inactive periphery area
  - sensor architecture scalable to a large-area detector system
- Development of new high-resolution sensors for beam telescopes as intermediate target
  Relaxed power-consumption (<500 mW/cm2) and timing requirements (100 ns)
- Staged approach allows further refinement of performance targets after next strategy update

Challenges for Vertex Detectors @ Lepton Colliders



Project proposal for WP1:

A versatile pixel matrix in TPSCo 65 nm for future trackers

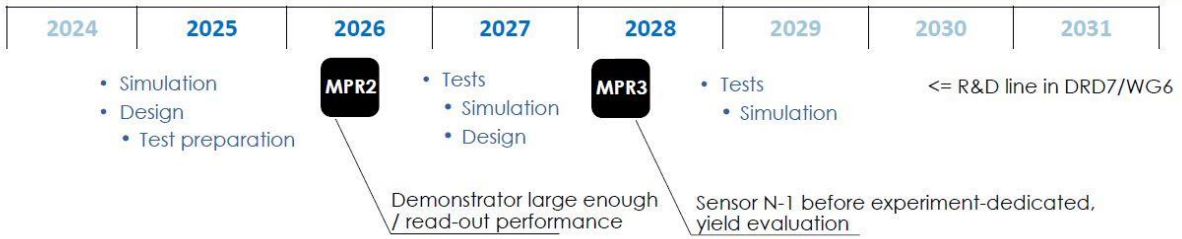
Jerome Baudot

Specifications: numbers!

Source: my own mix of LOI, recent talks and private communication

	ALICE3 OT	Belle II trk	CBM trk	LHCb UT	FCCee trk
Position resolution	~10 µm	<15 µm	~10 µm	<10 µm	<10 µm
Pixel pitch (µm)	50	50	~30	50	50
Hit rate (MHz/cm^2)	0.05 to 2	<1	60/180	160	<10
Data rate (Gb/s)			8	20	
Time figure (ns)	100	~1	25	~1 (<25)	20 to 1000
Triggering	no	yes	no	no	?
Power	~20	<50	~50	<100	~20?
TID (kGy)	50	10?	~10	2400	10?
NIEL	10^{14}	10^{11}?	few 10^{14}	$3x10^{15}$	10^{11}?

Timeline & Collaboration



- Interested groups so far (mostly under discussion)
  - France: CPPM, IPHC, IRFU, LPNHE, …
  - Germany: GSI, …
  - Italy: Bergamo/Pavia, …
  - Japan: under discussion
  - Spain: IFIC, IGFAE, …
  - USA: under discussion
  - …
- Expected strong synergies
  - DRD3-WP1 projects in same techno
    - Position resolution
    - Radiation tolerance
    - Time resolution
  - DRD7-WG6 for technology access

DRD3-WP1 project proposal

TPSCo 65nm MCMOS with high precision timing

D. Contardo, IP2I

DRD3-WP1 project proposal
TPSCo 65nm MCMOS with high precision timing

- Project motivation
  - contribute to developments toward full 5D* tracking with MCMOS sensors
- Targeted applications in several FCC-ee detector concepts
  - ToF PID in outer tracking layer(s) of a full Si-tracker or surrounding a LGVD** tracker
    - providing both $\lesssim$ O(10) µm and O($\lesssim$ 50) ps precision timing in a single sensor
  - applicable to preshower layers in a sampling calorimeter with embedded electronics (DRD6)
- Major constraints
  - high channel density and readout features (real estate) and related power dissipation
    - but rates are lower and material budget effect is less (not) constraining at large radii
- Technology choice
  - TPSCo 65 nm for high density and low power consumption
    - intrincic timing precision may be limited by process (electrode size, epitaxial layer thickness...)

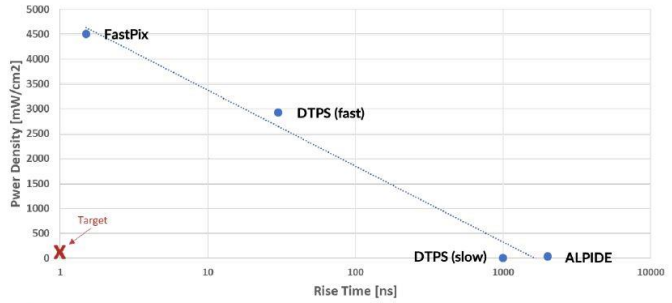
** 5D = space-point, time & amplitude (ToT amplitude for time walk correction and to complete binary output for space-point resolution in clusters)*
*** Large Gas Volume Detector: Drift Chamber or TPC*

(towards) Nanosecond timing MAPS & power over fiber

Caterina Vernieri on behalf of
Christos Bakalis, James E. Brau (Oregon U), Martin Breidenbach, Sander Breur, Angelo Dragone, Loukas Gouskos (Brown U), Christopher Kenney, Lorenzo Rota, Julie Segal, Mirella Vassilev, Charles Young

Target Specs vs. State of the Art

JINST 19 (2024) 04, C04033



No design fulfills all target specification → The need to develop a custom design

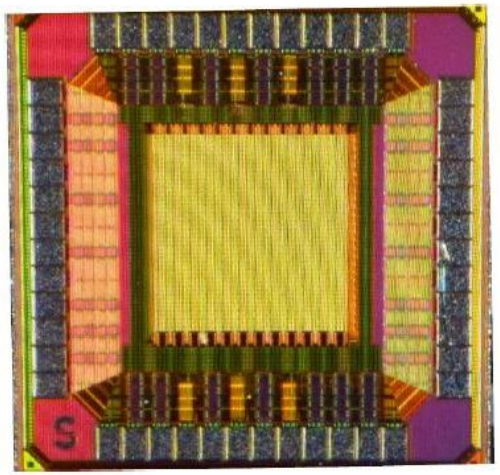
We decided to go with the Tower 65nm technology, which has been optimized by CERN WP1.2 to have low sensor capacitance allowing very good performance with low power consumption.
+ it has the possibility of a wafer-scale stitched sensor
+ it has been proven to be radiation tolerant

SLAC 7

NAPA_p1: **NA**nosecond **P**ixel for large **A**rea sensors – **P**rototype **1**

First prototype in TJ 65nm

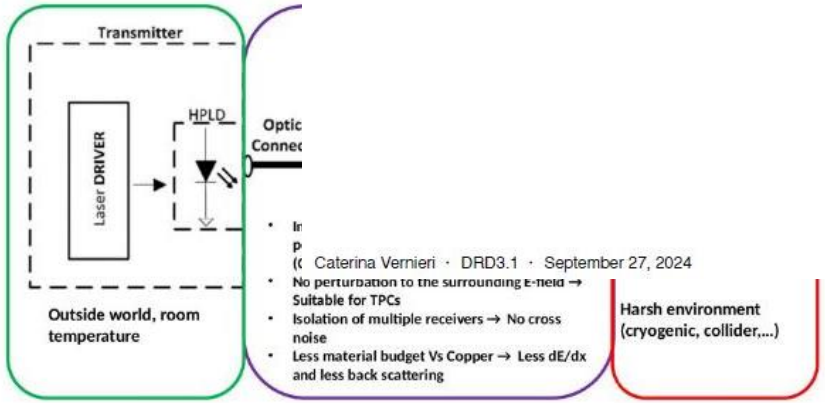
- The prototype design submitted with a total area 5 mm x 5 mm and a pixel of 25 μm x 25 μm, to serve as a baseline for sensor and pixel performance.
- Design motivation → simple architecture with minimum global signals to reduce failure risk in a large area implementation.
- Thanks to CERN WP1.2 effort on sensor optimization in TowerSemi 180 nm and 65 nm technologies



Picture of NAPA-p1 prototype from WP1.2 shared submission

JINST 19 (2024) 04, C04033

- Power over Fiber (PoF) offers an innovative solution by delivering power through optical fibers, which are immune to electric and magnetic fields, and boast 1000X lower thermal conductivity compared to coax.
- We are developing radiation-hardened photonic links that can be used in future e+e- collider environments, where radiation levels can exceed 100 krad.
- This approach will investigate advanced photovoltaic materials like perovskites and their potential to surpass current GaAs-based photodiodes in power-to-weight ratio and radiation tolerance.



UK Research and Innovation UNIVERSITY OF LIVERPOOL

Large area low-power Monolithic CMOS Tracking Detectors for future particle physics experiments

Yanyan Gao – University of Edinburgh
Yimin Li – IHEP
Attilio Andreazza - Università di Milano and INFN
For the ATLASPIX3 Silicon Tracker community

55nm High Voltage CMOS Technology

Started development in SMIC 55 nm HVCMOS technology

- Smaller technology node with respect to other technologies we are working with
  - AMS/TSI 180 nm, LF 150 nm
  - comparable to TPSCo 65 nm
  - also considering HLMC 55 nm
- The 55nm logic technology combines improved performance and reduced power consumption w increased design possibilities and cost efficiencies.

Project goal

1. New MAPS designs targeting low-power and high granularity, featuring smaller nodes (SMIC foundry 55nm), on-chip solutions allowing for efficient data aggregation (e.g. chip-to-chip communication) and Shunt LDO regulators allowing for serial powering, and multi-chip aggregation via hybrids or on wafer stitching
2. development of a large-scale system demonstrator, using state-of-the-art CMOS sensors, that has scalability for large area production as a core element of its design and includes a low-mass mechanical support and efficient cooling strategy. Ultra thin and curved designs will be investigated in the context of vertexing to minimize material budget.

Detailed layout of the project is being developed: scope of this presentation is to trigger a discussion about how it can fit (or be merged) with other WP1 projects

- ATLASPIX3 does not contains all the features needed for efficient integration
  - chip-to-chip data transmission
  - 4 input lines
- Some are available as part of engineering runs developing the ATLAPIX4 family or from LHCb Mighty Tracker
- With FCCee feasibility study and CEPC Detector TDR coming in the next months, we consider a demonstration of the integration process of significant value
- Relevant IPs should also be developed in new technologies, like SMIC 55 nm, to facilitate the convergence of sensor developments into full scale system-on-chip, like ATLASPIX3

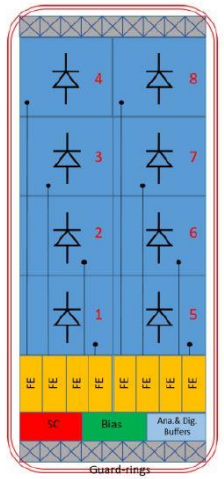
Towards large electrode sensors with intrinsic amplification for ultimate timing performance

CEA/Irfu/DphP and CEA/Irfu/Dedip
Yavuz DEGERLI, Fabrice GUILLOUX,
Jean-Pierre MEYER, Philippe SCHWEMLING (also Université Paris Cité)

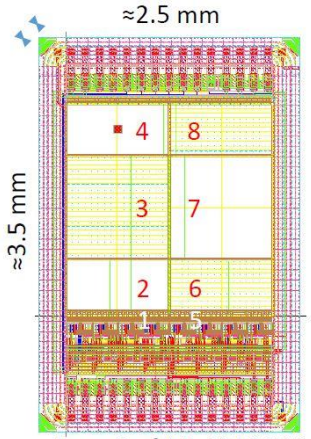
IFAE Barcelona
Raimon CASANOVA, Yujing GAN, Sebastian GRINSTEIN
University of Liverpool
Eva VILELLA

Tomasz HEMPEREK (U. Bonn, now at DECTRIS)

MiniCACTUS Sensor Chip



Block diagram of the MiniCACTUS chip (not to scale)



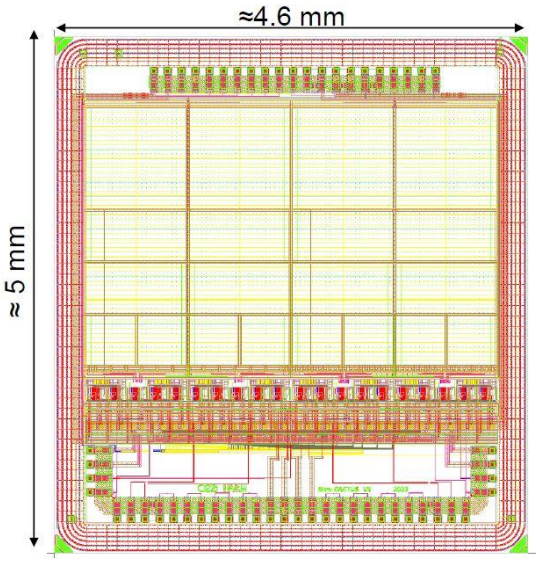
Layout of MiniCACTUS

Pixel Flavors :
Pixels 3 & 7 : 1 mm x 1 mm baseline pixels
Pixels 2, 4, 6 & 8 : 0.5 mm x 1 mm pixels
Pixel 8 : 0.5 mm x 1 mm pixel with in-pixel AC coupling capacitor (20pF)
Pixels 1 : 50 µm x 50 µm test pixel
Pixels 5 : 50 µm x 150 µm test pixel

- **MiniCACTUS** is a smaller detector prototype designed in order to address the *low S/N issue* observed on previous CACTUS large size demonstrator
- Main change in MiniCACTUS: FE integrated at column level, pixels mostly passive
- On-chip **Slow Control**, **DACs**, **bias circuitry**
- 2 discriminated digital (LVDS) and 2 analog monitoring (*slower than CSA output*) outputs for 2 columns
- 2 small pixels implemented as test structures to study charge collection (*FEs not power optimized*)
- Some detectors thinned to 100, 200, 300µm and than post-processed for backside polarization after fabrication

MiniCACTUS_V2 Sensor Chip

Irfu : Yavuz Degerli, Fabrice Guilloux, Jean-Pierre Meyer, Philippe Schwemling
IFAE : Raimon Casanova, Yujin Gan, Sebastian Grinstein



- ~ 2 times larger than MiniCACTUS
- 0.5 mm x 1 mm (baseline), 1 mm x 1 mm and 0.5 mm x 0.5 mm diodes
- 50 µm x 150 µm and 2 50 µm x 50 µm small test diodes
- 3 different preamps
- New multistage discriminator with **programmable hysteresis**
- Improved layout for better mixed-signal coupling rejection
- **CEA-IRFU** & **IFAE-Barcelona** coll.
- Submitted in May 2023, chips came back from post-processing end May 2024

How to improve further?

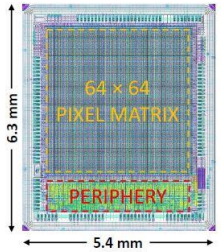
- Intrinsic gain allows to:
  - Improve S/N → Improve on time resolution
  - Reduce FE power consumption
  - Reduce pixel pitch
- Ultimate goal is reaching 20 ps resolution (RG 1.2)

Thin monolithic High Voltage CMOS sensors with excellent radiation tolerance

University of Liverpool – Jan Hammerich, Sam Powell, Eva Vilella, Ben Wade, Chenfan Zhang, Carleton University – Thomas Koffas, HEPHY – Thomas Bergauer, Christian Irmler, IFIC – Ricardo Marco-Hernández, JSI – Igor Mandic, NIKHEF – Uwe Kraemer, Jory Sonneveld, University of Bern – Silke Moebius, University of Sevilla – Rogelio Palomo

RD50-MPW4

- **Significant improvements**
  - For high breakdown voltage and high radiation tolerance
  - Multiple ring structure around the chip edge
  - Substrate backside-biasing to high voltage
- **Fabrication details**
  - 150 nm High Voltage CMOS LFoundry (LF15A)
  - P-type substrate with nominal 3 kΩ·cm high resistivity
  - 280 µm thin
  - Backside processed via third party (complex wafer loan)
- **Chip contents**
  - Pixel matrix with FE-I3 style readout
    - 64 x 64 pixels
    - 62 µm x 62 µm pixels with large collection electrode
  - Digital periphery (slow control, hit data transmission)
  - Tests structures (e-TCT, DLTS)



Chip delivered in Q1 2024
Evaluation is going very well
See Bernhard Pilsl's presentation for details

Detector community dedicated LF15A submissions

- **What is in the deal with LFoundry?**
  - Detector community joint submission(s) with several chips in the reticle
  - Price advantageous
  - Easy access to backside processing (potentially in-house at LFoundry)
  - Access to high resistivity wafers
  - Large number of fabricated wafers, so many samples for chip evaluation
  - Multi-layer mask type submission (MLM 1x3, maximum area is ~ 9 mm x 25 mm)
  - Including 6 metal layers and transistors

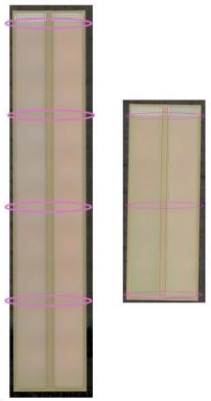
This proposal – Boosting the technology parameters

Parameter	Current value	Research goals
Spatial resolution	62 µm x 62 µm (pixel size)	62 µm x 62 µm (pixel size)
Timing resolution	10 ns (time-walk)	2 ns (time-walk)
Radiation tolerance	Several 10^{15} n_{eq}/cm^2, maybe 10^{16} n_{eq}/cm^2 (currently under test)	> 10^{16} n_{eq}/cm^2
Power consumption	Several 100 mW/cm^2 (currently under test)	A few 100 mW/cm^2
Fill-factor	Area hungry digital periphery Area hungry multiring structure	Reduced area digital periphery Reduced area ring structure

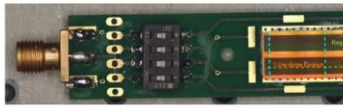
Monolithic CMOS Strip Sensors for large area detectors

Jan-Hendrik Arling , Marta Baselga, Naomi Davis, Jochen Dingfelder, Ingrid M. Gregor, Marc Hauser, Fabian Hügging, Karl Jakobs, Michael Karagounis, Roland Koppenhöfer, Kevin Kröninger, Fabian Lex, Ulrich Parzefall, Birkan Sari, Simon Spannagel, Dennis Sperlich, Jens Weingarten, Iveta Zatocilova

Existing CMOS Sensor structure



- Based on sensor design for ATLAS IT sensor produced on 8" wafer by a con
- **LFA150:**
  - L-Foundry 150 nm process (dee
  - Up to 7 metal layers
  - Resistivity of wafer: >2000 Ω·cn
  - Float-zone processing
- Frontside process: Reticle stitching f
- The strip sensors has 2 different leng



DESY. UNI

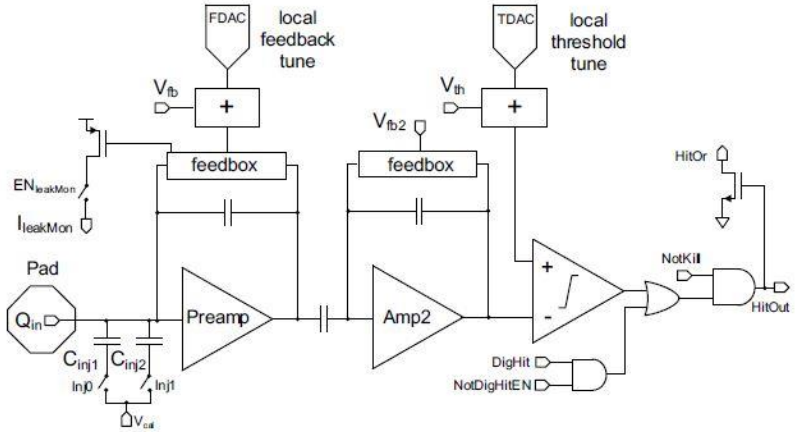
Ingrid-Maria Gregor - The CMOS Strips Talk

Next Steps

- Test monolithic analogue design for the large sensor capacitance of a strip detector
  - Foresee to test with different strip lengths by wire bonding long strips to the test chip
- Basic digital functionality (shortness of digital chip design person-power)
- Develop in FPGA before test submission ➔ Crucial due to funding situation

Going Fully Monolithic

- Dream for large area tracking detectors - minimise bonds (wire and/or bump bonds)
- Fully monolithic would ease the design significantly while possibly being more cost effective
- Working on the implementation of a front-end on strip level
  - **Submission spring 2025**



ATLAS FE-I4 style front-end

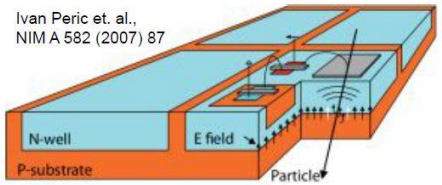
Collaborators welcomed in all areas (especially ASICS design)

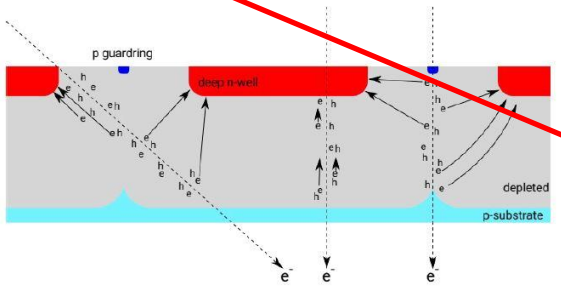
Project Proposals on large-fill factor HVCMOS sensors

Heiko Augustin for the Heidelberg HV-MAPS group
Physikalisches Institut Heidelberg

Two Proposals

1. Evaluation of new process options for large-fill factor HVCMOS sensors
2. Internal Gain Layer for HVCMOS sensors





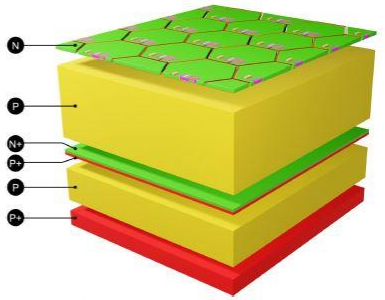
Evaluation of new process options for large-fill factor HVCMOS sensors

Explore Xfab

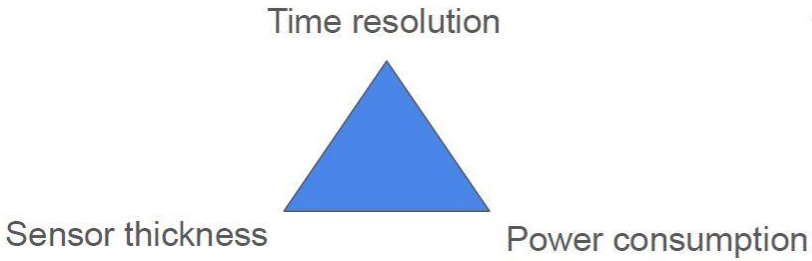
- 180nm node HVCMOS process
  → Affordable on Institute Level
- Variety of other processes and smaller nodes
- MPW/MLM possible via Europractice

Internal Gain Layer for HVCMOS sensors

- **State-of-the-Art**
  Prove-of-Principle in picoAD project
  Layer gain of 23 achieved
- **Potential in HVCMOS**



https://doi.org/10.1016/j.nima.2022.167807



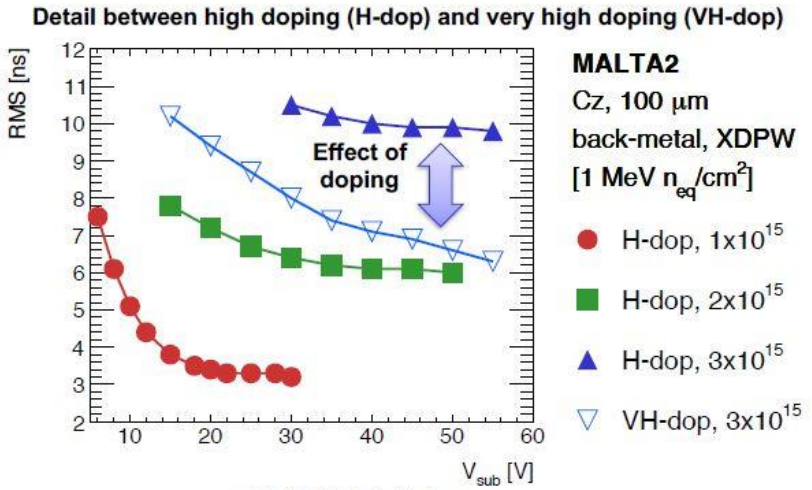
Radiation hard read-out architectures

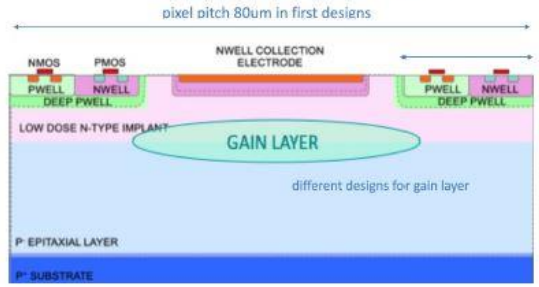
C. Solans
1st DRD3 week on Solid State Detectors R&D
18 June 2024

Proposal to DRD3 WG1

DRD3

- 4 months: resubmission Mini-MALTA3
  - Evaluate ultra-high doping (UH-dop) of n-layer
  - Very-high doping (VH-dop) improves wrt high doping (H-dop) after 3e15 n/cm2 Eur. Phys. J. C 83 (2023) 58
- Next 12 months: submission MALTA3
  - Demonstrator larger than 2x2 cm2
  - Optimized PLL for time tagging below 1 ns
  - Reduce the number of serial lines to the chip
  - Full command protocol for chip configuration
  - Optimize number of bits per hit
  - Multiple serial outputs from single chip
- Next 24 months:
  - Evaluate alternative pixel designs: CASSIA?
  - Evaluate alternative group geometries
  - Large area modules: interconnection designs





More details: "interconnections and multi-chip flex developments" (WG7 A. Sharma)

CMOS Active SenSor with Internal Amplification – CASSIA

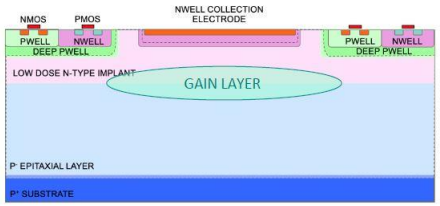
Tomislav Suligoj, Ivan Berdalović, Borna Požar

Sebastian Haberl, Anastasia Kotsokechagia, Jenny Lunde, Heinz Pernegger

CMOS Active SenSor with Internal Amplifica

Goal:

- Active sensor with in-pixel internal gain
- CMOS-compatible technology



CASSIA – Proposal to DRD3 WG 1

miNel

First ideas for future R&D

- actual R&D plan to be further developed with project partners in the next months

Electrical and optical prototype testing

Sensor TCAD simulations

Radiation hardness testing & beam tests

Chip 1: Prototype

Small LGAD & SPAD matrices

LGADs design & optimization

LGAD control & read-out circuits

SPADs design & optimization

SPAD quenching & control circuits

Electrical and optical characterization

Chip 2: Discrete sensor & small matrices

Larger LGAD/SPAD matrices

Implementation with existing or future pixel matrices and readout architectures

Tests towards applications as tracker & timing detector

Chip 3: Large matrices

Months

1 12 24 36 48

Conclusion

- **DRD3 aims to advance the performance of monolithic CMOS, combining sensing and readout elements, tackling several challenges** (very high spatial resolution, good timing performance, high data rate, high radiation tolerance, covering large, reducing power, etc.)
- **Several Work Package projects proposed within the DRD3 research goals.**
- **In several technologies.**

DRD3.1 research goals <2027	
1.1	Position resolution: ≤3 µm
1.2	Timing resolution: towards 20 ps
1.3	Readout architectures: towards 100 MHz/cm^2, 1 GHz/cm^2 with 3D stacked monolithic sensors, and on-chip reconfigurability
1.4	Radiation tolerance: towards e16 n_{eq}/cm^2 NIEL and 500 Mrad TID
1.5	Low-cost large-area CMOS sensors

Reports from experiment-oriented developments

Applying DMAPS technology to the Upgrade of the Belle II Vertex Detector

Maximilian Babeluk

on behalf of the Belle II VTX collaboration

The OBELIX chip

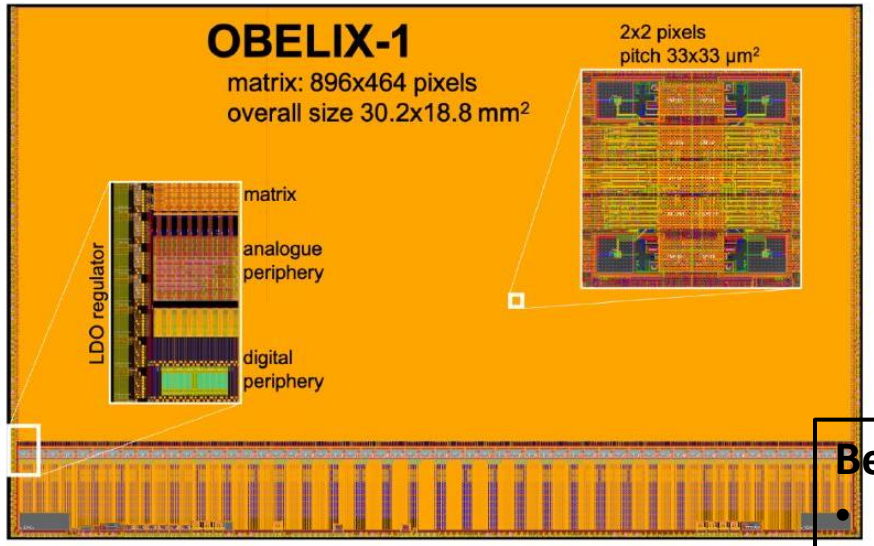
- Matrix inherited from TJ-Monopix2, size adjusted
- 464 rows and 896 columns
- Timestamp resolution: $\sim 50\,\text{ns}$
- Power: $< 200\,\text{mW/cm}^2$
- TID tolerance: 1 MGy
- NIEL tolerance: $5 \times 10^{14}\,\text{n}_{\text{eq}}/\text{cm}^2$
- Trigger latency 10 µs, Trigger rate of $> 30\,\text{kHz}$
- Hitrates up to $120\,\text{MHz/cm}^2$

⇨ Hitrate spikes due to injection background

⇨ Generous margin for all beam background scenarios

- For TJ-Monopix2 Results, see Talk from Lars Schall

OBELIX = Optimized BELle II pIXel sensor



TJ 180 nm technology

Belle II Vertex Upgrade

- Planned for LS2 (~2028)
- 5 straight layers with DMAPS
- Identical chips on all layers
- Different features enabled on different layers

DMAPS for measuring energy depositions and tracks of Galactic Cosmic Ray and Solar Energetic Particles

Presenter:
Haris Lambropoulos, Professor NKUA, lambrop@uoa.gr

HELLENIC REPUBLIC
National and Kapodistrian University of Athens
EST. 1837

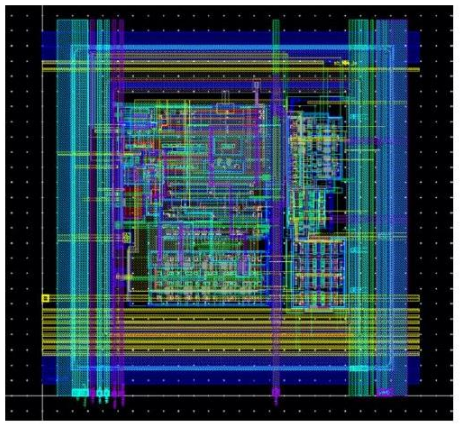
DMAPS Specifications

	LOW GAIN PIXEL	HIGH GAIN PIXEL
Pixel size	200x200 um^2	100x100 um^2
Charge range	40fC - 9pC	0.5fC -50fC
Gain	109 mV/pC	17.5 mV/fC (Q_{in}>3fC) 120 mV/fC (Q_{in}<3fC)
Idle power consumption	35nA/pixel	7.5uA/pixel
Noise charge	1.5fC	200aC
Digitization	Embedded SAR ADC 11 bits @ 10 MHz	
Communication	SPI @ 10 MHz	
Readout mode	Only hit pixels/all pixels/specific pixel	

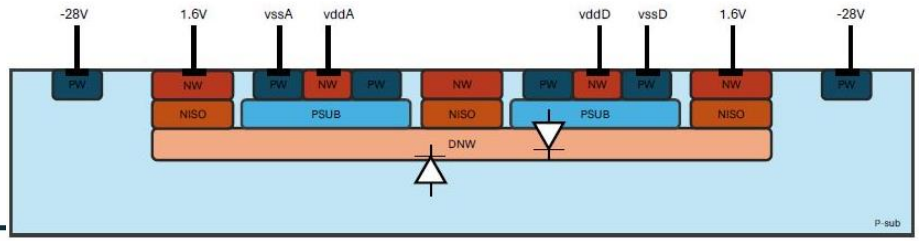
No charge amplifier !
idle power consumption ≈ 35nA @ 1.8 V = 63 nW/pixel
For 16 cm^2 covered by 40000 pixels
idle power consumption = 2.52 mW
A very low power figure !!!

idle power consumption ≈ 7.5uA @ 1.8 V = 13.5 µW / pixel
For 16 cm^2 covered by 160000 pixels
Idle power consumption = 2.16 W
High power consumption!

High Gain Pixel



- Low gain and High gain sensors combined cover a dynamic range from 0.5fC to 9pC
- Common top-level architecture and read-out circuitry for the two sensors



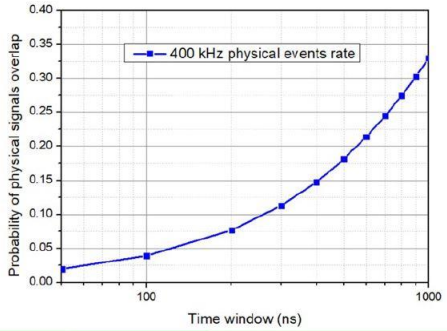
vssA = 0V, vddA = 1.8V
vssD = 0V, vddD = 1.8V

R&D of a MAPS based Inner Tracker for the STCF

Lailin Xu
University of Sci. & Tech. of China
On behalf of the STCF MAPS working group

Design targets

- Requirements on the STCF MAPS
  - Power consumption: $\leq 100 mW/cm^2$
  - Material budget per layer: $\leq 0.35\%\ X_0$
  - Spatial resolution: $\leq 30 \mu m$
  - Time resolution: $\leq 50 \mathrm{ns}$ (to deal with the pileup issue at high luminosity)
  - Time-over-threshold (TOT) measurement:
    - Time-walk correction
    - Correction of multi-coulomb scattering in track finding



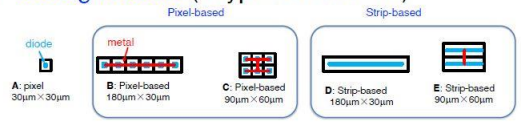
Probability of pileup(with an event rate of 400 kHz @ J/ψ, bunch crossing of 4ns):
- 4% within 100ns
- 8% within 200ns

STCF = Super Tau Charm Facility

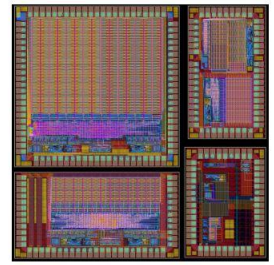
Higher priority on the power consumption than the spatial resolution

Prototype chips

- Designed 4 prototype chips based on the TJ 180nm technology
  - Chip 1: ALPIDE-like small pixels, 0/1 digital readout
  - Chip 2: large pixels ($96\mu m \times 60\mu m$, Strip-based + Pixel-based) with TOA+TOT readout
  - Chip 3: large pixels ($170\mu m \times 31\mu m$, Strip-based + Pixel-based) with TOA+TOT readout
  - Chip 4: 3T analog readout (5 types of sensors)



	Chip1	Chip2		Chip3		Chip4
Pixel size (μm×μm)	28.1x30.1	96.4x59.6		170.0x31.0		Mixed
Sensor	ALPIDE-like	Strip-based	Pixel-based	Strip-based	Pixel-based	Mixed
Pixel array	16x30	8x12	8x12	60x8	60x7	Mixed
Readout	Token	Token		Token		Analog readout
ToA & ToT	X	√		√		X



Total area: 5 mm×5 mm
Submitted in 2024 Q1

Reports from “generic” R&D

Large fill factor DMAPS development at PSI

Hans-Christian Kästli

May MPW Submission

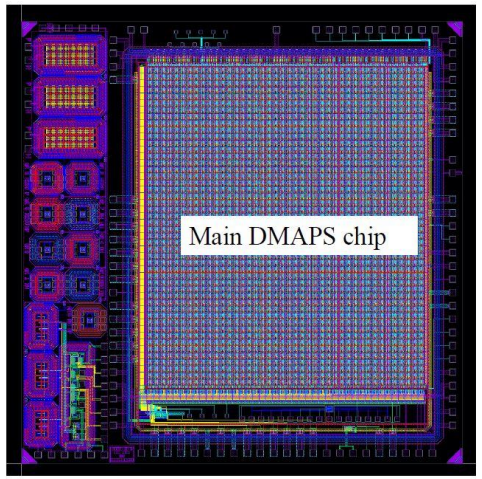
- Tape out date was May 6 2024
- MPW with 5x5mm² area
- 4x5 mm² DMAPS chip
- 1x5mm² sensor test structures
- 6 metals, deep N-well for charge collection and isolation, deep P-well for isolation
- High res wafers (~3 kOhm cm) supplied by LFoundry
- Post processing:
  - Thinning to 150 um:~12ke- signal (thinner sensors possible, but risk of breaking wafer increases)
  - backside p+ implant (much more uniform drift field, overdepletion possible→velocity saturation. Good for timing)
  - backside metalisation (protection from very sensitive back side)

DMAPS

Sensor variations

Guard ring variations

Edge TCT



7

DMAPS development at PSI 17. June 2024 8

DMAPS chip Panther

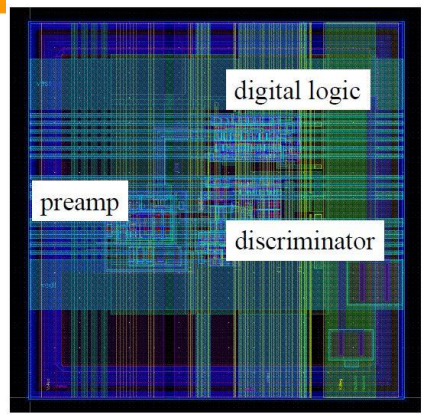
- 75µm x 75µm pixel.
- 48 rows, 3x14 columns:
  - 3 flavors of preamps, optimized for best timing, lowest power and highest S/N
  - No universally best preamp possible. Need to choose/optimize for each specific application
- Pixel has preamp, tunable discriminator, digital logic (kept minimal) and S&H circuit with analog PH readout
- TDC per column
- Triggered sequential, zero-suppressed readout
- Trigger output
- Most digital activity moved to col/row periphery. X-talk is a major issue in this technology!
- Enormous effort made to shield/decouple signals from extremely sensitive input node → my main concern

DMAPS development at PSI 17. June 2024

General R&D on DMAPS for future applications in smaller experiments:

- For in-house experiments at PSI
- Also applications outside physics
- Main motivation is low material budget
- Typical specifications are: relatively low data rates, low radiation tolerance, low-power and timing resolution of O(100-200ps)

LF15A pixel cell



- 75µm x 75µm pixel
- 3 flavours of preamps
- Discriminator with global threshold and 3 local trim bits, mask bit
- Sample & hold circuit for analog PH readout
- Injection circuit, analog and digital (for timing calibration)
- Column length: 48 pixel, ~0.36mm

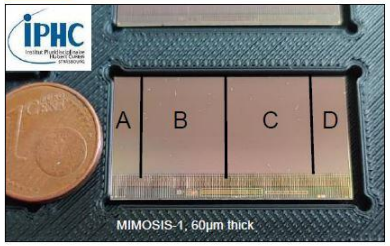
DMAPS development at PSI 17. June 2024 10

UK Research and Innovation UNIVERSITY OF LIVERPOOL

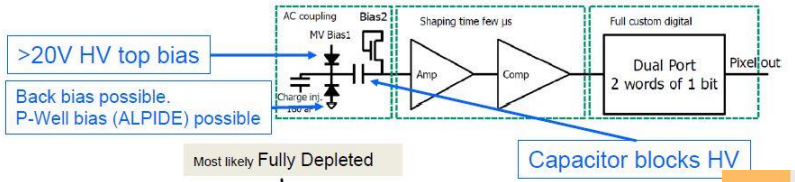
Research on CMOS MAPS at GSI/FAIR – Status and Next Step

M. Deveaux, GSI

The state of the art: MIMOSIS-1 (inspired by ALPIDE)



Size: 504 x 1024 pixels (27x30µm²), 5µs time binning
Full integrated: 20 MHz/cm² (80 MHz/cm² for 35µs), ~70mW/cm²
Fully depleted: >20V top bias



Most likely Fully Depleted

Standard | Rad. hard, candidate 2 | Rad. hard, candidate 1

MIMOSIS-1: 25 µm epitaxial layer. MIMOSIS-2.1: 25µm + 50µm epitaxial layer => stay tuned.

Micro Vertex Detector (MVD) of CBM

Summary and conclusion

GSI, IPHC and Goethe University Frankfurt are developing MIMOSIS:
- ✓ Fully depleted, >10^{14} n_{eq}/cm².
- ✓ 5 µm spatial resolution.
- ✓ 5 µs time binning.
- ✓ 20 MHz/cm² (80 MHz/cm² peak).
- ✓ Proven tolerance to heavy ion impacts.

Sensor design far advanced, expect final sensor within 2 years.

GSI intends to find partners to develop (at best):

- One sensor with tunable performance (power vs. rate).
- An integration toolset (DAQ, mechanics, software)…

…suited for multiple applications and small teams of end users at and beyond FAIR.

Guess-timate of sensor requirements (to be scrutinized)

Thanks to:
IPHC, Uni-Frankfurt, GSI (CBM-MVD) collaboration:
Julio Andary[1], Benedict Arnoldi-Meadows[1], Ole Artz[1], Jérôme Baudot[2], Grégory Bertolone[2], Auguste Besson[2], Norbert Bialas[1], Roma Bugiel[2], Gilles Claus[2], Claude Colledani[2], Hasan Darwish[1,2,3], Michael Deveaux[3], Andrei Dorokhov[2], Guy Dozière[2], Ziad El Bitar[2], Ingo Fröhlich[1,3], Mathieu Goffe[2], Fabian Hebermehl[1], Abdelkader Himmi[2], Christine Hu-Guo[2], Kimmo Jaaskelainen[2], Oliver Michael Keller[6], Michal Koziel[1], Franz Matejcek[1], Jan Michel[1], Frédéric Morel[2], Christian Müntz[1], Hung Pham[2], Christian Joachim Schmidt[3], Stefan Schreiber[1], Matthieu Specht[2], Dennis Spicker[1], Joachim Stroth[1,3,4], Isabelle Valin[2], Yue Zhao[2], Roland Weirich[1] and Marc Winter[2,5]
[1]Goethe-Universität Frankfurt, Germany, [2]Université de Strasbourg, CNRS, IPHC UMR 7178, Strasbourg, France
[3]GSI Helmholtzzentrum für Schwerionenforschung GmbH, [4]Helmholtz Forschungsakademie Hessen für FAIR,
[5]IJCLab, UMR9012 – CNRS / Université Paris-Saclay / Université de Paris, France, [6]FIAR GmbH,Germany
ALICE@GSI: Silvia Masciocchi et al.

	MIMOSIS	CBM tracker upgrade	CBM vertex upgrade
Spat. res.	~5 µm	~10 µm	~5 µm
Time res.	5 µs	25 ns	few 100 ns
Rad. hard.	> 3x10^{14} n_{eq} > 5 MRad	Few 10^{14} n_{eq} ~10 MRad	few 10^{14} n_{eq} few 10 MRad
Rate MHz/cm²	(20/80) (mean/peak)	(20/60) (mean/peak)	(60/180) (mean/peak)
Readout	8 x 320 Mbps	8 x 320 Mbps	~ 8 x 1 Gbps
Power	~70 mW/cm²	~ 50 mW/cm²	<100 mW/cm²

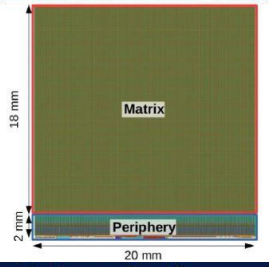
M. Deveaux, educated guess

The ATLASPIX3 CMOS pixel sensor and module performance

Attilio Andreazza - Università di Milano and INFN

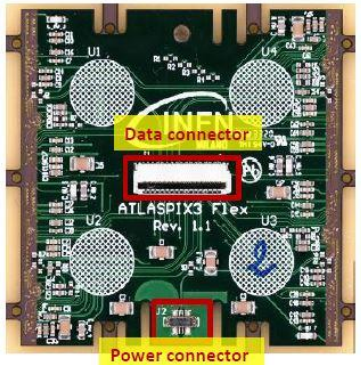
ATLASPIX3

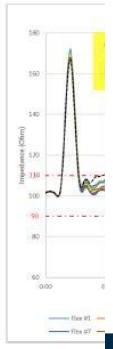
- **ATLASPIX3 general features**
  - **TSI 180 nm HVCMOS** technology
  - full-reticle size **20×21 mm²** monolithic pixel sensor
  - 200 Ωcm substrate (other substrates up to 2 kΩcm also possible)
  - **132 columns of 372 pixels**
  - **pixel size 50×150 µm²** (25×150 µm² on recent prototypes)
  - **breakdown voltage ~-60 V**
  - up to **1.28 Gbps downlink**
  - **25 ns timestamping**

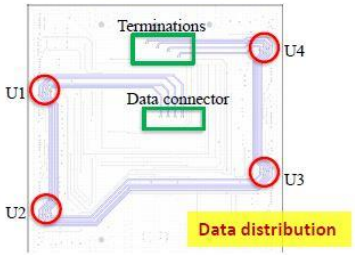


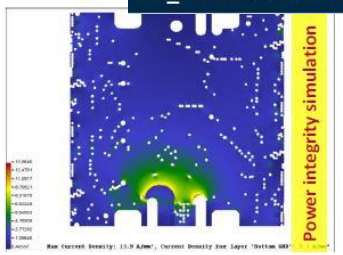
Module concept

- **Readout unit based on 4 chips**
  - shared services among 4 sensors by common power connections and configuration lines
  - benefits of in-chip regulators to reduce connections
  - avoids complications with stitching
  - design based on ATLAS quad-modules
- **Two configuration options**
  - command decoder (LVDS, default)
  - SPI (backup)
- **4-layer flex hybrid**
  - 2 power layers
  - 2 signal layers, impedance-matched lines

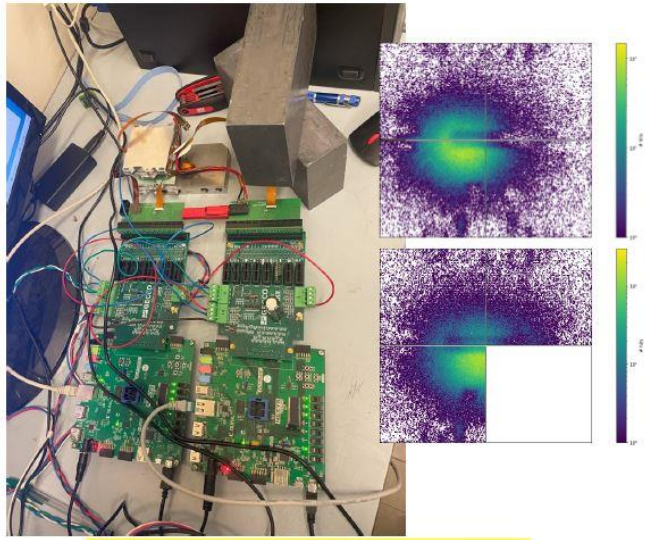




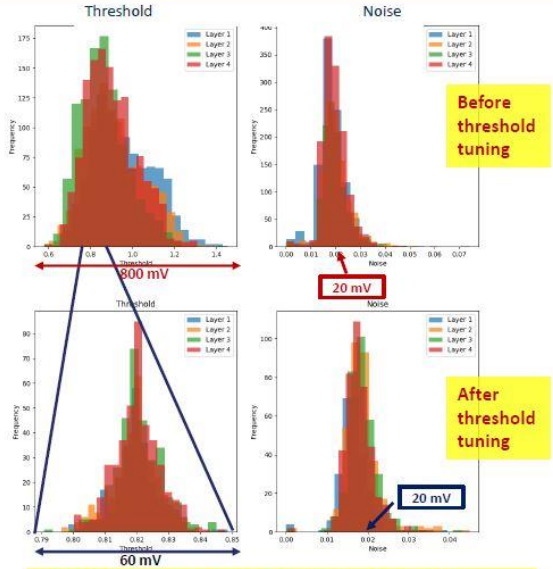




Quad-module performance



Two modules taking data with a 90Sr source
Visible are the shadows of the data connectors

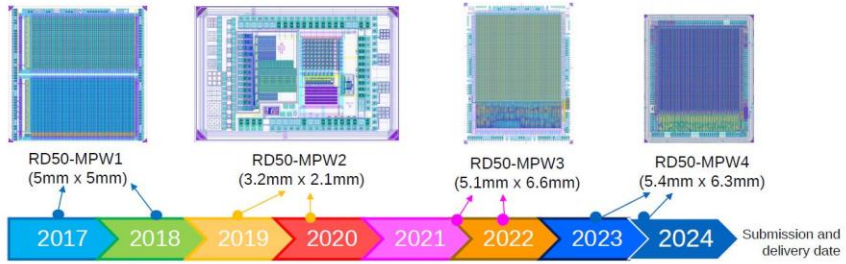


Threshold tuning and noise measurement on modules
No change in performance compared to single chips

Characterization of the RD50-MPW4 HV-CMOS pixel sensor

Bernhard Pilsl (HEPHY), Harald Handerkas (HEPHY)
on behalf of the (former) CERN RD50 CMOS working group

RD50 DMAPS Series

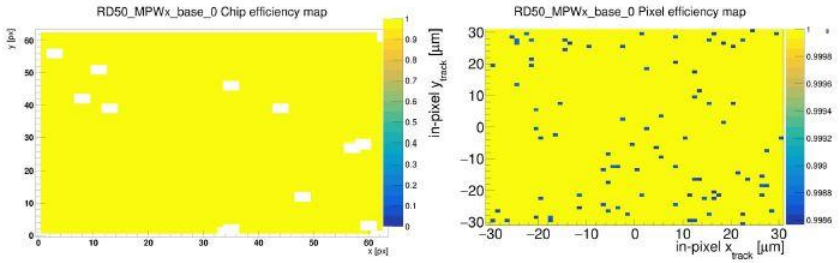


- HV-CMOS sensors fabricated in *LFoundry* 150nm process
- **Goals**: Evaluation of technology for
  - Radiation hardness
  - High granularity
  - Timing performance

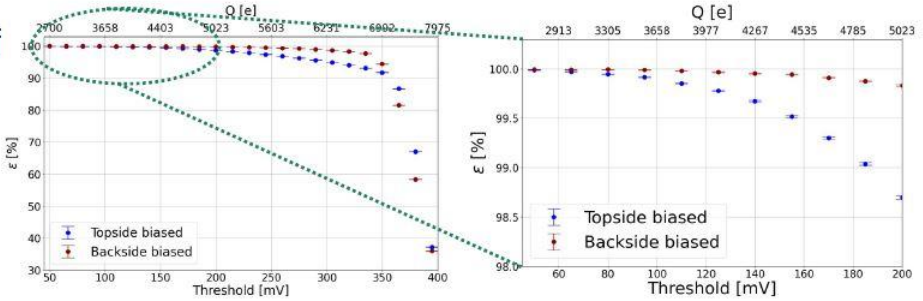
2

Efficiency

- Total efficiency > 99.99% evaluated
  - V_{Bias} = -190V
  - $Q_{Thr} \approx 2700e^-$
- Homogeneous in-pixel efficiency



- Efficiency >99% up to threshold of O(5000e$^-$)
  - Backside biased sample working better at high thresholds (compared to topside biasing)



Adaptation and Modularization of MPW4 Firmware for Integration into the Caribou Boreal Architecture: A Pilot project

J. Jiménez-Sánchez[1], F.R Palomo Pinto[1], Y- Otarid[2], J.M. Hinojo-Montero[1], H.Steininger[3], B.Pilsl[4], F. Muñoz-Chavero[1]

Caribou System Architecture

1) System-on-Chip (SoC) board

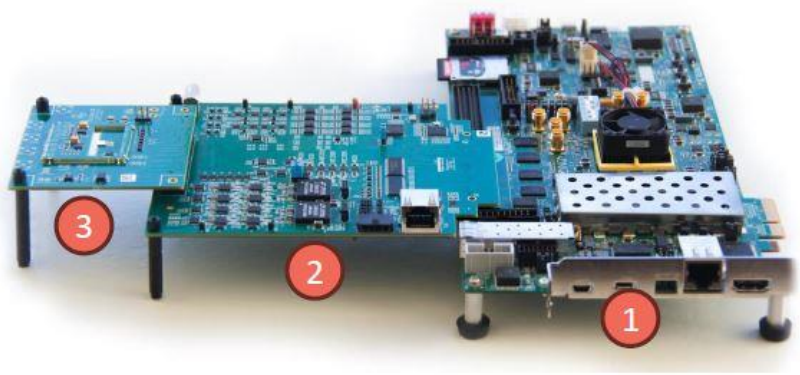
- ie: Xilinx ZC706 evaluation board
- Embedded CPU runs DAQ and control software
- FPGA runs custom firmware for detector control and readout

2) Control and Readout (CaR) interface board

- Physical interface from SoC to detector
- CaR – SoC connection extendable via FMC cable

3) Detector chip board

- Custom low-cost PCB



Current Caribou

	Legacy	Boreal Pilot project
Hardware	ZC-706	ZCU-102/ZC-706
Firmware	Propietary	Boreal Caribou
Software	Peary	Peary (Boreal adapted)
GUI	Propietary	Propietary (Boreal adapted)

Main goal is to organise into modules and adapt the RD50-MPW4 current firmware to the Caribou's new Boreal firmware architecture

RESULTS AND PERSPECTIVES OF THE MONOPIX2 DEPLETED MONOLITHIC ACTIVE PIXEL SENSORS

Lars Schall, Marlon Barbero, Pierre Barrillon, Christian Bespin, Patrick Breugnon, Ivan Caicedo, Yavuz Degerli, Jochen Dingfelder, Tomasz Hemperek, Toko Hirono, Fabian Hügging, Hans Krüger, Konstantinos Moustakas, Patrick Pangaud, Heinz Pernegger, Petra Riedler, Piotr Rymaszewski, Philippe Schwemling, Walter Snoeys, Tianyang Wang, Nobert Wermes, and Sinuo Zhang

UNIVERSITÄT BONN

Conclusion & Outlook

LF-Monopix2:

- Excellent radiation hardness without significant performance degradation up to 2 x 10^{15} neq/cm^2 NIEL fluence and 100 Mrad TID
  - Further irradiation up to 5 x10^{15} neq/cm^2 NIEL fluence planned

TJ-Monopix2:

- Very low noise and low threshold operation with excellent spatial resolution
- >99 % hit-detection efficiency and very high in-time ratio >99 % within 25 ns
- Fully functional after 100 Mrad TID
  - Characterization of irradiated samples up to 1.5 x 10^{15} neq/cm^2 NIEL fluence ongoing

Perspectives:

- New DMAPS based on TJ-Monopix2 under development for Belle II VXD upgrade -*talk by M. Babeluk*

Radiation hardness and timing performance of MALTA monolithic Pixel sensors in Tower 180 nm

Lucian Fasselt

17 June 2024

Summary

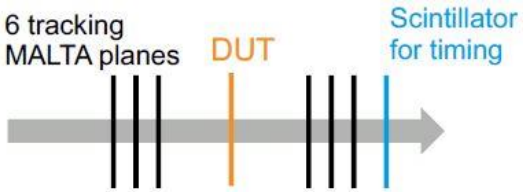
MALTA beam telescope @SPS with $\sigma_s = 4.5\ \mu m$ & $\sigma_t = 2.1$ ns

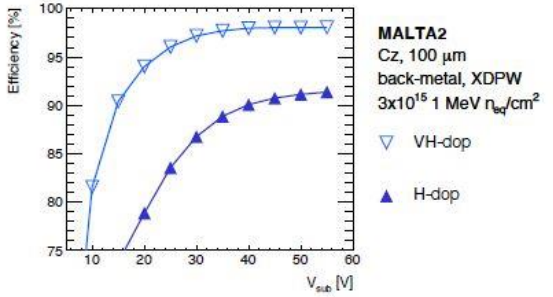
MALTA2 shows radiation hardness up to 3×10^{15} n_{eq}/cm^2
- > 98% efficiency
- > 95% of clusters collected within 25 ns (LHC bunch crossing window)
- Fulfills ATLAS ITk requirements for efficiency and noise

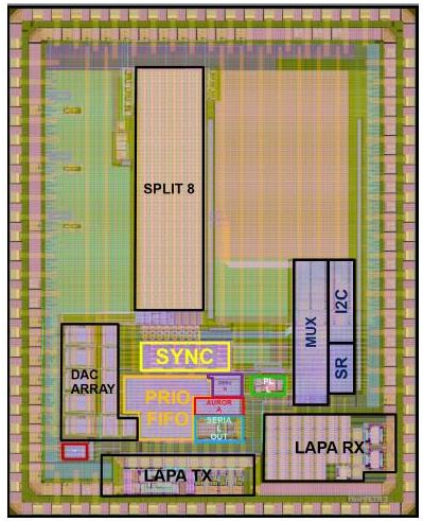
Depletion depth studies:
- Edge-TCT
- Grazing angle studies
- Amplitude reconstruction from binary hit data

MALTA3:
- Time-stamping logic on chip @ 1.28GHz aiming for **sub-nanosecond** timing
- Serialised data output in view of future detector integration

Future developments:
"Radiation hard read-out architectures" (WG1 C. Solans) Tue 9:00
"Interconnections and multi-chip flex developments" (WG7 A. Sharma) Wed 13:30







Mini-MALTA3
- 5×4 mm^2 demonstrator with 64 × 48 pixels
- Pixel size 36.4 × 36.4 μm^2 (same as MALTA2)
- Same front-end as MALTA2, no clock over the matrix
- Integrate **time-stamping** and **data serialiser on chip** in periphery
- Time-stamping logic at 1.28 GHz (for MALTA2 done in FPGA)
  → **aiming for sub-nanosecond** on-chip timing resolution
- Synchronization memory with 0.78 ns time resolution
- Fast clock generation with STFC PLL from 80 MHz clock
- Serialized high-speed output

Development of MAPS using 55nm HVCMOS Process for future tracking detectors

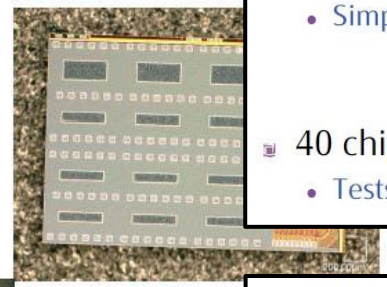
Yiming Li (IHEP, CAS)
On behalf of the COFFEE development team

Development in small feature size HVCMOS

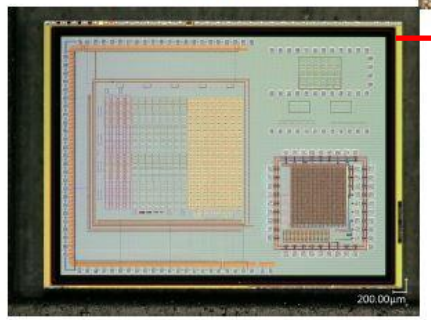
- HLMC 55nm HVCMOS process
  - Cancelled MPW plan in 2022
- SMIC 55nm Low-Leakage process
  - Not HV, yet with a similar deep n-well structure
  - MPW submitted in Oct 2022 in normal wafer
  - COFFEE1 received in Apr 2023
- SMIC 55nm HVCMOS process
  - HVCMOS process, with 1kΩ ·cm wafer
  - MPW submitted in Aug 2023
  - COFFEE2 received in Dec 2023

CMOS SENSOR IN FIFTY-FIVE NM PROCESS

COFFEE1



COFFEE2



- MPW submitted in Oct 2022 with SMIC 55nm Low Leakage process
  - NB: not an HV process! Yet it has similar deep N well separating the transistors and the sensor part
  - 3 × 2 mm² in area
  - Variation of passive diode arrays
  - Simple amplifiers added
- 40 chips received in end Apr 2023
  - Tests going on now

- MPW with SMIC HV 55nm
  - High-res wafer of 2k or 1k Ωcm available
  - Real validation of the sensor
  - 4mm * 3mm in area
  - Passive arrays similar as COFFEE1
  - Two pixel arrays with in-pixel amplifier and more digital design
  - Submitted in Aug 2023
  - Received in Dec 2023

NB: All dimensions mentioned in 55nm process from now on always has a scale factor of 0.9.
As it is scaled down from 65nm masks

17 Jun 2024

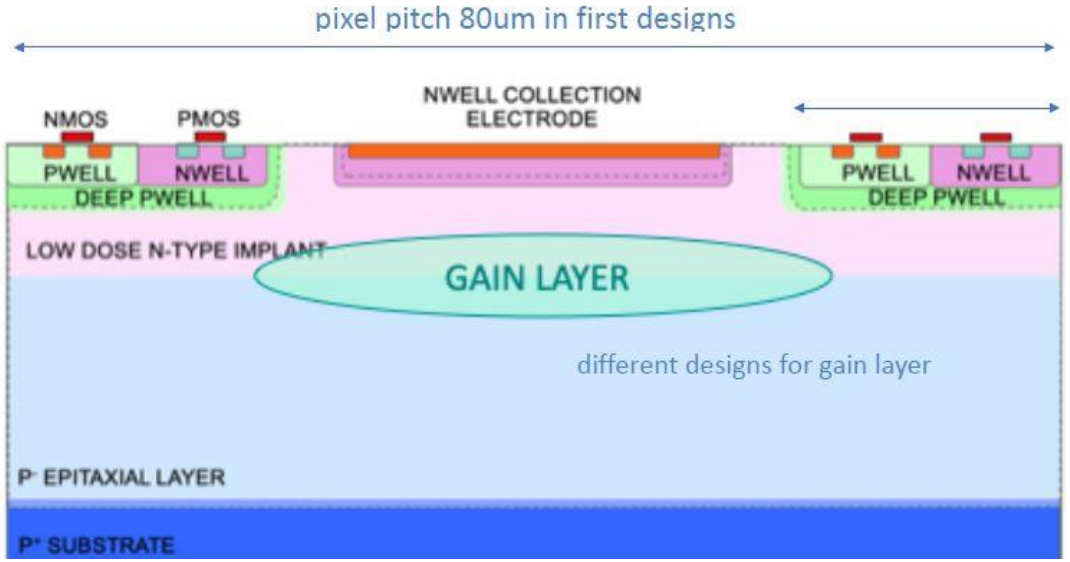
CMOS Sensors with internal gain

CASSIA **C**MOS **A**ctive **S**en**S**or with **I**nternal **A**mplification

Sebastian Haberl, Anastasia Kotsokechagia, Jenny Lunde,
Heinz Pernegger / CERN EP-ADE-TK
I. Berdalović, Borna Požar, T. Suligoj / FER University Zagreb

Initial design idea for sensor with internal gain

- inspired by development of LGAD sensors but applied to industrial CMOS process (200mm wafer, 0.18um CMOS process with high production volume)
- **"Tracker-like" pixels with 80um pitch** (first prototype)
  - larger round electrodes (~40um diagonal) but also enlarged area for analog and digital circuit
  - DPW for full CMOS electronics in pixel already foreseen now to allow future scaling of results to larger matrix



DPW/PW space reserved for future pixel analog and digital circuits

- Pixel implant structure with internal gain for tracking, timing or time-tagging
- Inspired by development of LGAD sensors, but applied to industrial CMOS processes (180 nm CMOS)
- First prototype available and tested, aimed at studying gain layer performance as function of several process parameters

ALL-SILICON LADDER CONCEPT FOR CMOS MONOLITHIC PIXEL DETECTORS

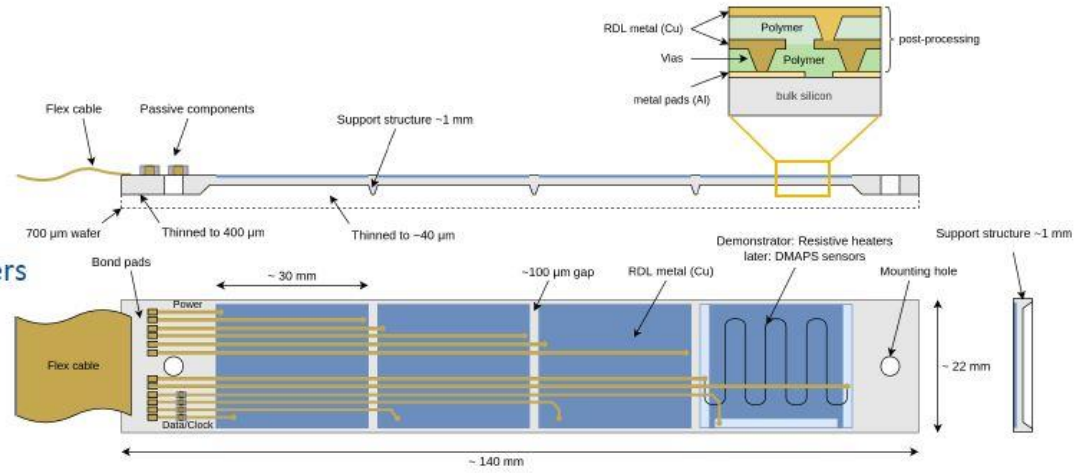
J. Dingfelder[B], J. Grosse-Knetter[G], H. Krüger[B], C. Lacasta[V], C. Marinas[V], A. Quadt[G], A. Ulm[B], M. Vogt[B]
Affiliations: U. Bonn (B), U. Göttingen (G), IFIC Valencia (V)

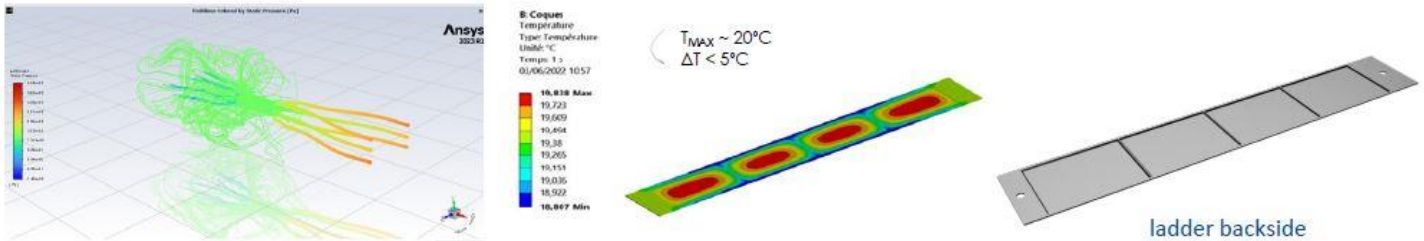
UNIVERSITÄT BONN FTD

ALL-SILICON LADDER CONCEPT

All-silicon ladder
- Single piece of silicon
- 4 sensors cut in one piece from the wafer

Post-processing of wafer
- Redistribution metal layers for data and power
- Heterogeneous backside thinning





Thermal and airflow simulations for Belle II iVTX (IJClab, Paris)

- Motivation is Belle II LS2
- Monolithic active CMOS pixel sensor OBELIX
- Also generic R&D for future colliders (e.g. FCC)

UK Research and Innovation UNIVERSITY OF LIVERPOOL

Innovations in CMOS Pixel Sensor Technology at IPHC: Projects and Future Prospects

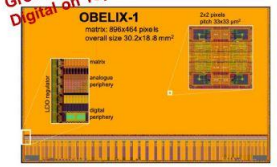
Frédéric Morel on behalf of IPHC teams

Focus on two technologies:
- Tower 180 nm is a well-established technology
- Tower 65 nm is where future cutting-edge developments are made

Application-oriented sensor in Tower 180 nm

- MIMOSIS — CBM-MVD
  - Fully designed at C4Pi
    - Collaboration with IKFrankfurt & GSI
  - 5 µm — 5 µs — 20 (70) MHz/cm² continuous read-out
    - Modified process & AC-diode (full or partial depletion)
  - Series of submission: 2017 ⟶ 2025
  - More in M. Deveaux's talk
- OBELIX — Belle II-VTX
  - Design within a wide collaboration:
    - Uni.Bergamo, Uni.Bonn, CPPMarseille, Tech.Uni.Dortmund, HEPHY-Vienna , IFIC-Valencia, INFN-Pavia, KEK-Tsukuba
  - 10 µm — 50 ns — 120 MHz/cm² triggered read-out
    - Modified process & DC or AC-diode (full depletion)
  - Started 2022: 1st version in 2024
  - More in M. Babeluk's talk

Growing experience in Digital on Top methodology

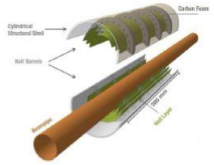


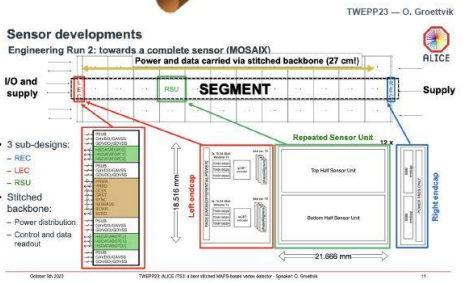
Technological R&D in Tower 180

- TIIX
  - Small size prototype (5x7 mm²) for ion tracking & identification
  - Design with: IP2I-Lyon
  - 12 µm / 10 ns / 100 kHz/cm² continuous read-out
    - linear dynamic up to ~800 ke- for energy measurement over a wide range
    - Modified process (full depletion)
  - Series of submissions: 2020 ⟶ 2024
- QUARTPIC submissions
  - Multi-project engineer runs organised by C4Pi
    - Include internal R&D with small chips
    - Mostly focus on DRD7 activities
  - 1st run 2021 (French projects + China)
  - 2nd run 2024 (French projects + CERN + China)
  - 3rd run under discussion for 2025

Ap

- MOSAIX — ALICE-ITS3
  - Wafer scale sensor ASICs with stitching
    - Ultra-thin and bendable: 50 µm
    - Tower 65 nm
  - 5 µm — 2 µs — ~6 MHz/cm² continuous read-out
  - Series of submission: 2021 ⟶ 2025
    - Large design team
  - IPHC design effort:
    - Responsibility of matrix integration (DoT)
    - Contribution in analogue biasing





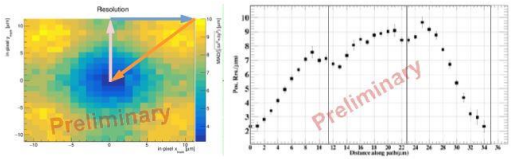
Technological R&D in Tower 65 nm: Charge collection study

- CE65 chips
  - Small matrix (2x2 mm²) exploring new process
  - Simple architecture:
    - **Analog output**
    - Rolling shutter readout
  - Variations on:
    - Process Standard—Modified—Modified with gaps
    - Diode arrangement (squared or staggered)
    - Pitchs 15—18—22.5 µm
  - Series of 2 submission 2021 and 2023
  - Partners share analysis and measurements
    - IPHC — CTU Prague – UZH Zurich

Process	Pitch (µm)	Spatial Res. (µm) Tel. res. Subtracted (2.1 µm)
GAP	22.5	~5.1
GAP	18	~4.1
GAP	15	~3.2
STD	22.5	~2.4
STD	18	~1.8
STD	15	~1.3

Preliminary

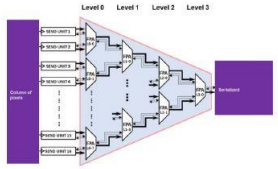
Only square diode arrangement

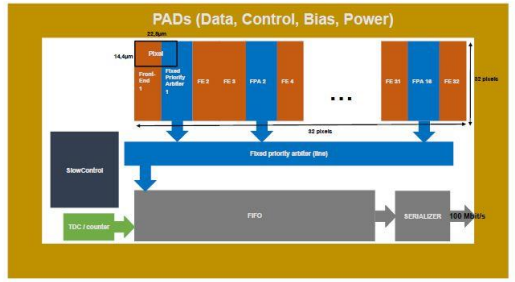


Process — GAP
Pitch — 22.6 µm

Technological R&D in Tow

- SPARC
  - Small prototype (2x2 mm²) for new matrix read-ou
  - Design with: IRFU-Saclay
    - Contribution from CERN-EP R&D & ALICE-ITS3 (DPTS pixel front-end)
  - Full asynchronous read-out logic
    - Clockless 20 ns time-stamping
    - ~10 mW/cm² in matrix
  - 1st submission 2024





UK Research and Innovation

UNIVERSITY OF LIVERPOOL

The H2M project: Porting the functionality of a hybrid readout chip into a monolithic 65 nm CMOS imaging process

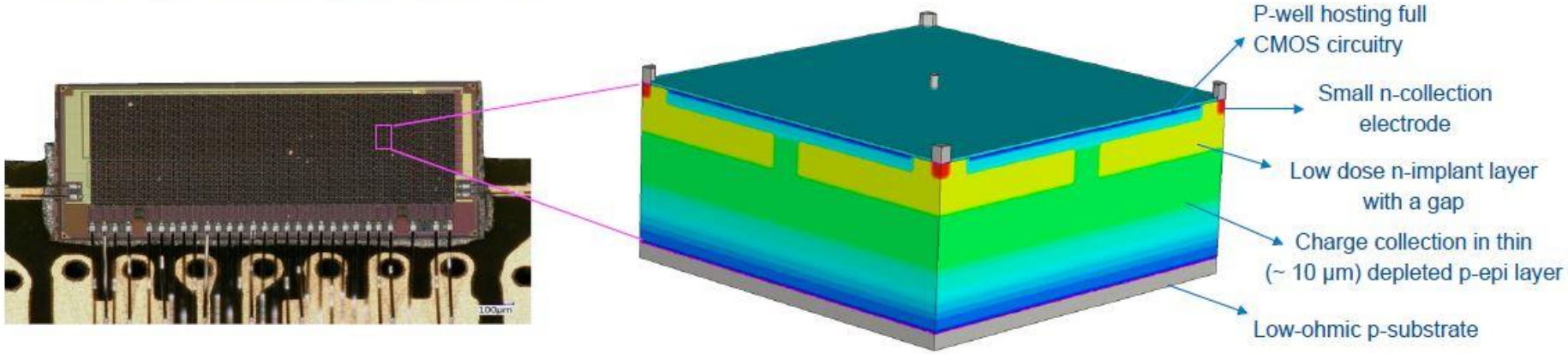
Rafael Ballabriga, Eric Buschmann, Michael Campbell, Raimon Casanova Mohr, Dominik Dannheim, Ana Dorda, Finn Feindt, **Philipp Gadow**, Ingrid-Maria Gregor, Karsten Hansen, Yajun He, Lennart Huth, Iraklis Kremastiotis, Corentin Lemoine, Stefano Maffessanti, Larissa Mendes, Younes Otarid, Christian Reckleben, Sebastien Rettie, Manuel Alejandro del Rio Viera, Sara Ruiz Daza, Judith Schlaadt, Adriana Simancas, Walter Snoeys, Simon Spannagel, Tomas Vanat, Anastasiia Velyka, Gianpiero Vignola, Håkan Wennlöf

H2M (Hybrid-to-Monolithic)

- Ports a **hybrid pixel detector architecture into a monolithic chip**.
- **Digital-on-top** design workflow.
- Manufactured in a TPSCo **65 nm CMOS imaging process**.

- **35 µm pixel pitch in 64x16 pixel matrix** (total sensitive area: 2.24 × 0.56 mm²). Total thickness ~ 50 µm.
  ↳ (p-epitaxial layer ~ 10 µm)

- Analog and digital front-end per pixel.



Conclusions

Fully functional digital-on-top sensor in a 65 nm CIS.

Calibration and characterisation of performance with laboratory and test beam measurements.

- Fully efficient operation in test beam:
  - 27 e- noise, 200 e- minimum threshold, >99.1% efficiency.
- Impact of n-wells on charge-collection efficiency observed and qualitatively confirmed by simulations.
- Timing performance dominated by sensor effects? > ~30 ns.

Outlook: investigating the possibility of backside-thinning the chips from 50 um to <~30 um, to explore impact of thickness on performance.