CEPC vertex Detector

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- Requirements
- Technology survey and our choices
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- Detailed design including electronics, cooling and mechanics
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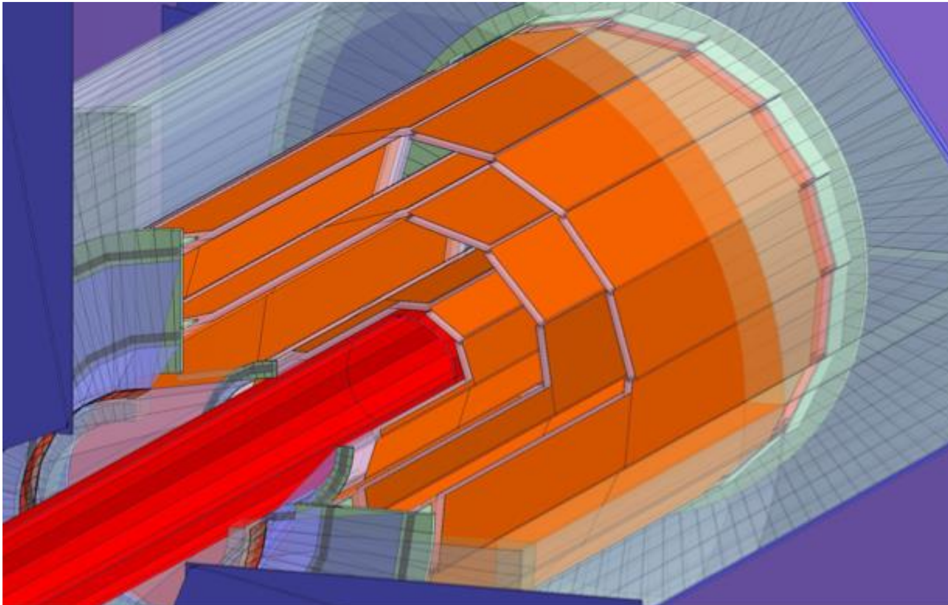
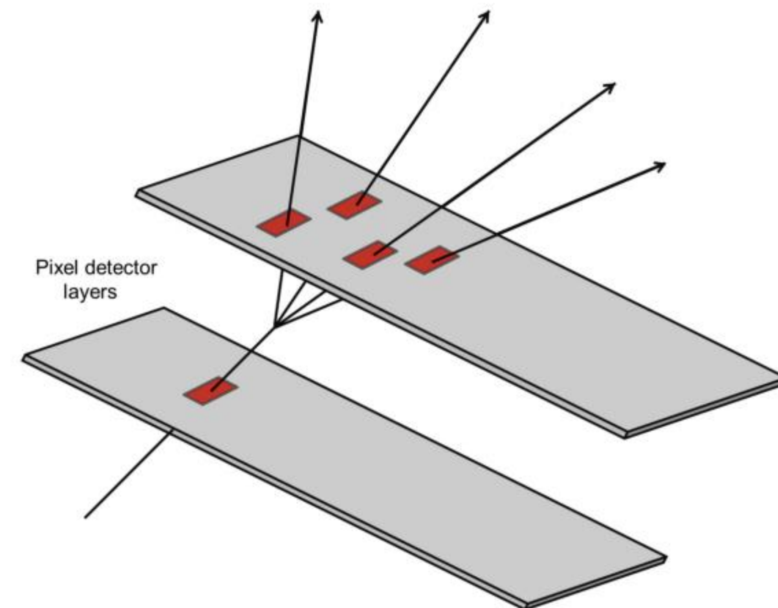
- Summary

Introduction: vertex detector

- Vertex detector optimized for first 10 years of operation (ZH, low lumi-Z)
- Motivation:
  - Aim to optimize impact parameter resolution and vertexing capability
  - Key detector for H → cc and H → gg physics, which is an important goal for CEPC





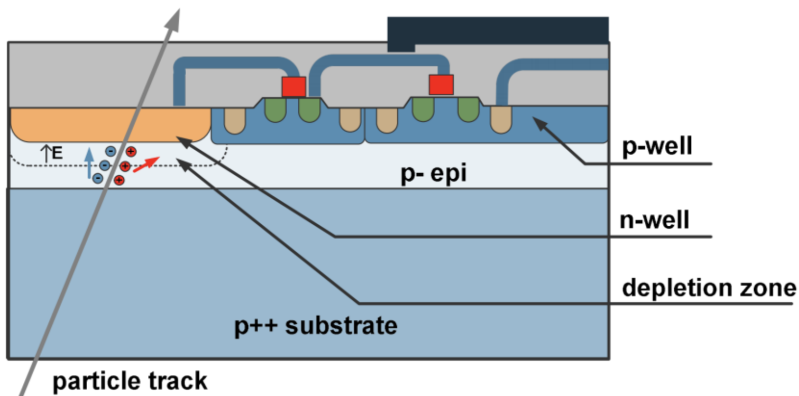
Vertex Requirement

– Inner most layer (b-layer) need to be positioned as close to beam pipe as possible
  - **Challenges:** b-layer radius (11 mm) is smaller compared with ALICE ITS3 (18 mm)
– High data rate: (especially at Z pole , ~43 MHz)
  - **Challenges**: >1 Gbps per chip high data rate especially at Z pole
– Low material budget (less than 0.15%X_0 per layer)
– Detector Cooling with air cooling (power consumption<= 40 mW/cm^2)
– Spatial Resolution (3-5 μm)
– Radiation level (~2.1 Mrad per year in average)

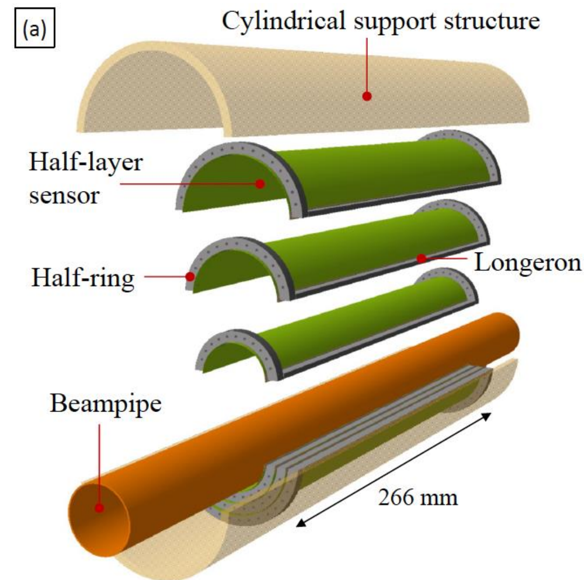
Technology survey and our choices

- Vertex detector Technology selection
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design [1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: Ladder design based on CMOS MAPS

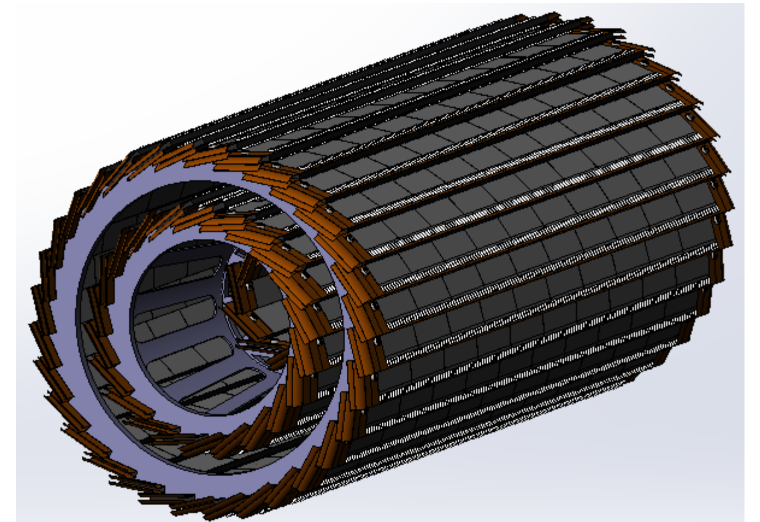
Monolithic active Pixel Sensor (MAPS)



Baseline: curved MAPS



Alternative: ladder based MAPS



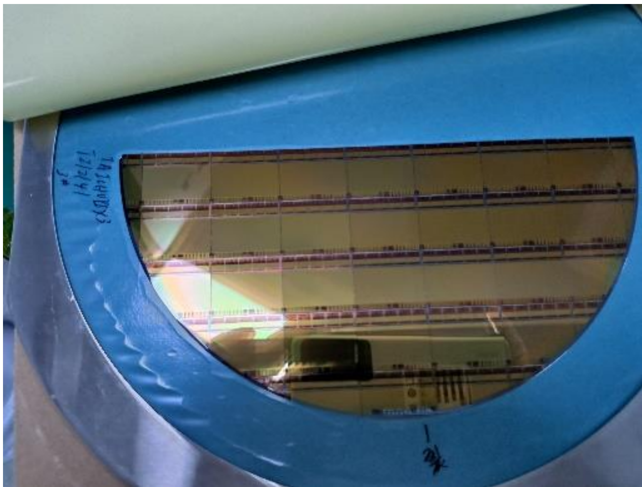
[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

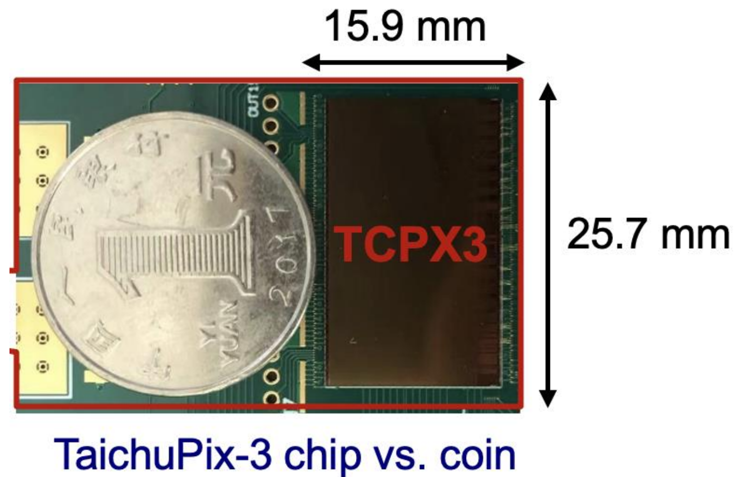
R&D status and final goal

Key technology	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180 nm CIS	TJ 65nm CIS
Detector integration	Detector prototype with ladder design	Detector with bent silicon design
Spatial resolution	4.9 μm	3-5 μm
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power
Bent CMOS silicon	Bent Dummy wafer radius ~12 mm	Bent final wafer with radius ~11 mm
Stitching	11×11cm stitched chip with Xfab 350 nm CIS	65nm CIS stitched sensor

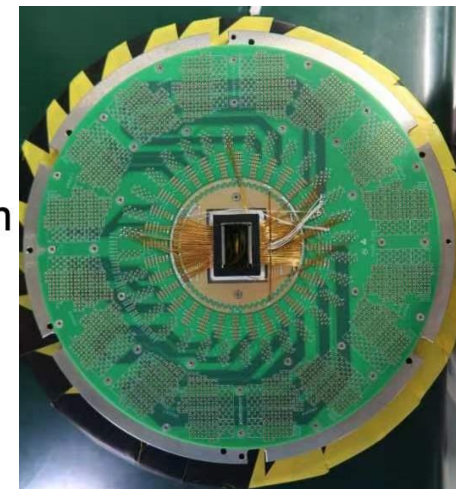
R&D efforts: Full-size TaichuPix3

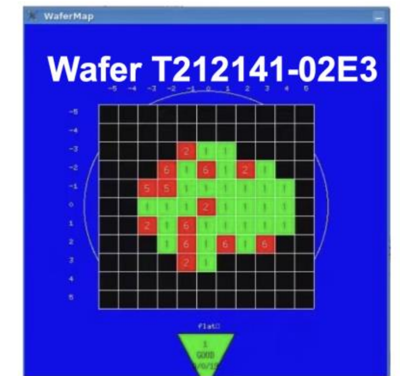
- Full reticle-size CMOS chip developed, 1st engineering run
  - 1024×512 Pixel array, Chip Size： 15.9 mm×25.7 mm
  - 25 μm×25 μm pixel size with high spatial resolution < 5 μm (@ detection eff. > 99%)
  - Process: TowerJazz 180nm CIS process
  - Fast data-driven readout (50 ns/pixel) to cope with all operation modes in CDR
    - Dead time < 500 ns, Max. hit rate 36 MHz/cm^2





TaichuPix-3 chip vs. coin

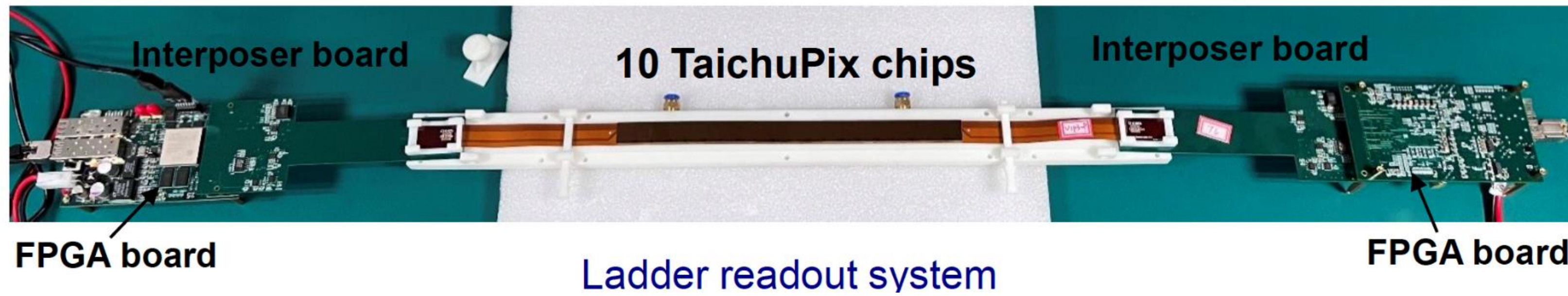




An example of wafer test result

	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	TJ 65nm CIS

R&D effort: vertex detector prototype

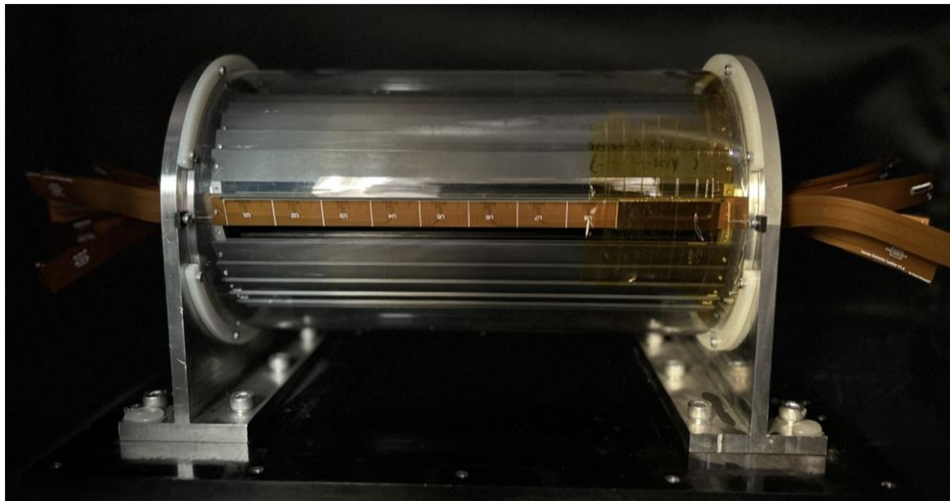


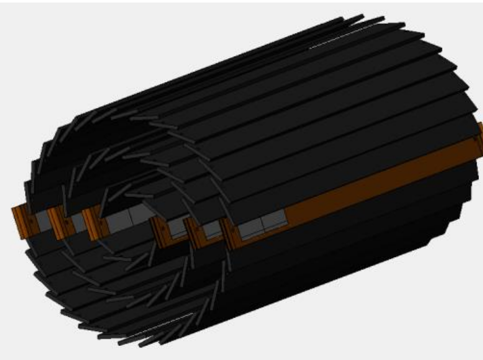
Ladder readout system

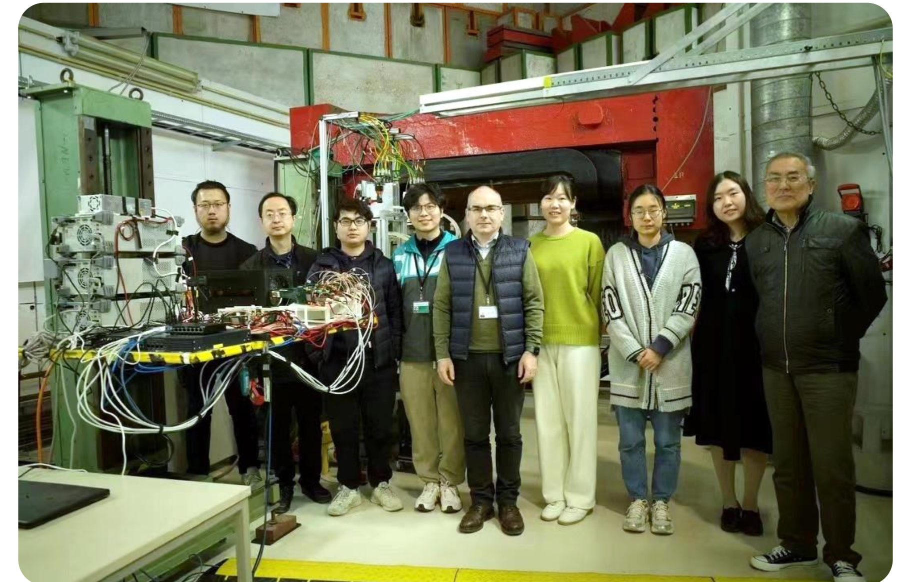
TaichuPix-based prototype detector tested at DESY in April 2023

Spatial resolution ~ **4.9 μm**

6 double-sided ladders





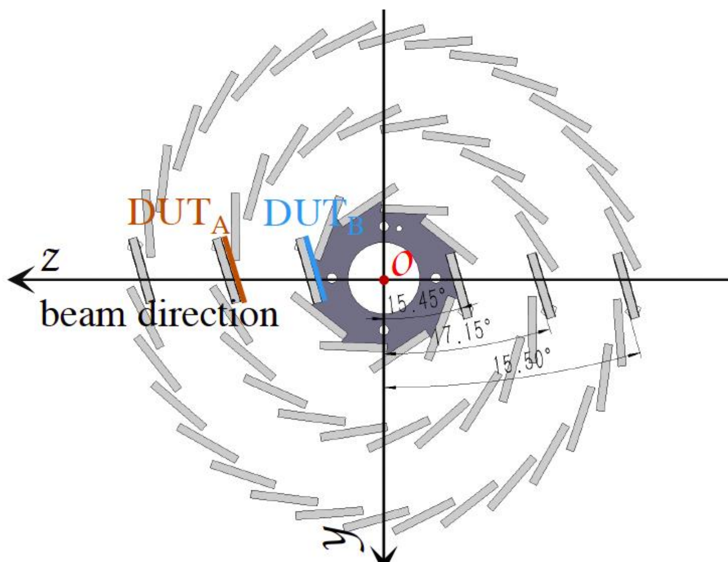


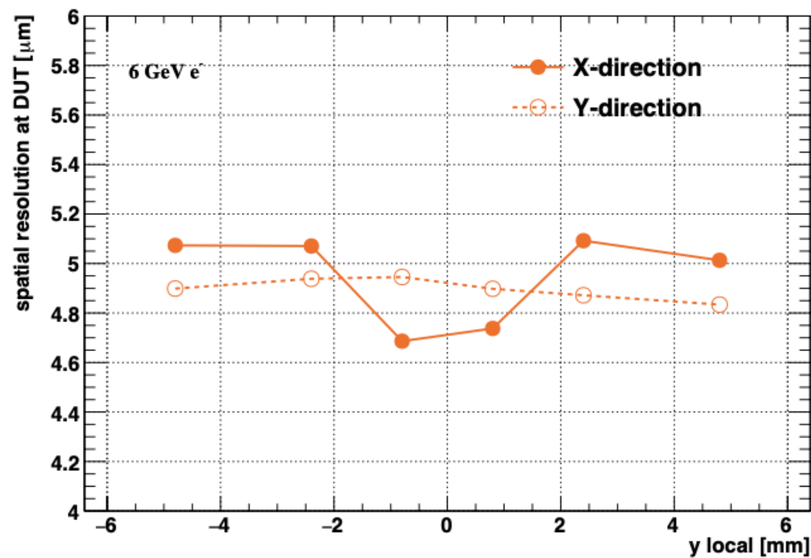
	Status	CEPC Final goal
Detector integration	Detector prototype with ladder design	Detector with bent silicon design

R&D efforts and results: vertex detector prototype beam test

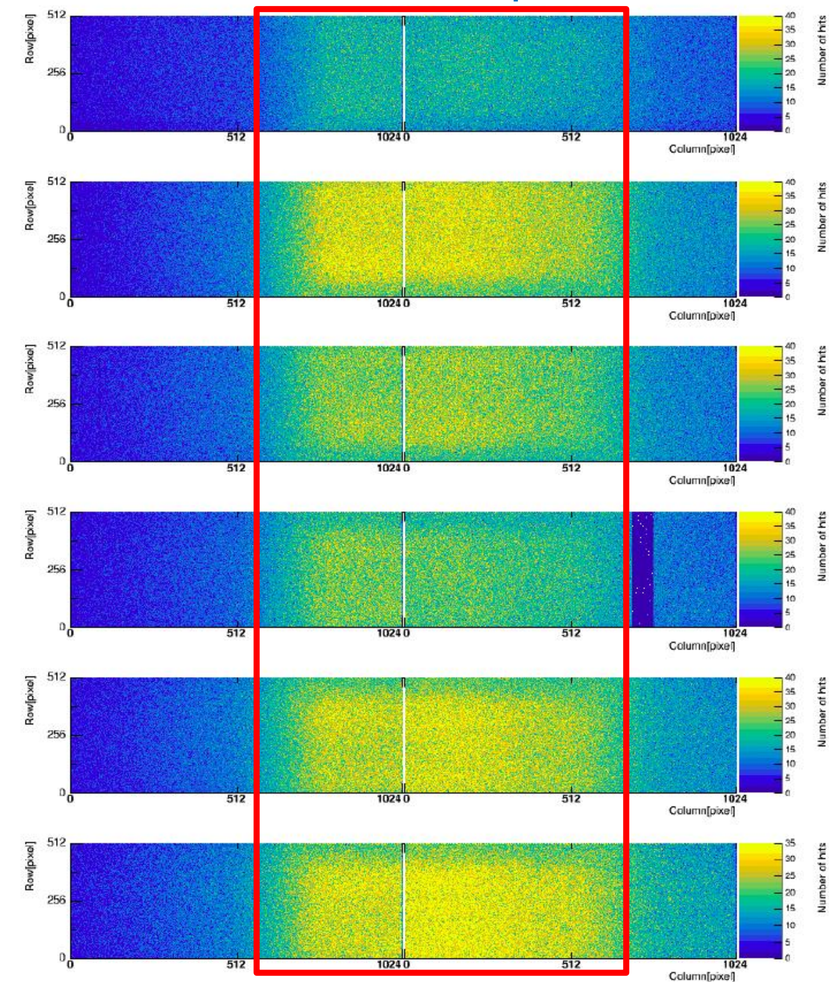
Spatial resolution ~5 μm Efficiency >99%

Hit maps of multiple layers of vertex detector





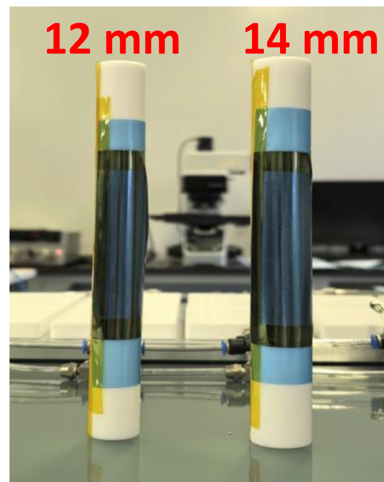
Beam spot

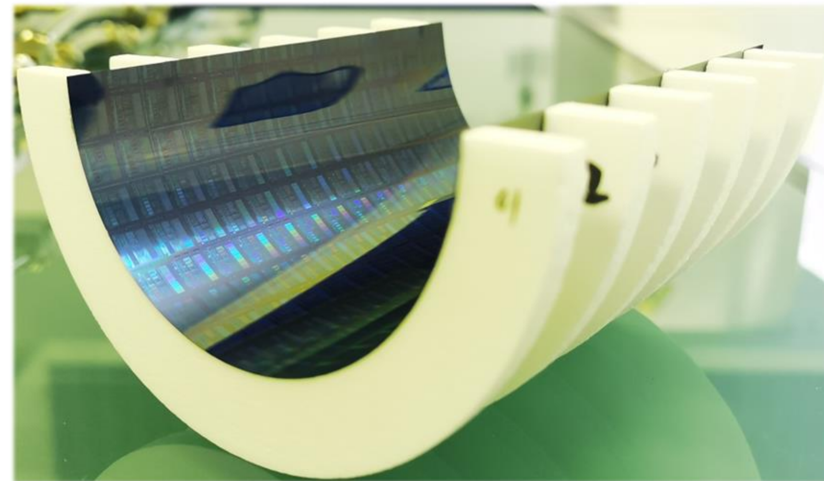


	Status	CEPC Final goal
Spatial resolution	4.9 μm	3-5 μm

R&D efforts curved MAPS

– CEPC b-layer radius (11 mm) smaller compared with ALICE ITS3 (radius=18 mm)
– Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12 mm
  - The dummy wafer has been thinned to 40 μm

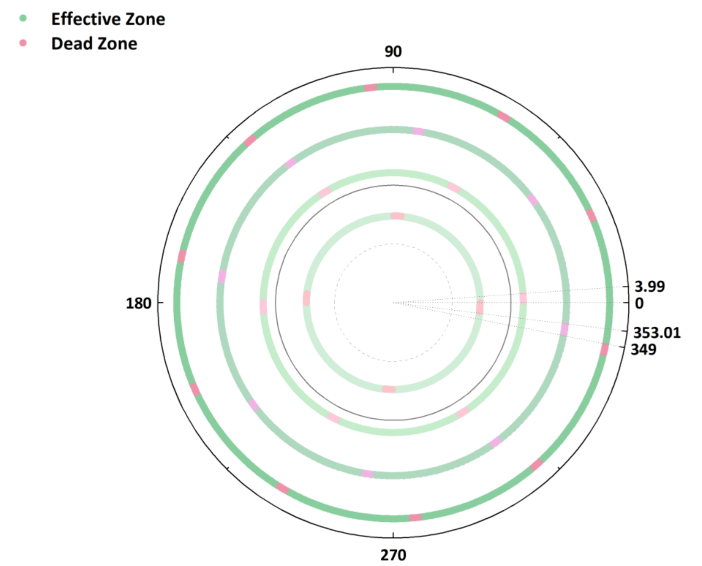




	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm

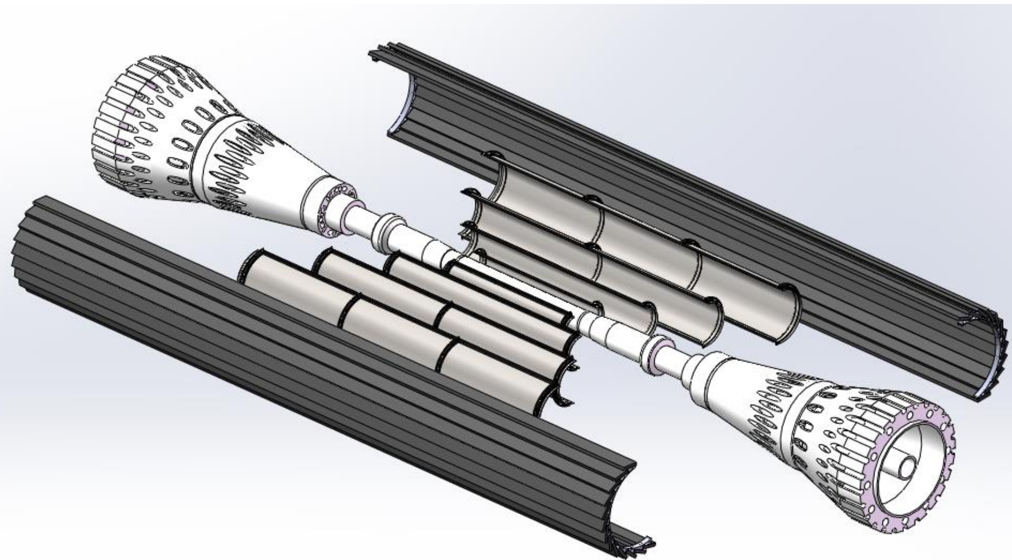
Baseline: bent MAPS

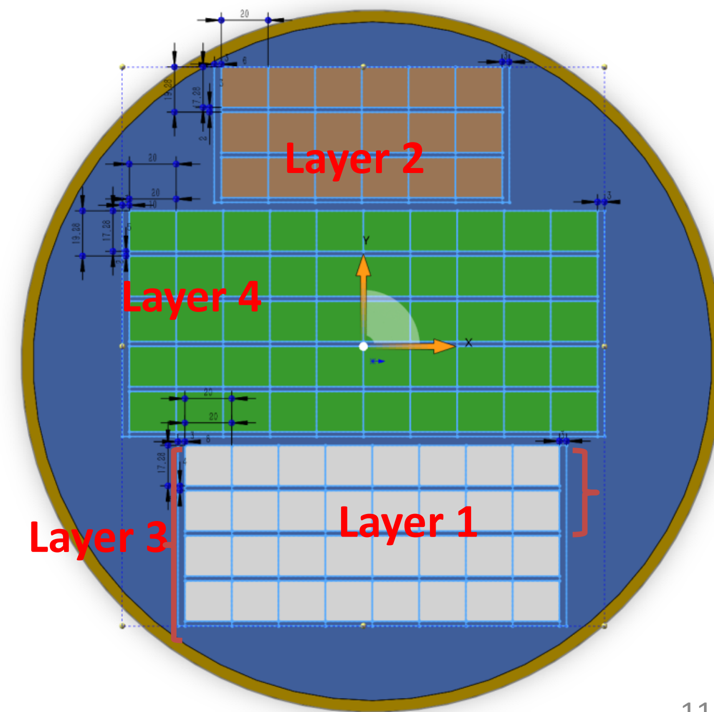
- 4 single layer of bent MAPS + 1 double layer ladder
  - Material budget is much lower than alternative option
- Use single bent MAPS for Inner layer (~0.15 m^2)
  - Low material budget 0.06% X_0 per layer
  - Different rotation angle in each layer to reduce dead area



layer	Radius	Material
Layer 1	11mm	0.06% X_0
Layer 2	16.5mm	0.06% X_0
Layer 3	22mm	0.06% X_0
Layer 4	27.5mm	0.06% X_0
Layer 5/6 (Ladders)	35-40 mm	0.33% X_0
Total		0.57% X_0

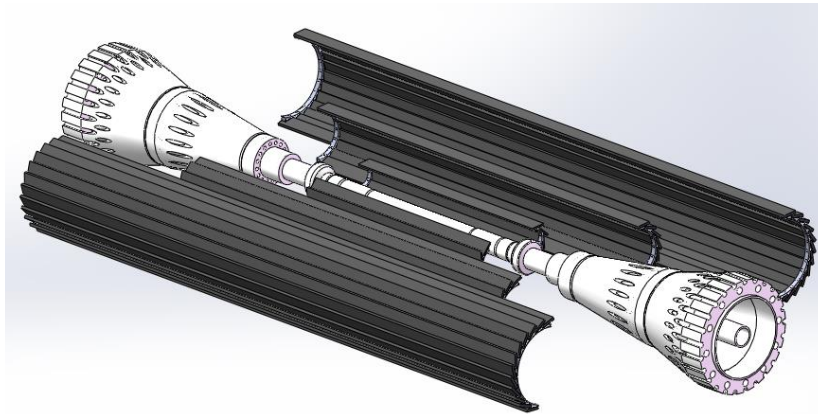
Long barrel layout (no endcap disk) to cover cos $\underline{\theta}$<=0.991



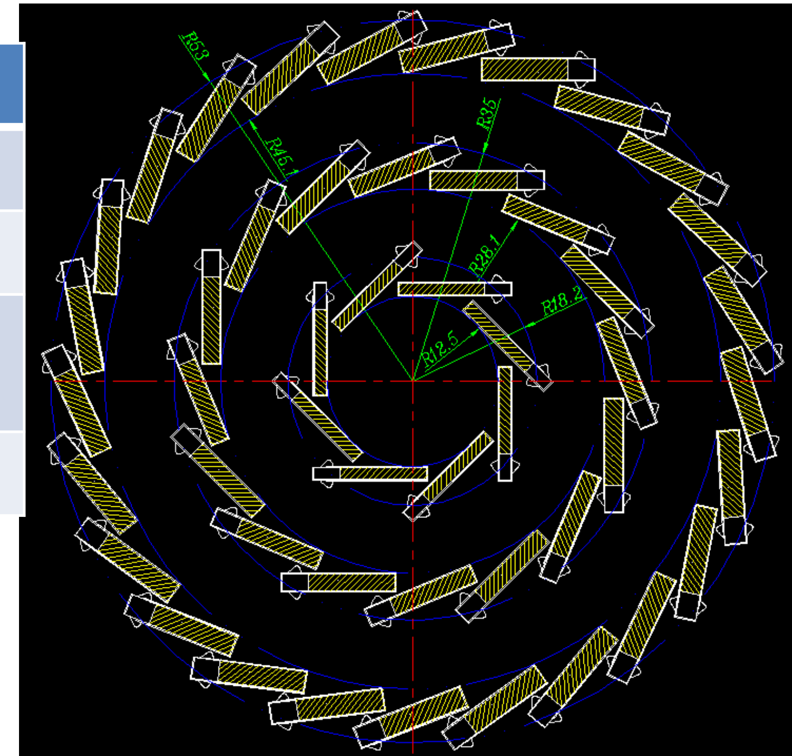


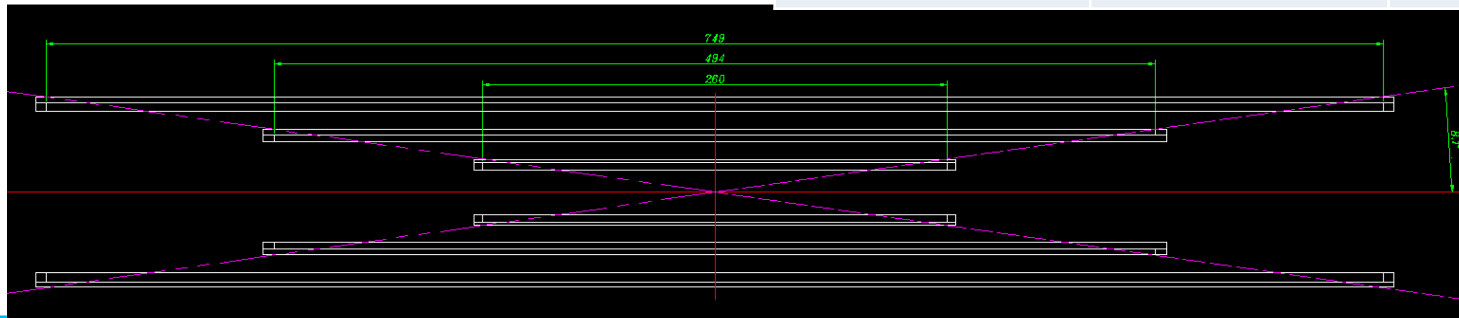
Alternative： CMOS ladder

- Alternative: CMOS chips with a long ladder layout
  - 3 double-side layer with long ladders design
  - We have built a vertex prototype based on the short ladders design
  - No effective solution for inner layer cooling yet.



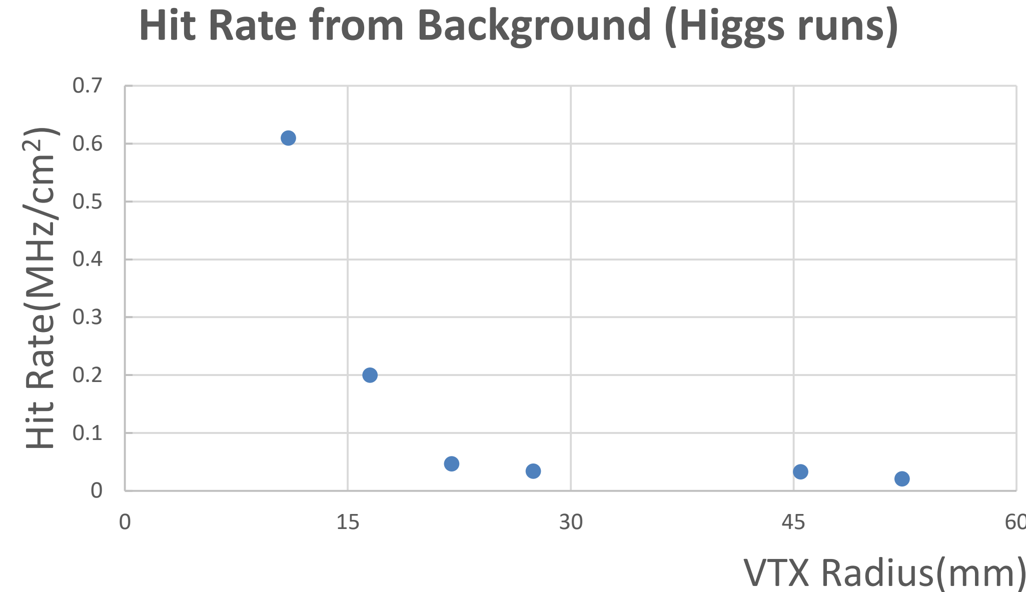
layer	Radius	Material
Layer 1/2	12.5 -18 mm	~0.33% X_0
Layer 3/4	28 - 35mm	~0.33% X_0
Layer 5/6 (Ladders)	45 - 53mm	~0.33% X_0
Total		~1% X_0





Data rate estimation of vertex detector

	Hit rate (MHz/cm²)	Data rate@triggerless (Gbps)	Data rate@trigger (Gbps)
Higgs	0.61	0.18	<0.01
W	3.16	0.98	<0.01
Low-lumi Z pole	3.9	1.2	~0.1



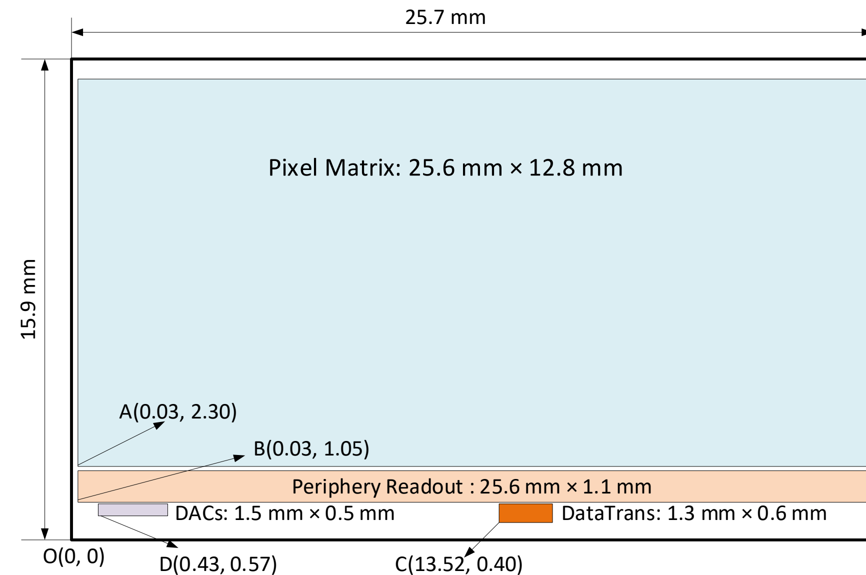
- Data rate is dominated by background from pair production
  - Estimated based on old version of software
  - More details in Haoyu's MDI talk on Friday
- WW runs and low Lumi Z runs (20% of high lumi Z)
- Data rate @1.2 Gbps per chip for triggerless readout

Chip design for ref- TDR and power consumption

- Power consumption estimation
  - Fast data-driven readout for low-lumi Z (~1 Gbps/chip)
  - Using 65/55nm CIS technology

  Power consumption can reduced to ~40 mW/cm²

- Air cooling feasibility study
  - Baseline layout can be cooled down to ~20 ℃
    - Based on 3 m/s air speed, estimated by thermal simulation



	Matrix	Periphery	DataTrans.	DACs	Total Power	Power density
TaiChuPix3 180 nm chip @ 3.84 Gbps/chip **(CDR Higgs, W, Z)**	304 mW	135 mW	206 mW	10 mW	655 mW	160 mW/cm²
Chip in 65 nm for TDR @ 1 Gbps/chip (**TDR LowLumi Z**)	60 mW	80 mW	36 mW	10 mW	186 mW	~40 mW/cm²

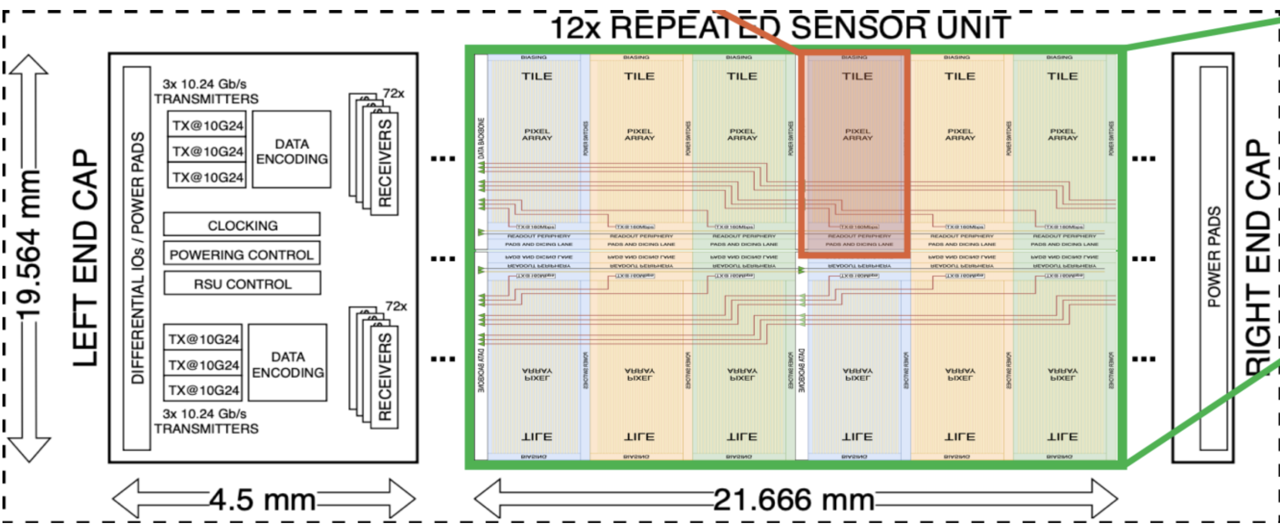
Ladder Electronics

– Baseline: stitching and RDL metal layer on wafer to replace PCB

– Alternative: flexible PCB

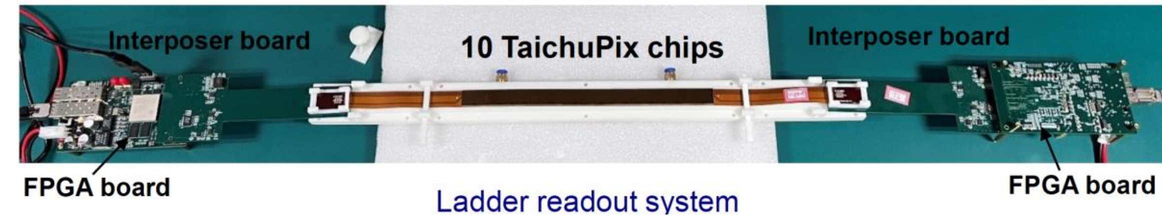
- Signal, clock, control, power, ground will be handled by control board through FPC

Baseline: ALICE ITS3 like stitching



[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

Alternative: flexible printed circuit (FPC)



Ladder readout system

叠层 **Stack Up**

Layer	Thickness		Material		Base copper					
	12.5	um	Coverlay	(yellow)						
	20	um	Coverlay Adhesive	Soldmask (green)						
Layer 1	24	um	ED Base Copper		12	um	um +	Plated	18	um
	13	um	Polyimide (Adhesiveless)							
	12.5	um	Adhesive							
Layer 2	12	um	ED Base Copper		12	um				
	25	um	Polyimide (Adhesiveless)							
Layer 3	12	um	ED Base Copper		12	um				
	12.5	um	Adhesive							
	13	um	Polyimide (Adhesiveless)							
Layer 4	24	um	ED Base Copper		12	um	um +	Plated	18	um
	20	um	Coverlay Adhesive							
	12.5	um	Coverlay	(yellow)						

Flex Thickness 绕折区

补强区

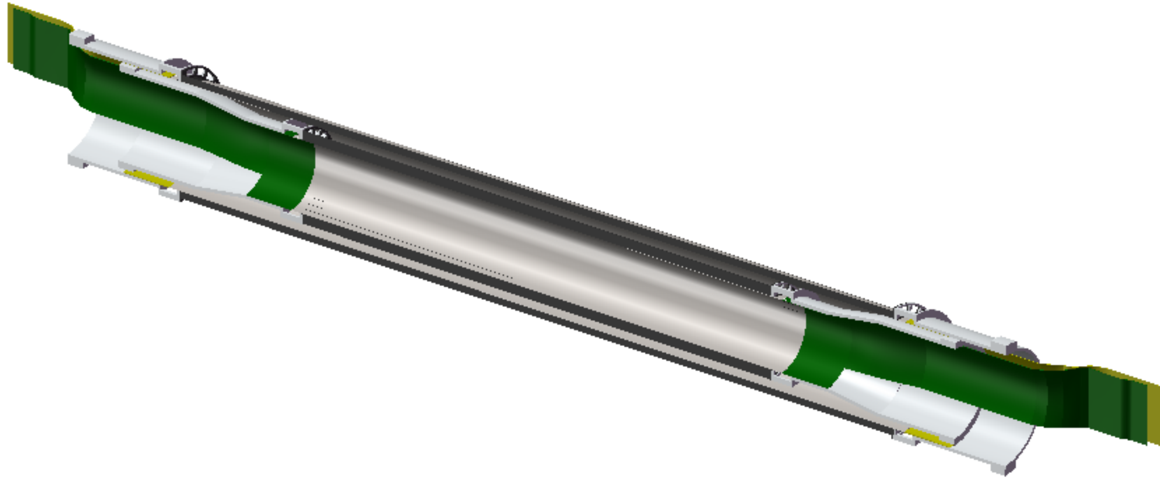
FPC厚度: 213 um Spec: 210 um +/- 50 um

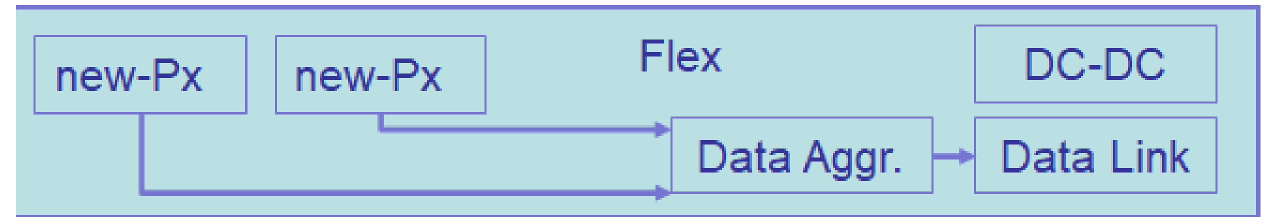
Created By: HLJ

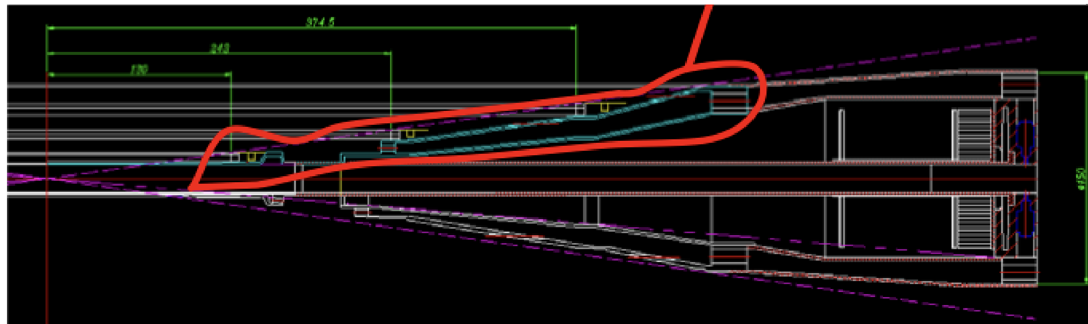
Date:

Vertex technologies: Cables and services

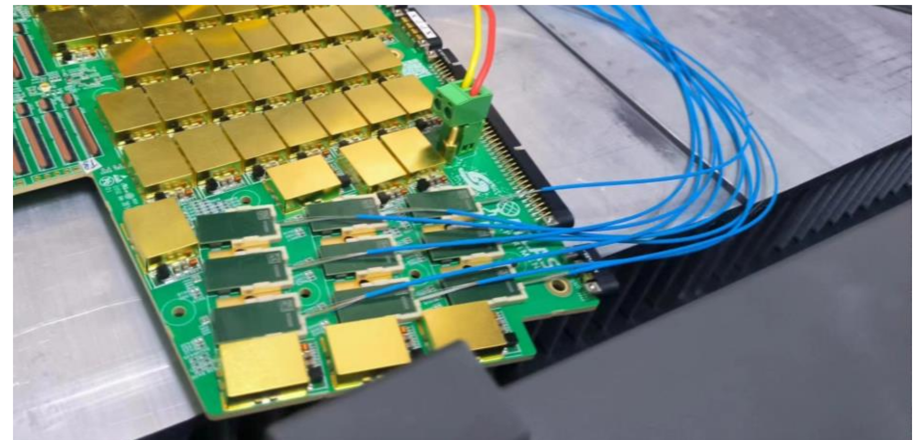
- Limited space in the MDI region for cables and services
  - Signal are transmitted through a flexible PCB and then converted to optical fiber.
  - Utilizes DC-DC converter to distribute the power.







Example from ATLAS HGTD upgrade



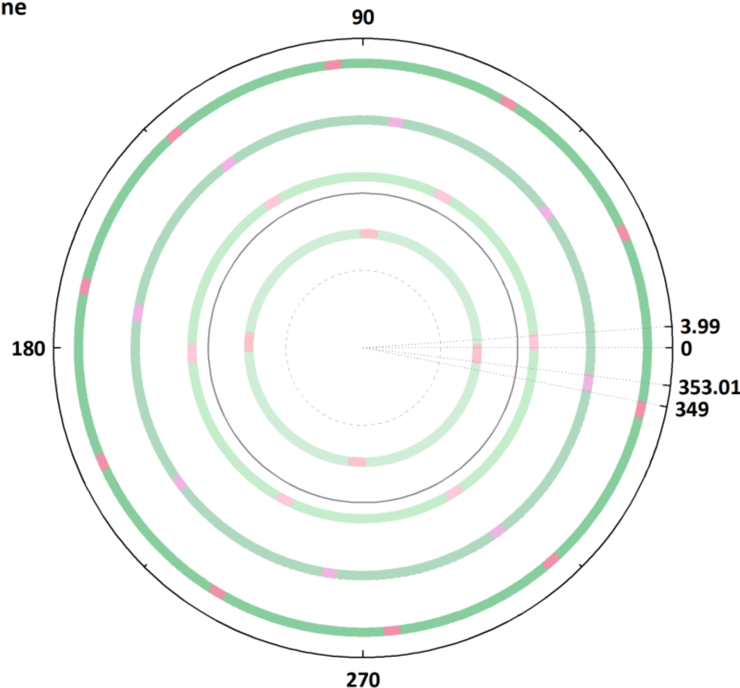
Performance: impact parameter resolution

- Compared to alternative (ladder) option

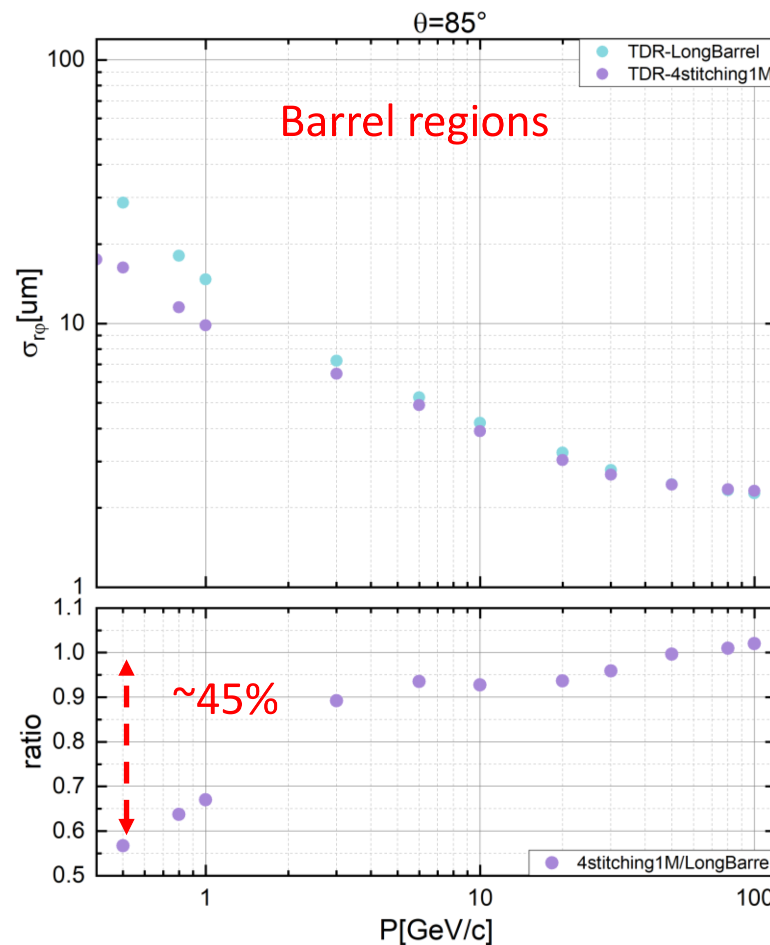
More details in Poster #67

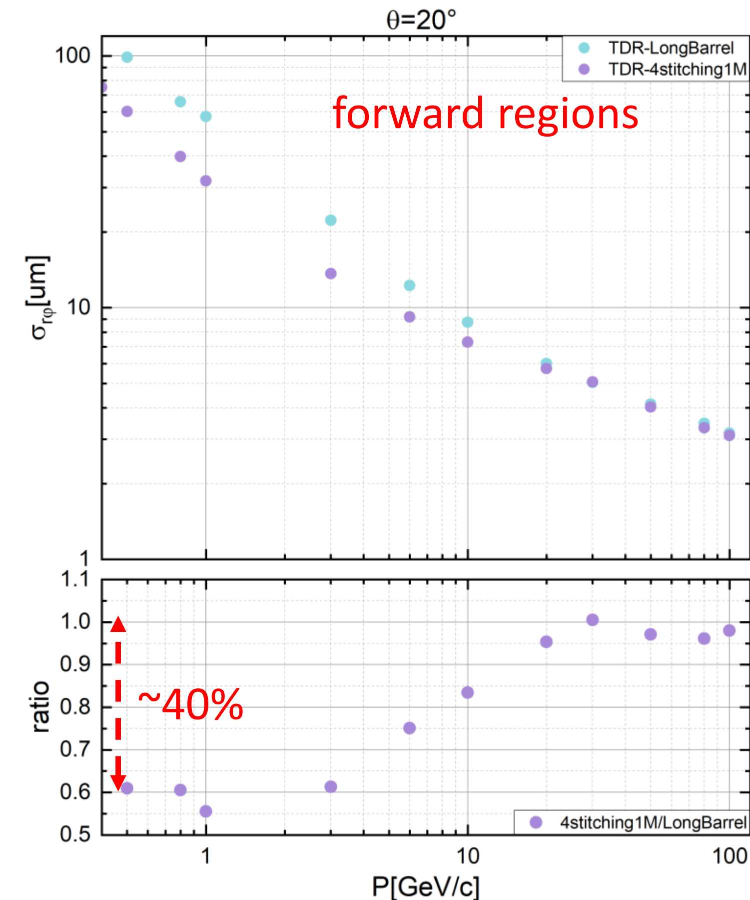
  – baseline (stitching) has significant improvement (~45%) in low momentum case

Different rotation angle in each layer to reduce dead area



Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.





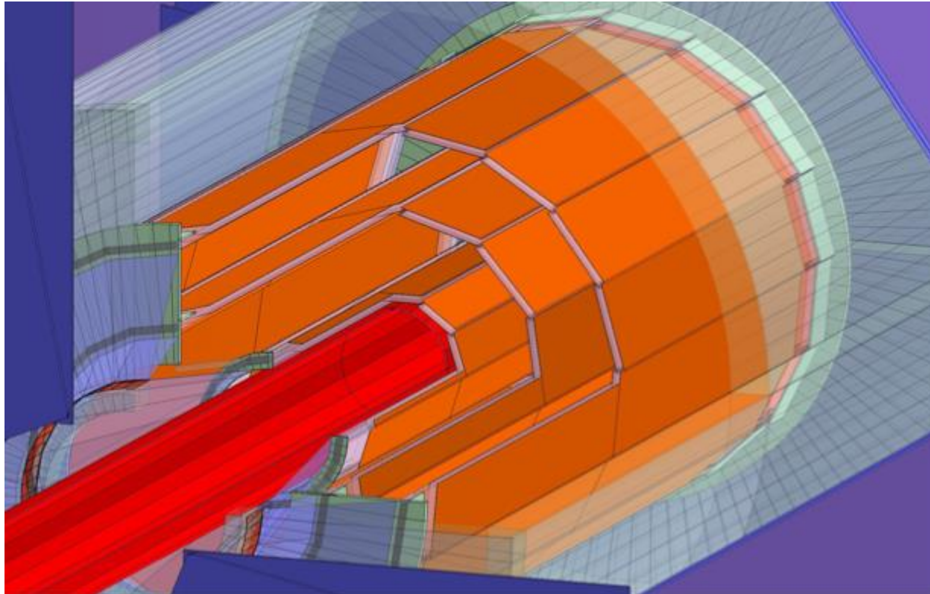
Research team

- IHEP: Joao Costa, et al, 15 faculty, 5 postdoc, 6 students
  - CEPC vertex prototype, X-ray camera, ATLAS ITK strip and HGTD upgrade
- IPHC/CNRS: Jerome Baudot (3 faculty)
  - Collaboration in framework of FCPPL, BELLE II upgrade
- IFAE: Chip design , Sebastian Grinstein et al (2 faculty)
  - CEPC TaichuPix chip design, ATLAS ITK pixel and HGTD upgrade
- ShanDong U.: Stitching chip design (3 faculty, 1 postdoc, 3 students)
- CCNU: chip design, ladder assembly (3 faculty, 1 postdoc, 5 students)
- Northwestern Polytechnical U. : Chip design (5 faculty, 2 postdoc, 5 students)
- Nanchang U. : chip design, (1 faculty, 1 students)
- Nanjing U.: irradiation study, chip design : (2 faculty, 4 students)
- Total : 36 faculty, 9 postdoc, 26 students

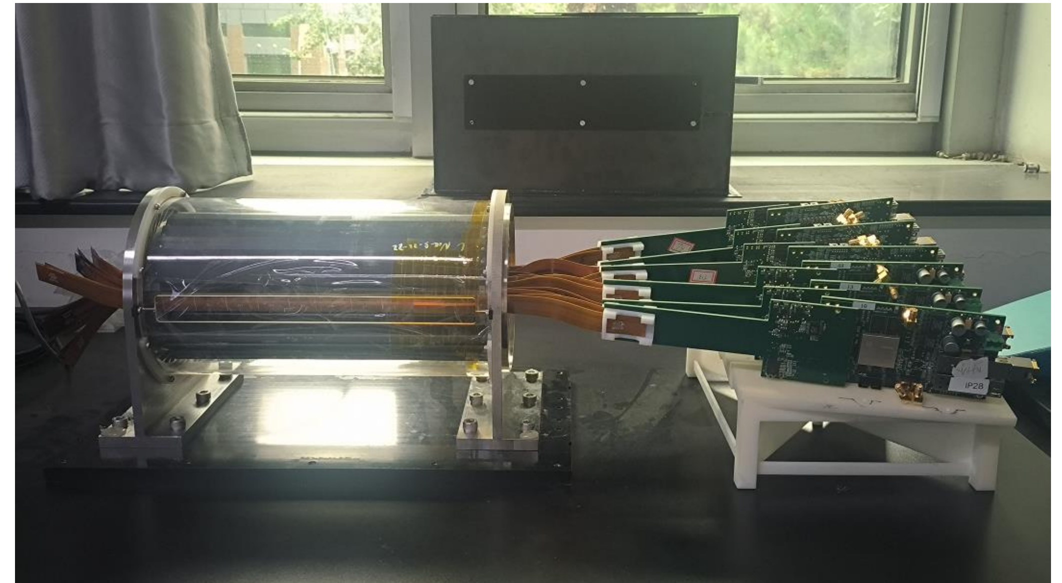
Summary

- 1st full-size Prototype based the ladder design for CEPC vertex detector has been developed
- The bent MAPS option has been chosen as baseline for the reference detector TDR.
- We active expanding international collaboration and explore synergies with other projects
  - We are members of ECFA DRD3 collaboration (solid state detectors)

CEPC vertex conceptional design (2016)



CEPC vertex prototype (2023)



Summary: working plan

- CEPC vertex detector timeline is about 3-4 years after ALICE ITS3 upgrade
  - It will benefit from experience from ALICE ITS3 upgrade

	CEPC Final goal	CEPC Expected date	ALICE ITS3 schedule
CMOS chip technology	65nm CIS	2028 Full-size 65nm chip	2025
Spatial resolution	3-5 μm with final chip	2028	2025
Stitching	65nm CIS stitched sensor	2029	2026 wafer production
Bent silicon with small radius	Bent final wafer with radius ~11mm	2030	2027
Detector cooling	Air cooling with full power	2027： thermal mockup	2027
Detector integration	Detector with bent silicon design	2032	2028

Thank you for your attention!

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