Large Area Low-power Monolithic CMOS Tracking Detectors for the CEPC

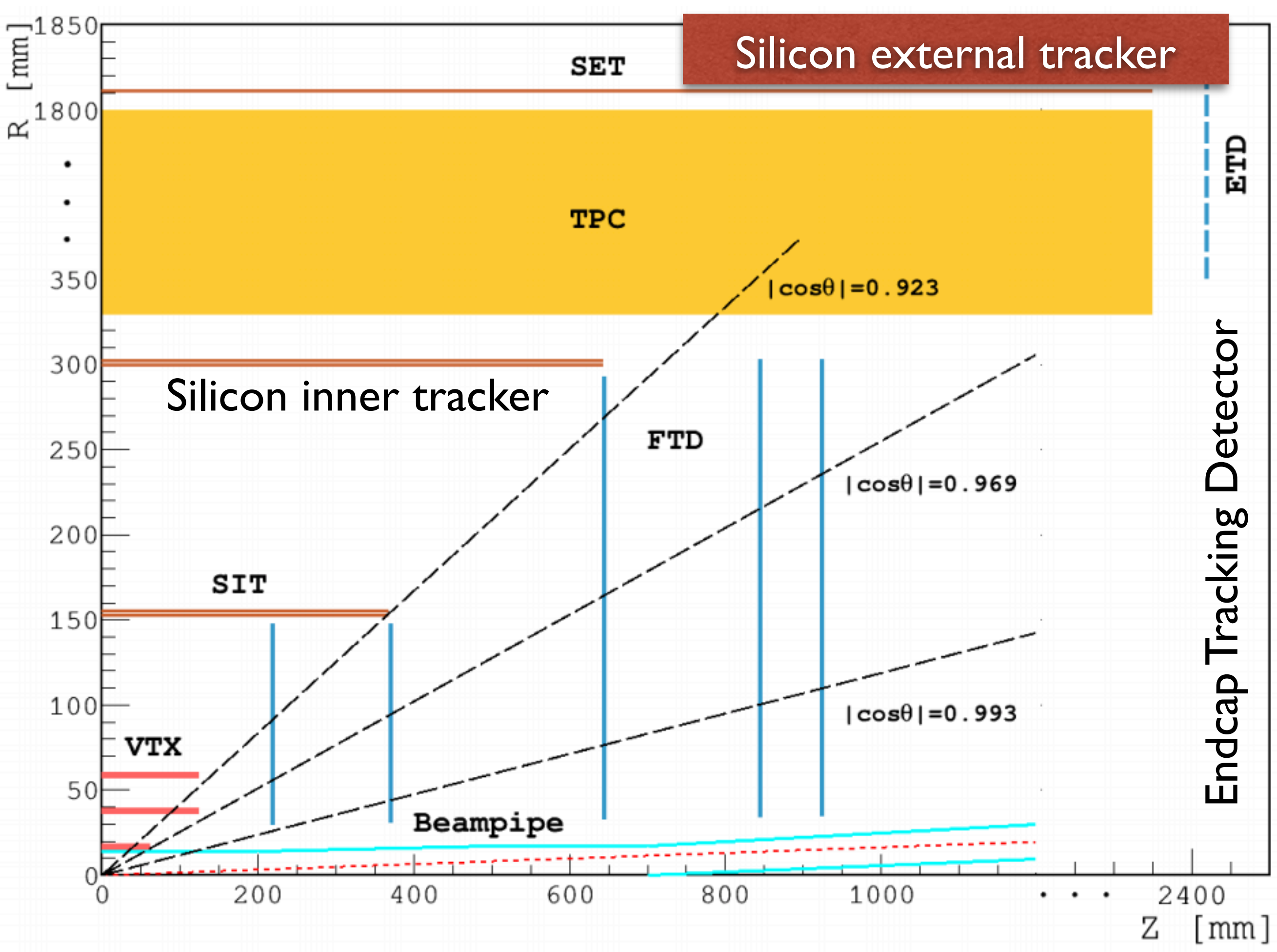
Yanyan Gao (University of Edinburgh)

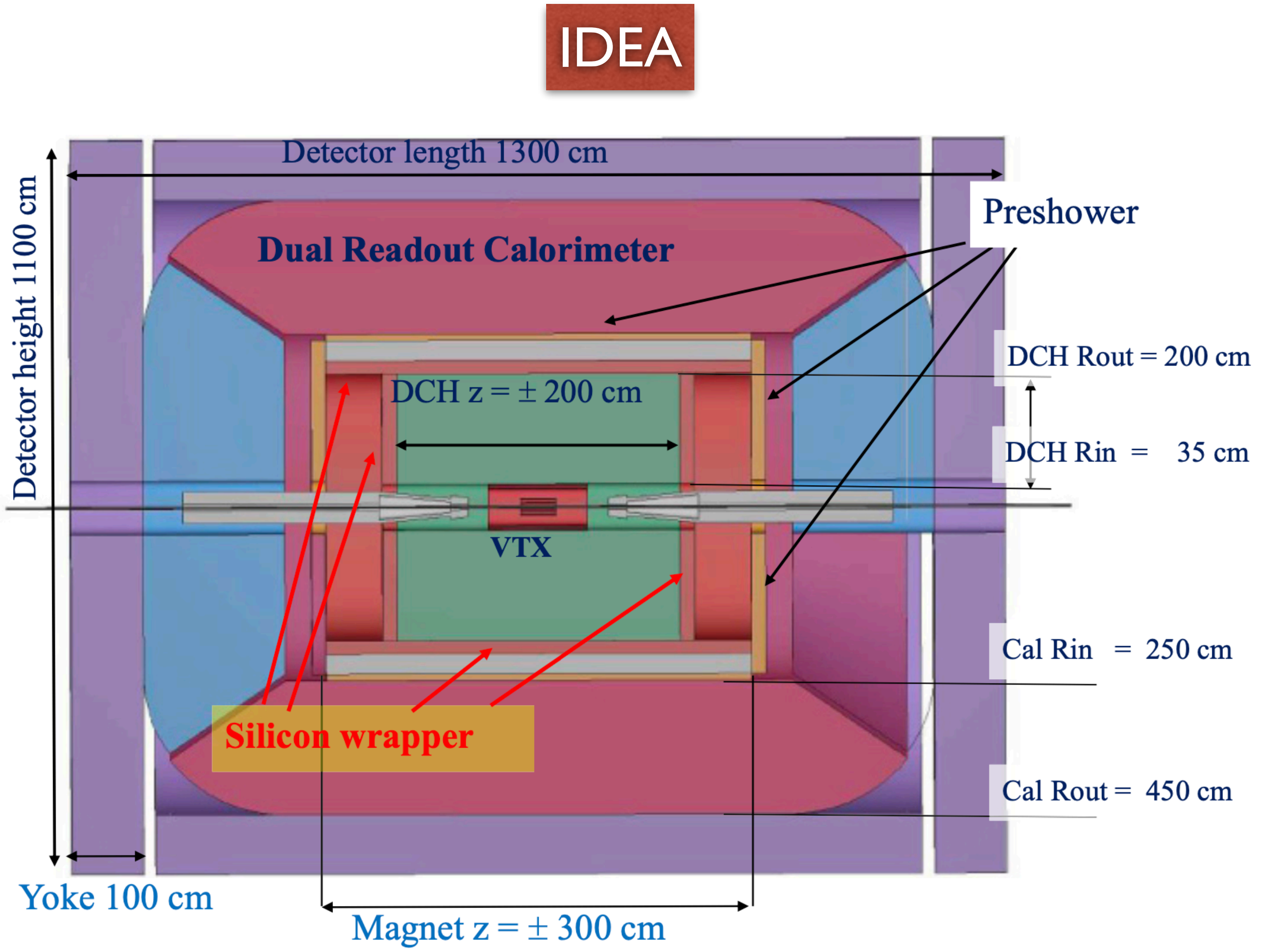
The 2024 International Workshop on the High Energy Circular Electron Positron Collider, 24-Oct-2024

With contributions and inputs from colleagues in many institutes, especially Hochschule RheinMain, INFN Milano, IHEP, KIT, Lancaster

Setting the theme

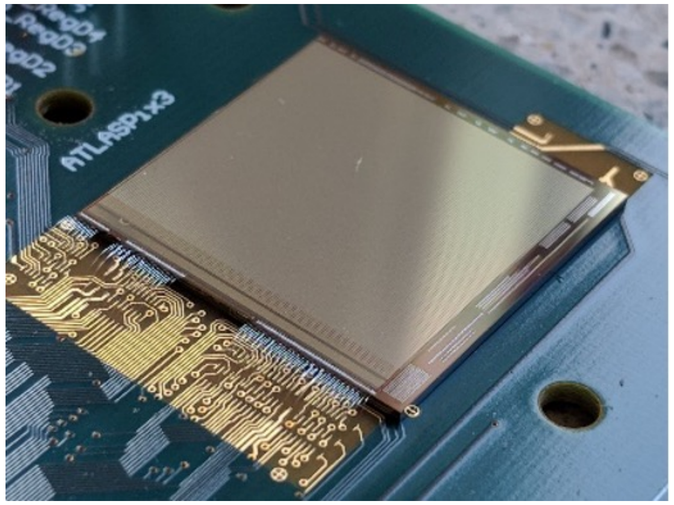
- Several detector designs envision O(100m²) silicon tracker in the middle/outer layers
  - Thanks to recent progress in several experiments (e.g. ATLAS ITk, ALICE ITS and Mu3e), Monolithic CMOS offers a promising solution for large area applications
  - However, being O(10) larger than the current CMOS trackers, system level R&D (powering, services, assembly..) needs to be carried out in parallel to sensor development

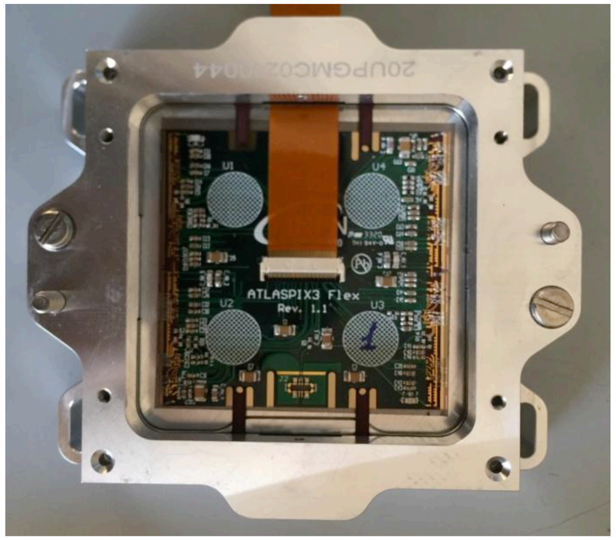


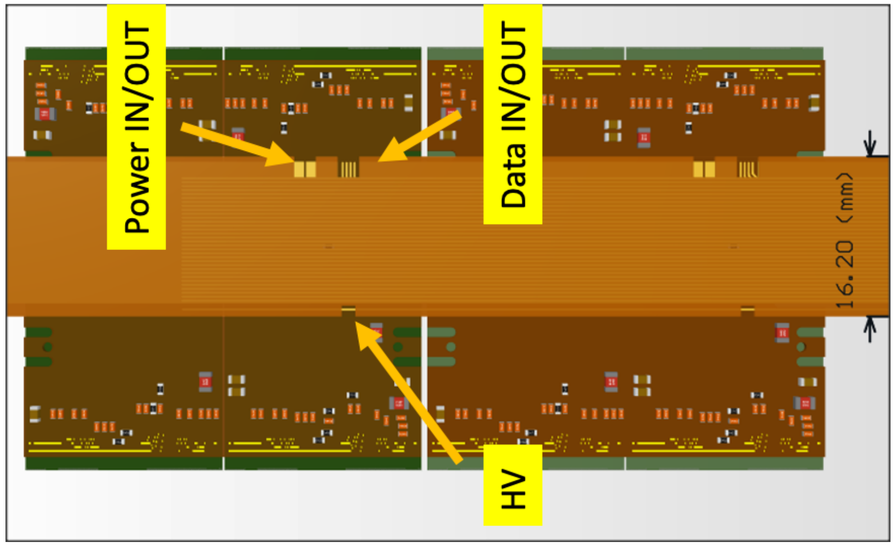


This talk

- Progress on ATLASPix3 based multi-chip Serial Powering System prototype





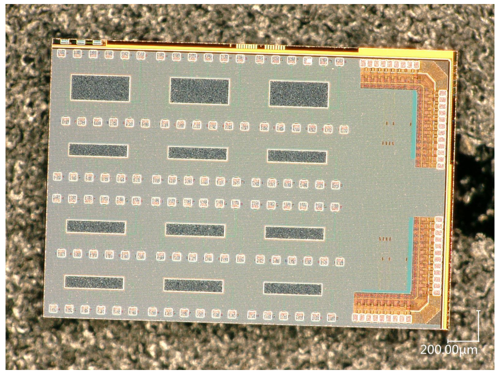


- New development in small feature size 55nm HV-CMOS with SMIC

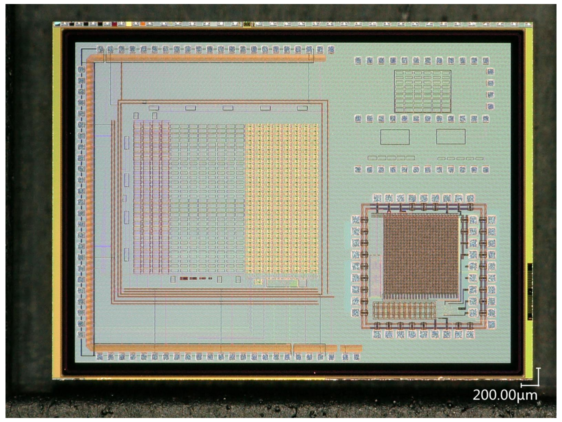
COFFEE

CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

COFFEE1



COFFEE2



Global collaborated efforts

- CEPC tracker R&D group (2019-), meeting every two weeks
    - Coordinators: Harald Fox (Lancaster) and Yiming Li (IHEP)

- China
    - Institute of High Energy Physics, CAS
    - Shang Dong University
    - Tsinghua University
    - University of Science and Technology of China
    - Northwestern Polytechnical University
    - T.D.Lee Institute-Shanghai Jiao Tong University
    - Harbin Institute of Technology
    - University of South China
    - Hunan University
    - Zhejiang University
    - Dalian Minzu University

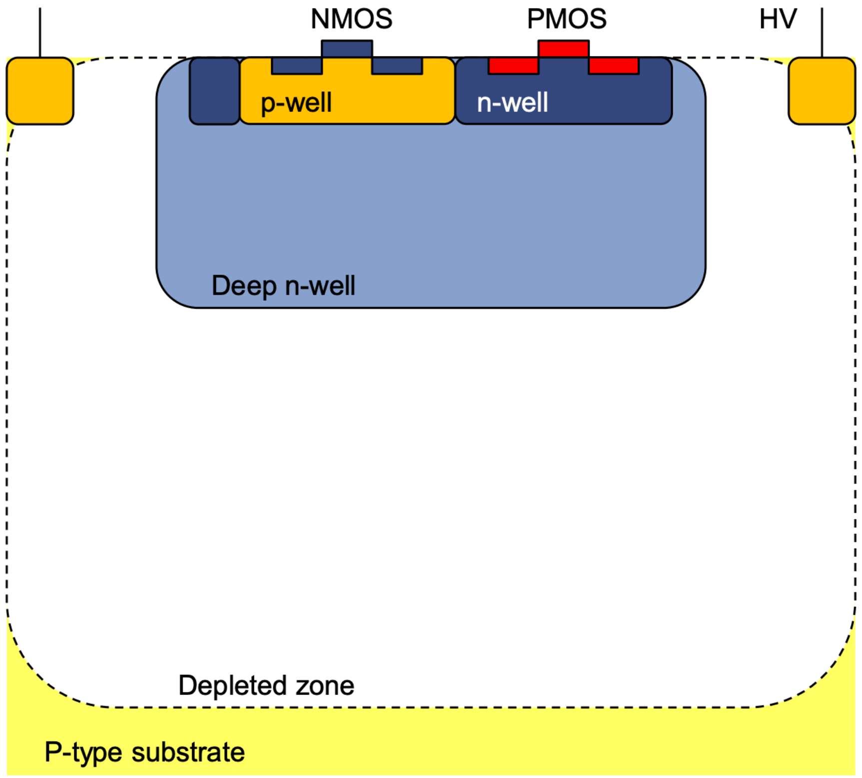
UK
- University of Bristol
- University of Edinburgh
- Lancaster University
- University of Liverpool
- STFC-Rutherford Appleton Laboratory

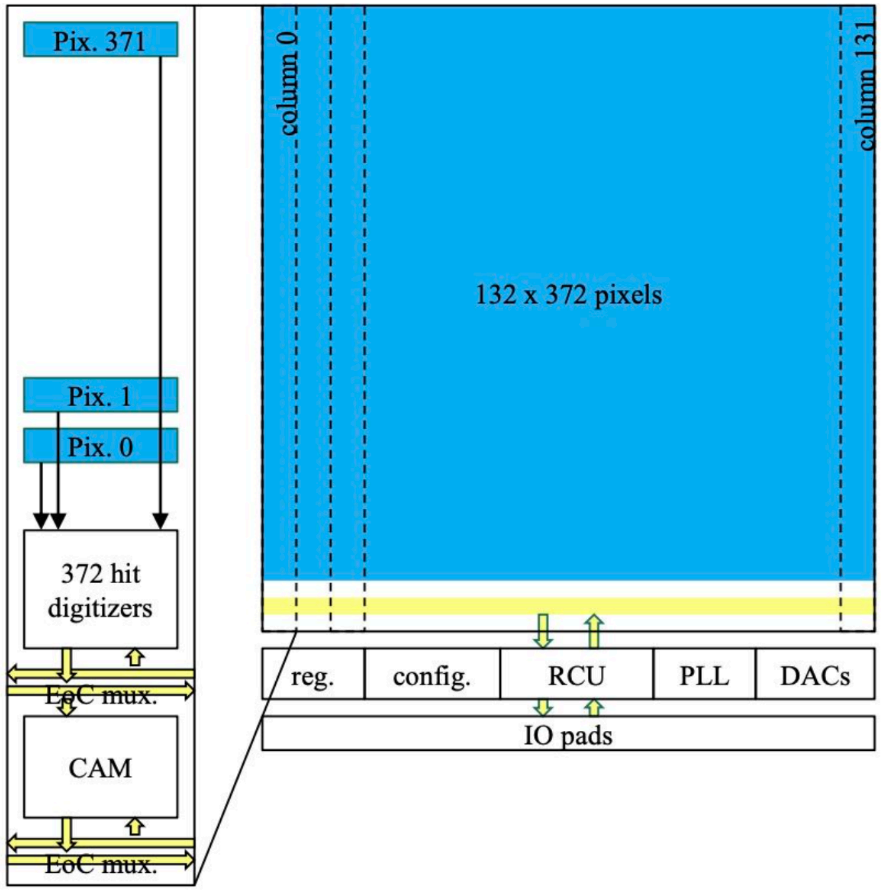
- Germany
    - Karlsruhe Institut für Technologie
    - Hochschule RheinMain
- Italy
    - INFN Sezione di Milano, Università degli Studi di Milano
    - INFN Sezione die Pisa, Università di Pisa

- A lot of synergies with HL-LHC upgrade projects, Belle2, Mu3e, and EIC detector R&D
- The common R&D with ECFA roadmap is now pursued within the DRD3 collaboration

ATLASPix3/3.1 general features

- AMS/TSI 180nm process, substrates 300 Ωcm
  - Breakdown (unirradiated): ~-65V
  - Full reticle size of 2.2 cm x 2.0 cm
    - Matrix size: 132 x 372
    - Pixel size: 50µm x 150µm
  - Individual amplifiers and threshold tuning circuits
    - Threshold can be tuned to 800e, with dispersion ~60e, noise ~ 70e
  - Digital part separated from the analog in the peripheral
  - Triggerless/Triggered readout
    - Data output: up to 1.28 Gbit/s 64b/66b (triggered), 1.6 Gbit/s 8b/10b (un-triggered)
  - 25ns time stamping
  - Good time resolution: ~4 ns (corrected)
  - Shunt/LDO (SLDO) regulators for Serial Powering
  - Power consumption 140 mW/cm^2

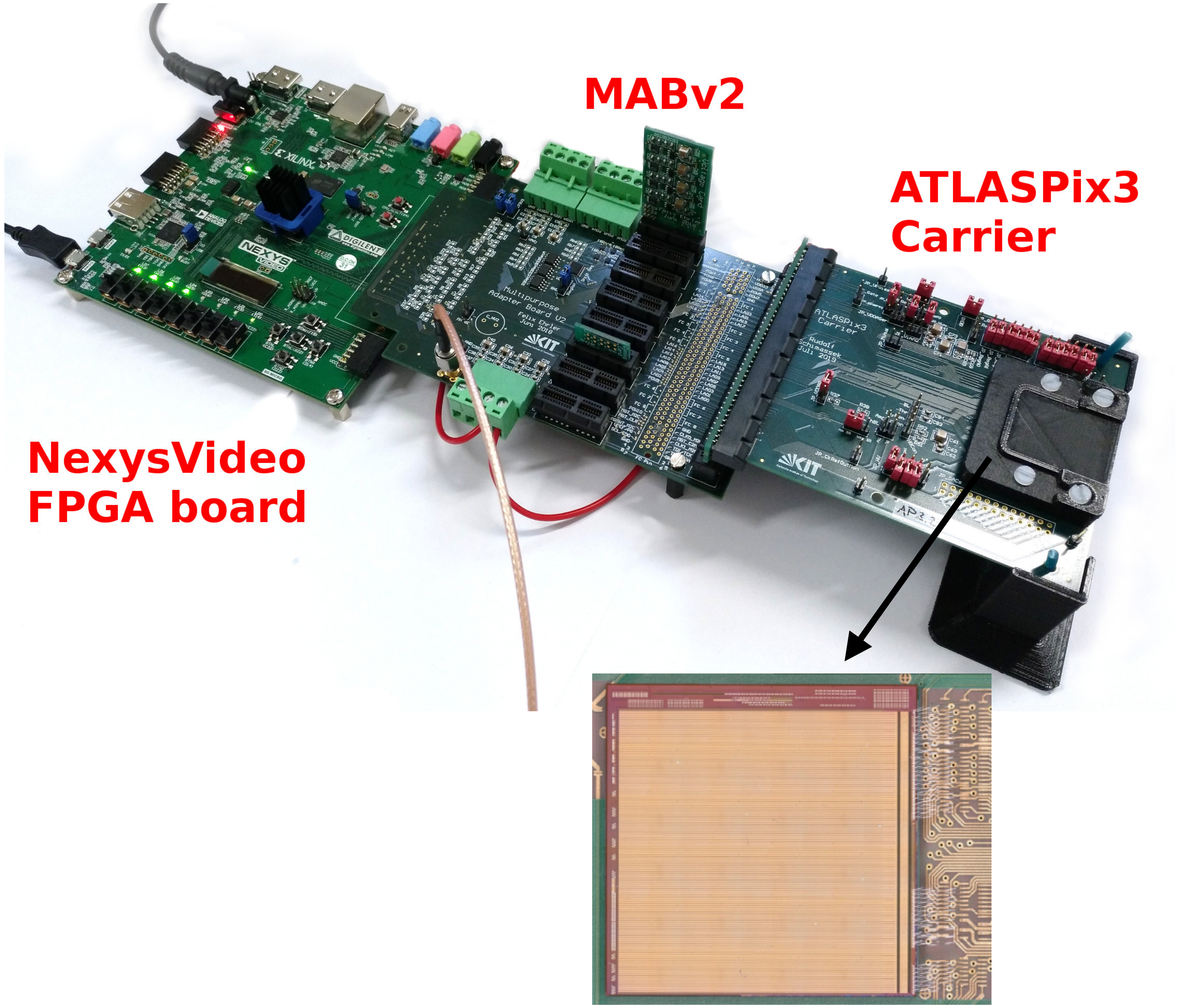




I. Peric et al., High-Voltage CMOS Active Pixel Sensor, IEEE JSSC, Volume: 56, Issue: 8, Aug. 2021 https://ieeexplore.ieee.org/document/9373986

ATLASPix3 - GECCO Readout System

- Versatile Readout system
  - Digilent Nexys Video FPGA board
  - GEneric Configuration and COntrol
  - Device carrier boards supporting:
    - Single chip card (SCC)
    - 4-chip Telescope
    - Quad-module
  - Qt-based software GUI

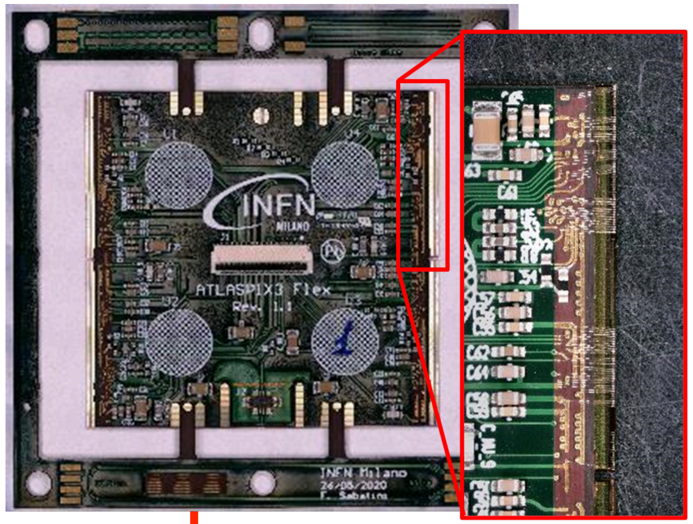


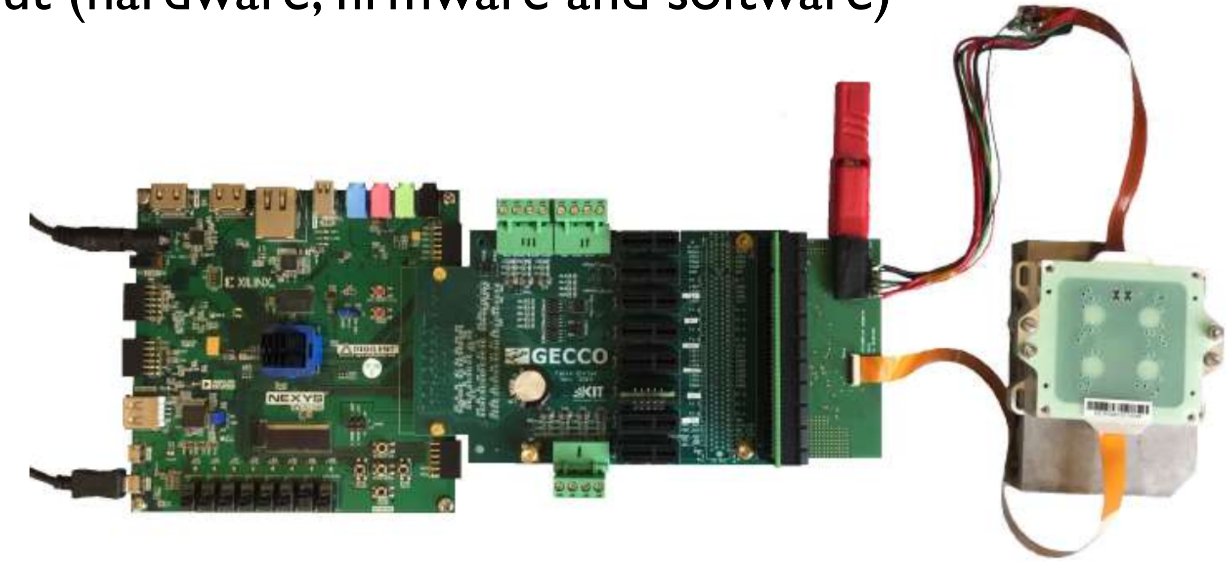
Progresses so far

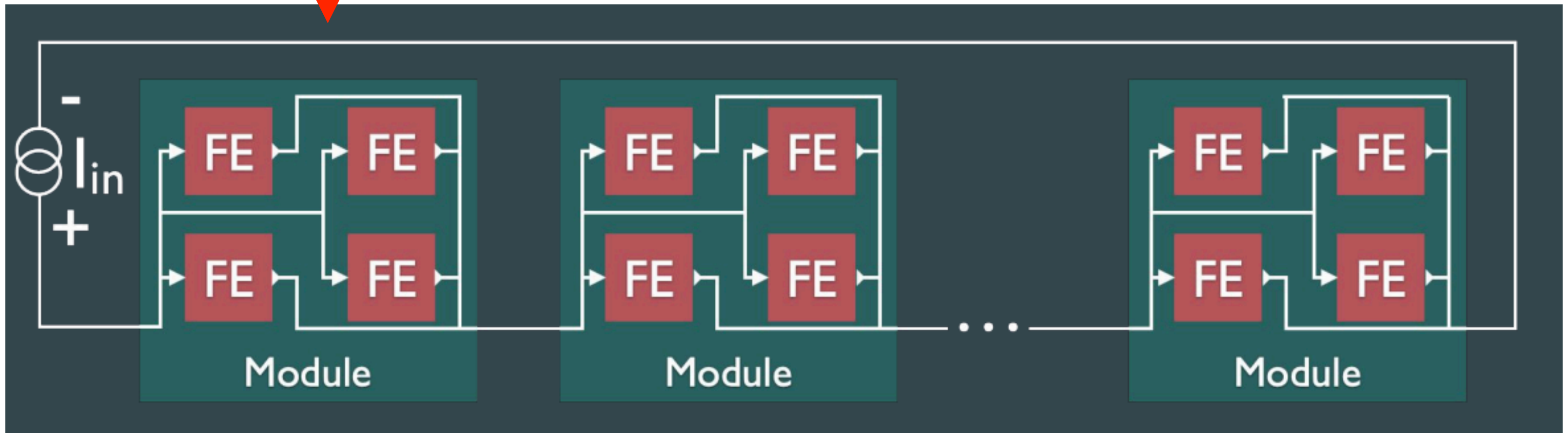
- 2 ATLASPix3.0 and 3 ATLASPix3.1 wafers diced (most thinned to 150um)
  - Joint production contributions: Edinburgh/Lancaster/KIT/Milan/RAL with the help from Heidelberg
- O(100) GECCO boards and single chip carriers produced in IHEP and distributed globally
  - Many institutes commissioned single chip lab test setup and electrical measurements
  - Supplied also to the other projects such as the LHCb MT upgrade
- ATLAS ITk pixel inspired quad-module has been developed
  - First quad-module based on APix3 has been manufactured and tested in lab and Testbeam
  - Second quad-module based on APix3.1 (with functional Shunt-LDO) are ready to be assembled
    - These quad-modules will be the basis for the serial powering chain demonstrator
- Two testbeam (DESY and CERN):
  - DESY: 2 telescopes, one quad
  - CERN (Sep 2024): triggered output together with calorimeter
- Preliminary mechanical support has been prototyped (INFN Pisa, not covered in this talk)

Quad module and Serial Powering (SP) Chain

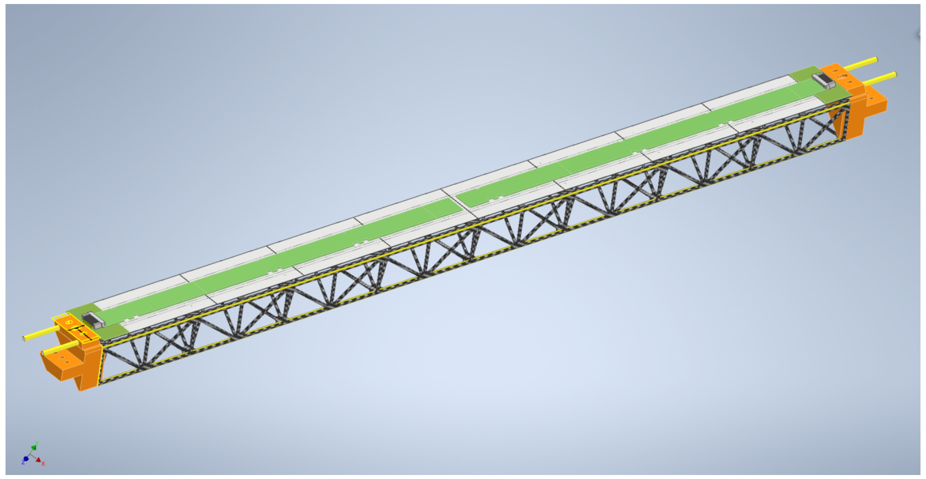
- ATLAS ITk pixel detector inspired quad module and SP chain is being developed using APix3 for data aggregation and power distributions
    - Bias 4 sensors in parallel, all sensors share data output and powering
    - Dedicated changes in flex, readout (hardware, firmware and software)







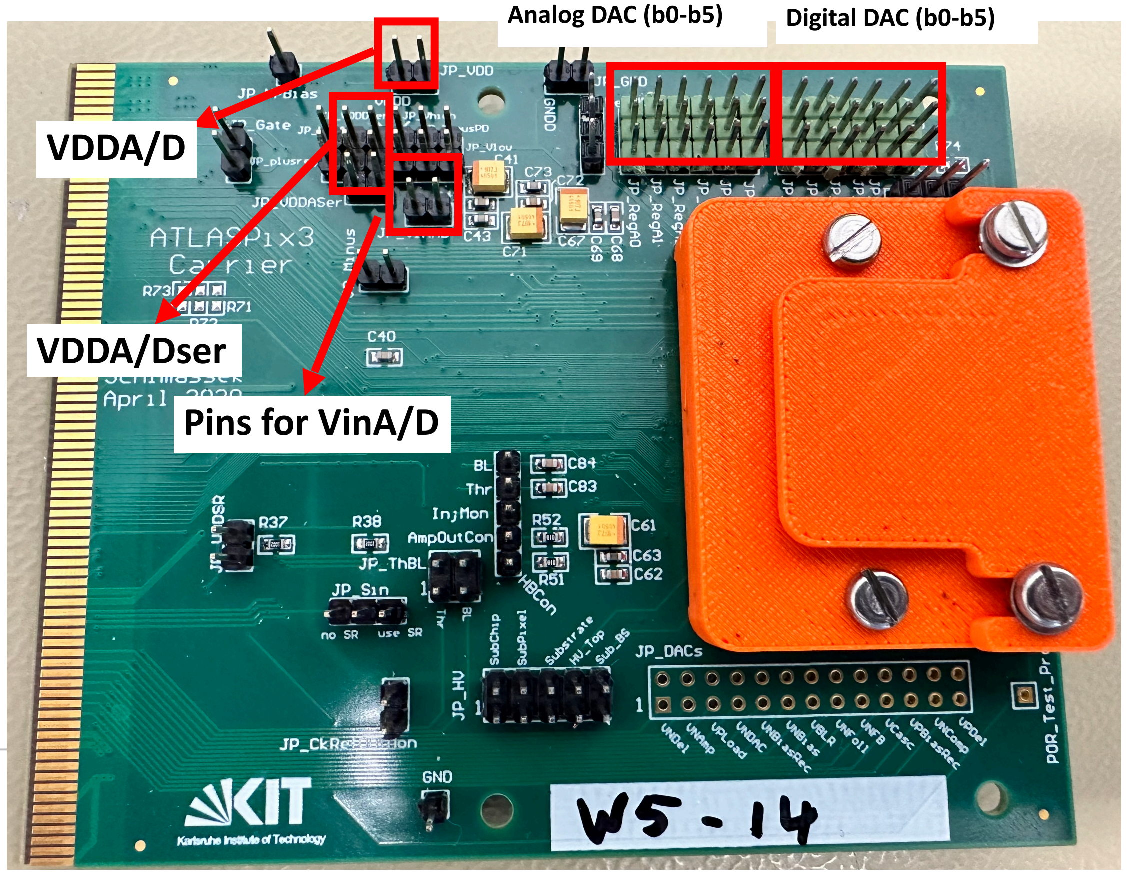
SP illustration by J. Chan, ATL-ITK-SLIDE-2022-674



Work integrated within IDEA community and DRD3 INFN (Milano and Pisa) and UK (Edinburgh)

ATLASPix3 SLDO features

- Two steps SLDO regulators for VDDD/A separately
  - 3 bits to tune threshold of shunt regulator
  - 3 bits to tune VDD
  - gatenmos, outref, gatepmos are for monitoring
  - regresetoutb can be used as power on reset
- This allows for constant current operation mode
  - Greatly simplified the operation power supply
  - Serial Powering chain of multi-quads

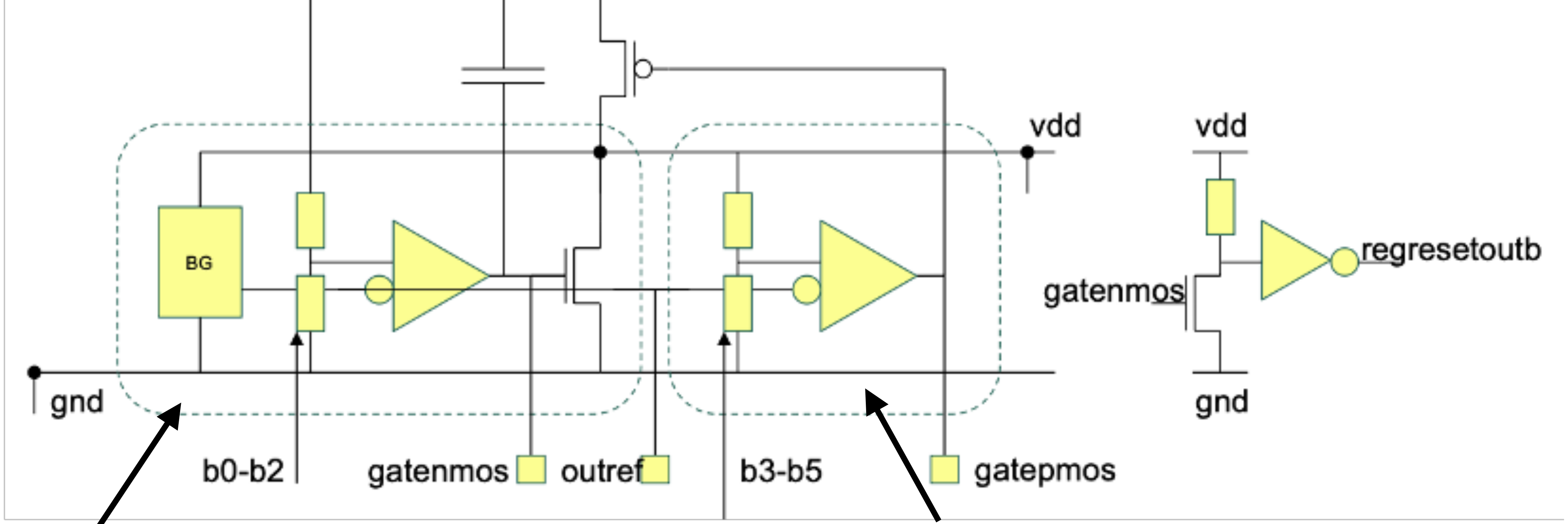

Analog DAC (b0-b5)

Digital DAC (b0-b5)

VDDA/D

VDDA/Dser

Pins for VinA/D



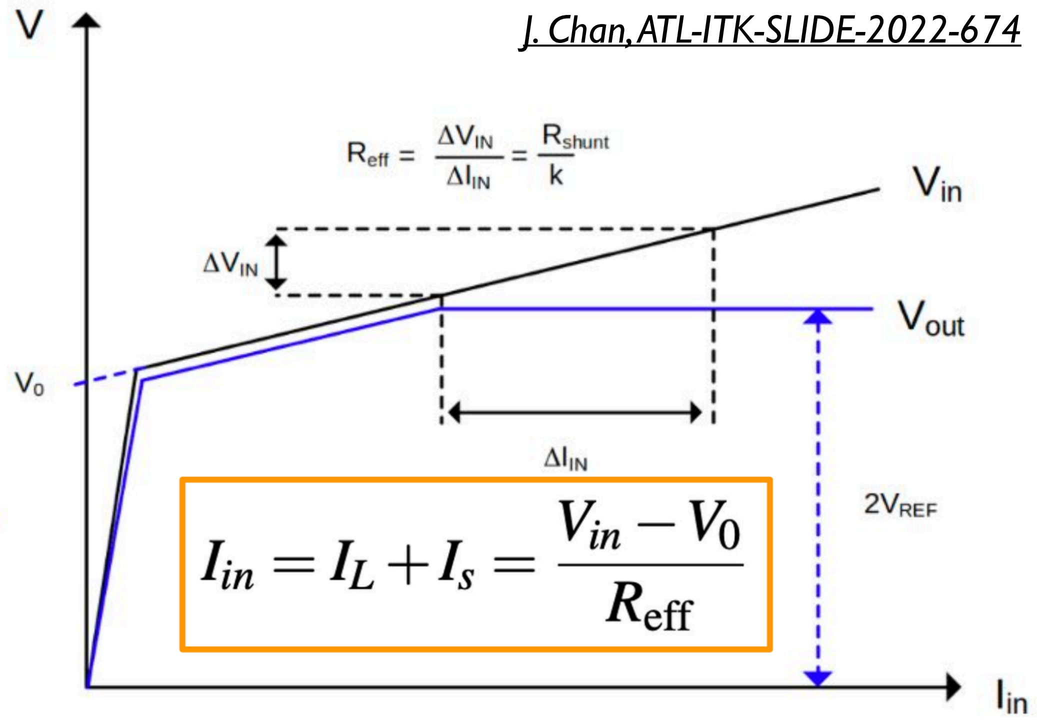
First Loop: Shunt regulation

Second Loop: VDDD/A regulation

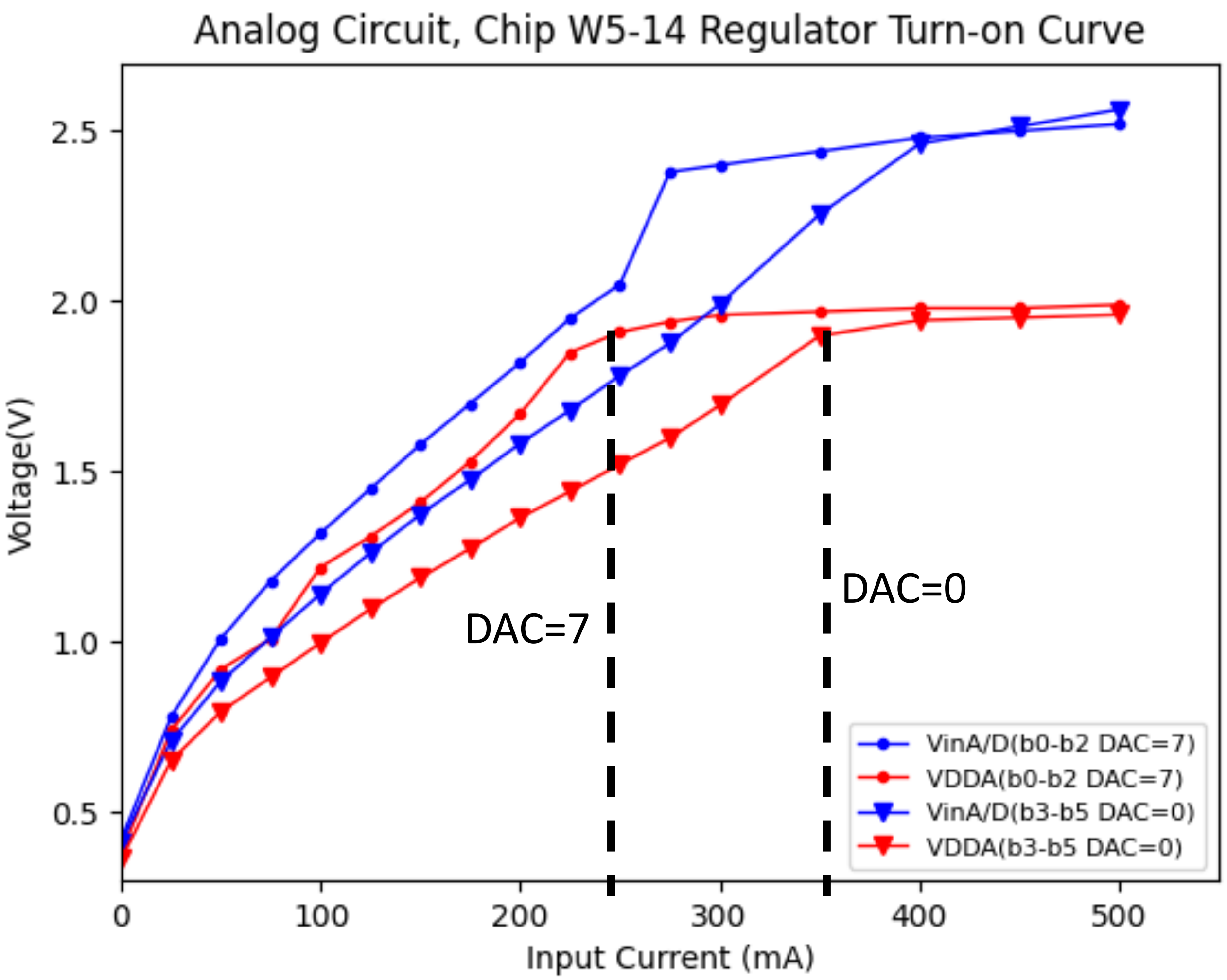
SLDO IV characterisations - single chip

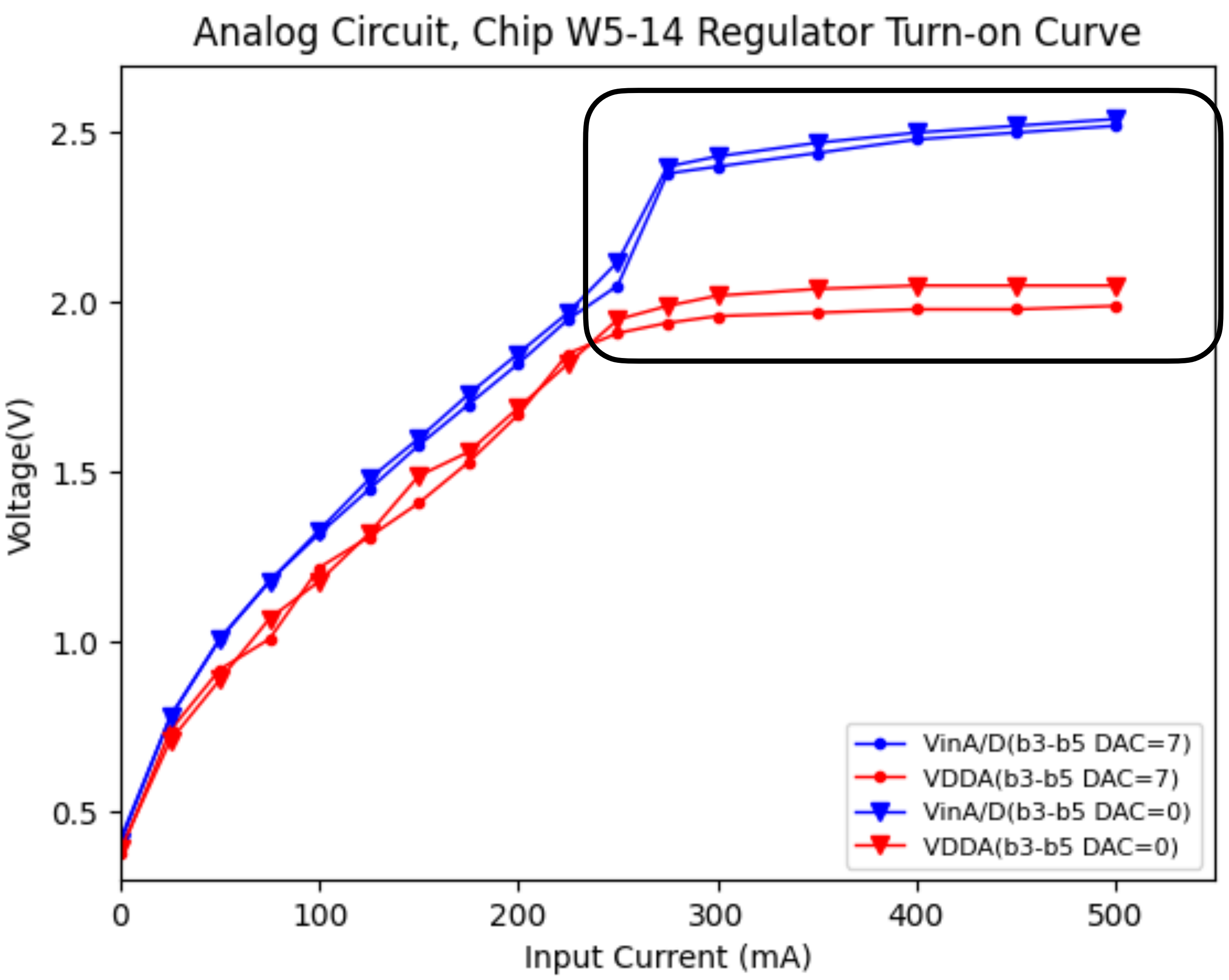
- Current threshold can be tuned within ~50mA (measurements fluctuate a bit)
- Ohmic behaviour is verified after threshold
- Output Small tuneable range for the output

J. Chan, ATL-ITK-SLIDE-2022-674

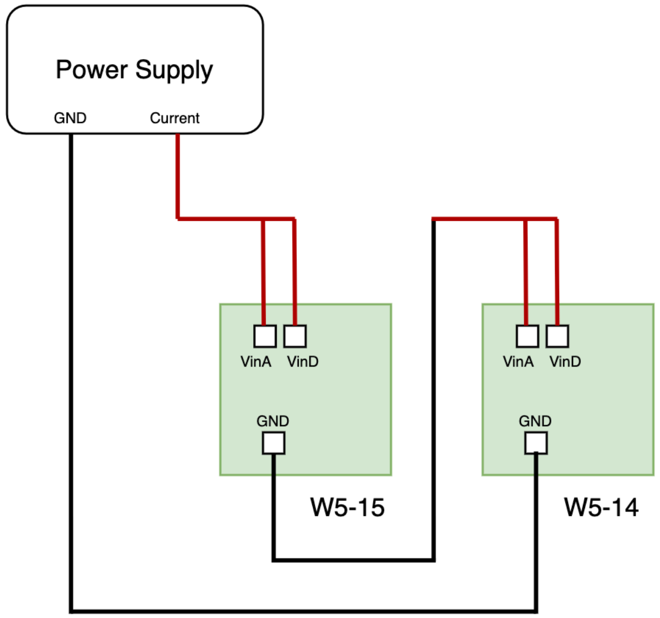


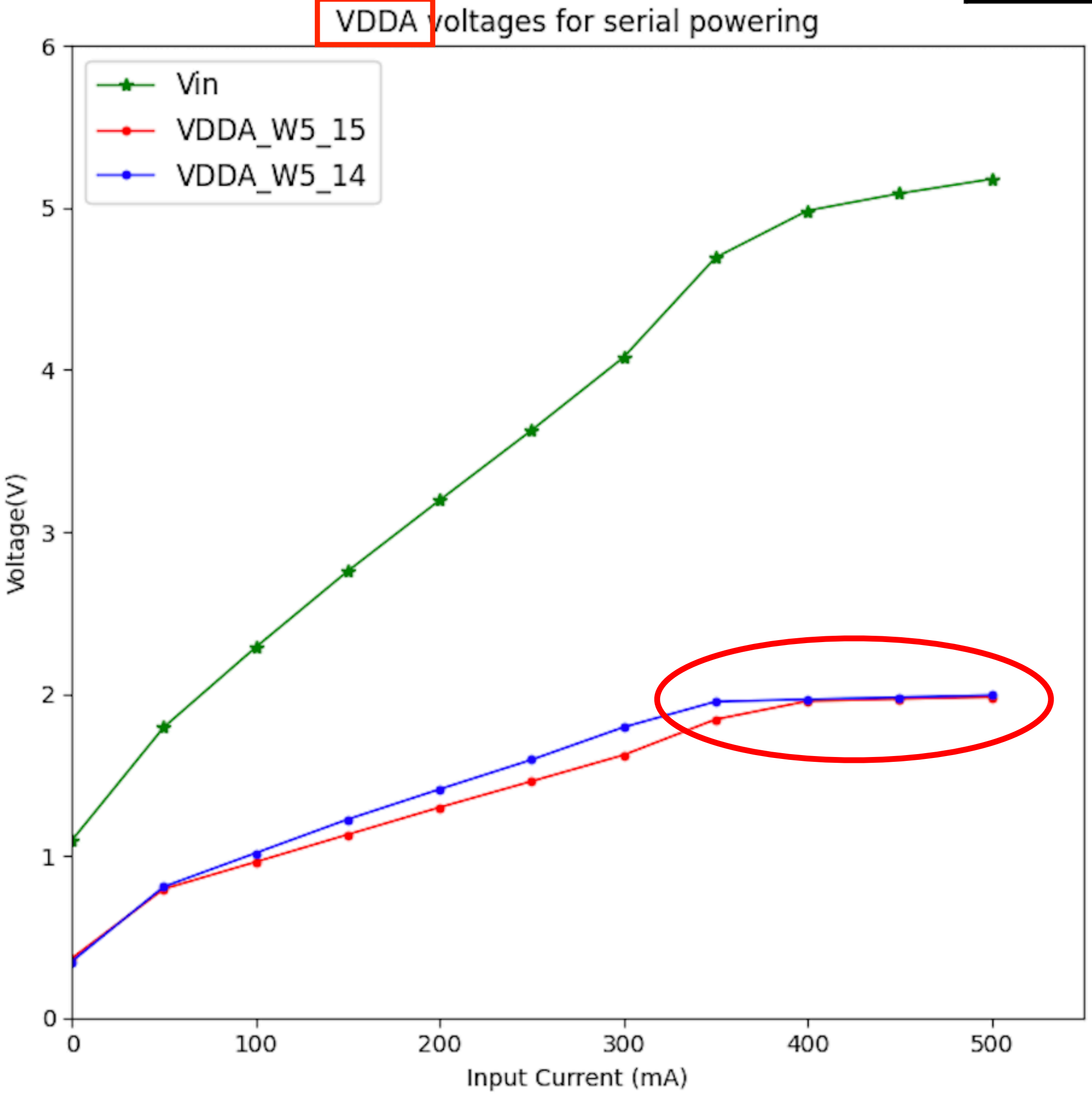
$$I_{in} = I_L + I_s = \frac{V_{in} - V_0}{R_{\text{eff}}}$$

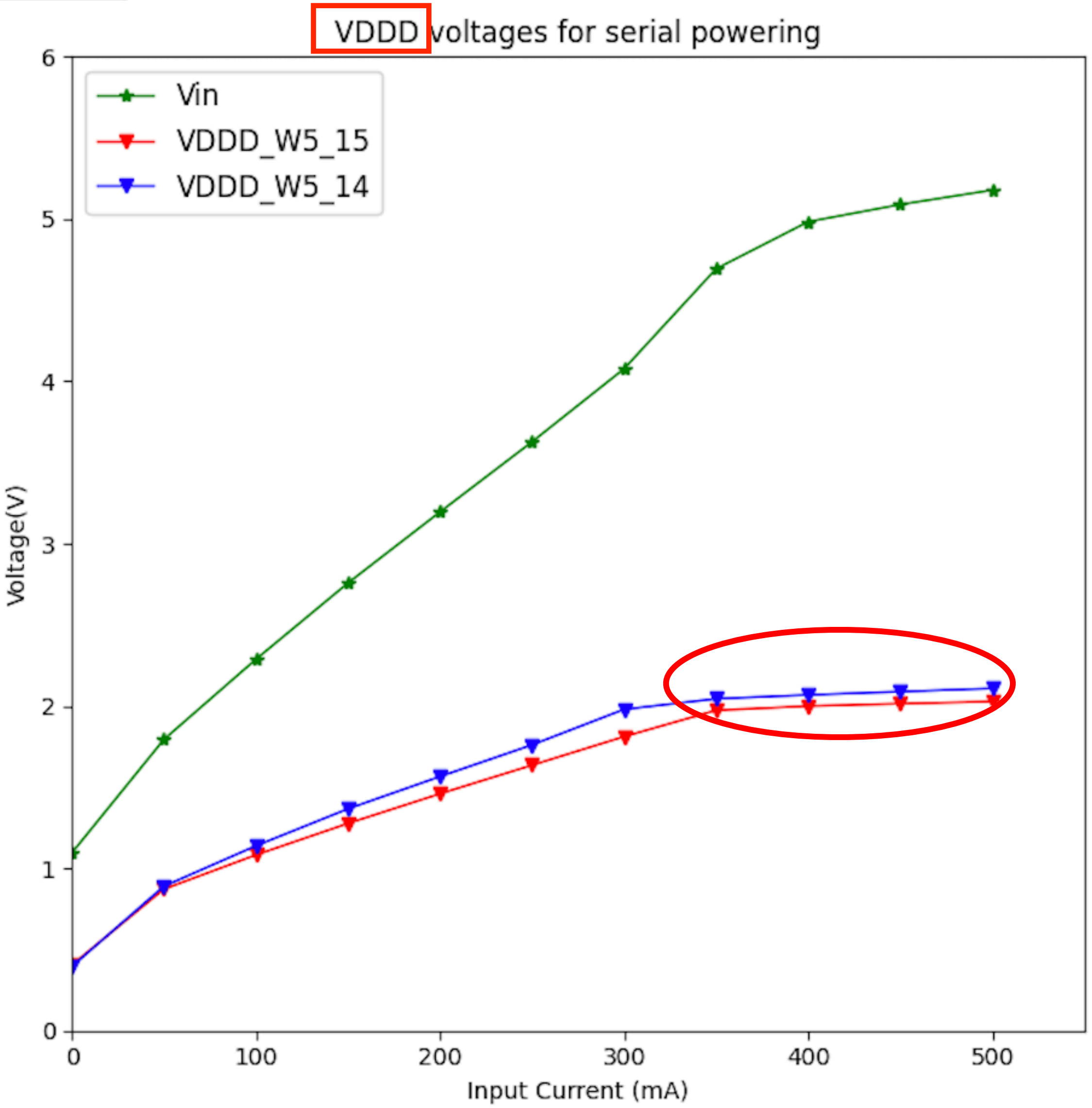




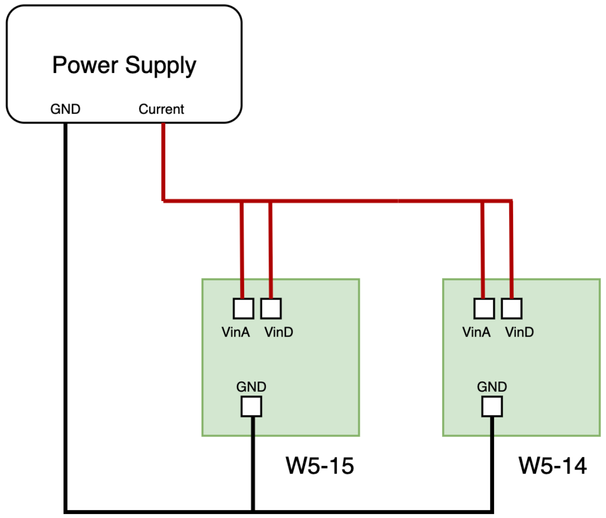
SLDO characterisation - Two chips in Serial

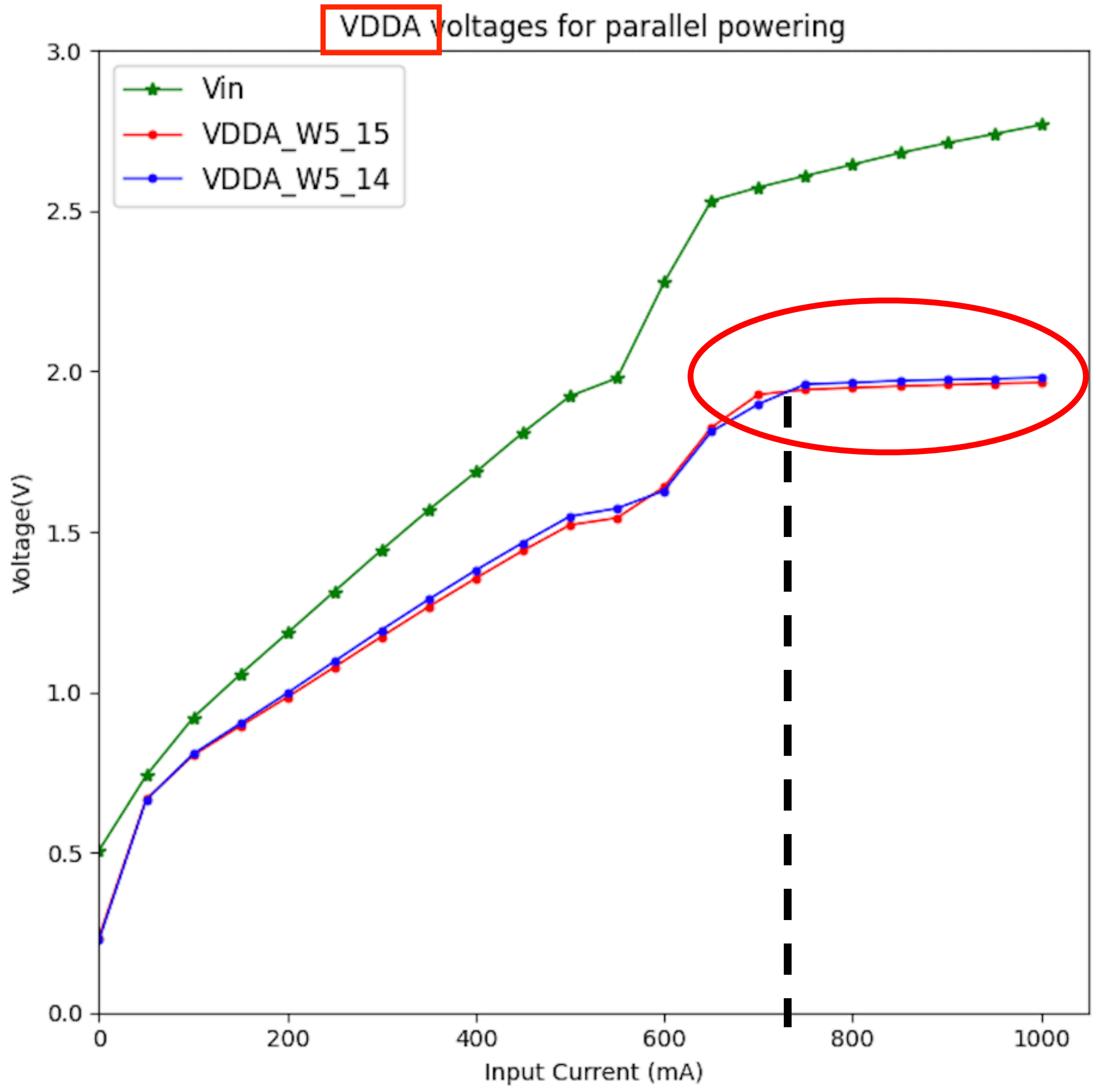


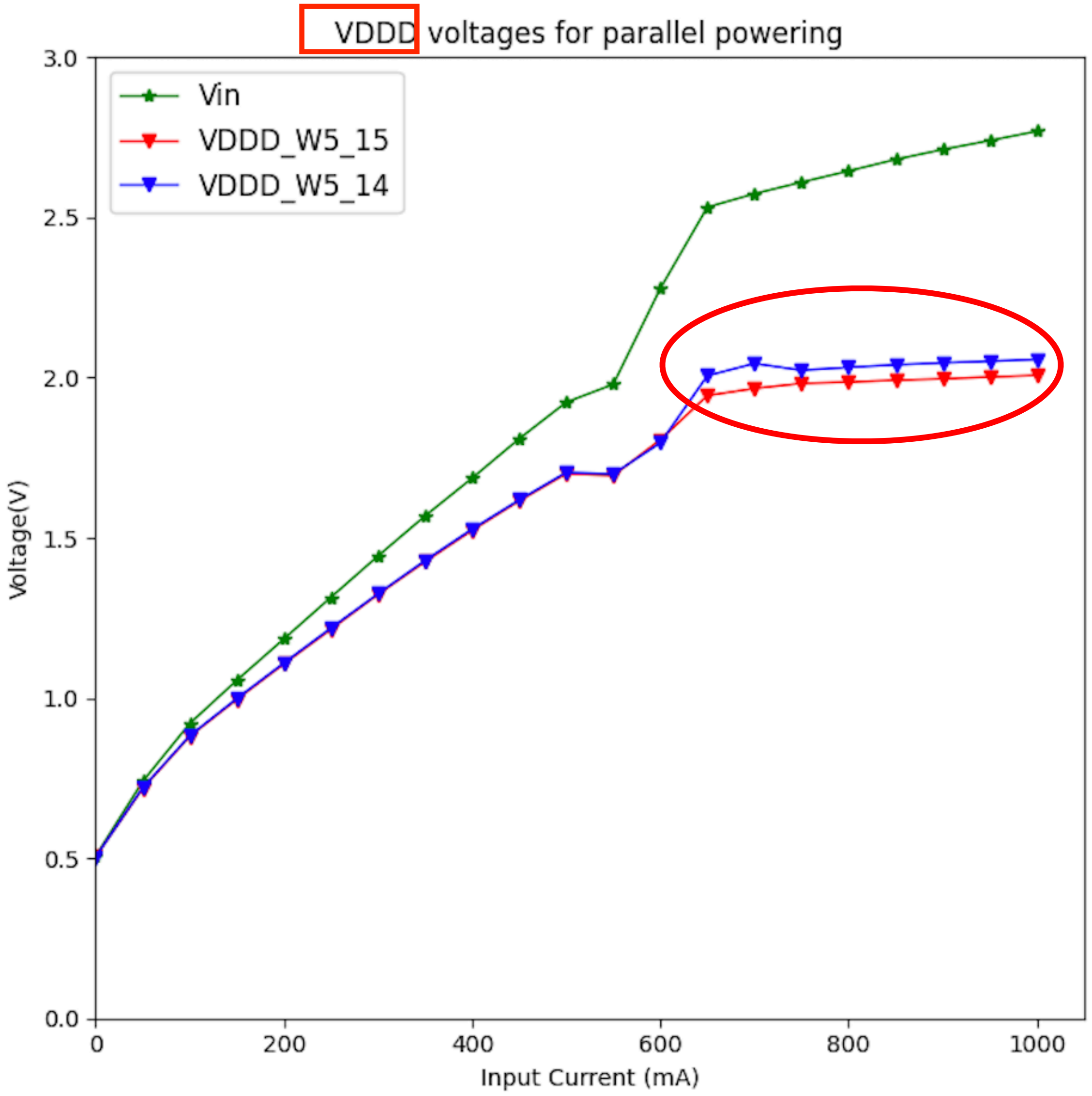




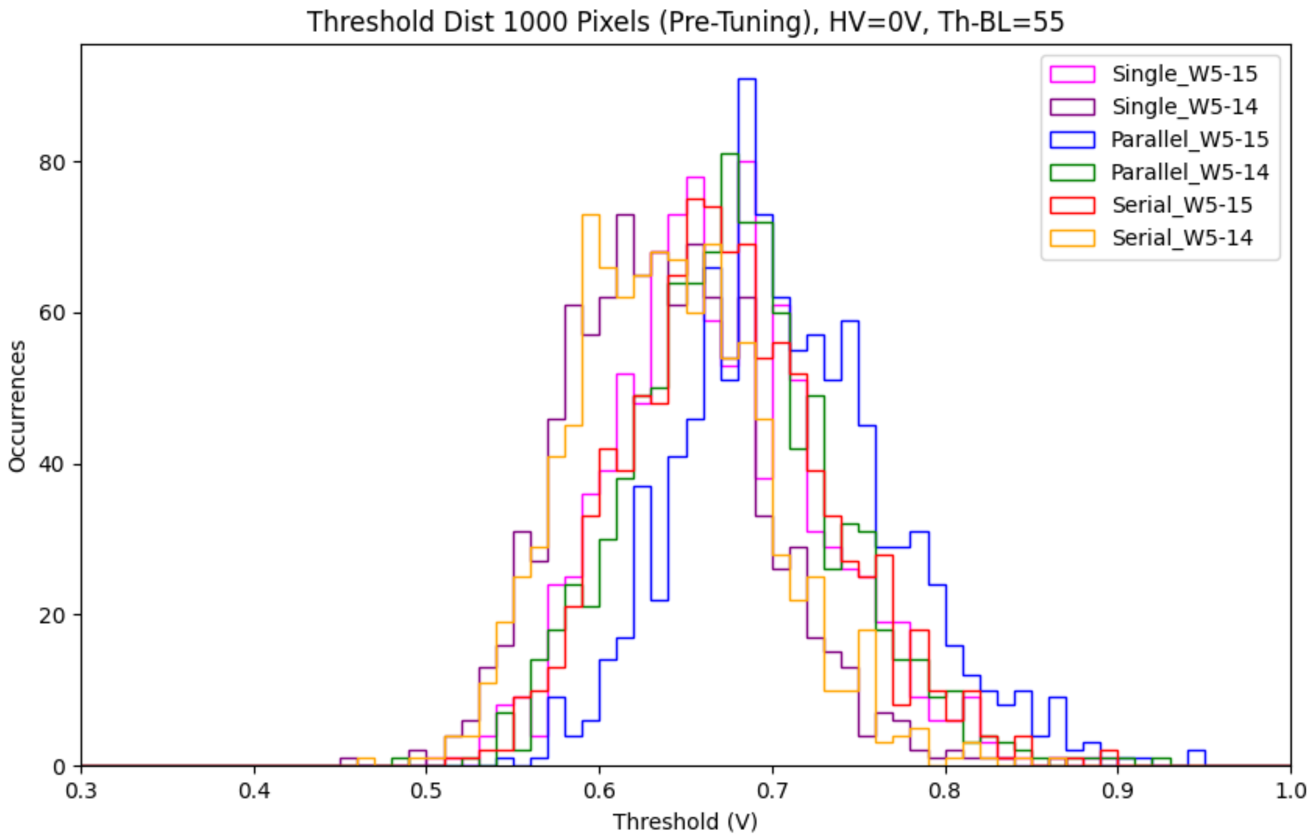
Shunt-LDO characterisation - Two chips in Parallel

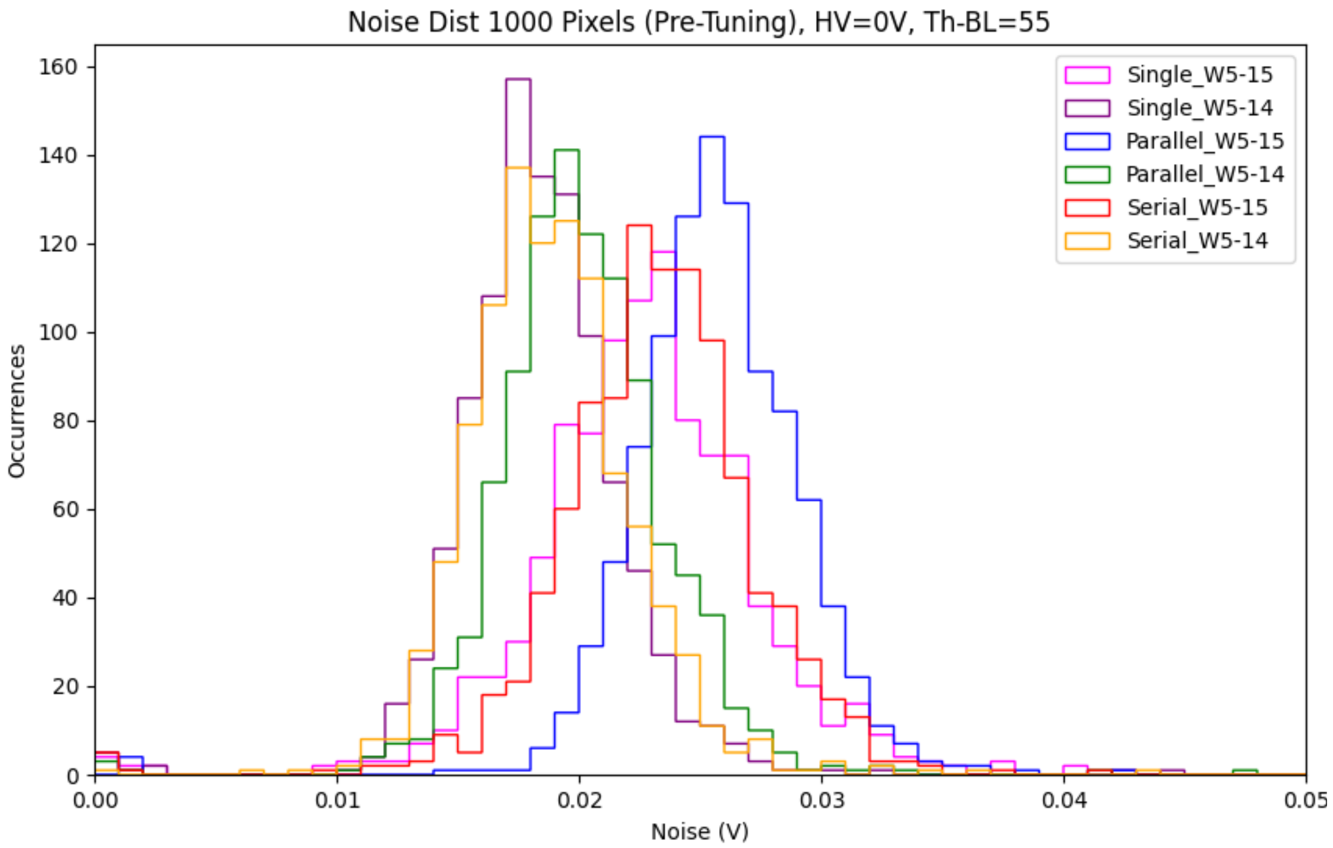






Multi-chip readout and characterisation



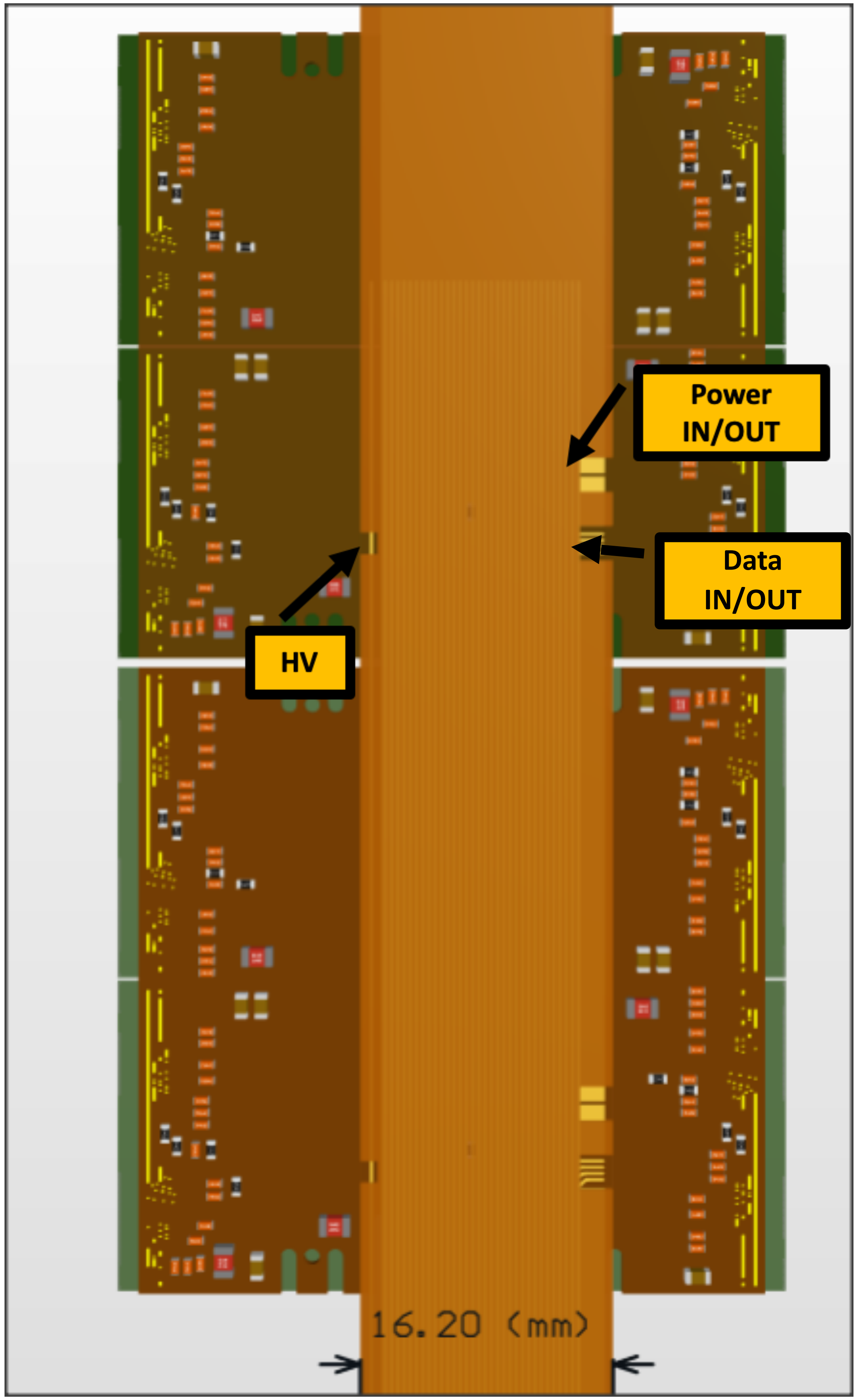


- Very minor degrading with the same thresholds when connected in parallel

	Constant Current Single		**Constant Current Parallel Connection**		**Constant Current Serial Connection**	
	Threshold (V)	Noise (V)	Threshold (V)	Noise (V)	Threshold (V)	Noise (V)
SCC (W5-15)	**0.670 ± 0.0591**	**0.0227 ± 0.00462**	0.710 ± 0.0613	0.0257 ± 0.00348	**0.676 ± 0.0593**	**0.0233 ± 0.00407**
SCC (W5-14)	**0.638 ± 0.0554**	**0.0184 ± 0.00341**	0.678 ± 0.0591	0.0202 ± 0.00408	**0.640 ± 0.0558**	**0.0189 ± 0.00341**

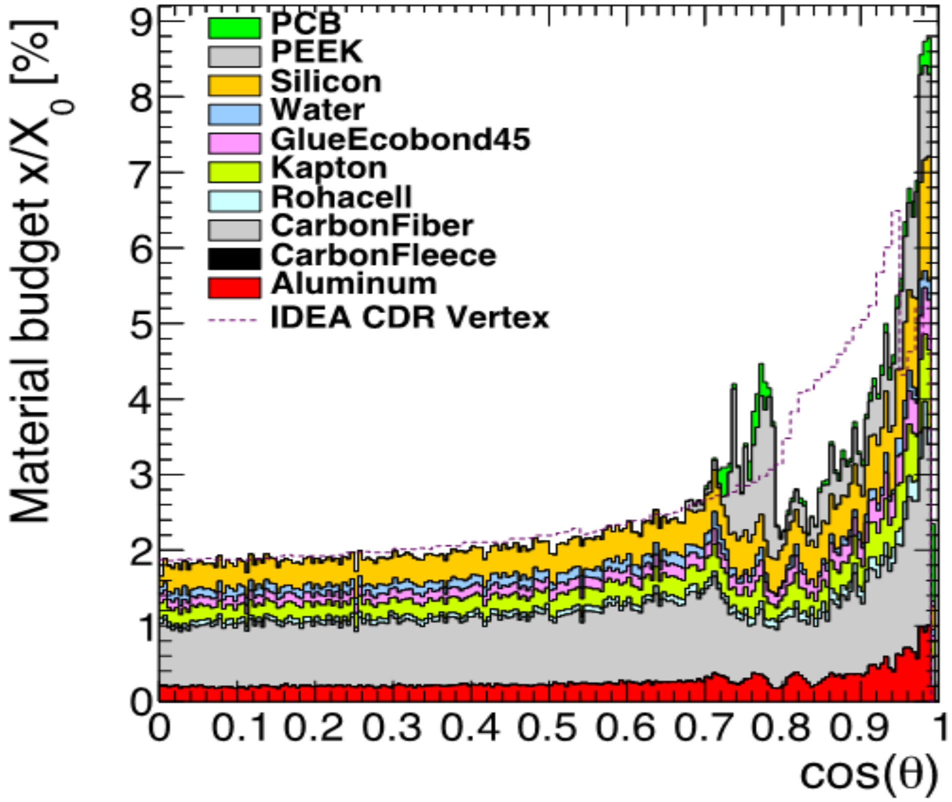
Quad-module → Stave electrical bus

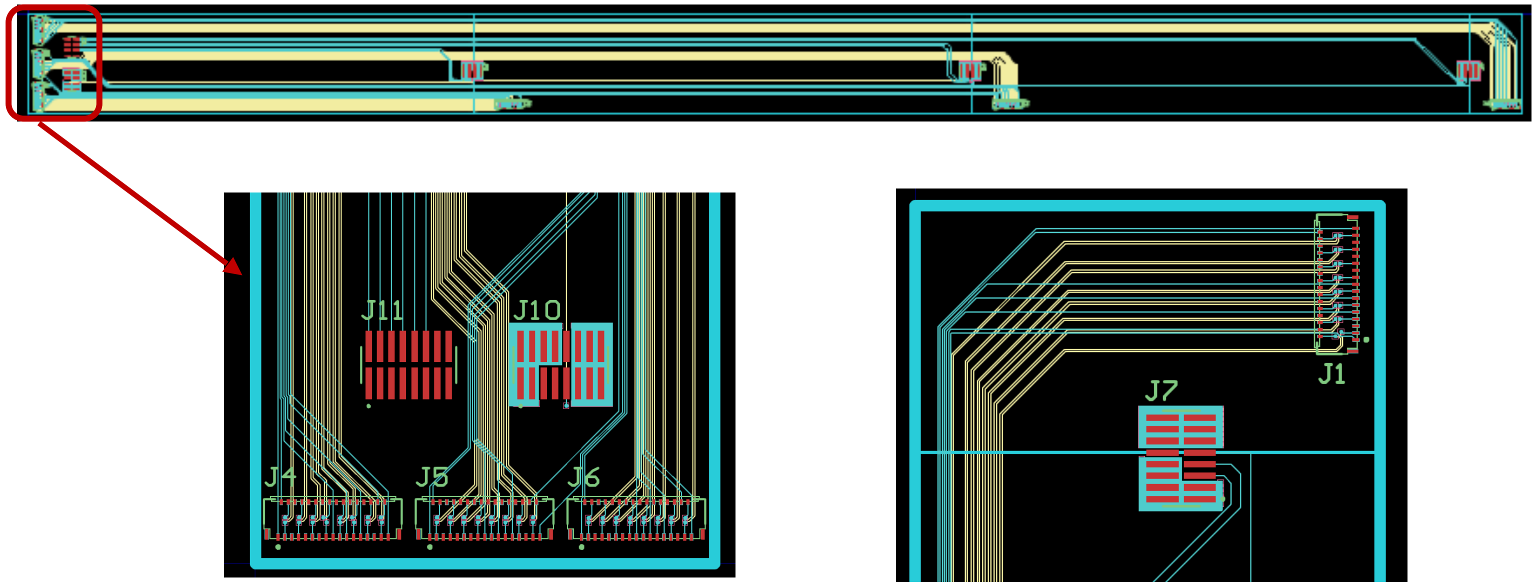
- Distribution of power and data along the stave
  - reducing power dissipation on the distribution lines
  - minimise the number of connections
- Read-out units
  - Multi-chip modules (example 2x2 quad modules)
    - Or large stitched detectors
  - Bias in parallel all sensors in a module
- Serial powering chain supplied by constant current
  - All biases are generated internally by SLDO and on-chip regulators
- Al-based PCB to reduce material



Bus tape R&D in Al

- Bus tape in Al to chain multiple modules
  - The radiation length for Al is six times smaller than the one for Cu.
  - Goal is to reduce material at the end (dominant contribution to stave material)
  - Design submitted to CERN production lab (Rui de Oliveira)
  - characterize the process (line impedence, voltage drops...)
  - synergies with BelleII (similar stackup and feature size) and possibly with LHCb MightyTracker



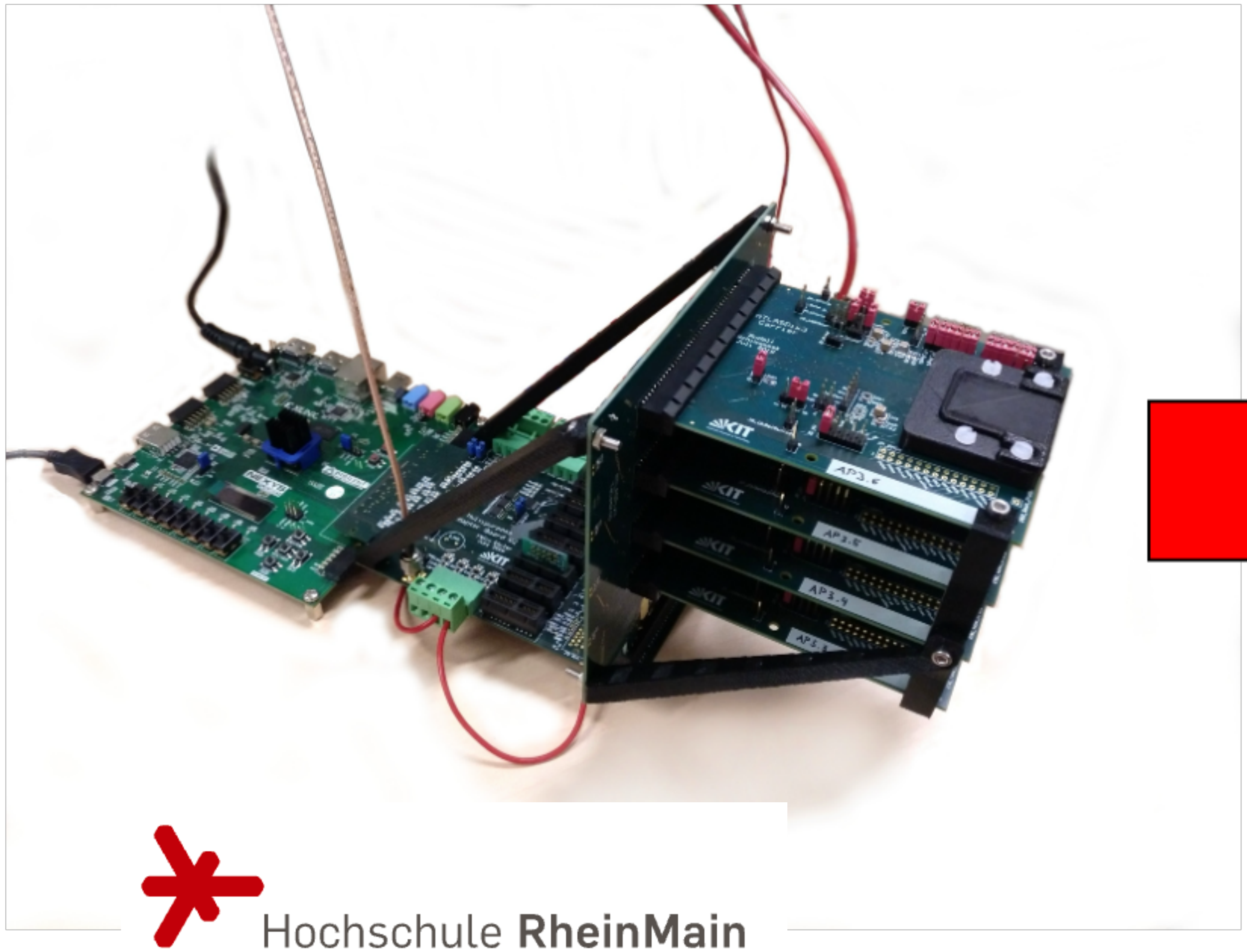


End of stave side

Last module side

Test multi-chip readout at nominal speed

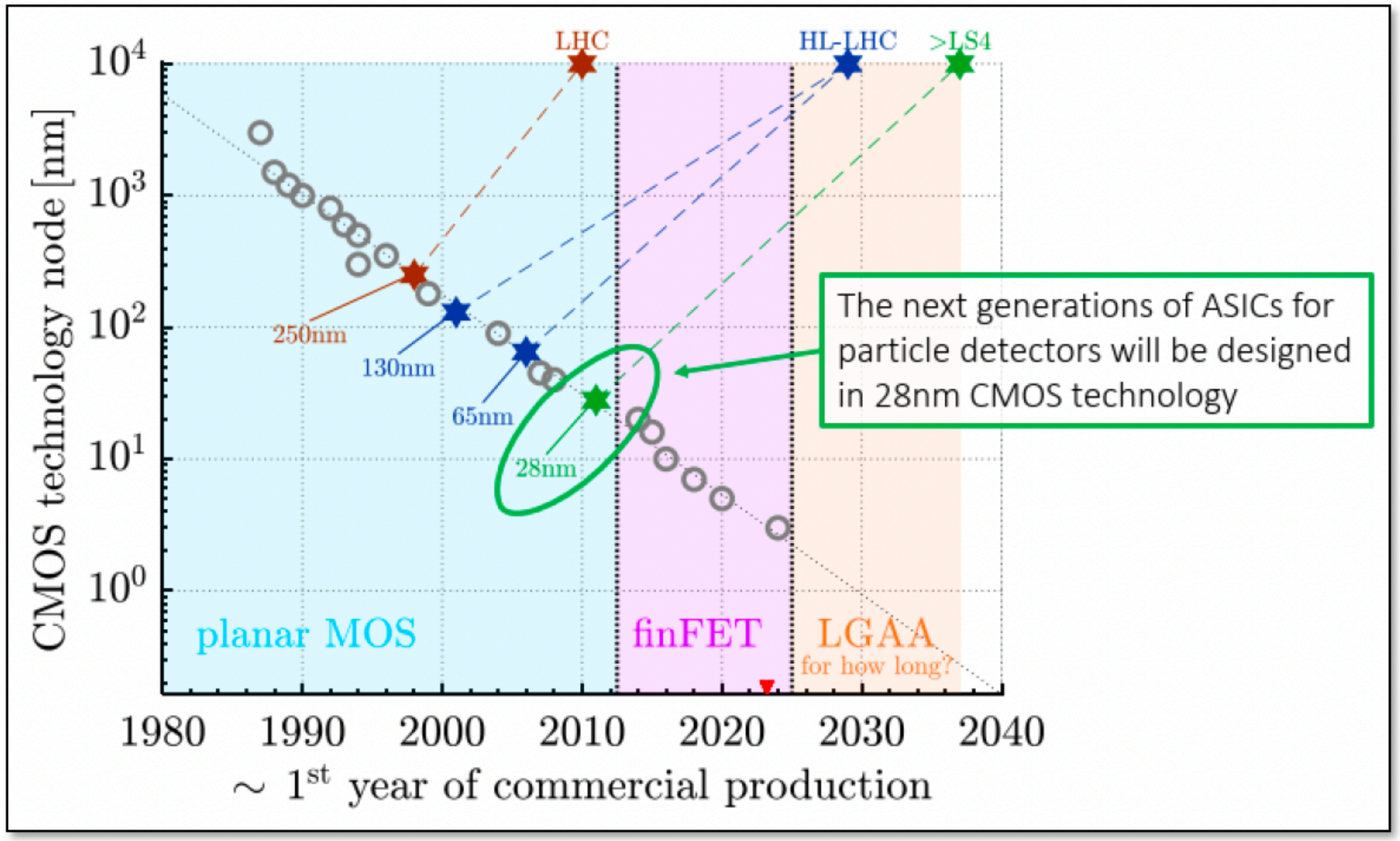
- APix3 nominal readout has been tested so far with the single chip setup
  - Multi-chip readout has been limited to 400Mb/s
- Improve the multi-chip telescope setup aiming towards testing the full speed readout
  - Clock speed limited to 200 MHz, resulting in 400 Mbit/s data rate instead of 1.2 Gbit/s design value
  - limited time resolution and prevented us from investigating APix3 design time resolution at full clock speed



Hochschule RheinMain

Global efforts towards smaller feature size

- For better performance:
    - Higher circuit density
    - More functionality in the same area
    - Less power consumption
- Much R&D on 65nm CMOS (in small electrode) has started
    - E.g. TPSCo65 (ALICE and EPIC)
    - ECFA DRD3 central programme



The next generations of ASICs for particle detectors will be designed in 28nm CMOS technology

[P. Moreira @ CEPC workshop, Oct 2023]()

CMOS Development in 55nm Process with SMIC

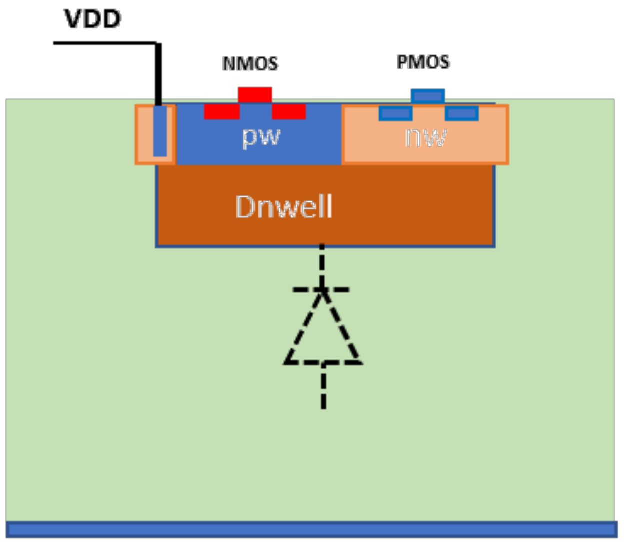
- SMIC 55nm Low-Leakage process
    - Not HV, yet with a similar deep n-well structure
    - MPW submitted in Oct 2022 in normal wafer
    - COFFEE1 received in Apr 2023
- SMIC 55nm HVCMOS process
    - HVCMOS process
    - MPW submitted in Aug 2023
    - COFFEE2 received in Dec 2023
- Several posters/talk in this workshop
    - Poster by Jianpeng Deng: TCAD simulations for HVCMOS
    - Poster by Leyi Li: Design of COFFEE2
    - Poster by Zhiyu Xiang: Test of CMOS chip using 55nm process
    - Yang Zhou (talk on Friday): focused on design in the silicon and electronics session

CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

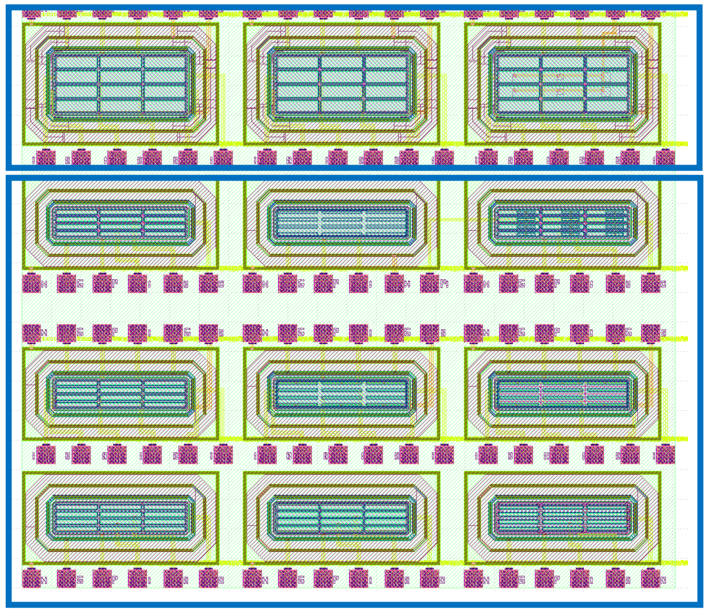
COFFEE1: MPW in Low Leakage process

- SMIC 55nm Low Leakage process
  - Not HV, but with similar deep N well separating the transistors and the sensor
  - 3×2 mm² in area
  - Variation of passive diode arrays
    - With/without P stop between pixels:
    - Space between pixels: 5um, 10um, 15um
    - Connection method
  - Simple amplifiers added
- Tests on the passive diode arrays
  - IV shows breakdown ~ 9V
  - Single pixel capacitance ~ 180fF
  - Response to laser observed

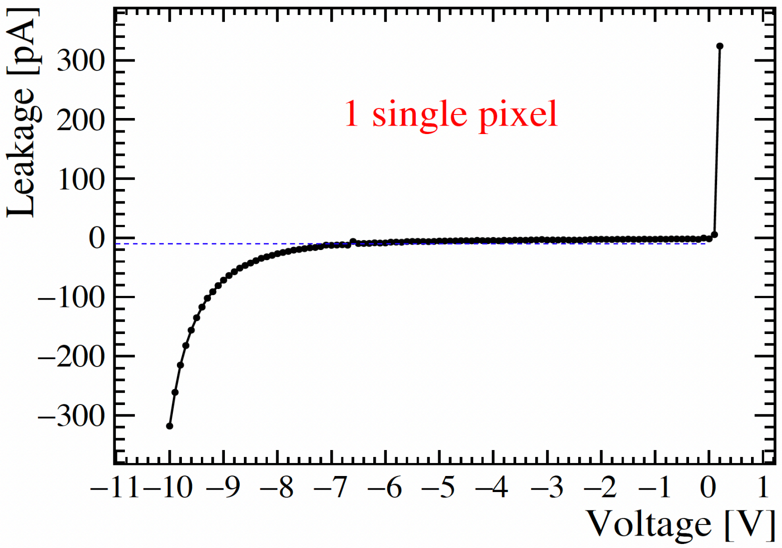
LL process

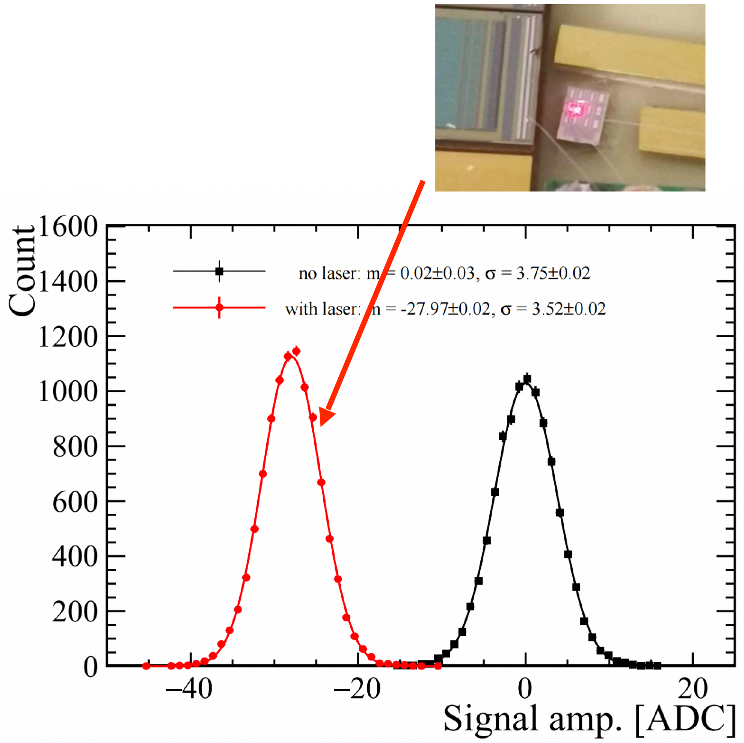


Pixel size:50x150um



Pixel size:25x150um



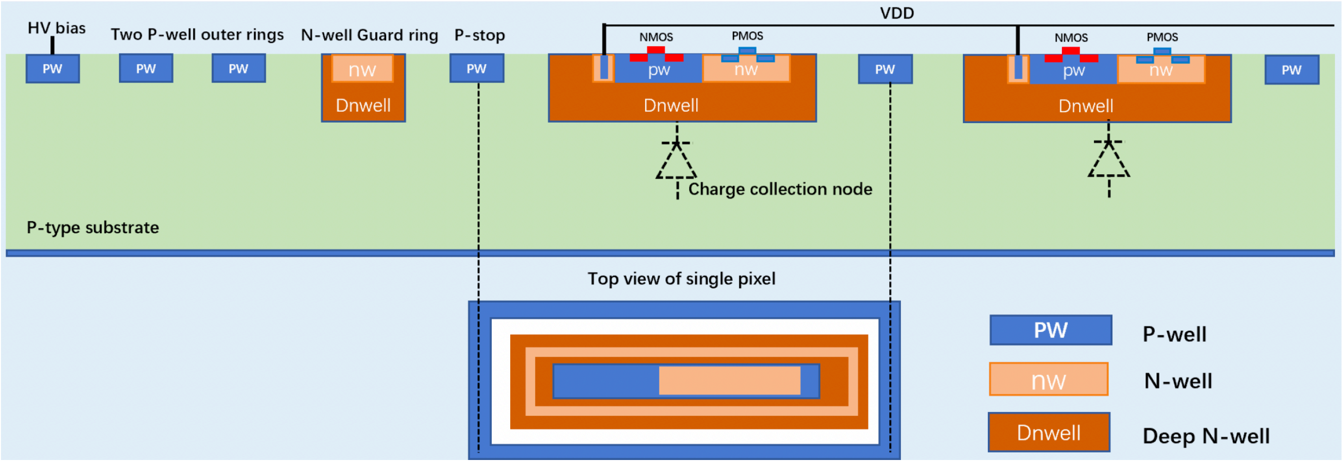


NIM A 1069 (2024) 169905

COFFEE2: MPW in HVCMOS process

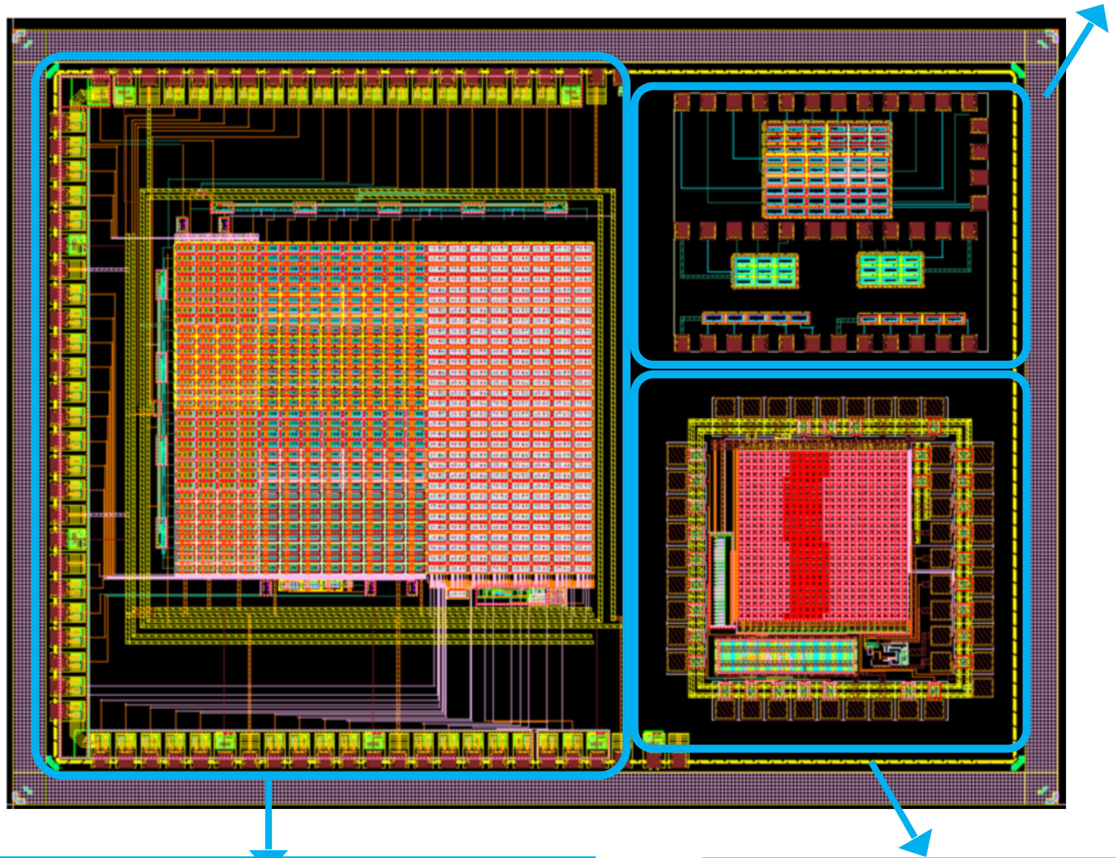
- 2023 MPW: SMIC HV 55nm process
  - 4mm * 3mm in area
  - Passive arrays similar as COFFEE1
  - Two pixel arrays with in-pixel amplifier and more digital design

Cross-section of pixel structure



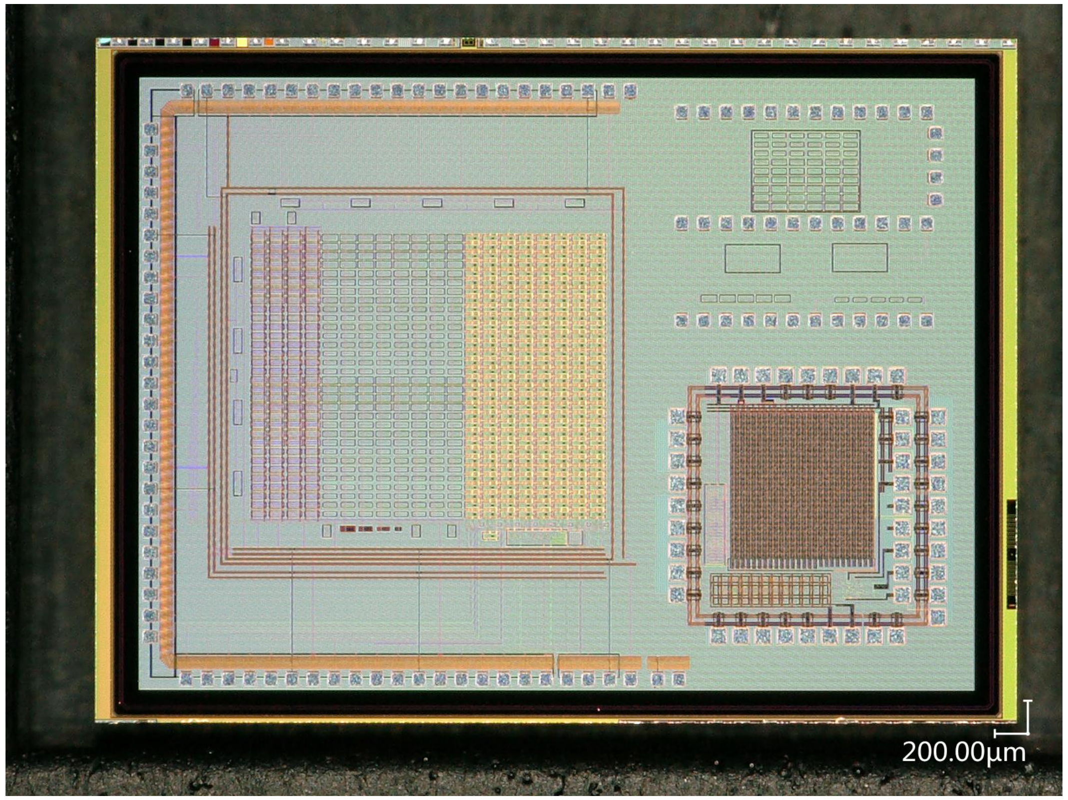
COFFEE2 floorplan

1. Passive diode arrays



2. Pixel arrays with diodes and in-pixel electronics

3. Pixel arrays with peripheral digital readout



COFFEE2 photo

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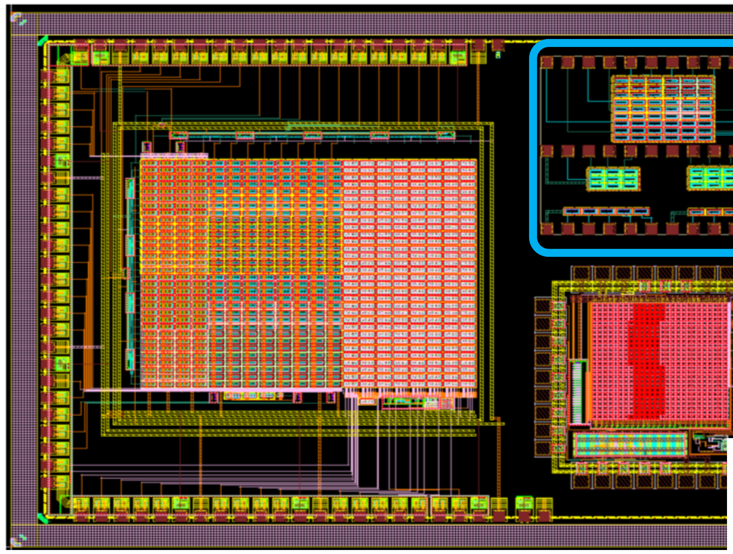
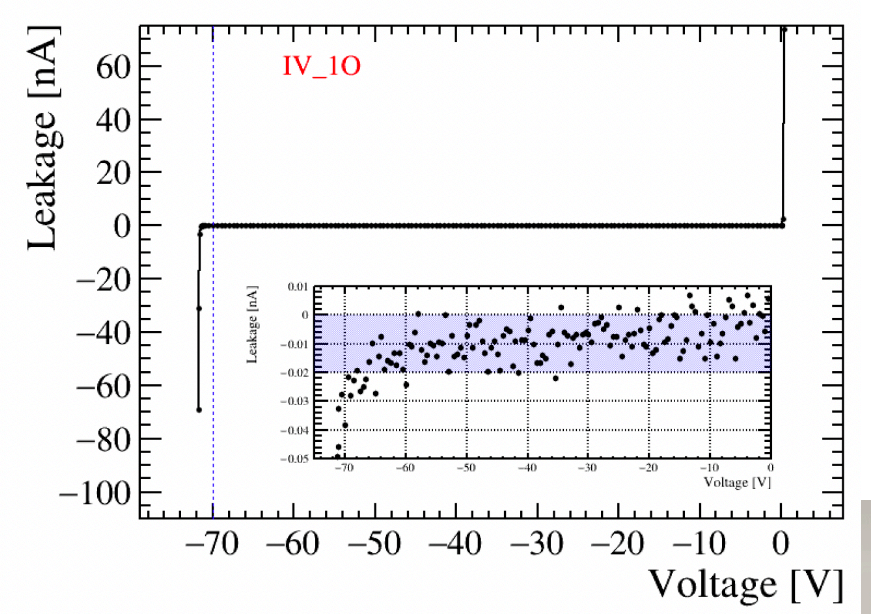
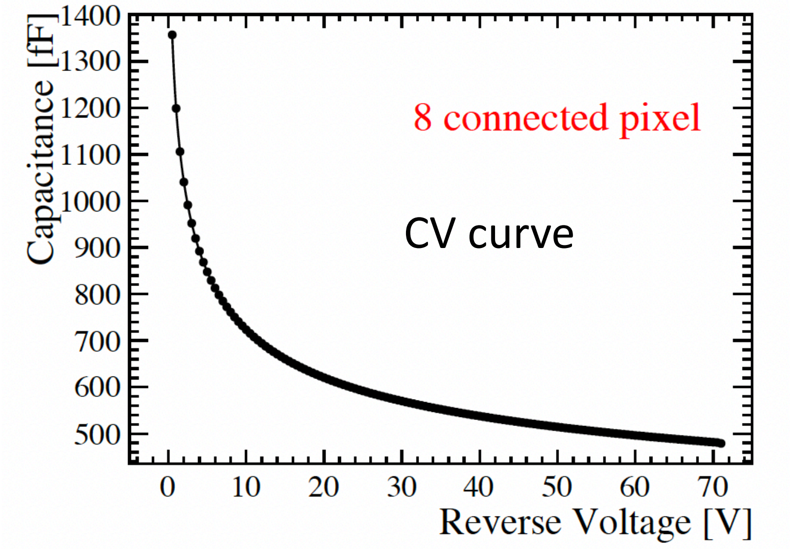
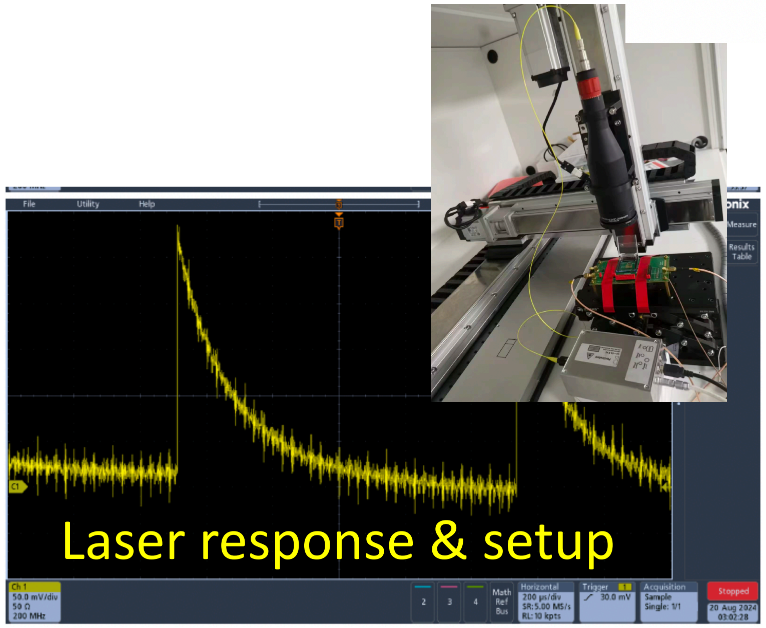
COFFEE2: Initial Test Setup and Results



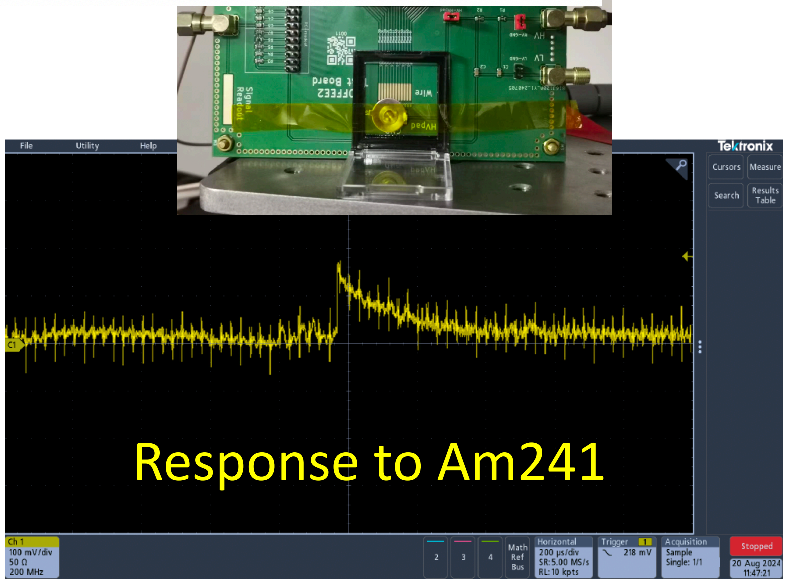
- So far tests have been focused on passive sensor arrays
  - IV (breakdown at –70V)
  - CV (single pixel ~30-40fF)
  - Leakage current increased from ~10pA to ~1nA after $10^{14} n_{eq}/cm^2$ radiation
  - Laser and radiative source responses observed



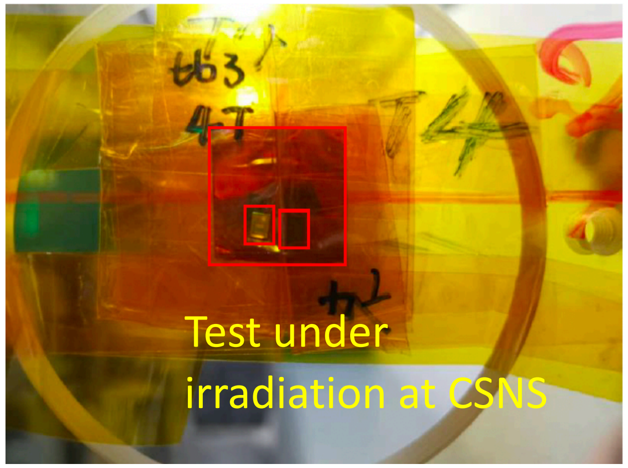




Laser response & setup



Response to Am241

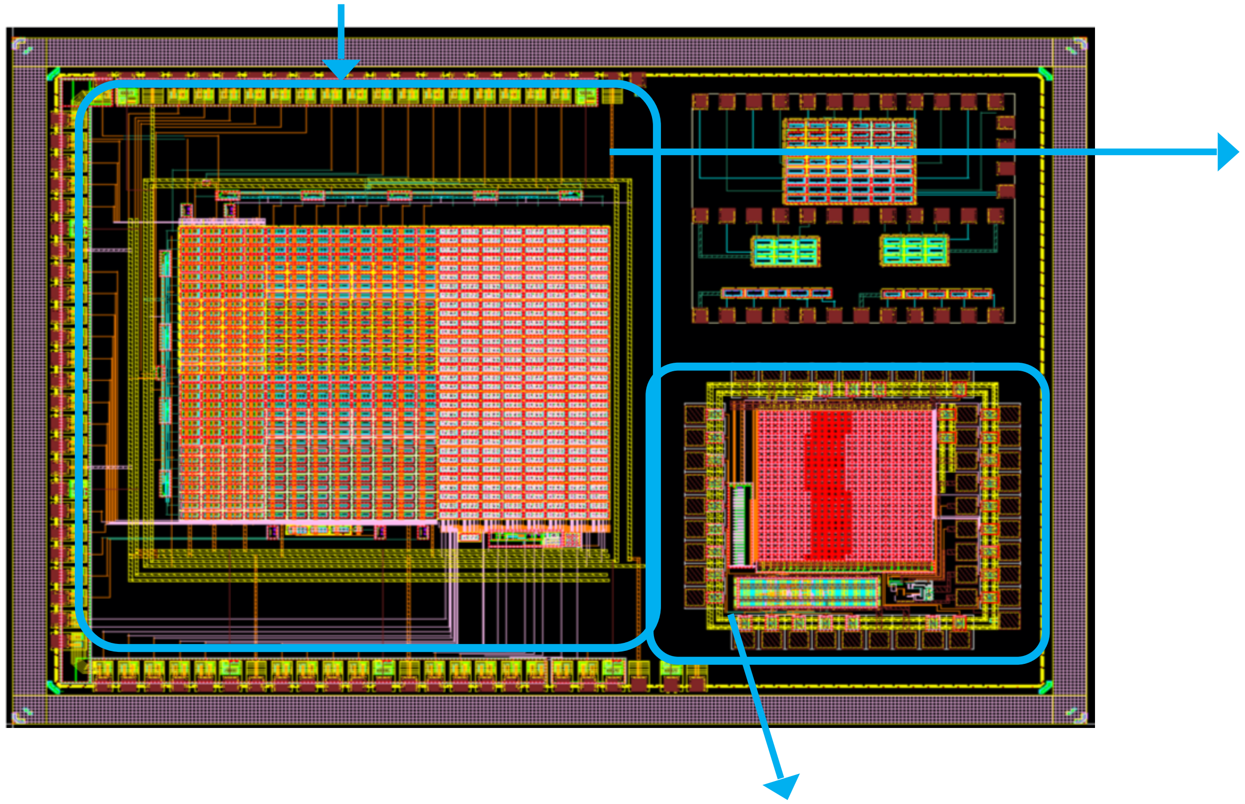


Test under irradiation at CSNS

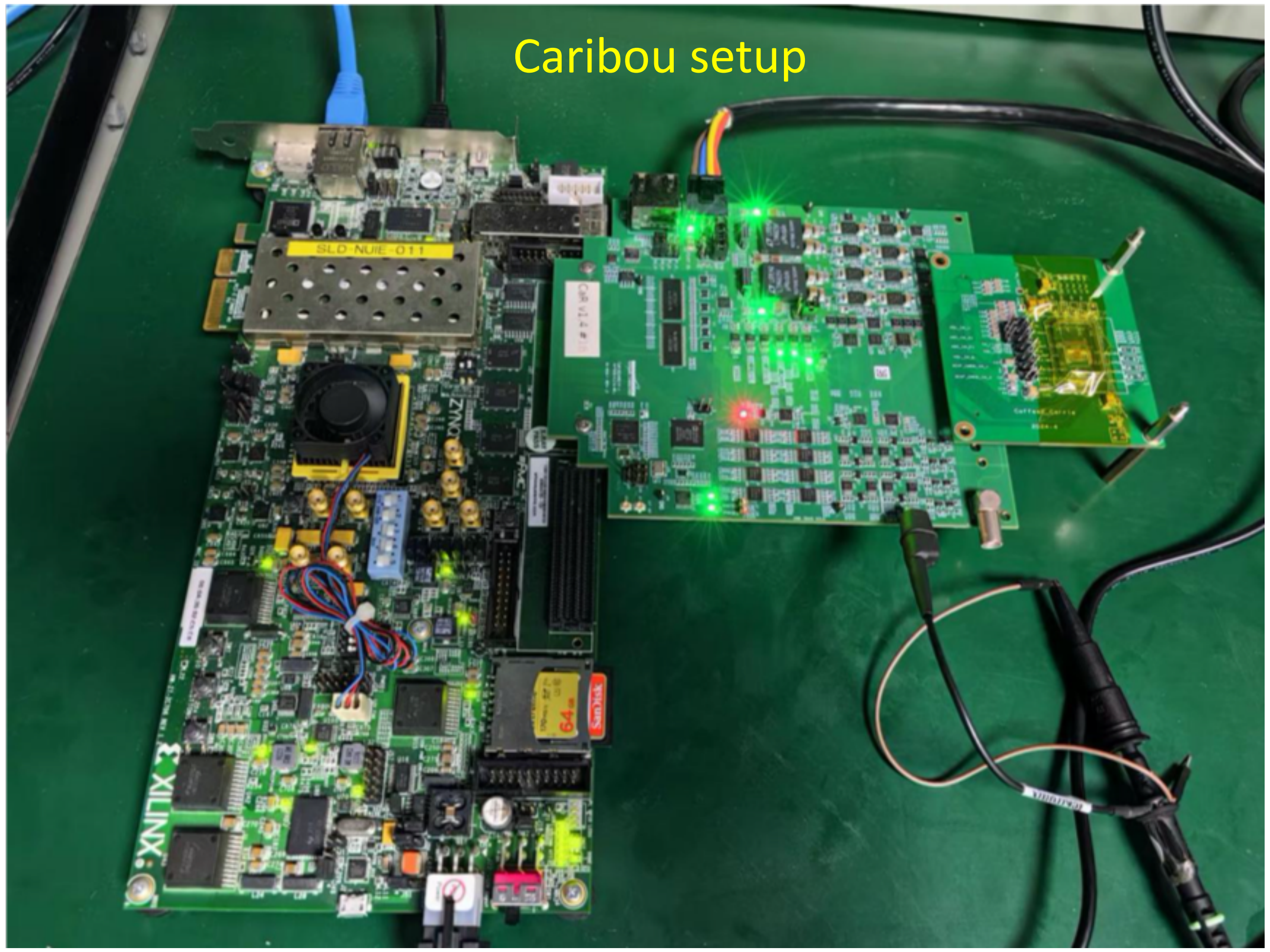
COFFEE2: main circuit test setup nearly ready

- Commissioned new readout system based on Carbibou
  - Dedicated carrier board designed and fabricated
  - Caribou system installed, final firmware debugging

Pixel arrays with diodes and in-pixel electronics



3. Pixel arrays with peripheral digital readout, see Hui Zhang’s poster at TWEPP



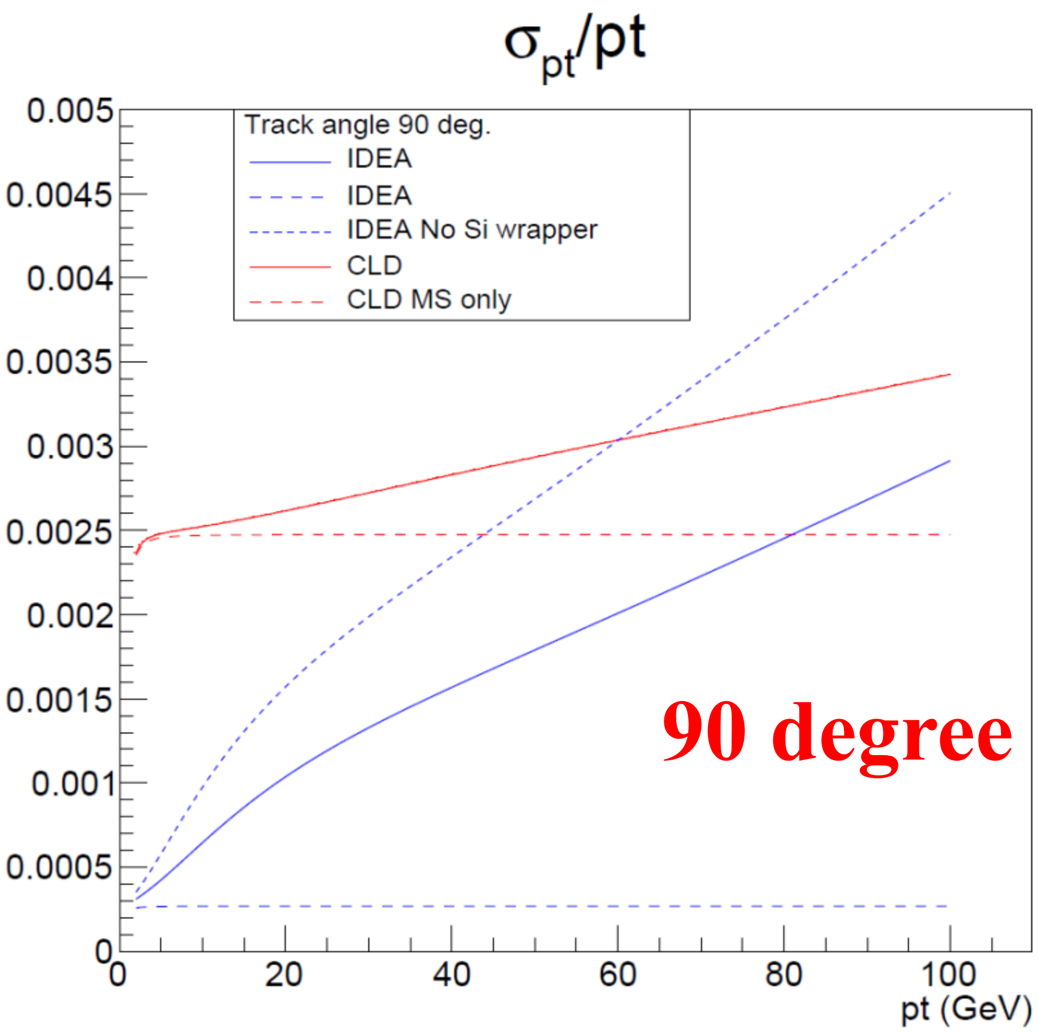
Summary and Next Steps

- Updates on APix3.1 based multi-chip system prototyping
  - APix3.1 Shunt-LDO has been verified at single chip and double-chip structure
  - Second quad flex have been produced and ready to be assembled into quad-modules
  - New multi-chip telescope setup is being developed to test the full speed readout
- Next steps for APix3 and 180nm R&D in the next 2-3 years
  - Assembly O(5) quad-modules and integrate into 1-2 SP chain(s) in 2025-26
    - Main aim: characterise SLDO in HV-CMOS in a realistic SP chain
  - If funding allows, explore small scale MPW (180nm/130nm) contributions to investigate more efficient data communication (e.g. chip-to-chip communication) and future power reductions
  - Long-term goal is to incorporate this into the sensor of choice in 3 year's time
- Excellent progress in the 55nm HV-CMOS development with SMIC
  - First HV-CMOS MPW has been fabricated and initial electrical tests are promising
  - Identified a 3-year plan towards sensor technology verifications for large area applications
- A lot of the on-going work is now pursued within the DRD3 collaboration

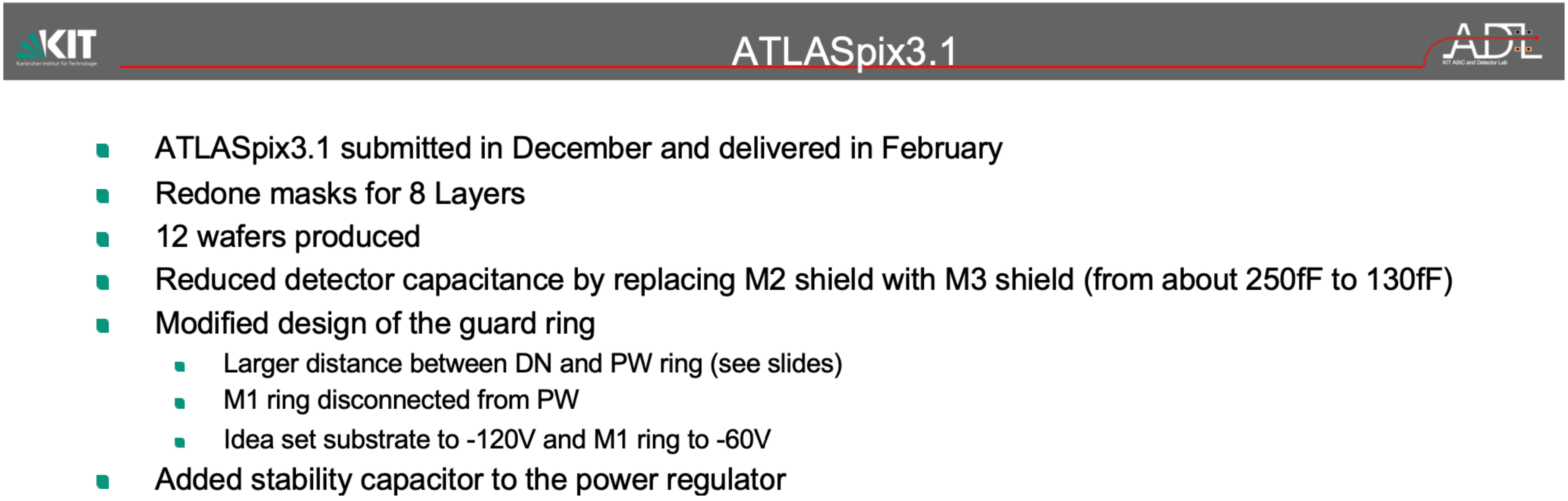
Backup slides

Large Area Tracker: case for the IDEA outer layer

- Outer layer: precision silicon layer around the central tracker
  - Improve momentum resolution by providing additional measurements
  - Extend tracking coverage in the forward/backward region
  - Covered area ~90 m2
- Significant impact on services and system readout
  - Need a technology suitable for large scale production (low cost and efficient assembly)
  - Limited space for services
  - Material budget is concern
- These need to be addressed during R&D together with sensor designs



ATLASPix3.1new vs 3.0



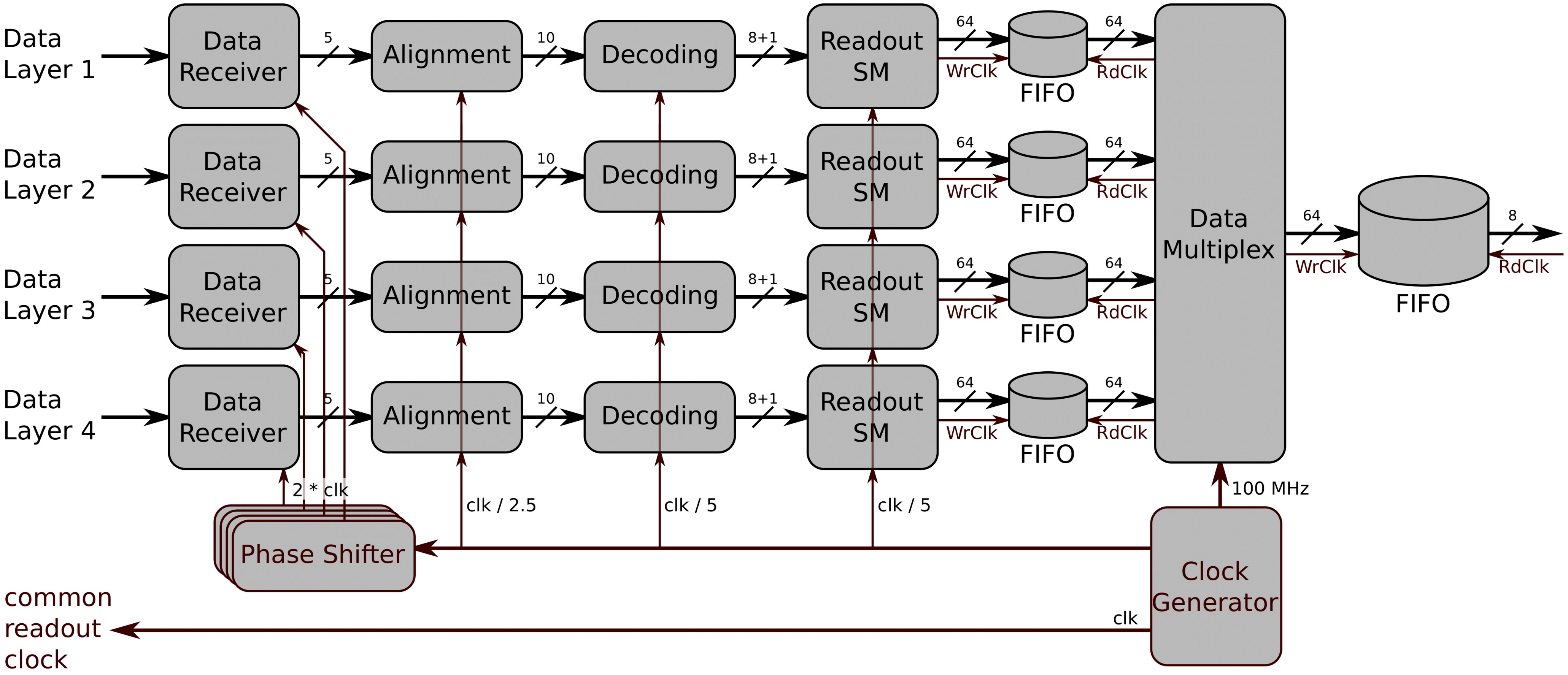
ATLASpix3.1

- ATLASpix3.1 submitted in December and delivered in February
- Redone masks for 8 Layers
- 12 wafers produced
- Reduced detector capacitance by replacing M2 shield with M3 shield (from about 250fF to 130fF)
- Modified design of the guard ring
  - Larger distance between DN and PW ring (see slides)
  - M1 ring disconnected from PW
  - Idea set substrate to -120V and M1 ring to -60V
- Added stability capacitor to the power regulator

Ivan Peric

Firm-/Software changes for quad

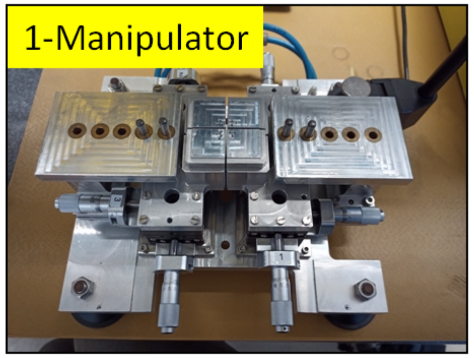
- Firmware:
  - Multiplication of the **elemental structure** for the single chip
- Software:
  - Configuration with SPI and CMD
  - Chips can be configured **simultaneously** or **individually**

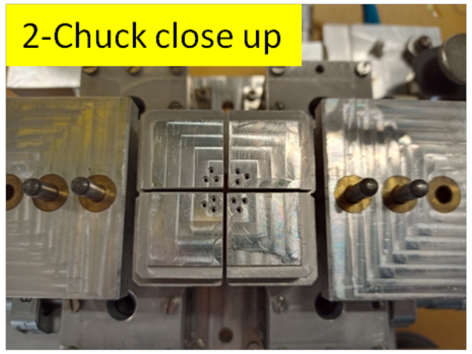


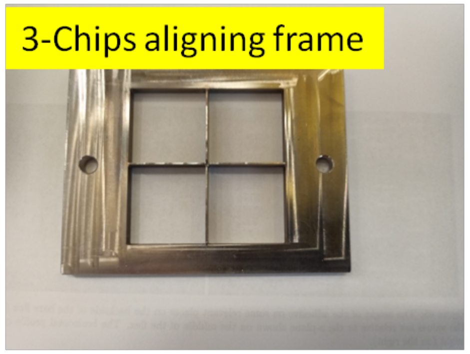
c/o R. Schimassek, KIT

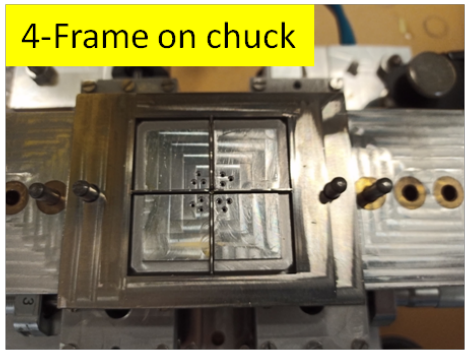
Assembly procedure

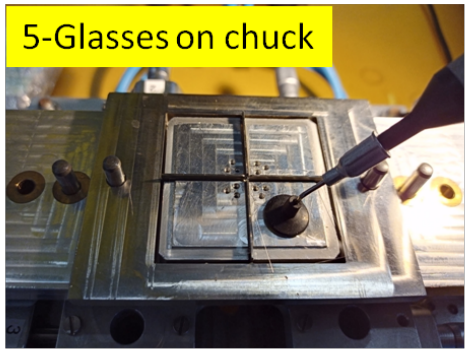
- Shown with **glass squares**: same procedure also used for real module assembly
- Gap between chip of **100 um ± 50 um** has been achieved

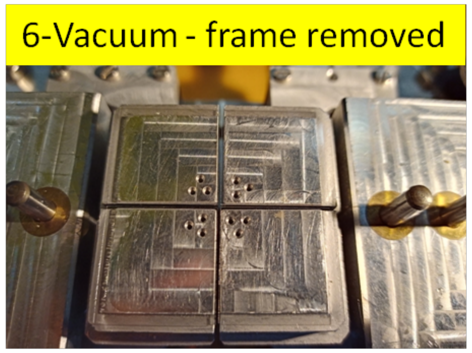

1-Manipulator

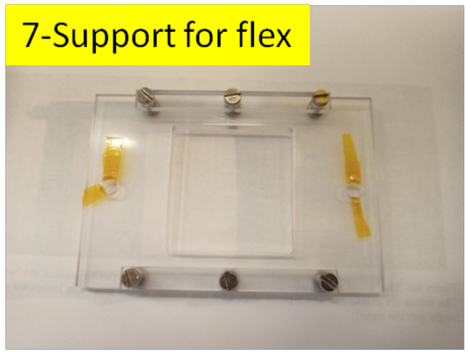

2-Chuck close up


3-Chips aligning frame

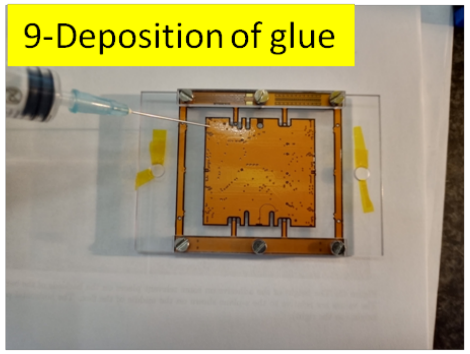

4-Frame on chuck

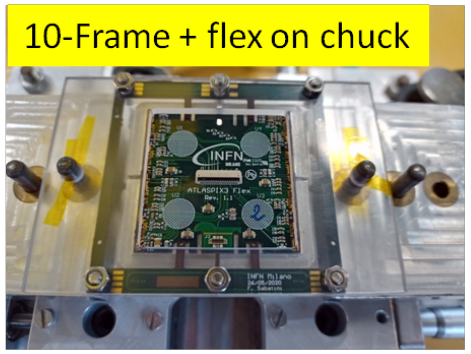

5-Glasses on chuck

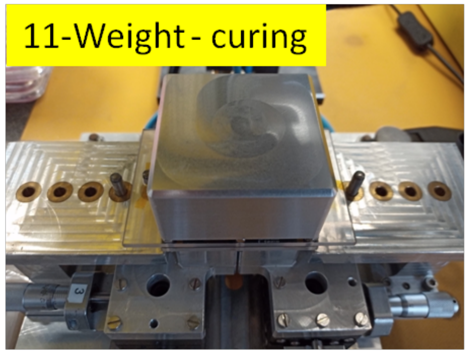

6-Vacuum - frame removed

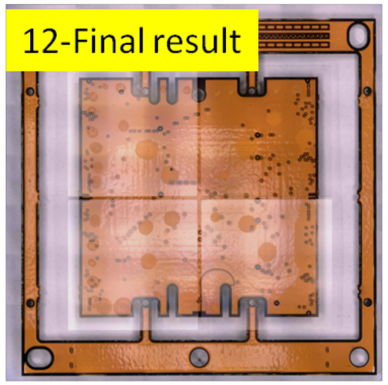

7-Support for flex


8-Flex mounted on support


9-Deposition of glue

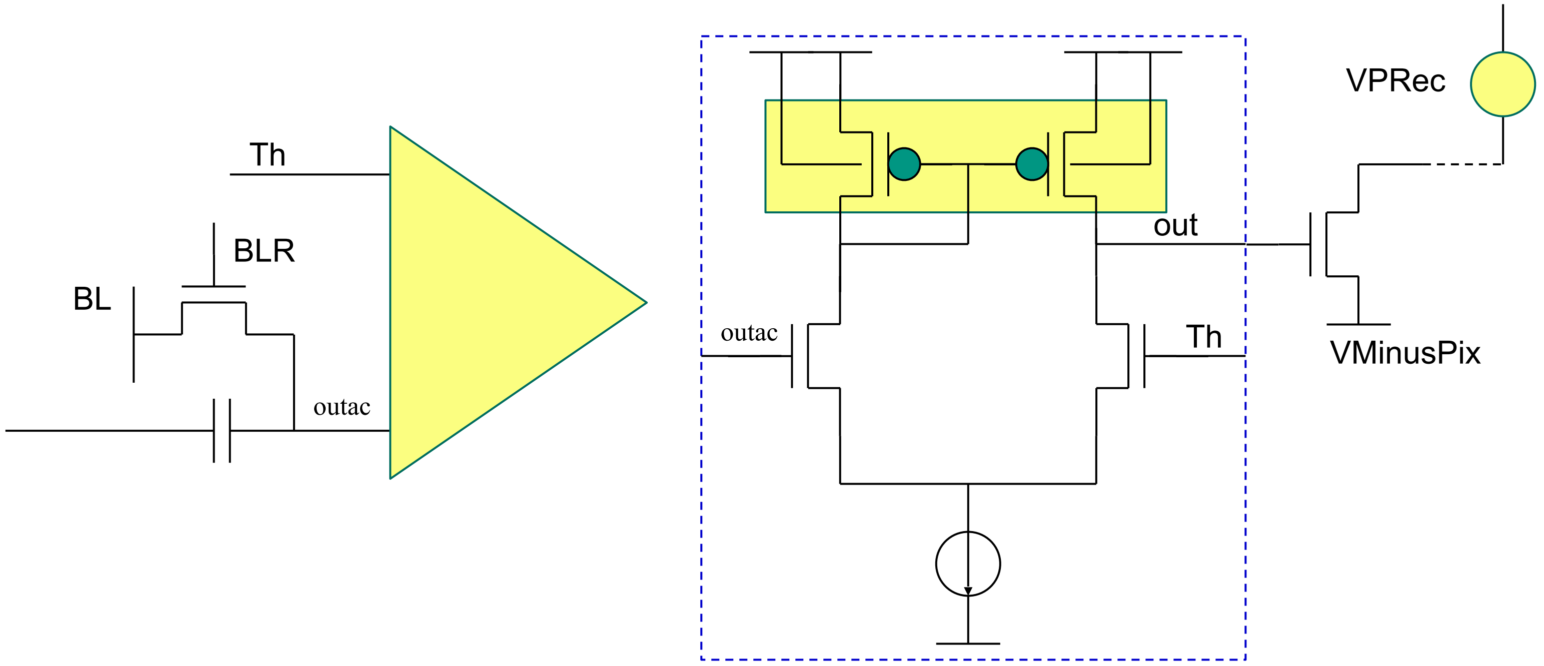

10-Frame + flex on chuck

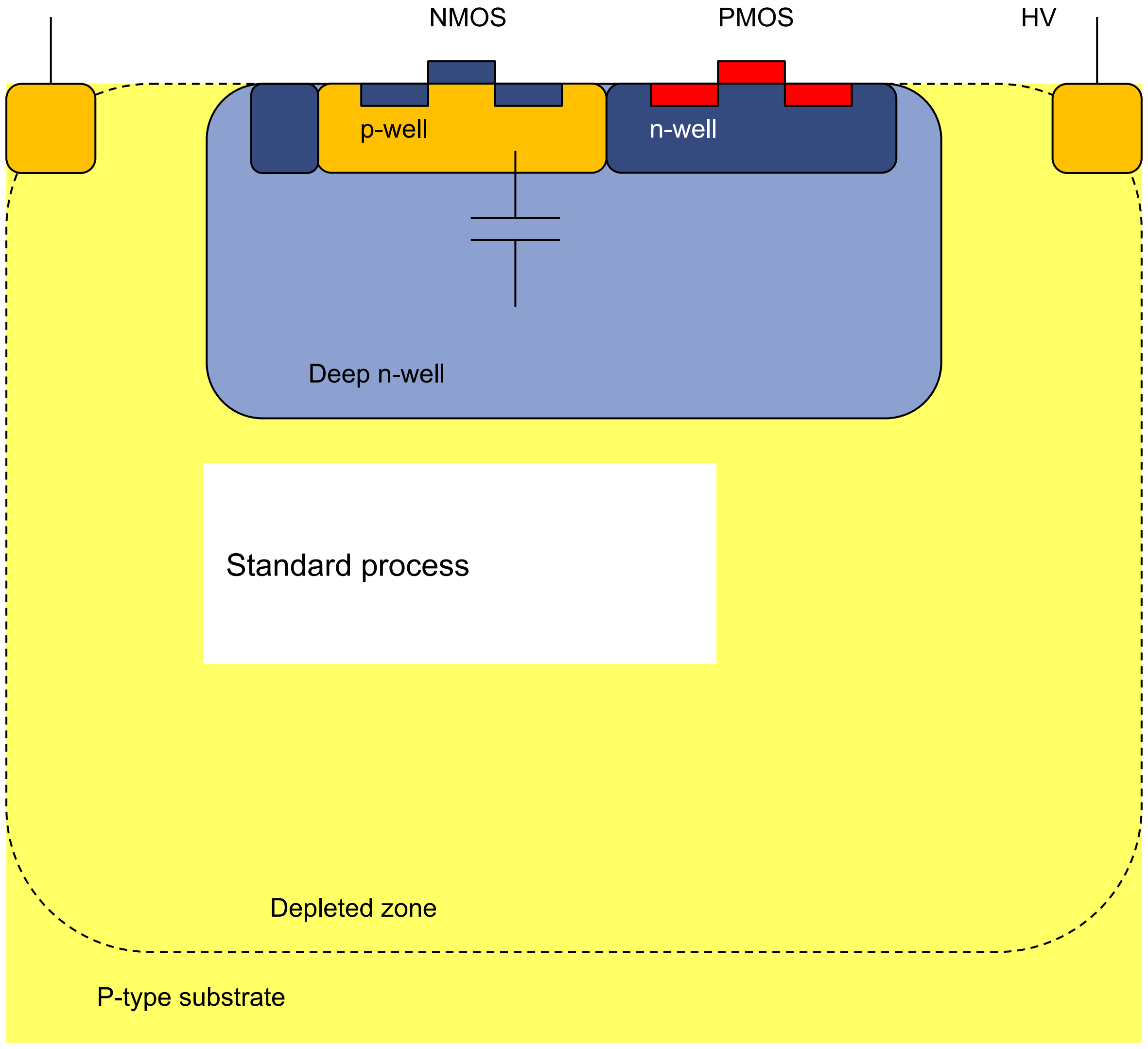

11-Weight - curing

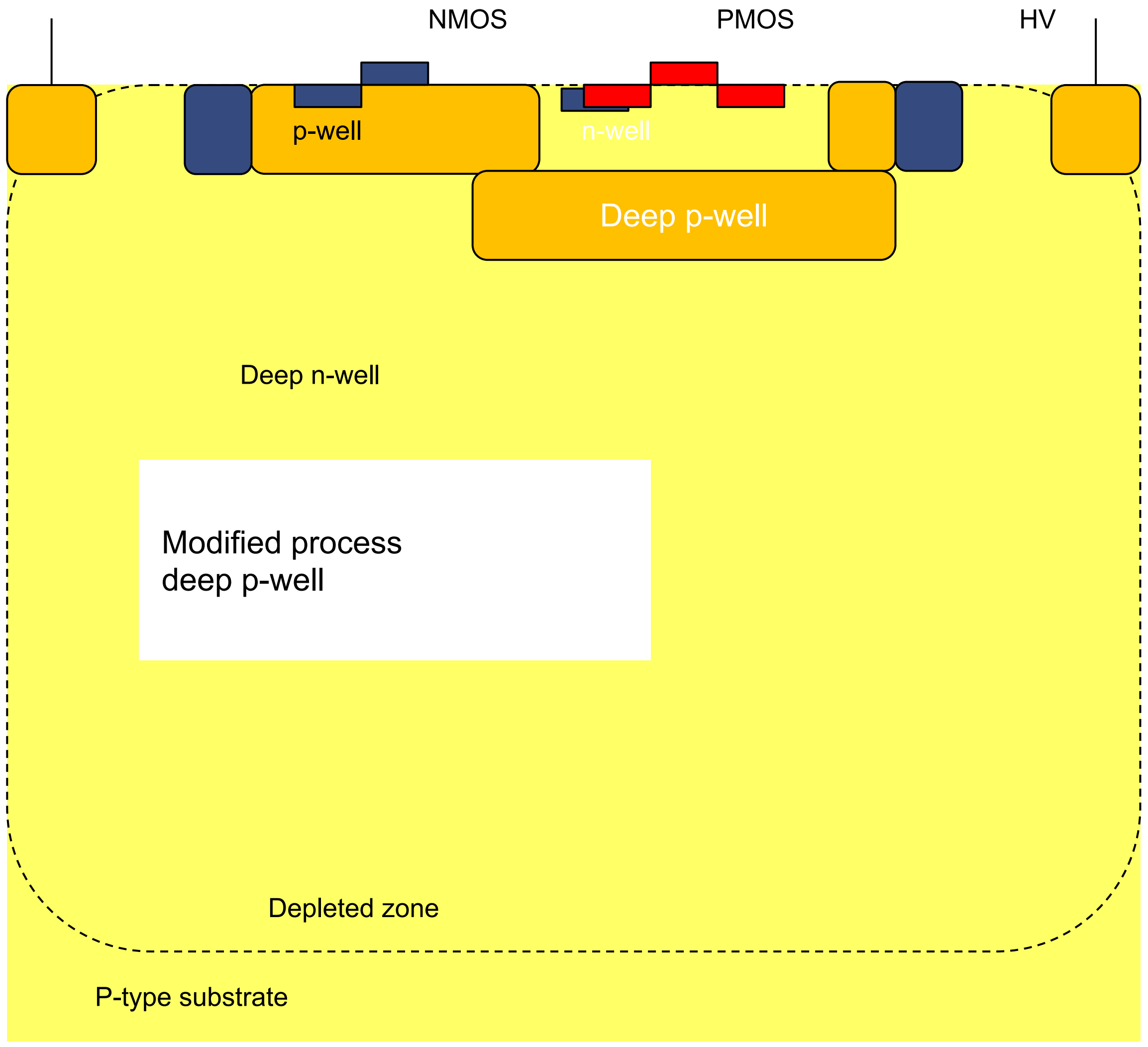

12-Final result

CMOS comparator

- Needs deep p-well
- Works with smaller bias current

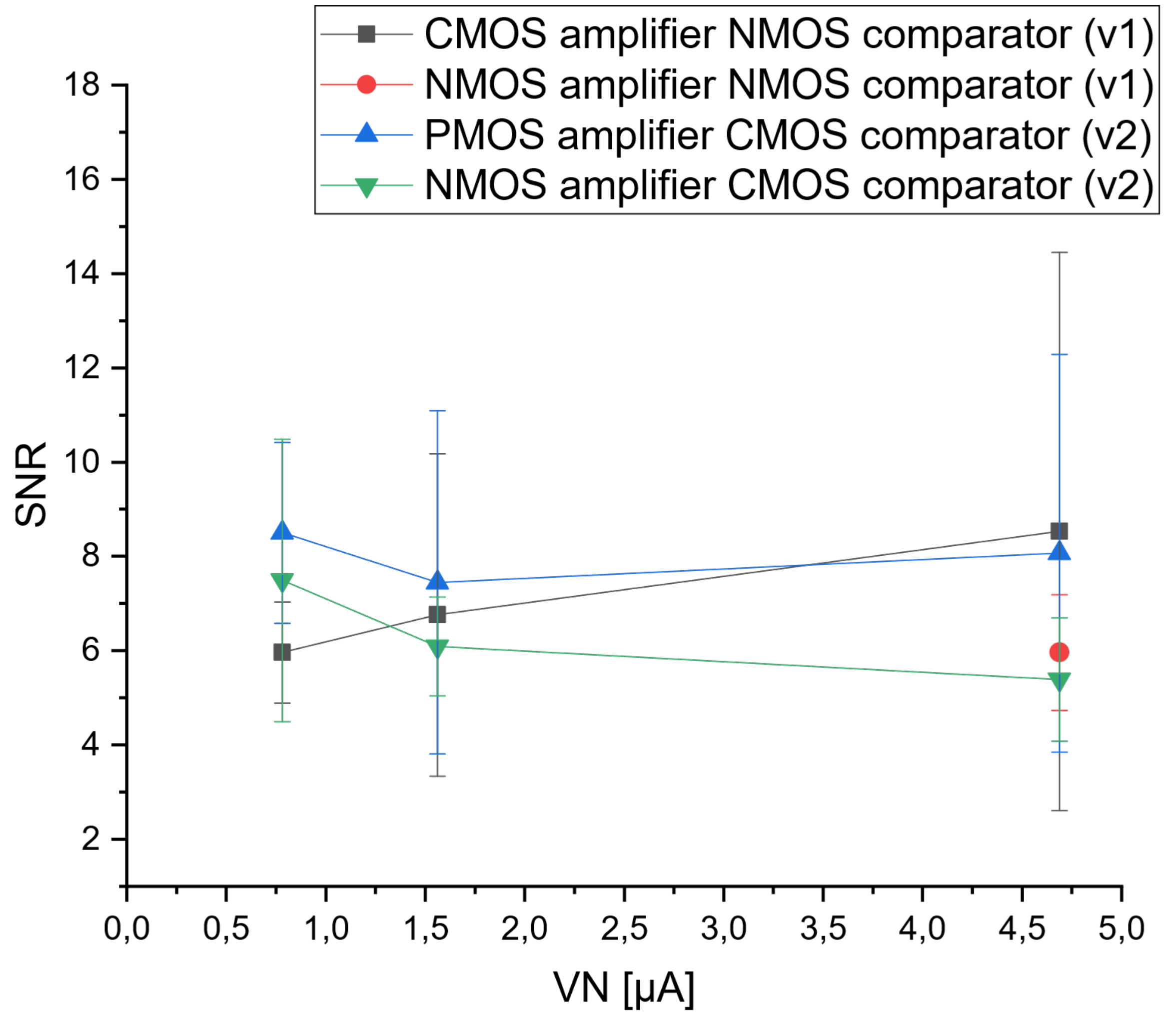


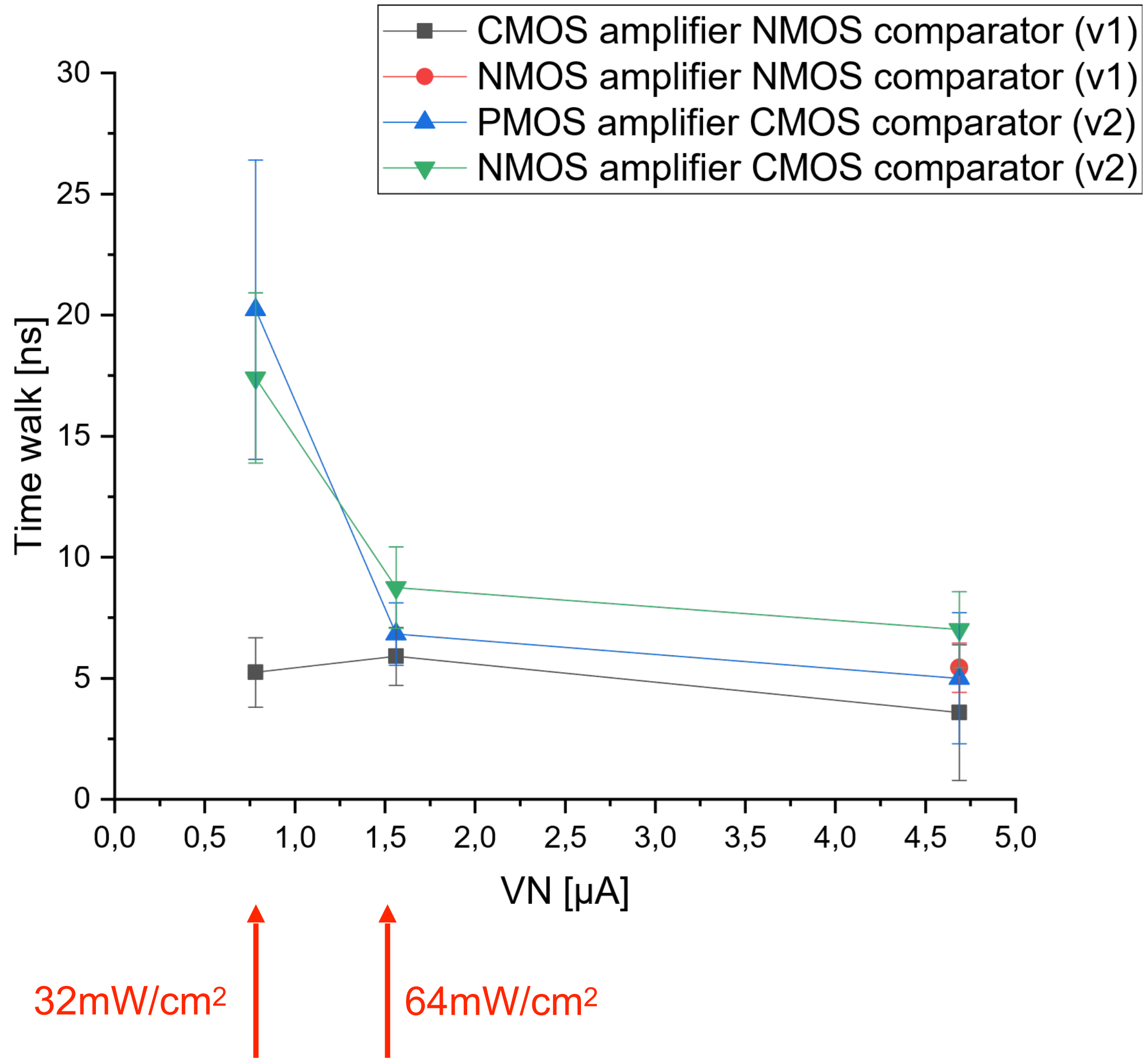




Preliminary measurements and implications

- Pixel matrices with three amplifier types have been operated with smallest possible threshold
- Signal to noise ratio (from ToT) and time walk for signals larger than 3200e have been measured
- CMOS amplifier has smallest time walk
- **Low power consumption is possible (up to factor of 4 reduction compared with ATLASPix3)**

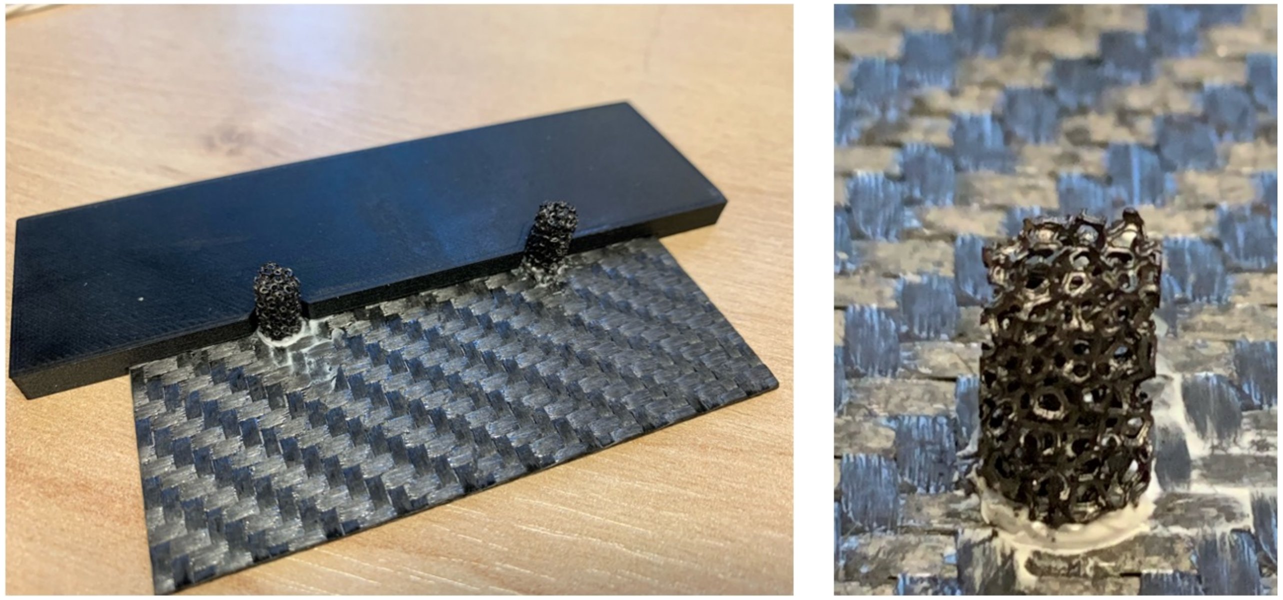




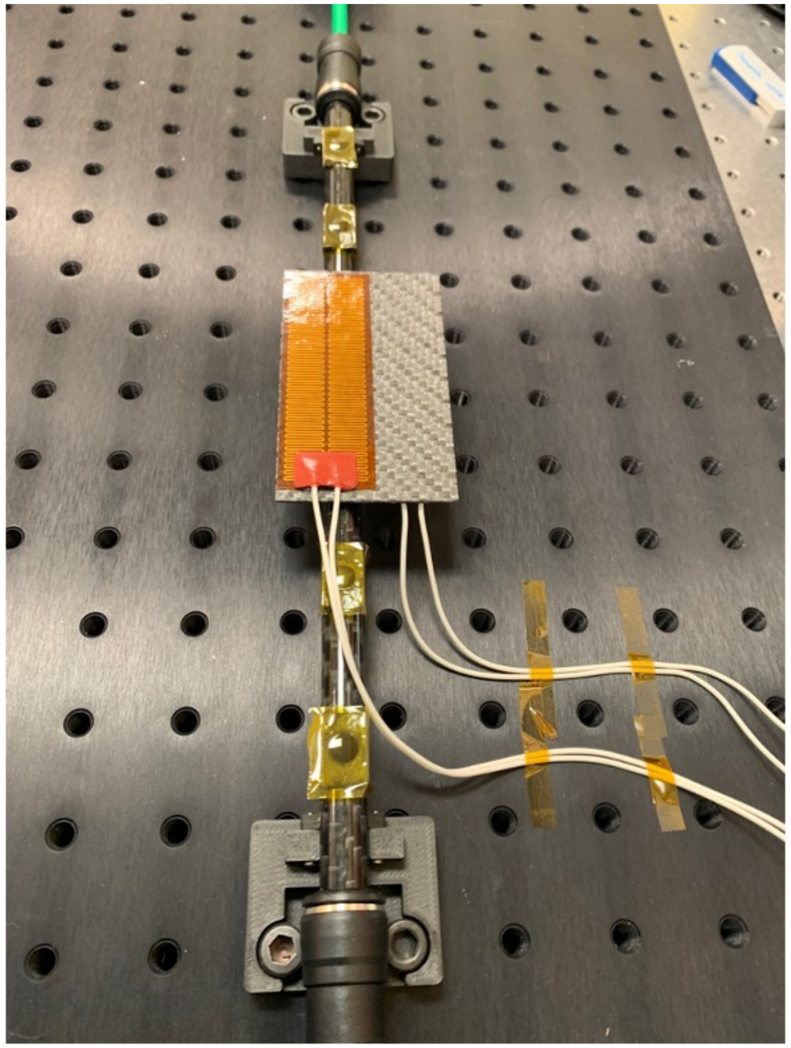
ATLASPIX3: 140mW/cm^2

Pre-prototype thermal evaluations

Pre-prototype:
Base attached to
tube & heaters on



- Investigate performance of high-thermal conductivity (eg Allcomp) foams as a heat exchanger
  - Combination of large area and increased stream velocity through foam can lead to high efficiency
- Characterise performance (i.e. temperature rise vs power) for different flow velocities
- Develop FEA models simulating the fluid flow through foams



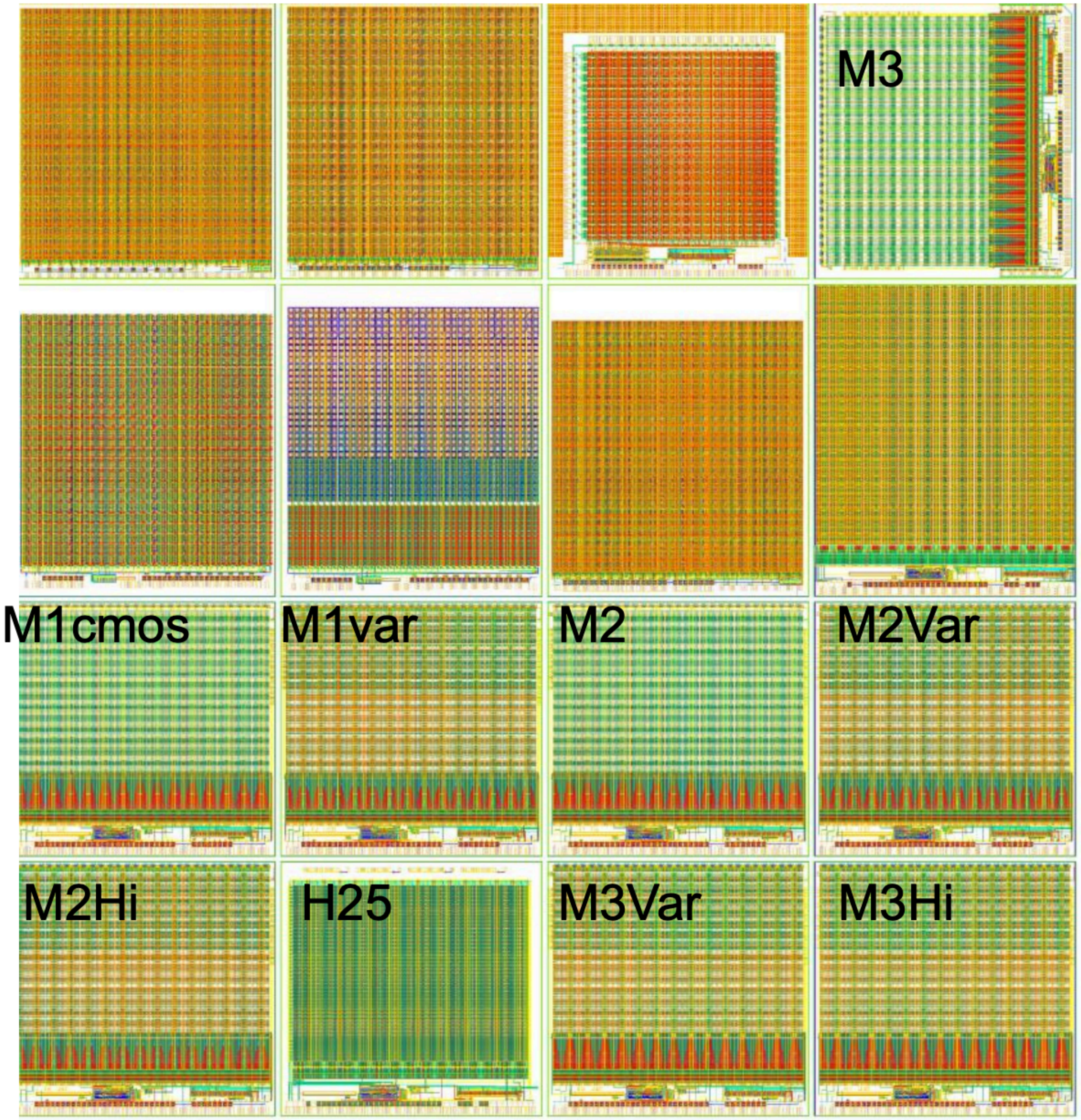
*First look: at 3.1W power (expected from 8cm*4cm area), temperature rise ~10 degrees w.r.t. CDA*

Liverpool

Improvements beyond ATLASPix3 (180nm)

Karlsruher Institut für Technologie

- Engineering run 2020 and 2021
  - TSI 180nm
  - Several designs for future electron colliders and DESY telescope upgrade (TELEPIX)
  - Pixel 25um × 165 um
- Improvements beyond ATLASPix3
  - Improved breakdown voltage by better design of guard ring (60V → 120V)
  - Reduction of power consumption by optimized amplifier and comparator designs



https://adl.ipe.kit.edu/english/26.php

Improvements for sensors beyond ATLASPix3

Ivan Peric

- Options:
  - Different pixel sizes
  - Different amplifier types (NMOS and PMOS)
  - Different comparator types (NMOS, CMOS and distributed)
  - Different TDAC types (placed in pixels or in periphery)
- Fixed improvements versus ATLASPIX3
  - Hit buffer cell with time to digital converter (supports time resolution ~ 100ps), TDAC, differential receiver for distributed comparator
  - Possibility of daisy-chain readout – one chip acts as data collector for another
  - Possibility to bias pixel n-well with voltage higher than 1.8V, and to bias pixel p-well with voltage lower than 0. It reduces capacitance. Reduced capacitance means better time resolution for the same power consumption.
- PMOS amplifier has lower noise than the NMOS amplifier when the bias current is high (~10μA). It has better (smaller) time walk for threshold of nine sigma noise. PMOS amplifier is more suitable for larger pixels i.e. pixels with larger capacitance (larger than 150fF)
- NMOS amplifier has better time walk for nine sigma noise for small bias currents (~1μA). It is a good choice for small pixels with little capacitance. Some risk because NMOS has more flicker noise and because we have little experience with this amplifier type
- NMOS comparator is the standard comparator type we used so far. It has some disadvantages: rather high current consumption (~3μA), larger delay than CMOS comparator, need for additional bias voltage of 2.1V, output signal of reduced amplitude, it occupies large area and causes large detector capacitance
- CMOS comparator does not have the disadvantages of NMOS comparator, it is faster for the same current consumption, potentially more radiation tolerant, smaller. Disadvantage is that CMOS comparator needs additional deep p-well implant (iso-PMOS option). This implant will be produced by TSI for the first time – there is some risk that it does not work.
- Distributed comparator has only three transistors in the pixel and adds very little capacitive load. The receiver and TDAC are placed in the hit buffer at the periphery. It is fast, low power and does not require additional iso-PMOS. The disadvantage is that it requires two lines per pixel to connect it with the hit buffer. This is not a problem for pixels larger than 50μm x 150μm.
- TDAC can be placed in pixel but it adds detector capacitance. TDAC can also be placed at the periphery, in this case it makes periphery slightly larger

Serial Powering and Al-Flex prototype in ITk

- Prototyping has been performed within ITk upgrade

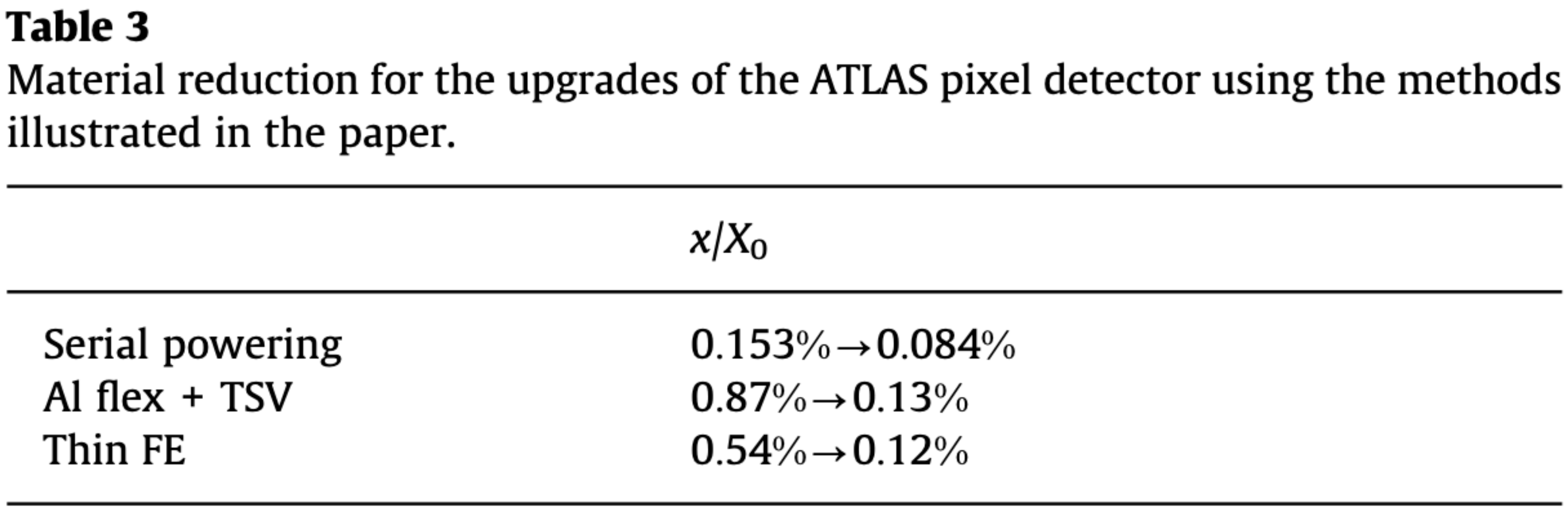


Table 3
Material reduction for the upgrades of the ATLAS pixel detector using the methods illustrated in the paper.

	x/X_0
Serial powering	0.153%→0.084%
Al flex + TSV	0.87%→0.13%
Thin FE	0.54%→0.12%

L. Gonella , F. Hugging, N.Wermes, DOI: 10.1016/j.nima.2010.11.162