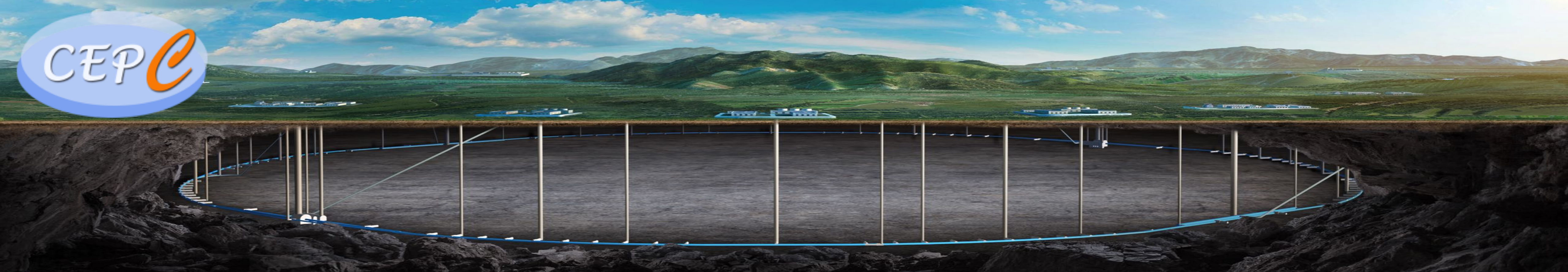


CEPC Inner Tracker towards Ref-TDR

LI Yiming 李一鸣

on behalf of the CEPC Silicon Inner Tracker team

中国科学院高能物理研究所

Institute of High Energy Physics

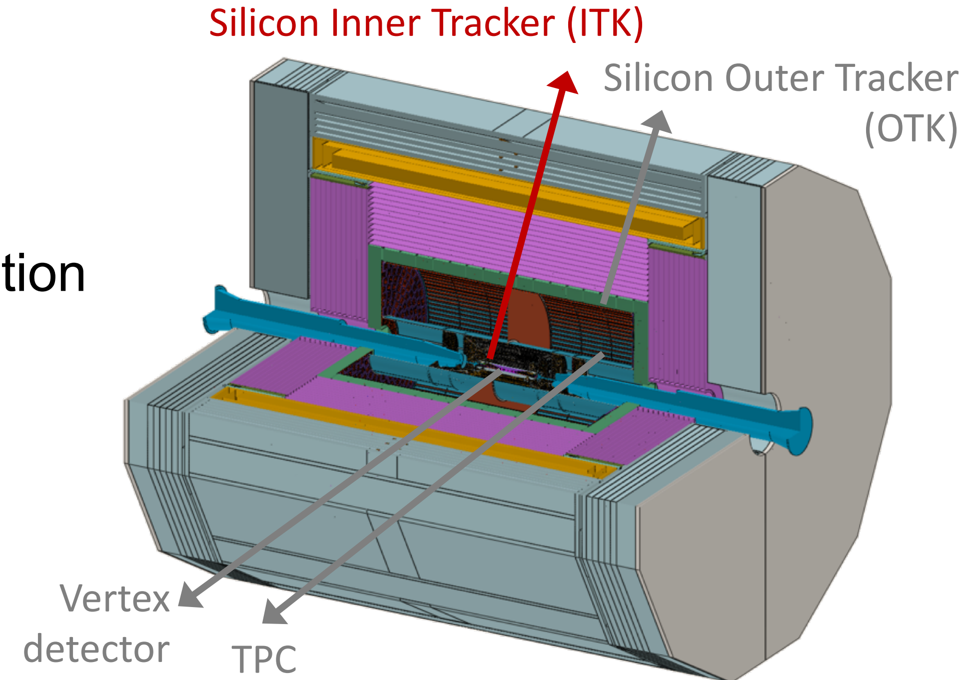
Chinese Academy of Sciences

Content

- Introduction & requirements
- Technology survey and R&D efforts
- Readout electronics
- Mechanical design
- Performance from simulation
- Workplan and summary

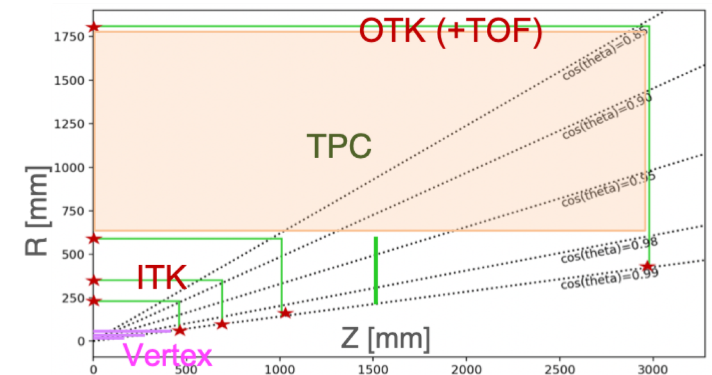
Requirement

- Large area silicon tracker: technical challenges
  - ~15 m^2 => cost-effectiveness crucial
  - < 10 um spatial resolution required by momentum resolution
  - A few ns timing resolution to tag 23ns bunches at Z-pole
  - Low material budget (<1% X_0 per layer)
  - Moderate power consumption (liquid cooling possible)



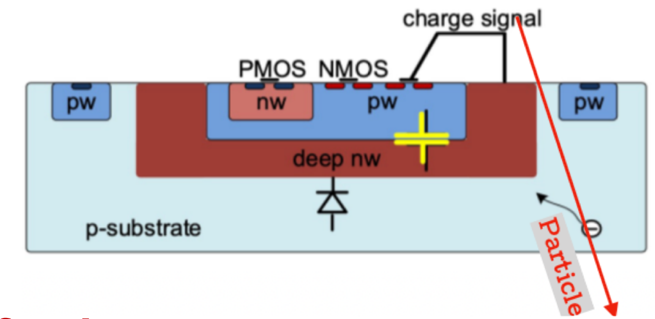
$$\sigma_{1/p_T} = a \oplus \frac{b}{p \sin^{3/2}\theta} \quad [\mathrm{GeV}^{-1}]$$

$$a \sim 2 \times 10^{-5}\,\mathrm{GeV}^{-1} \qquad b \sim 1 \times 10^{-3}$$



Technology Survey – Silicon Pixel

- HVCMOS ：a promising technology



  – Full depletion possible due to large electrode
  – Intrinsically **radiation hard**
  – **Fast charge collection → good time resolution**
  – Based on commercially available process without modification → **cost-effective**

- Towards smaller feature size

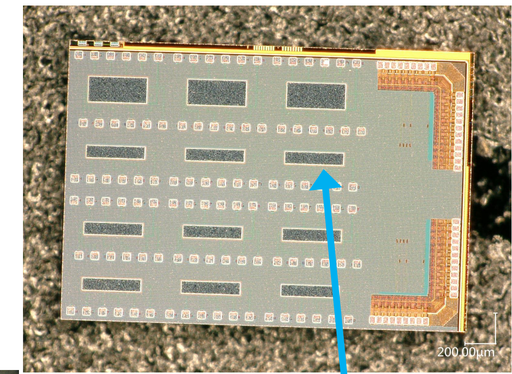
  – Current HVCMOS chips mostly in 180nm (MuPix, ATLASPix) / 150nm process (MonoPix, RD50-MPW)
  – For better performance:
    • Higher circuit density / More functionality in the same area / Less power consumption
  – For higher reliability:
    • Current process may be unavailable when mass production begins
  – CMOS with small electrode is pushing for 65nm process (mainly driven by ALICE upgrade)

Development in Small Feature-Size HVCMOS

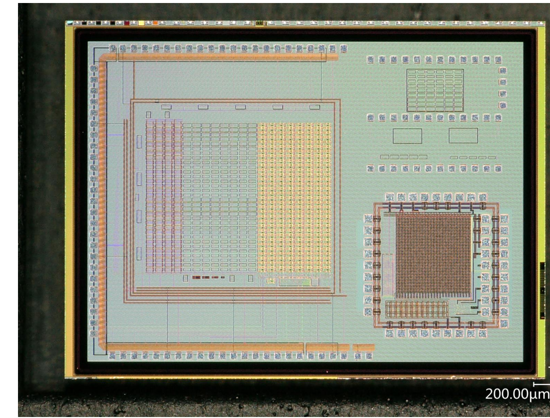
- First attempts to realize HVCMOS in 65nm or less
- SMIC 55nm Low-Leakage process
  - Not HV, yet with a similar deep n-well structure
  - MPW submitted in Oct 2022 in normal wafer
  - COFFEE1 received in Apr 2023
- SMIC 55nm HVCMOS process
  - First HVCMOS sensor in 55nm process
  - MPW submitted in Aug 2023
  - COFFEE2 received in Dec 2023

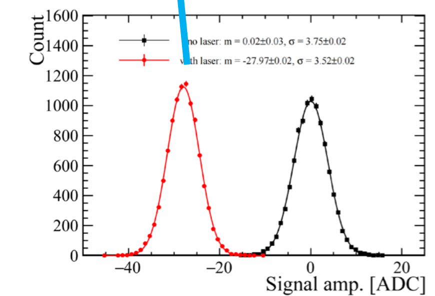
Yanyan Gao's talk (Thursday) for more R&D status
Yang Zhou's talk (Friday) for COFFEE2 design details

COFFEE1



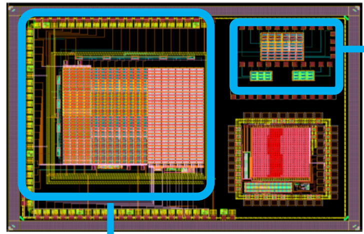
COFFEE2





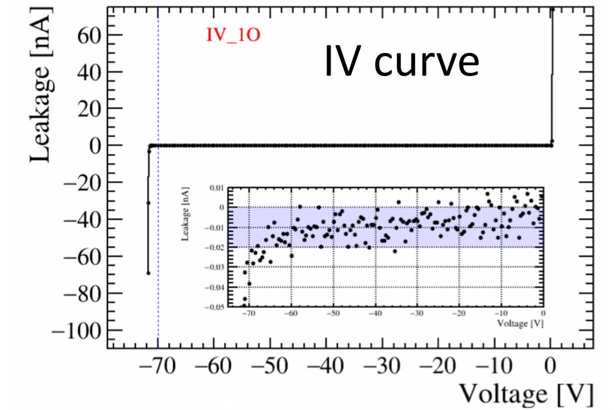
Response to laser observed

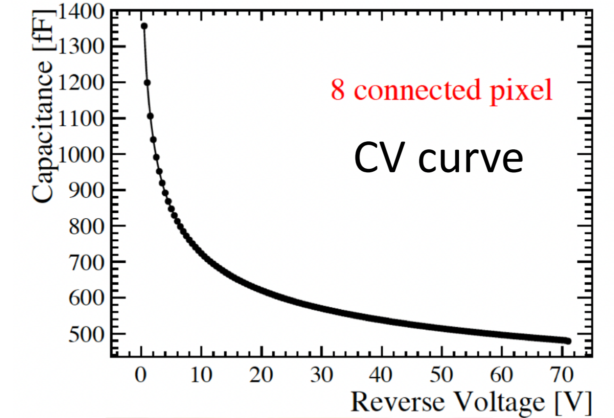
HVCMOS (COFFEE2) Chip Test



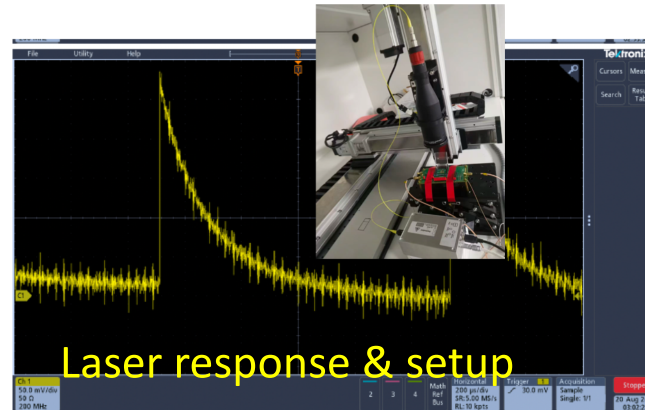
- So far tests have been focused on passive diode arrays
  - IV (breakdown at –70 V)
  - CV (single pixel ~30-40 fF)
  - Leakage current increased from 0.01 nA to ~1 nA after $10^{14} n_{eq}/cm^2$ radiation
  - Laser response observed
  - Radioactive source observed

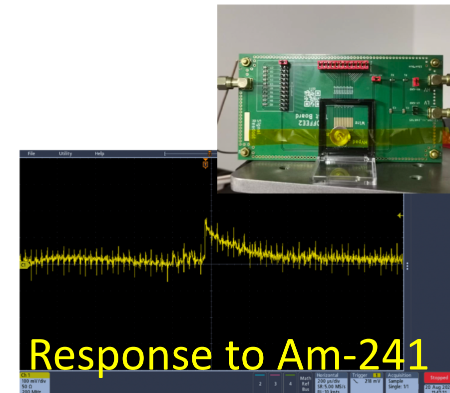
- Circuit test almost ready
  - Carrier board fabricated
  - Caribou system installed, final firmware debugging

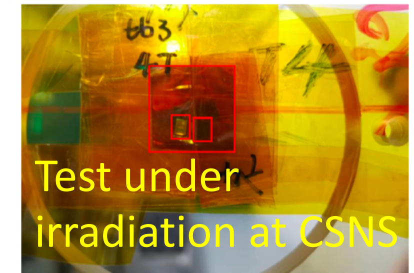




Caribou setup


Laser response & setup

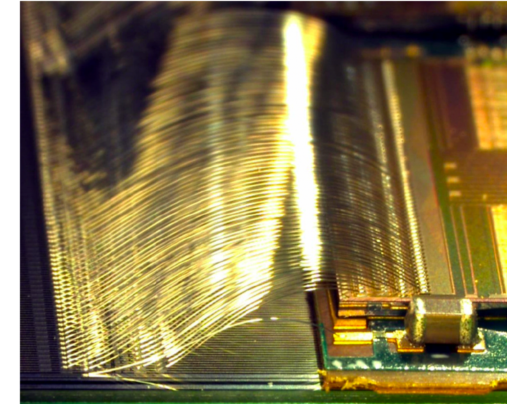

Response to Am-241


Test under irradiation at CSNS

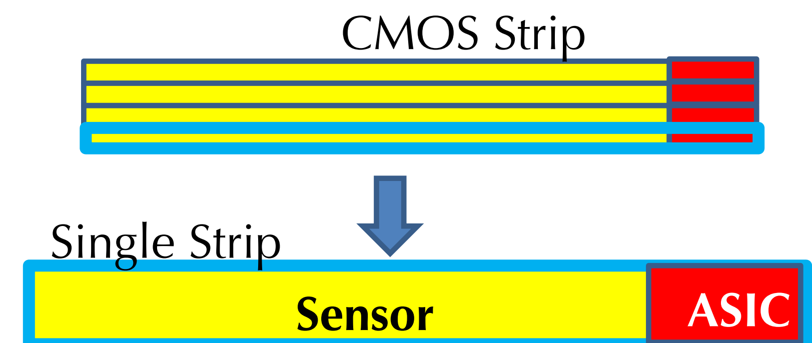
More details & analysis covered in posters of Zhiyu Xiang (#21), Jianpeng Deng (#55) and Leyi Li (#53)

Technology survey – Silicon Strip

- Silicon microstrip sensors considered in CDR
  - Pitch 50 um in the bending plane
  - Wire-bonding would be challenging for smaller pitch
- Silicon strips implemented using CMOS is a promising solution
  - Integration of sensor and FE ASIC => largely simplifying the assembly
  - Aiming for 20 um pitch in the bending plane
  - Cost-effective using commercial CMOS process
- First submission of CMOS Strip Chip (CSC1) being planned
  - 180 nm CMOS process (CSMC, Wuxi Shanghua)



Wire-bonds on ATLAS-ITk strip module (strip pitch 75.5 um)



Xin Shi's talk (Thursday) for more R&D status

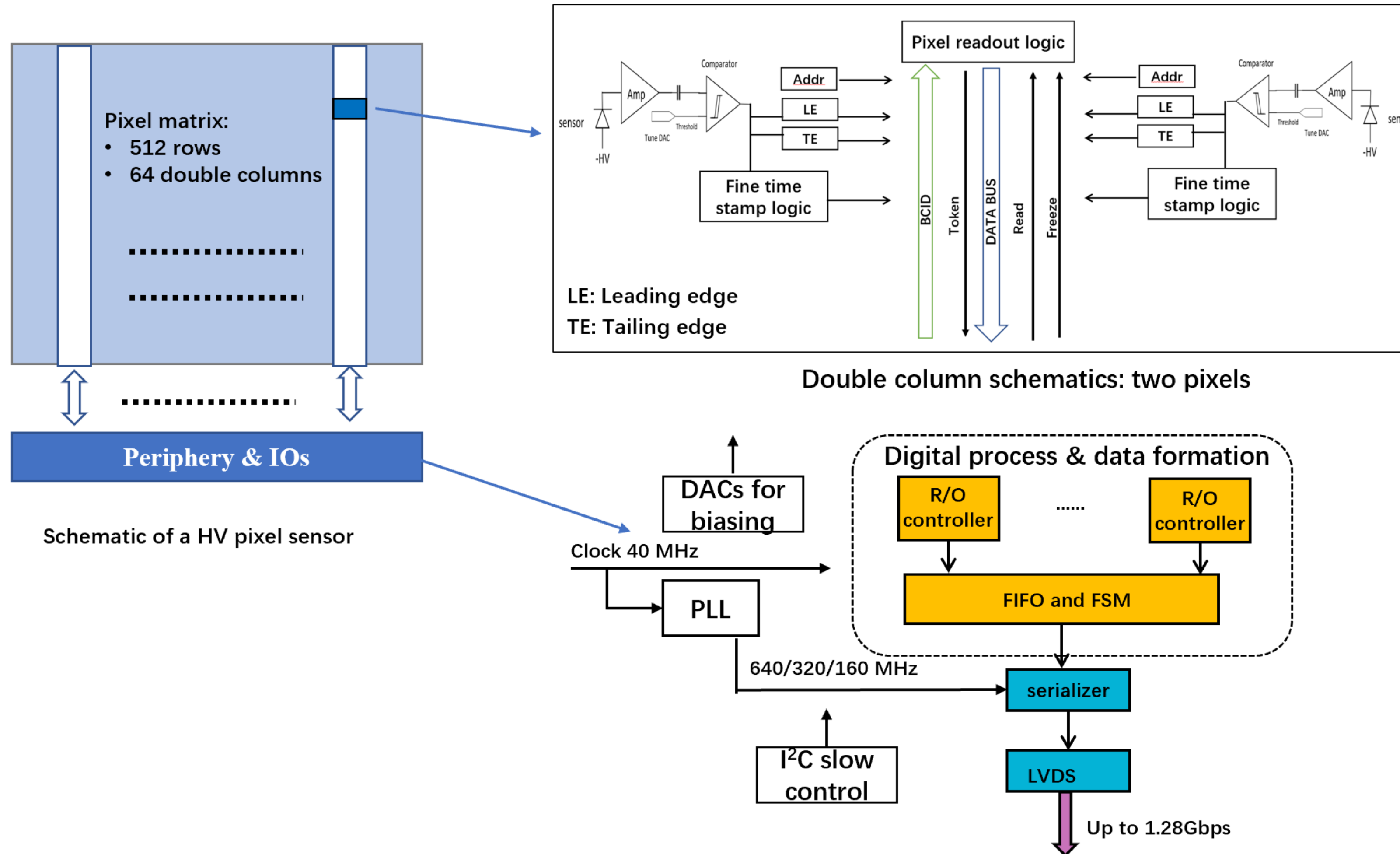
R&D goal of sensors

	Monolithic HVCMOS pixels	Monolithic CMOS strips
Pixel Size (Strip Pitch Size)	34 μm × 150 μm	20 μm
Sensor size	2 cm × 2 cm (active area: 1.92 cm x 1.74 cm)	2.1 cm × 2.3 cm (active area: 2.05 cm x2.05 cm)
Array size (Strip number)	512 rows × 128 columns	1,024
Spatial resolution	σ_{φ} ~8 μm (bending), σ_z~40 μm	σ~5 μm
Timing resolution	~3-5 ns	~3-5 ns
Data size per hit (1 readout)	42 bits (14b BXID, 7b+9b address, 6b TOT, 5b fine TDC, 1 polarity)	32 bits (10b BXID, 10b address, 6b TOT, other 6 bits)
Data rate per sensor	Maximum ~0.1 Gbps* (pair production)	Maximum ~0.2 Gbps* (pair production)
LV / HV	1.2 V / 150 V	1.8 V / 150 V

* Maximum hit rate: ITK barrel~4.1×10^5 Hz/cm^2, ITK endcap~7.5×10^5 Hz/cm^2, based on preliminary background estimation

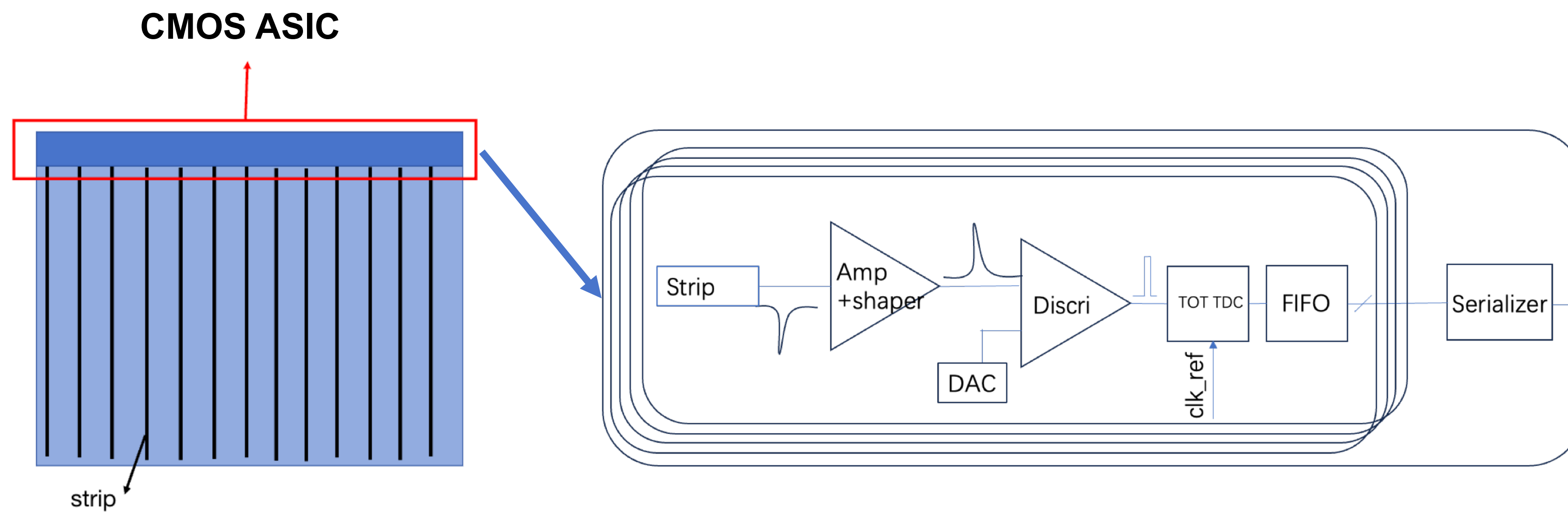
Beam background study see [Zhan Li's poster (#61)]

Frontend electronics – HVCMOS

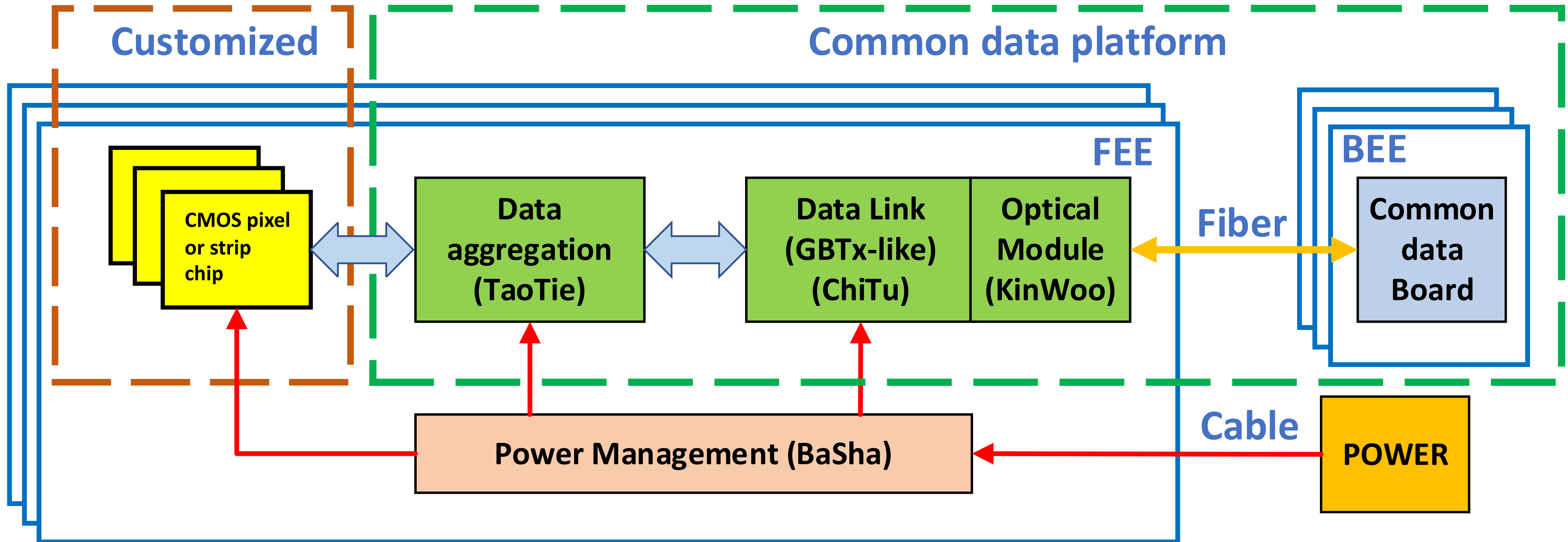


Front-End Readout: ASIC for CMOS strip

- Strips

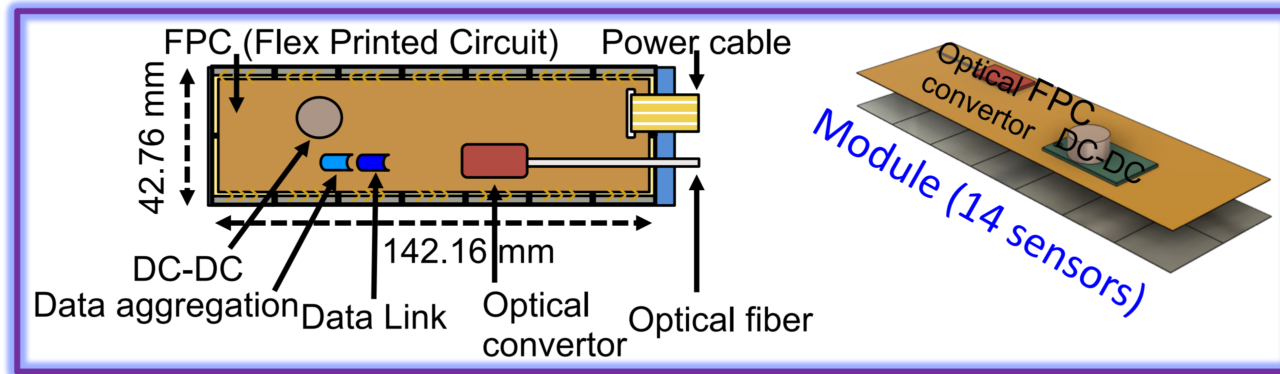


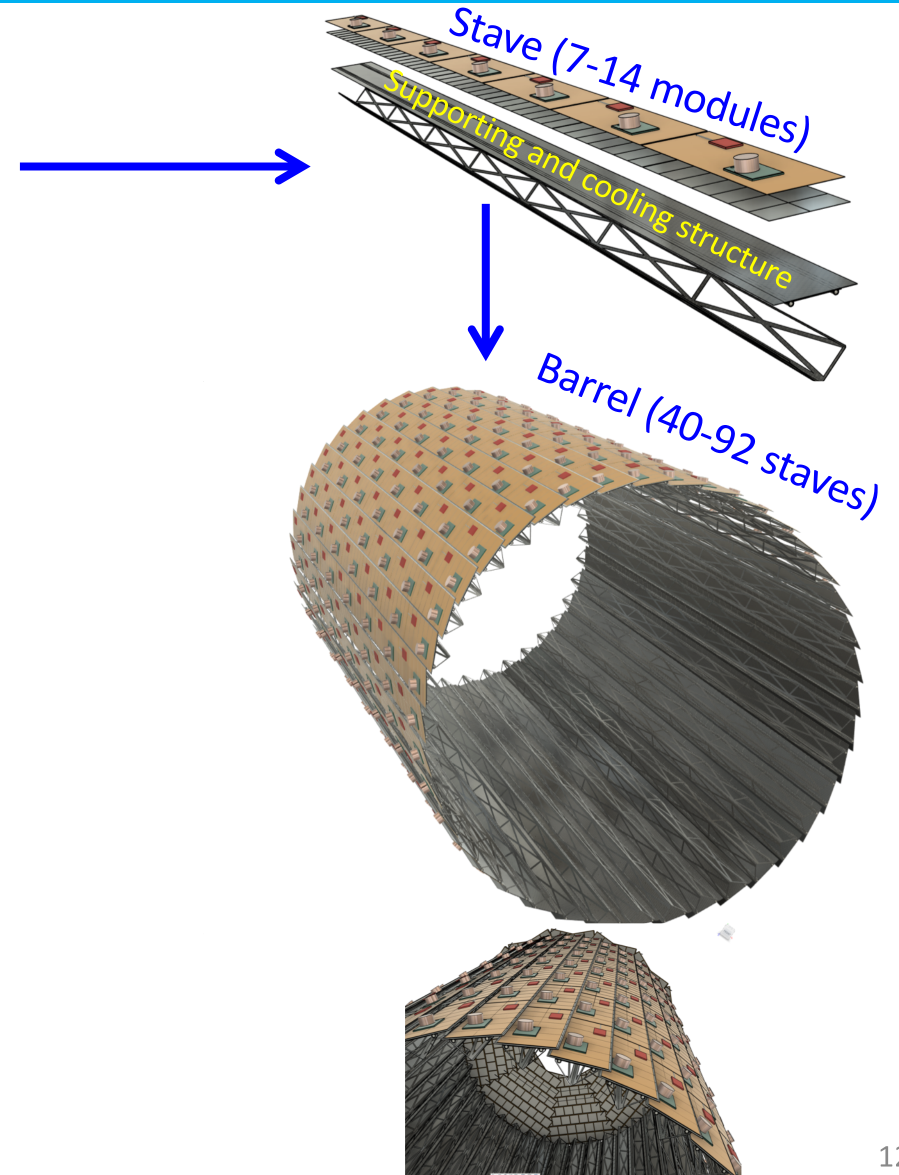
Common Electronics



- Data transmission: common data platform
- Trigger mode: triggerless

CEPC ITK Barrel Design (HVCMOS Pixels)

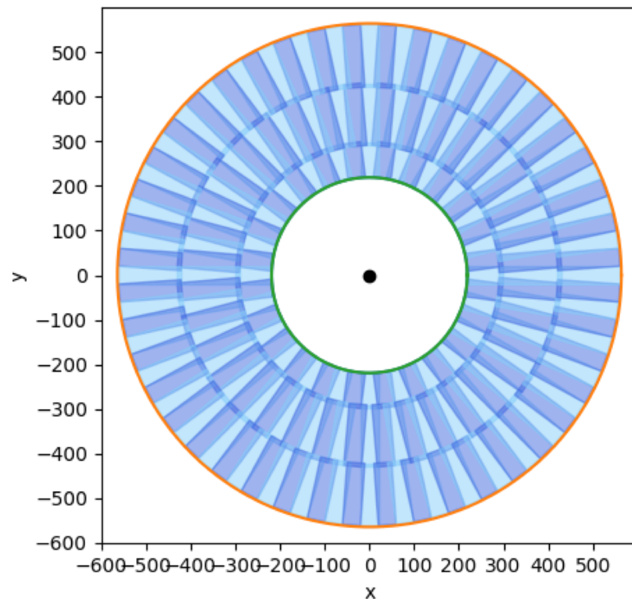


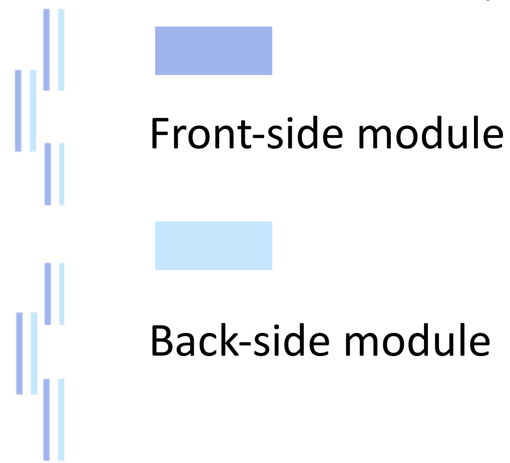


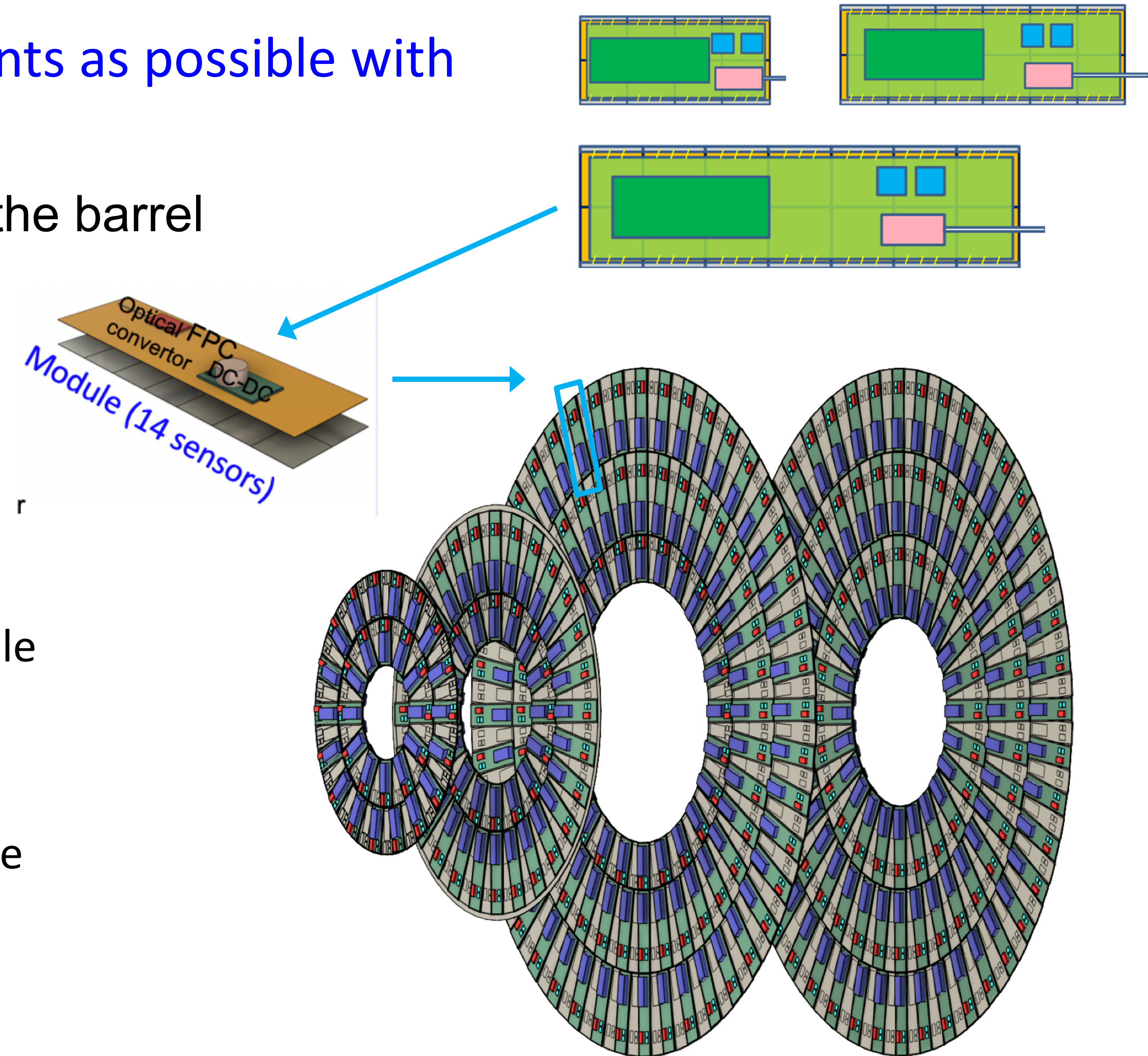
- HVCMOS pixels for CEPC:
  - Utilizes 55 nm process
  - Wafer resistivity: 1k-2k Ω·cm
  - Chip size: 2 cm × 2 cm
  - Array size: 512 rows × 128 columns
  - Pixel size: 34 μm × 150 μm
  - Time resolution: 3-5 ns
  - Power consumption: ~200 mW/cm^2

Preliminary endcap design using pixels

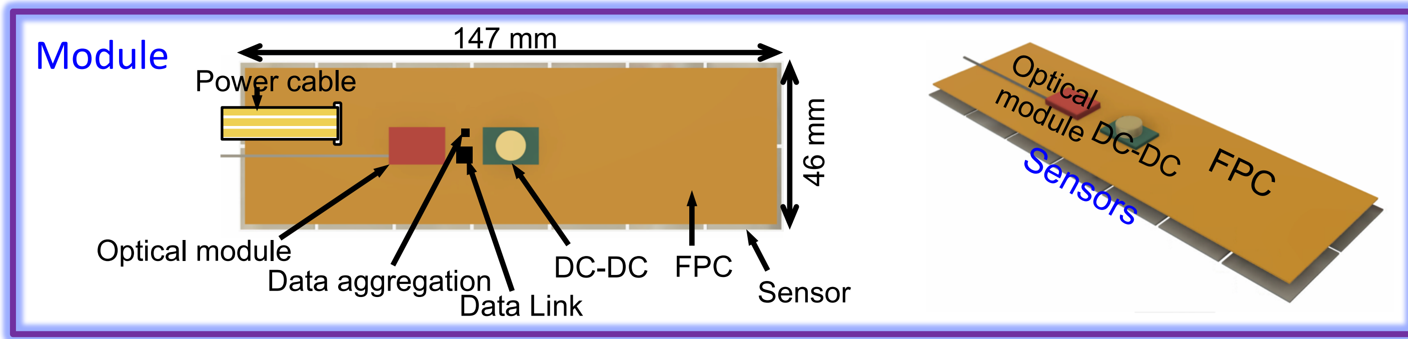
- Endcap using HVCMOS share as many components as possible with the barrel
  - 3 types of modules, one of which the same as the barrel
  - 516 modules, 6576 chips in total
  - Division into 8 or 4 sections possible

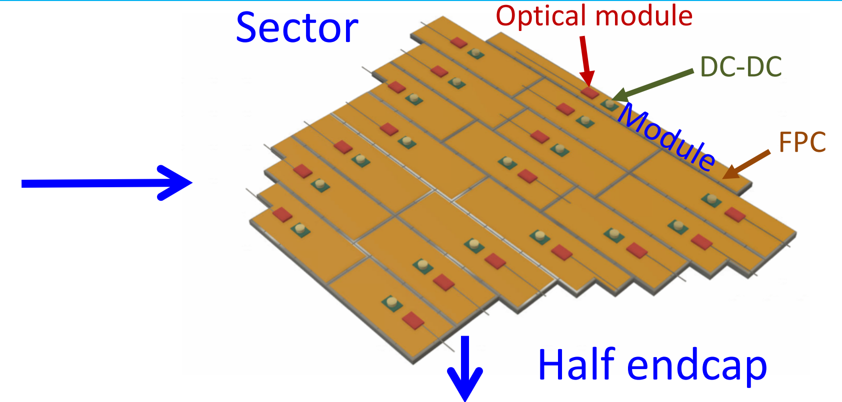






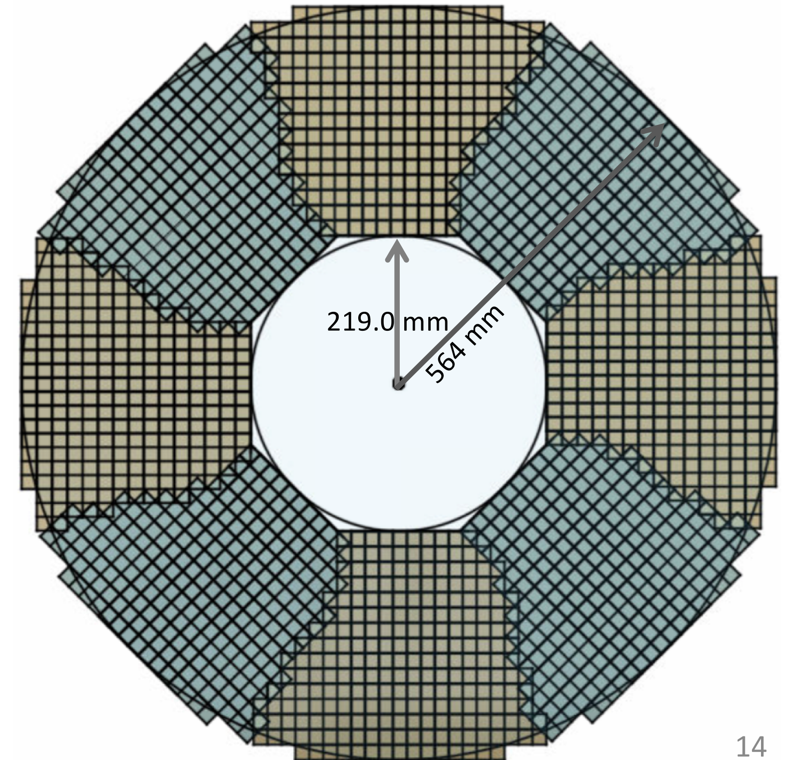
CEPC ITK Endcap Design (CMOS Strips)





- CMOS Strip Chip (CSC) for CEPC:
  - Utilizes 180 nm process (CSMC, Wuxi Shanghua)
  - Wafer resistivity: 2k Ω·cm
  - Chip size: 2.1 cm × 2.3 cm
  - Strip number per chip: 1,024
  - Strip pitch size: 20 μm (spatial resolution <5 μm)
  - Time resolution: 3-5 ns
  - Power consumption: ~80 mW/cm^2

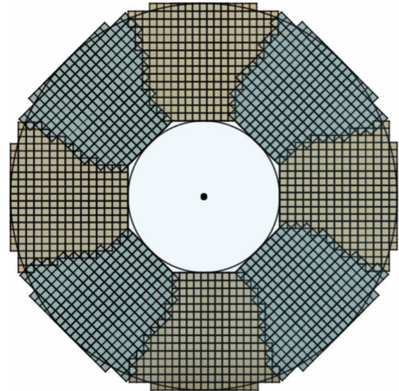
Each half endcap is divided into 8 sectors, with each sector consisting of CMOS strip modules. The overlapping areas between the neighboring sectors are designed to be minimal.



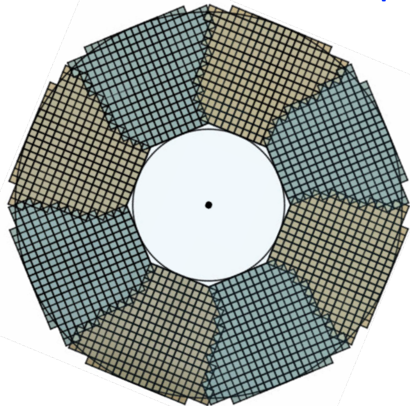
CEPC ITK Endcap Design (CMOS Strips)

Two half endcaps are rotated 22.5° relative to each other to form one complete endcap:

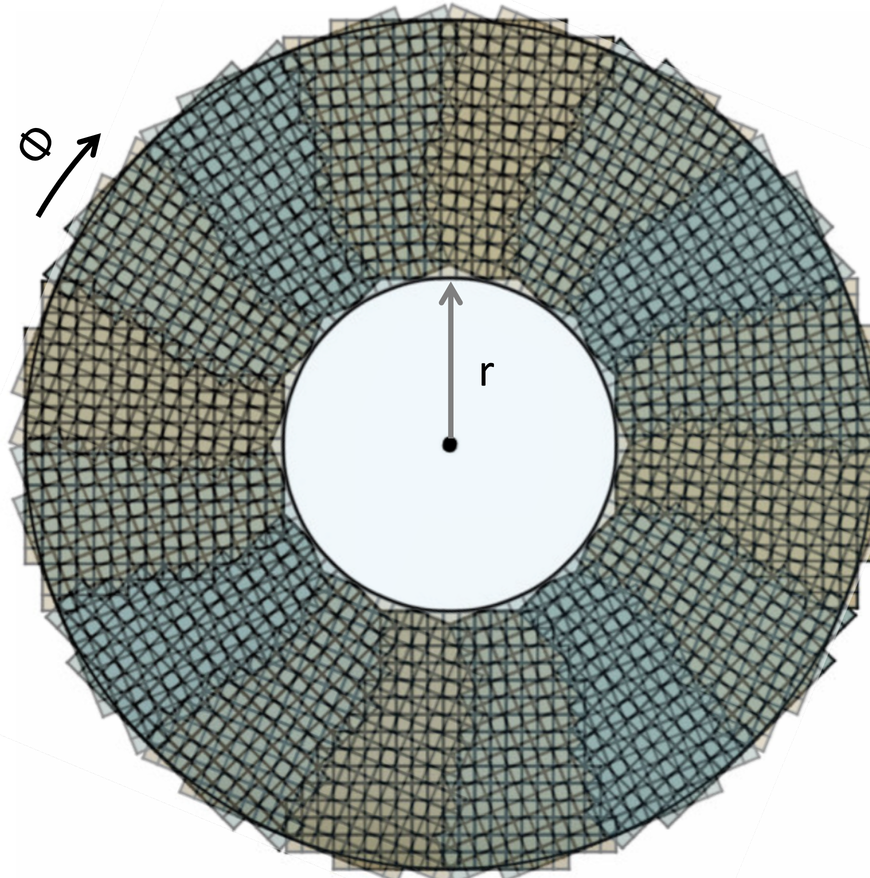
- Maximize track resolution in bending direction ϕ
- Minimize track ambiguity

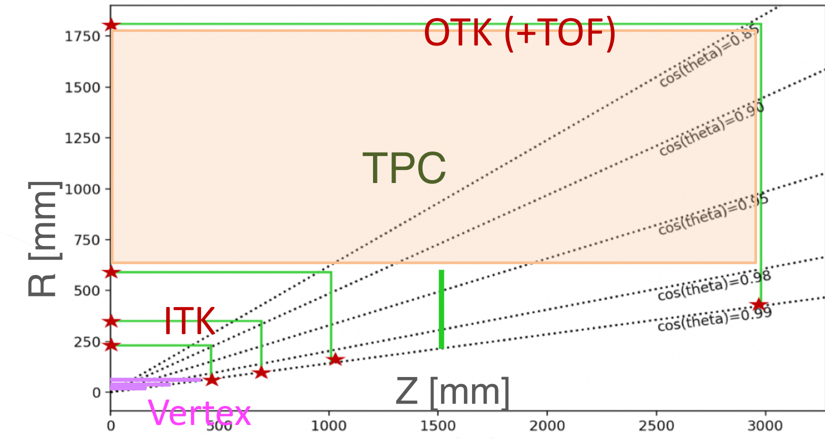


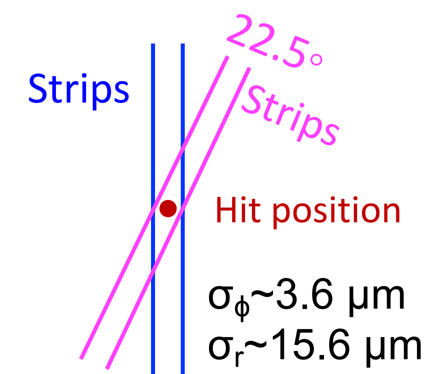
Normal half endcap



22.5° half endcap



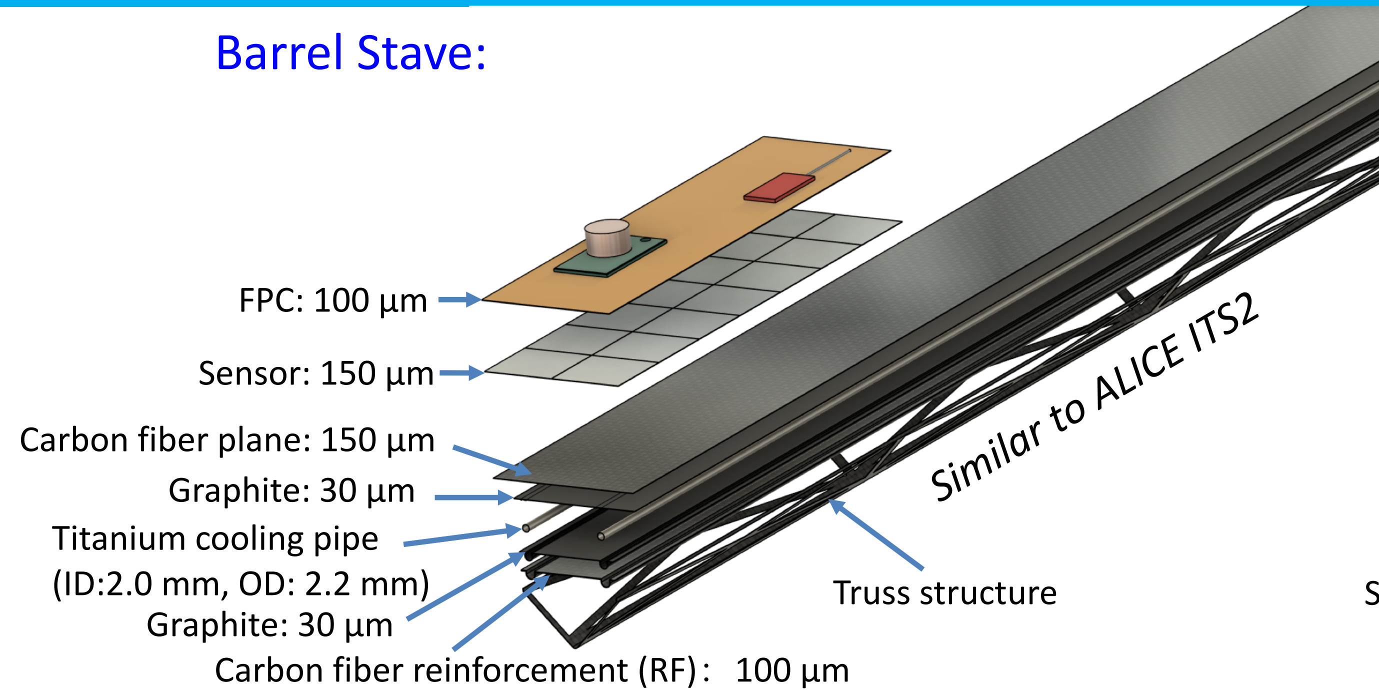




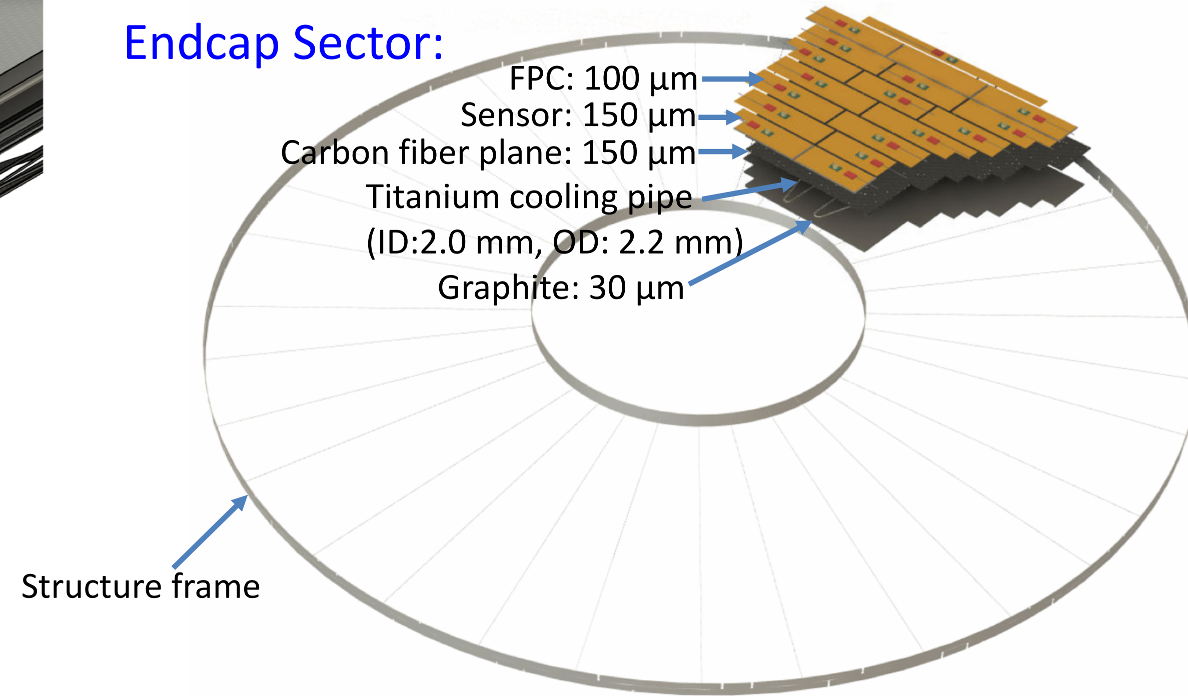
Detection precision using 20 μm pitch strips

The CEPC ITK barrels using pixels is considered for minimal material, while ITK endcaps using strips is optimized for high momentum measurement and particle identification (no TPC).

ITK Mechanical and Cooling Structure

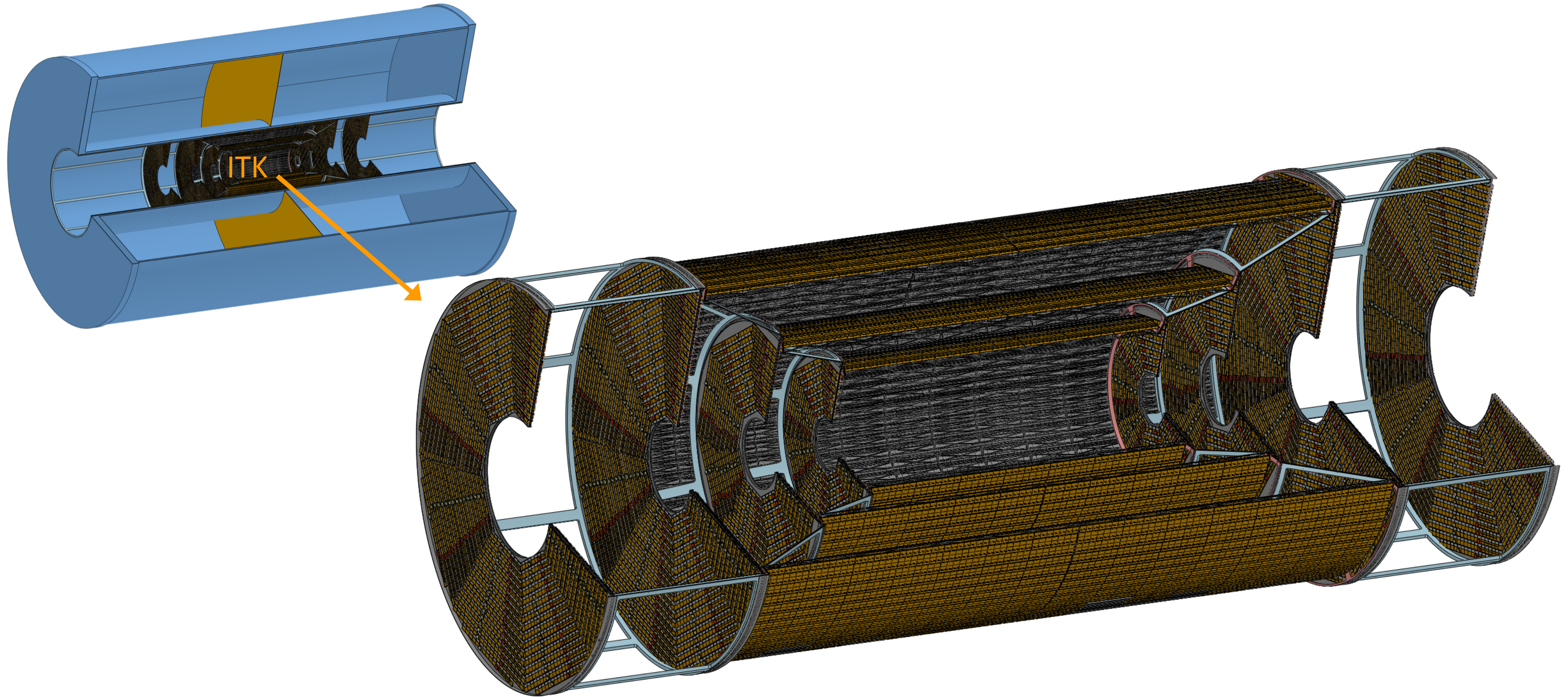


Materials	Thickness (mm)	Radiation Length [% X_0]
FPC	0.10	0.14
Sensor	0.15	0.18
Carbon fiber×2	0.25	0.10
Graphite×2	0.06	0.03
Others		0.05
Total		0.50



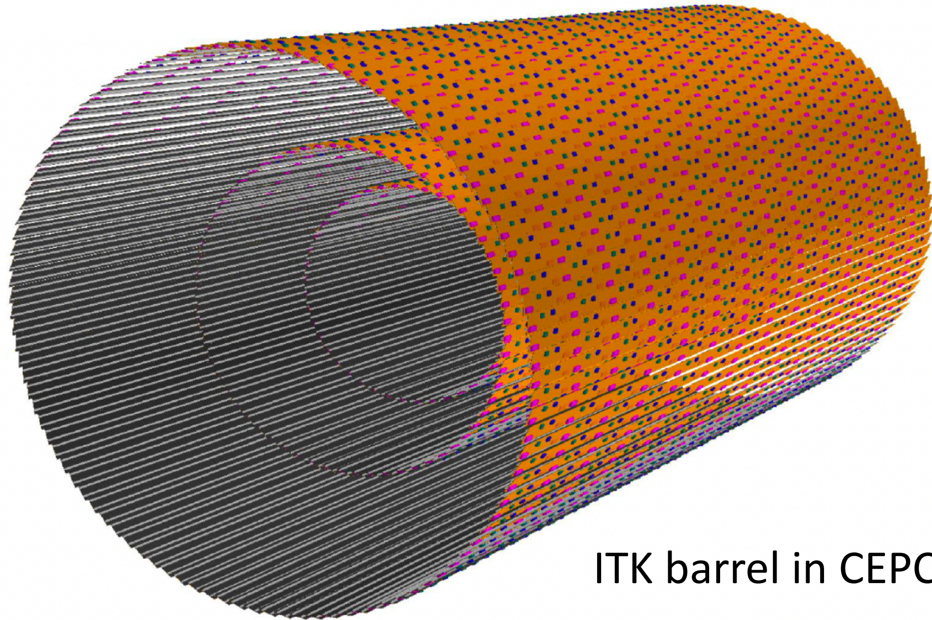
Materials	Thickness (mm)	Radiation Length [% X_0]
FPC	0.10	0.14
Sensor	0.15	0.18
Carbon fiber	0.15	0.06
Graphite	0.03	0.02
Others		0.03
Total		0.43

Mechanical Structure for ITK system

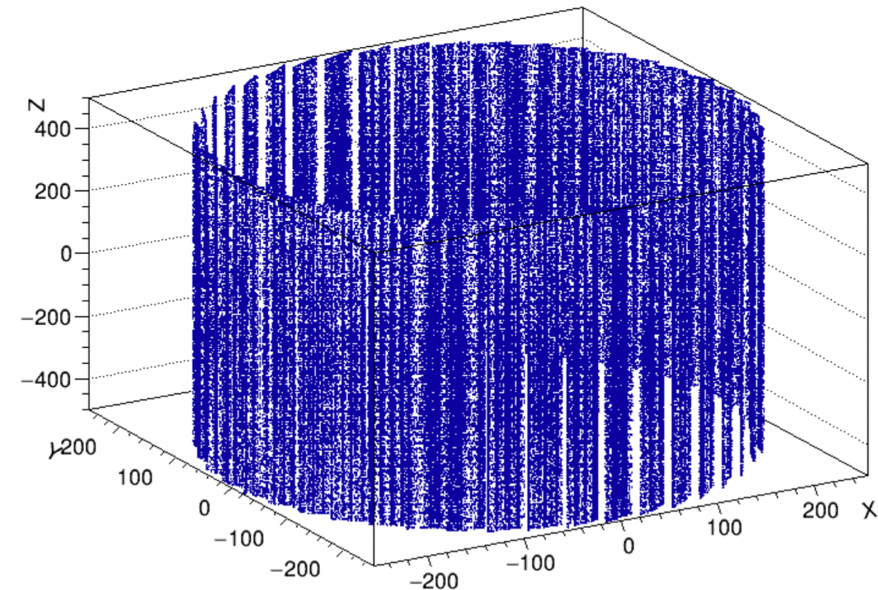


ITK Implementation in CEPCSW

- The ITK design has been implemented in the CEPCSW framework, and can be used for full simulation validation



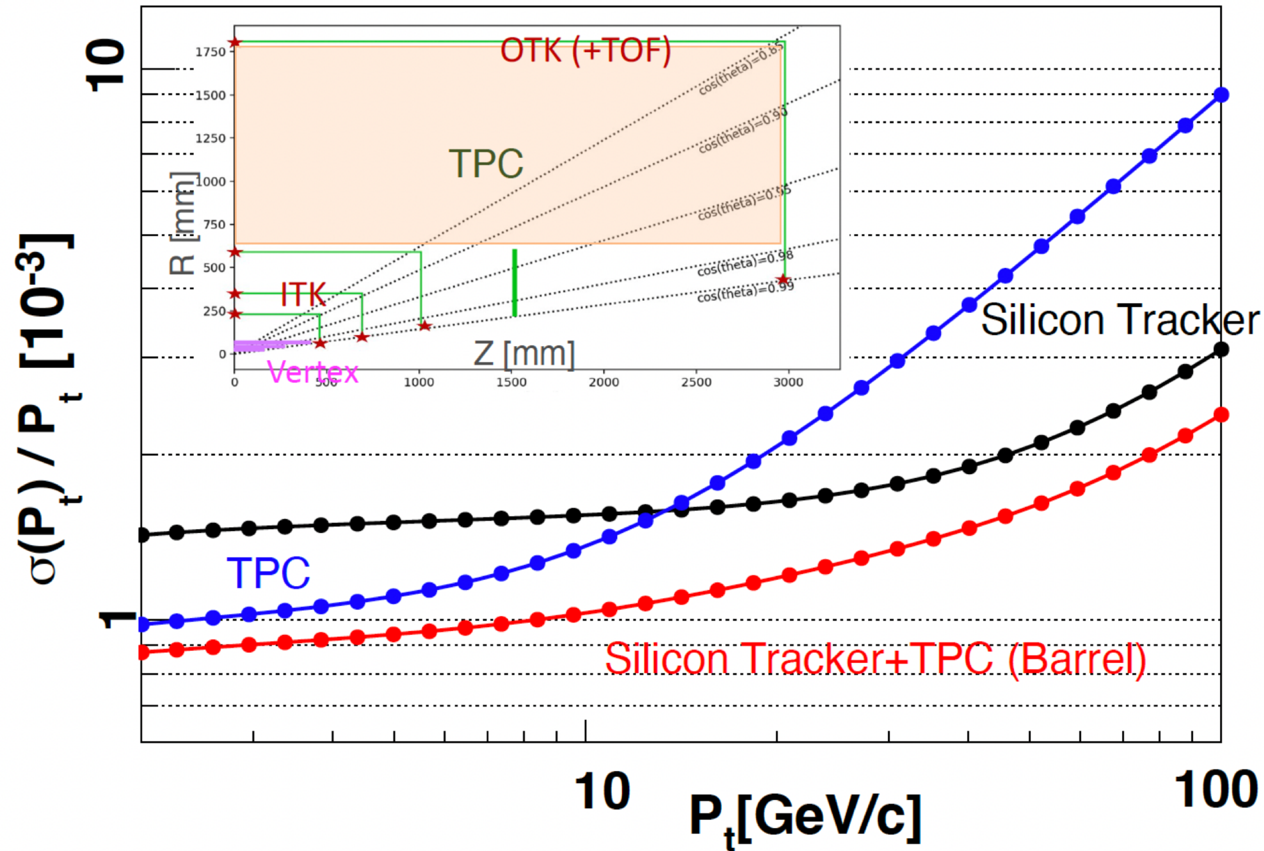
ITK barrel in CEPCSW

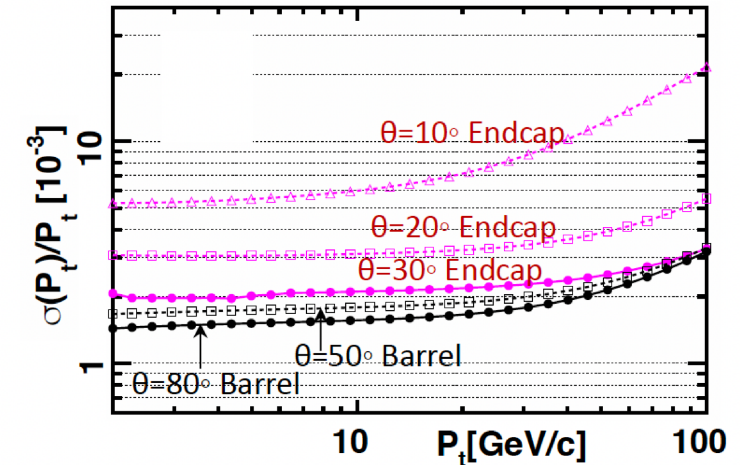


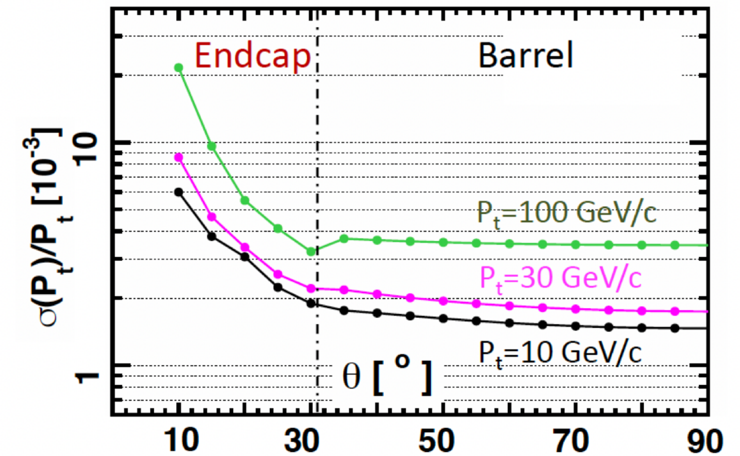
Hitmap in 1 barrel layer generated using 50GeV muon events shows no dead area between neighbouring staves

Xiaojie Jiang's poster (#344) for more details

Tracker Performance: Momentum Resolution







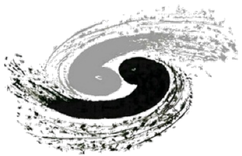
Silicon Tracker momentum resolution angular dependence

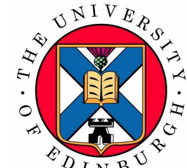
Qinglin Geng' poster (#88) for more details

Working Plan

	2024	2025		2026		2027
HVCMOS Pixel Chip	Q4 COFFEE2 full characterization	Q2 MPW submission for key module verification	Q4 Test & spec finalization	Q3 Quarter chip submission to validate full-column readout	Q2 Module prototype	Q4 Full-size full-function chip

- **CMOS Strip Chip**
  - CSC1: Passive CMOS strip sensor and separate front-end electronics CMOS circuit
  - CSC2: Small size and large pitch prototype
  - CSC3: Full size and full function 20 μm pitch chip

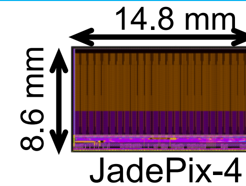


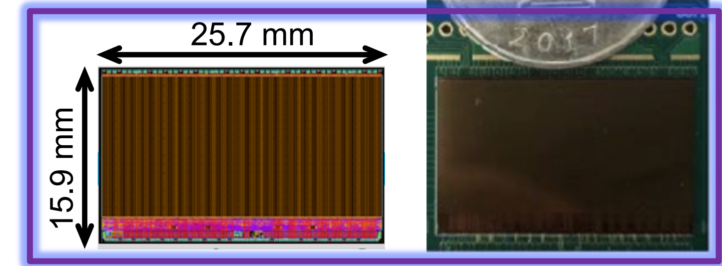


Experience in Silicon Detector Development

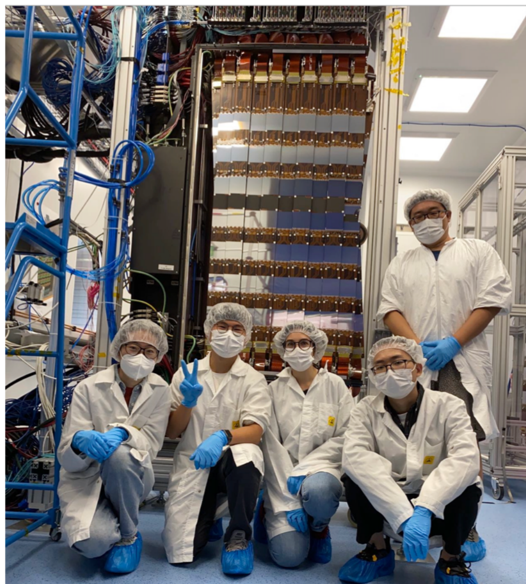
- The team has successfully developed several fully functional MAPS:
  - JadePix, TaichuPix, CPV, etc
- Major contributions to silicon detector construction, testing, integration, and operation:
  - LHCb Upstream Tracker, AMS L0 upgrade, ATLAS ITK, etc

CIS process:

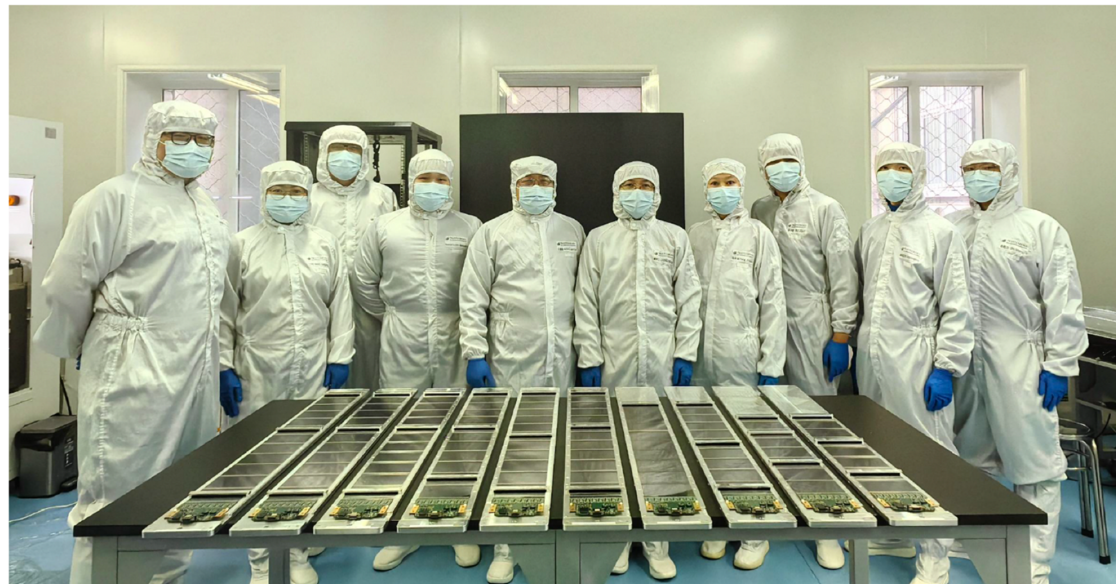




TaichuPix-3



LHCb UT A-side assembly



AMS L0 ladder production

ATLAS ITK strip module

Summary

- The design of silicon inner tracker in preparation of the CEPC reference detector TDR is proposed, based on R&D of advanced detector technologies
- A lot more development in sensor technology, electronics, mechanics and physics benchmarking expected, for the Ref-TDR and beyond
- Collaboration & your participation welcome

Thank you for your time!