ARCADIA

FDMAPS development with LFoundry 110nm CIS

Manuel Rolo (INFN),

on behalf of the **ARCADIA Collaboration.**

Istituto Nazionale di Fisica Nucleare

ARCADIA

CEPC

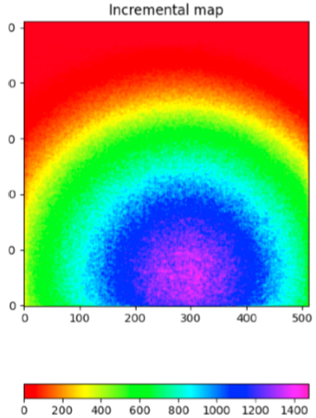
2024 International Workshop on the High Energy Circular Electron Positron Collider (CEPC)

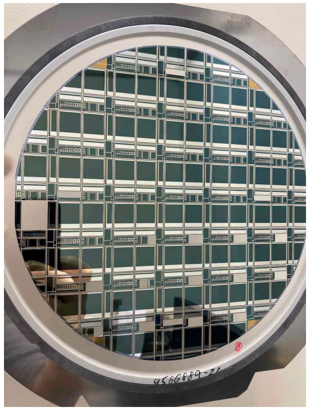
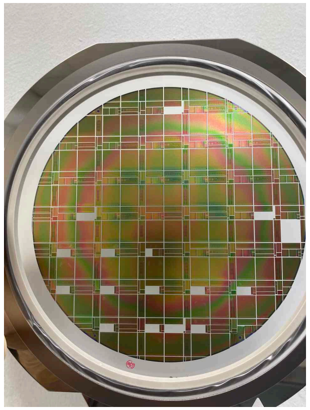
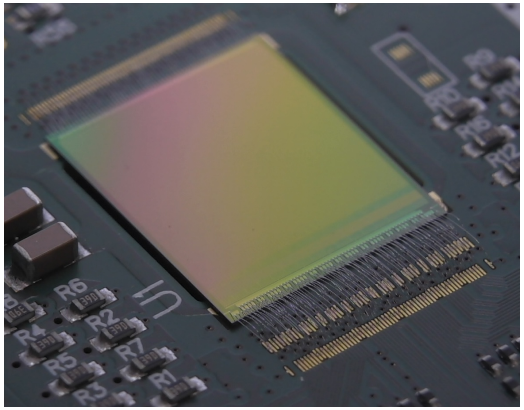
Oct 23-27, 2024, Hangzhou

ARCADIA DMAPS R&D at INFN

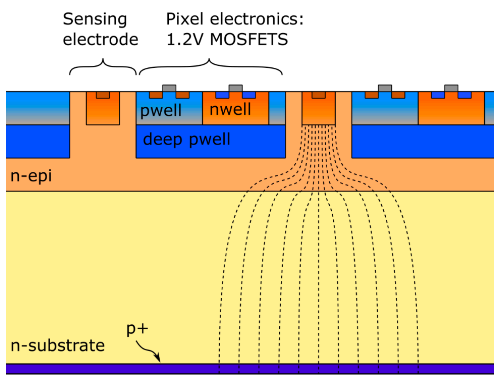
Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

* **ARCADIA:** CMOS sensor design and fabrication platform on LF11is technology
  - Sensor R&D and Technology, CMOS IP Design and Chip Integration, Data Acquisition
  - MD3: demonstrator full-chip FDMAPS for Medical (pCT), Future Leptonic Colliders and Space Instruments
  - Scalable FDMAPS architecture with very low-power: **10 mW/cm^2**
  - Fully-depleted monolithic active micro strips with fully-functional embedded readout electronics
  - Ongoing R&D for the implementation of monolithic CMOS sensors with gain layer for fast timing
  - Custom BSI process allow to develop fully-depleted thick sensors (400μm) for X-ray imaging

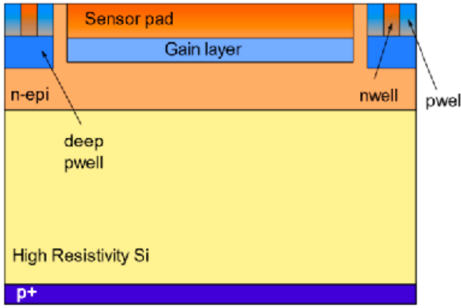


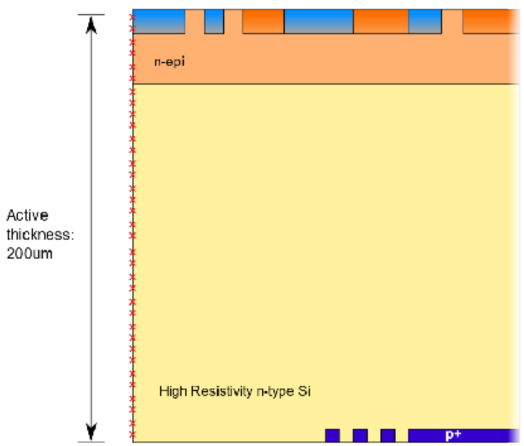
Sensor Concepts and post-processing



- n-type high resistivity active region + n-epi layer (reduces punch-through current between p+ and deep pwells)
- sensing electrodes can be biased at low voltage (< 1V)
- BSI Reverse-biased junction: depletion grows from back to top
- Ongoing R&D: Fully Depleted PAD sensors with gain layer



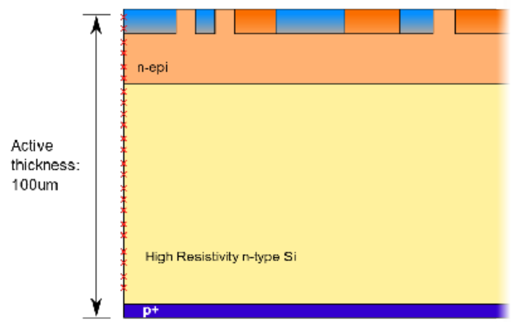
HR wafers - backside litho



Masked backside implantation

- thinning, lithography, backside p+ implantation and laser annealing, insulator and metal deposition to create backside guardring structures

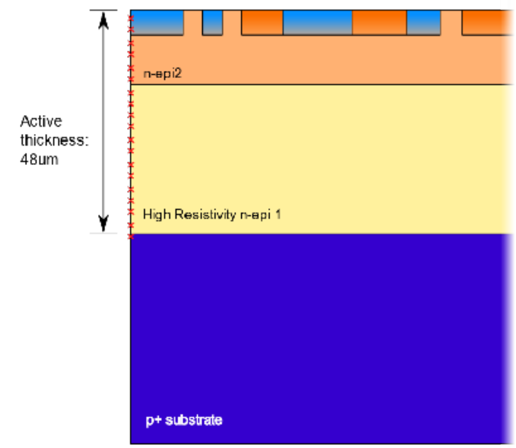
HR wafers - no backside lithio



Maskless backside implantation

- thinning, backside p+ implantation and laser annealing, no patterning on backside

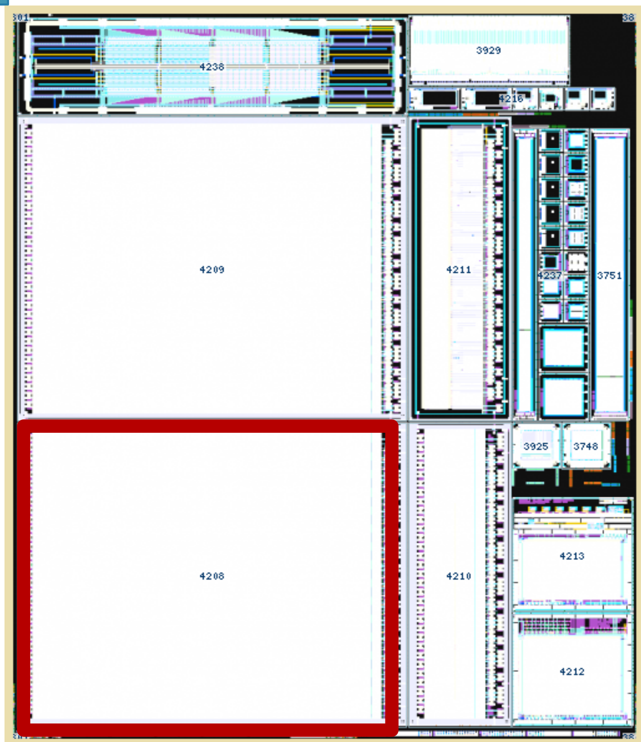
p+ wafers - double epi

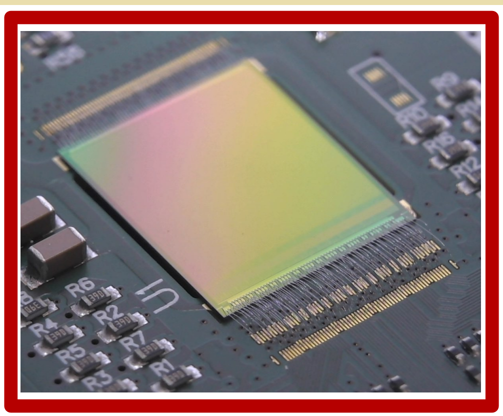


Total thickness: 300um

- thinning down to 100μm total thickness on a p+ starting substrate, active thickness below 50μm

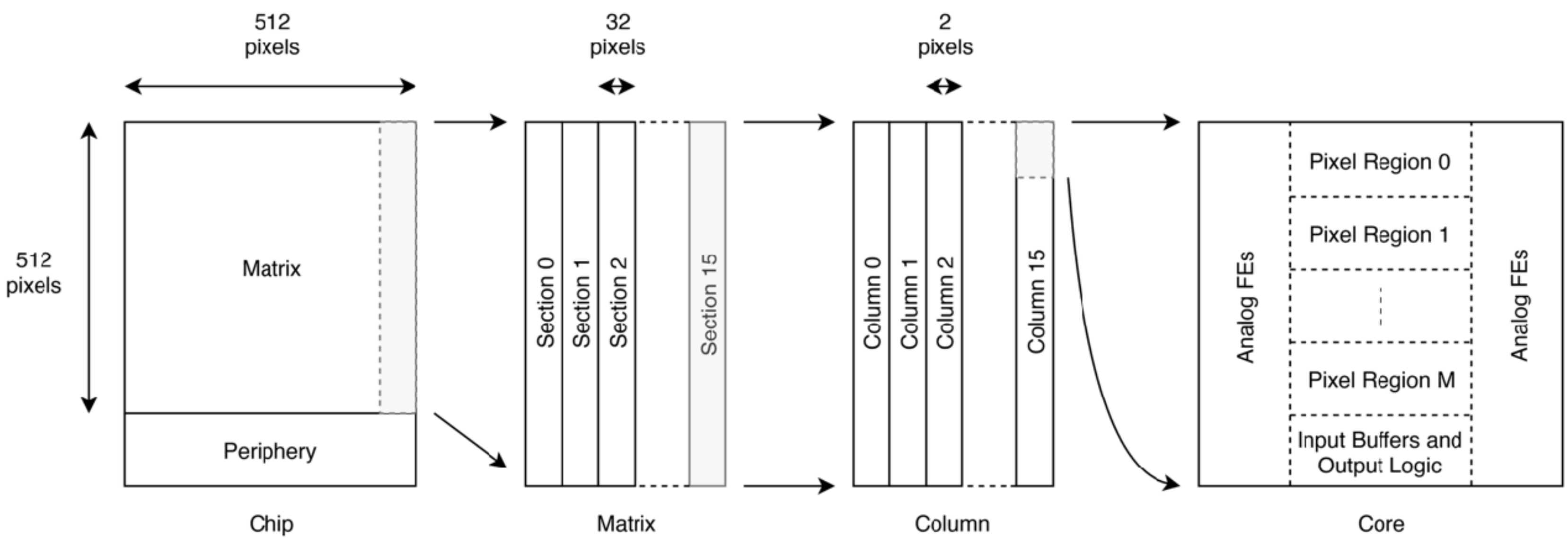
ARCADIA Technology demonstrators





- ARCADIA-MD3 Main Demonstrator (512 x 512 pixels)
- MAPS and test structures for PSI (CH)
- MATISSE Low Power (ULP front-end for space instruments)
- pixel and strip test structures down to 10μm pitch
- ASTRA 64-channel mixed signal ASIC for Si-Strip readout
- 32-channel monolithic strip and fully-functional readout electronics
- (ER2) HERMES: small-scale demonstrator for fast timing
- (ER3) Small-scale demonstrator of a X-ray multi-photon counter
- (ER3) Wafer splits with timing layer, new R&D towards <<50 ps timing performance: test structures and
- (ER3) MADPIX: multi-pixel active demonstrator chip for fast timing

ARCADIA-MD3: Chip Architecture

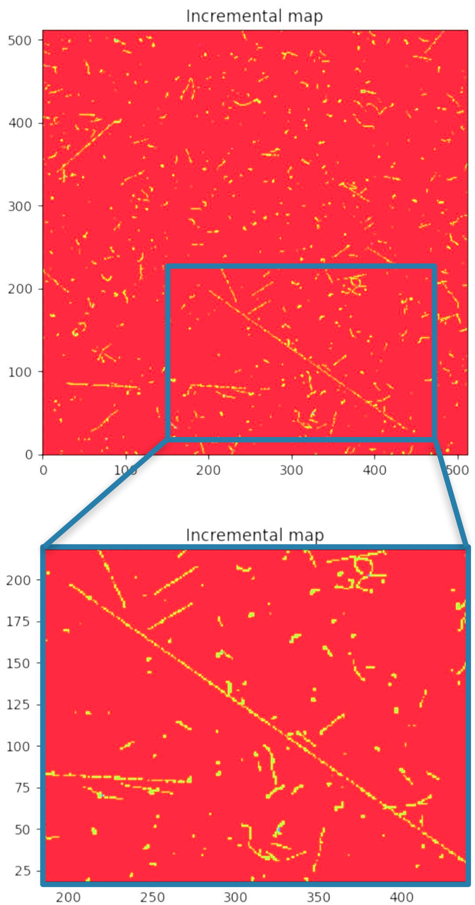


A. Paternò, S. Garbolino

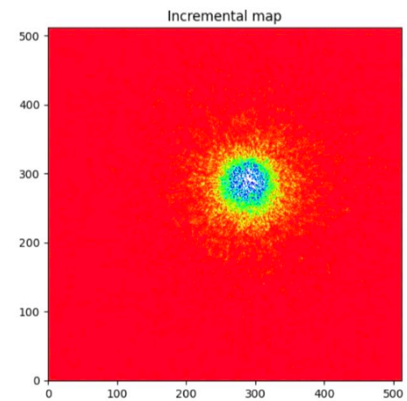
- Pixel size 25 μm x 25 μm, Matrix core 512 x 512, 1.28 x 1.28 cm^2 silicon active area, "side-abuttable"
- Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
- Event rate up to 100 MHz/cm^2 (design post-layout simulations)
  - High-rate operation (16 Tx): 17-30 mW/cm^2 depending on transceiver driving strength (measured)
  - Low-power operation (1 Tx): **10 mW/cm^2** (all data conveyed in 1 transceiver, others turned-off)

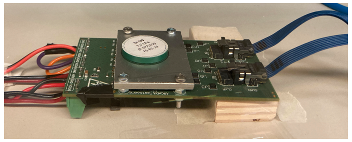
ARCADIA-MD3: charged particles

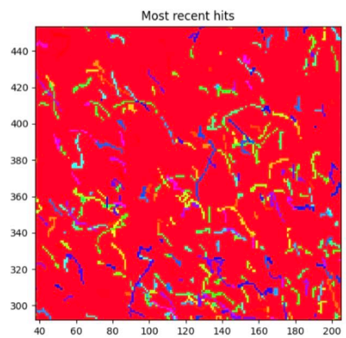
Cosmic rays
(tilted sensor)



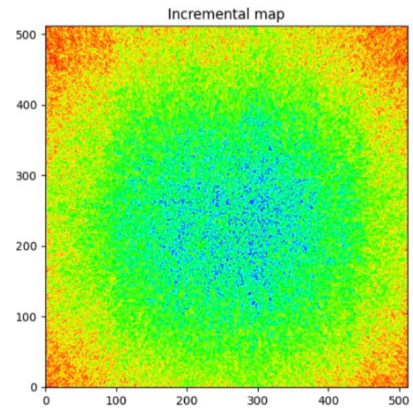
^{90}Sr
(collimated 1mm)

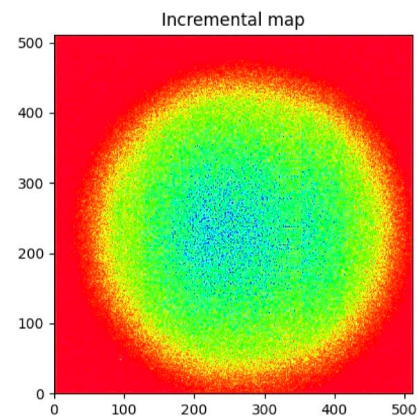




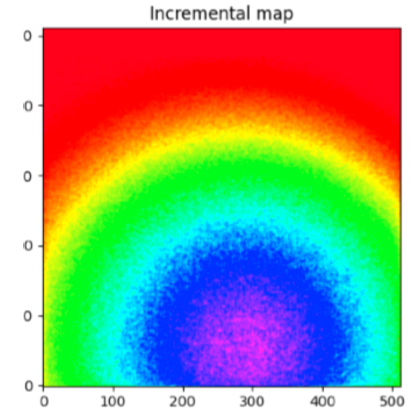


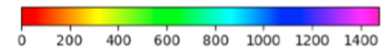
^{90}Sr
(uncollimated)

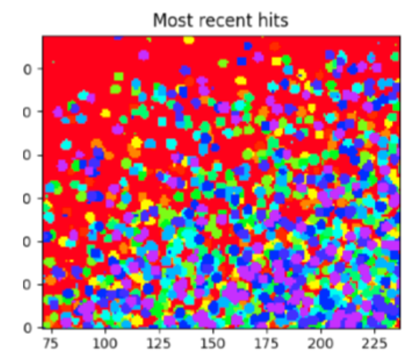




^{241}Am



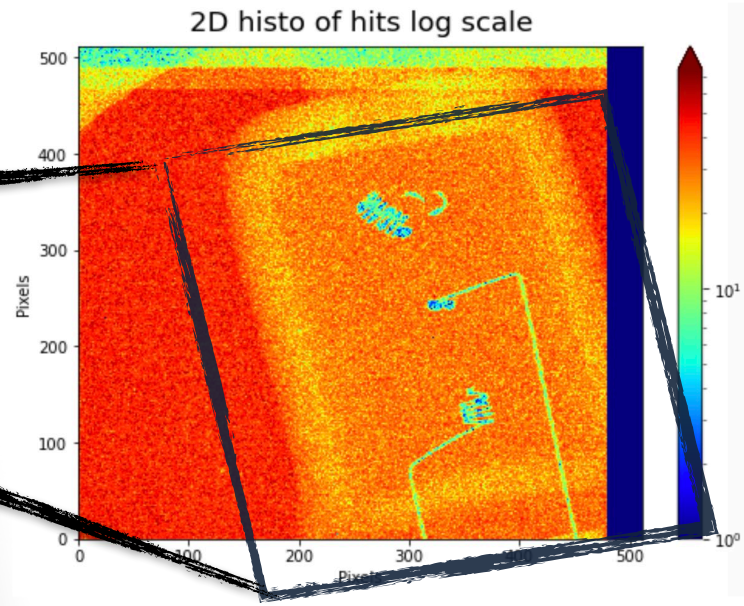


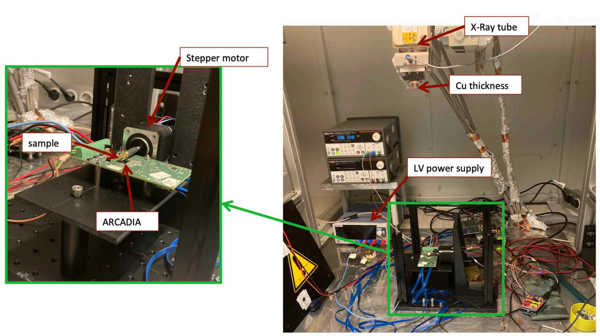


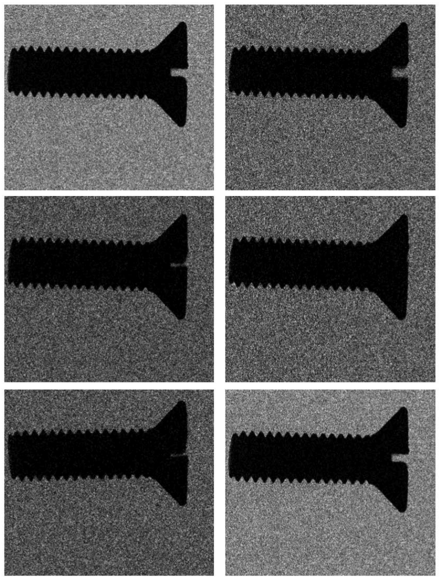
ARCADIA-MD3: X-ray tube and CT

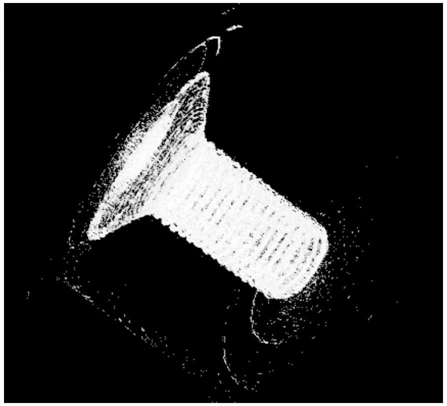
- X-ray setup (2 mA, 40 kV) with W tube (8.40 keV and 9.67 keV)
- Radiography samples and CT reconstruction (stepper motor, 1.8 deg)

S. Ciarlantini



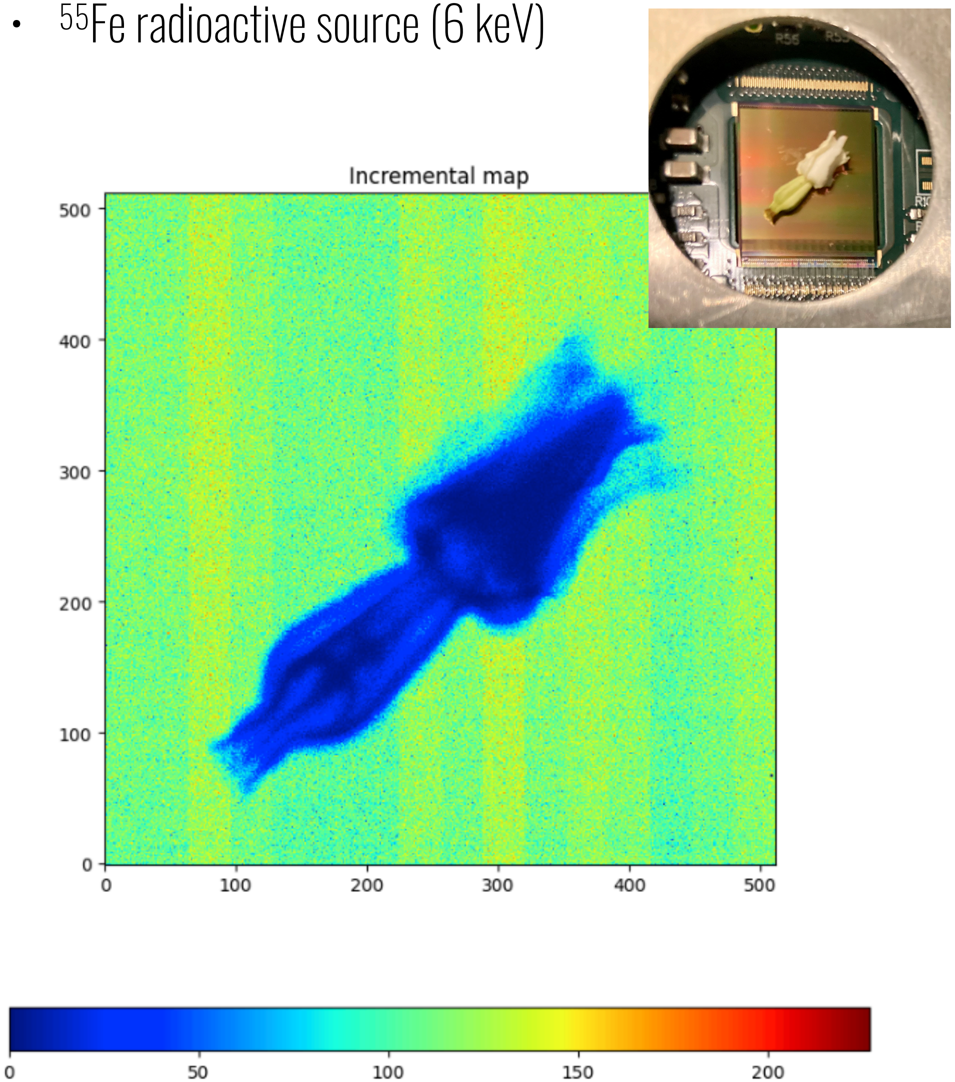


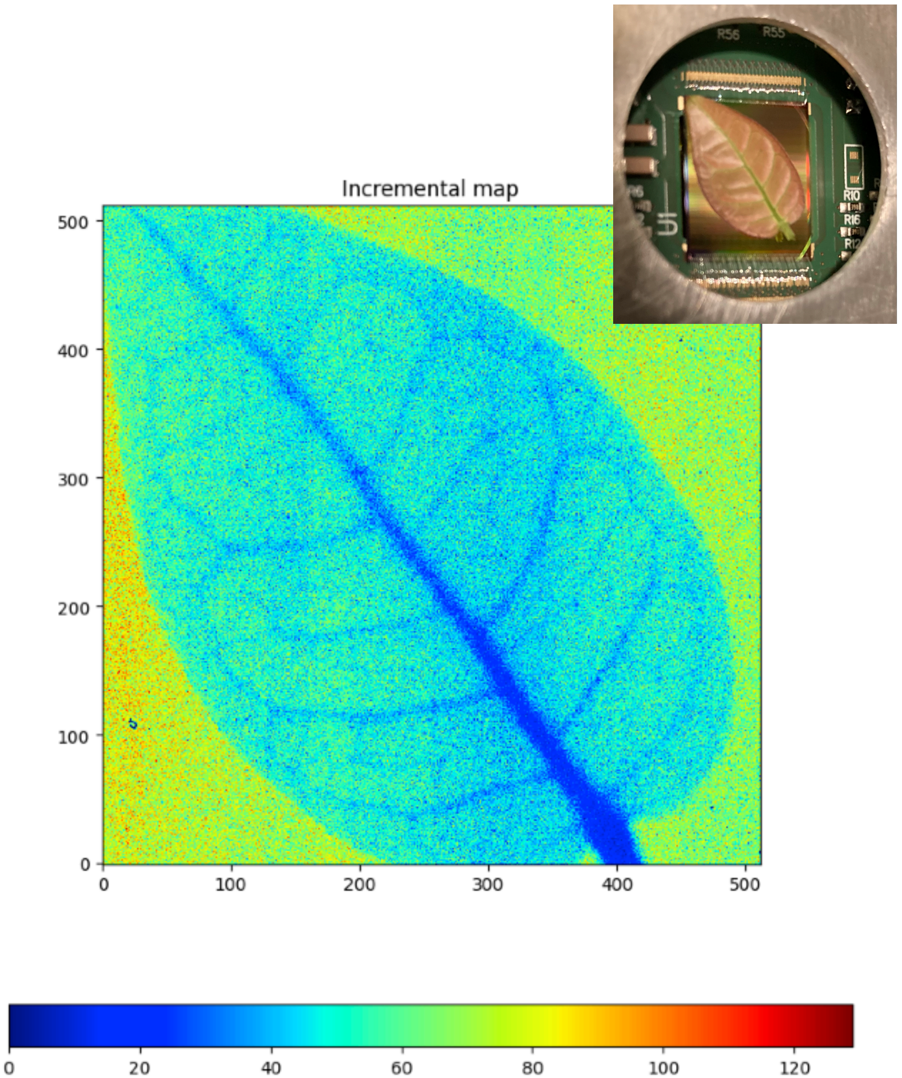




ARCADIA-MD3: X-ray radioactive source

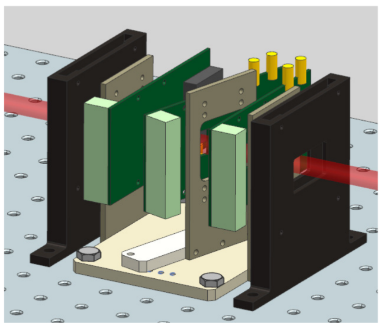
- ^{55}Fe radioactive source (6 keV)

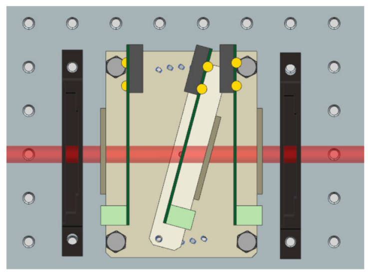


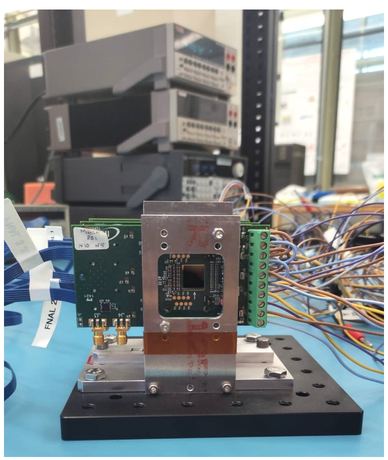


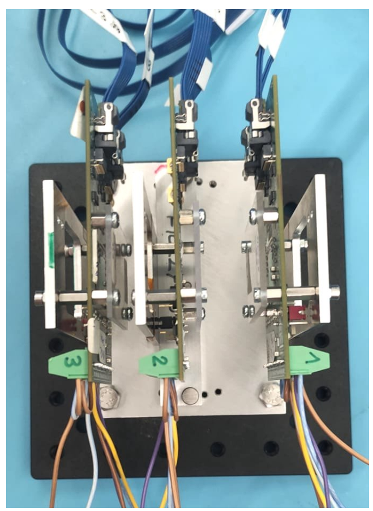
Test beam with ARCADIA-MD3

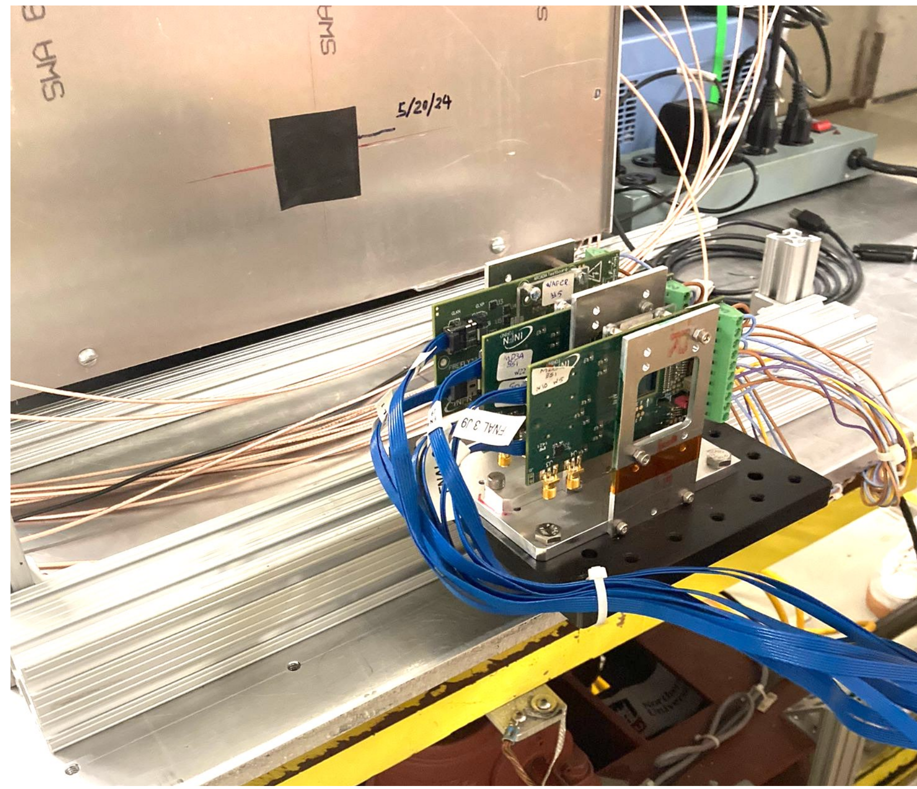
- Test beam at FNAL (120 GeV protons): very good results from <u>data analysis ongoing</u>
- mini-telescope with 3 ARCADIA-MD3 sensors
- Threshold, sensor HV and incidence angle parametrisation: study of cluster size, collection efficiency, spatial resolution



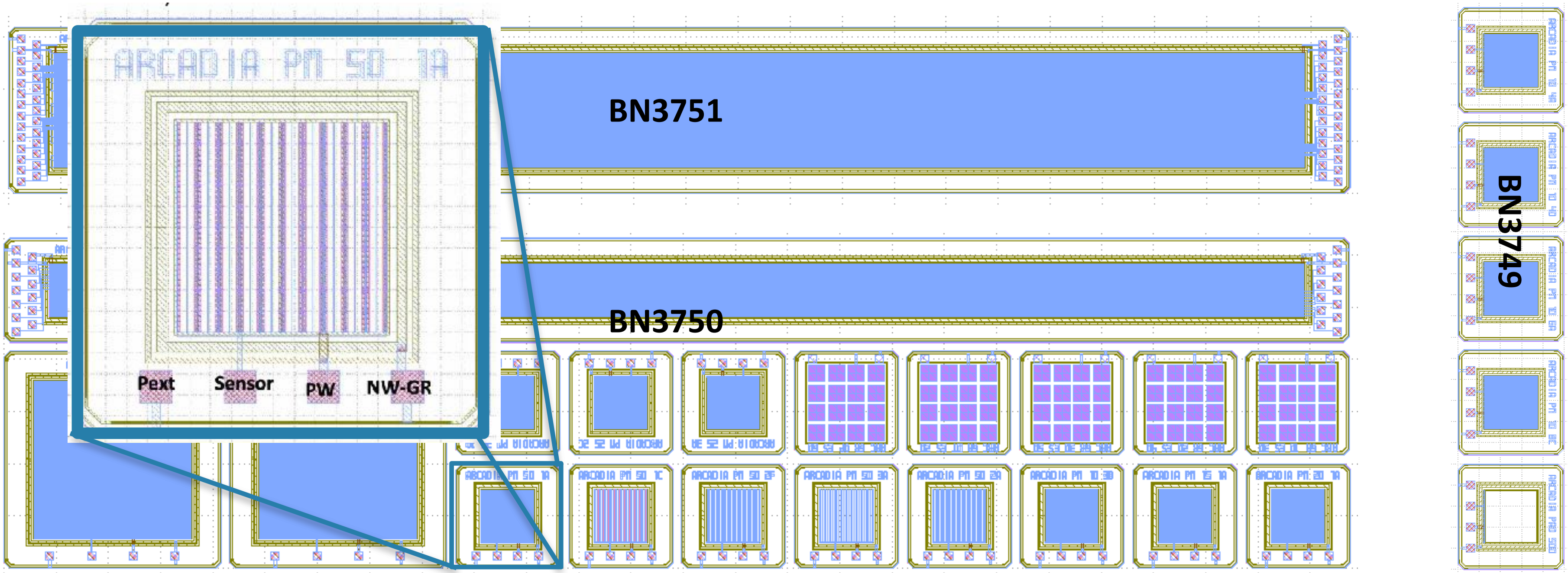








Pixel/Strip Test Structures

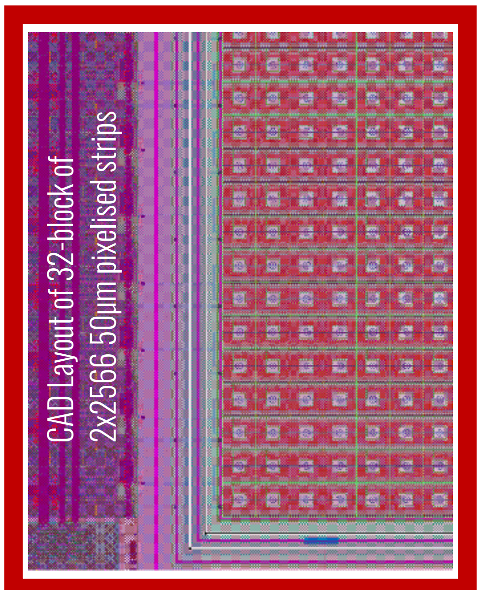


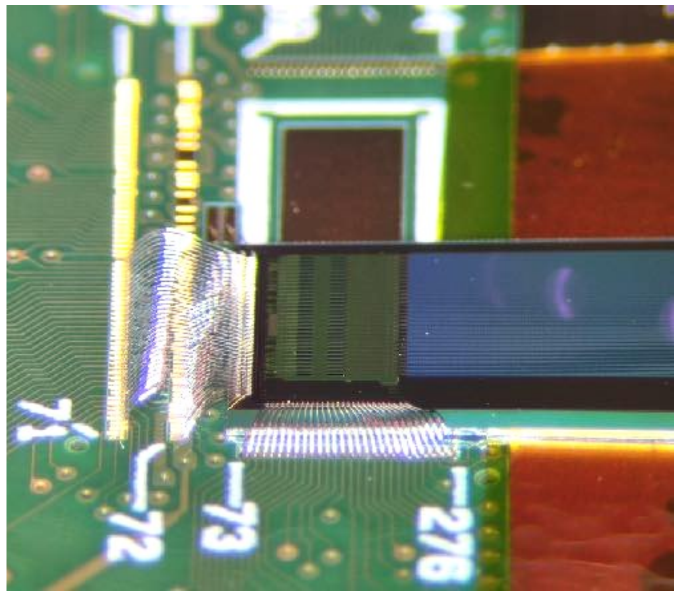
- pixels come in different flavours:
  - Pseudo-Matrices of 1x1 and 2x2 mm^2
  - 50 μm (5 variants)
  - 25 μm (3 variants)
  - 10 μm (6 variants)
- and strips as well:
  - 25 μm pitch pixelated + 25 μm continuous (10+10) [2 variants]
  - 10 μm pixelated (4 groups of 12 strips connected to pads) [4 variants]

L. Pancheri

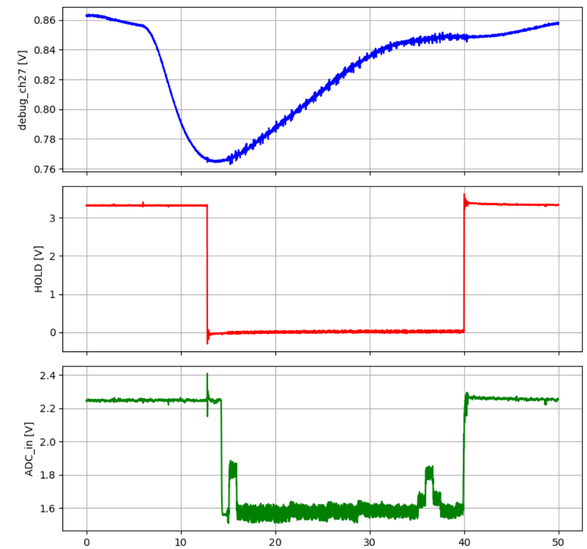
FD Monolithic Active Microstrips

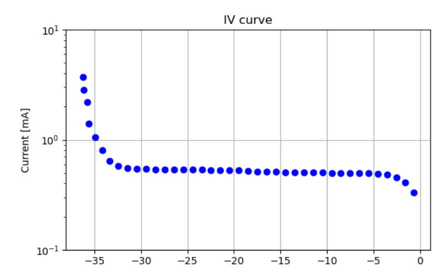
- Design and Production of continuous and "pixelised" strips, range 10 - 100µm pitch
- Proof-of-concept: ***CMOS monolithic strips and embedded readout electronics*** (active sensor area is 12,8 × 3,2 mm^2)
- Analogue (MUX-differential output buffer) and Digital readout (Wilkinson ADC + serialiser)





Example of event with beta-emitter radioactive source



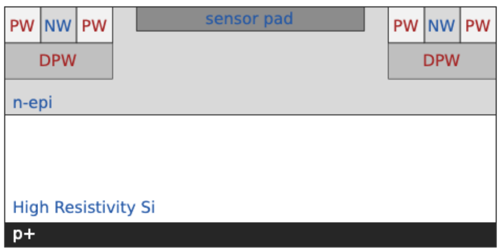


Fully Depleted Monolithic Active Microstrip Sensors: TCAD Simulation Study of an Innovative Design Concept. Sensors 2021, 21, 1990. https://doi.org/10.3390/s21061990

ARCADIA: R&D for fast timing

M. Mandurrino

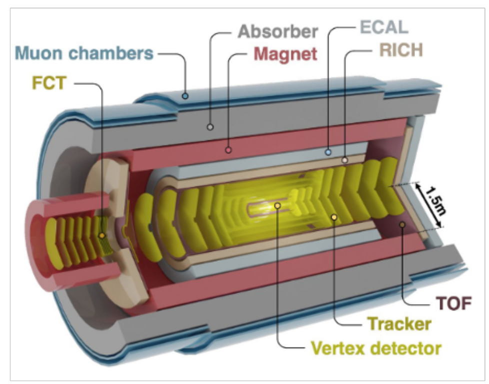
development of fully-depleted MAPS



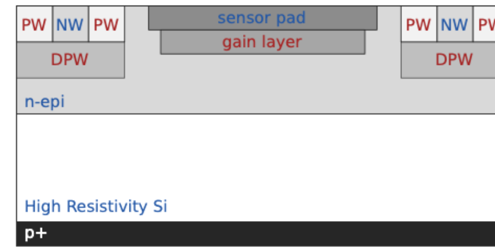
Standard 110 nm CMOS process at **LFoundry**

ALICE3 TOF detector:

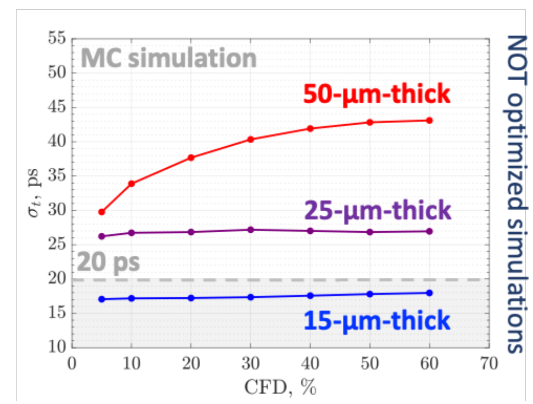
- high-resolution **tracking**
- **particle ID** with low $p_T \Rightarrow \sigma_t \sim$ **20 ps**



CMOS-LGAD



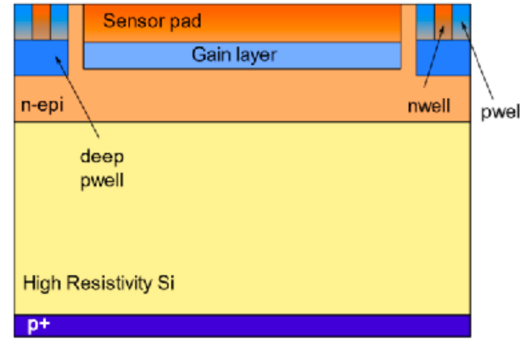
Add-on ***p*-gain** implant (**gain** target: **10 – 30**)



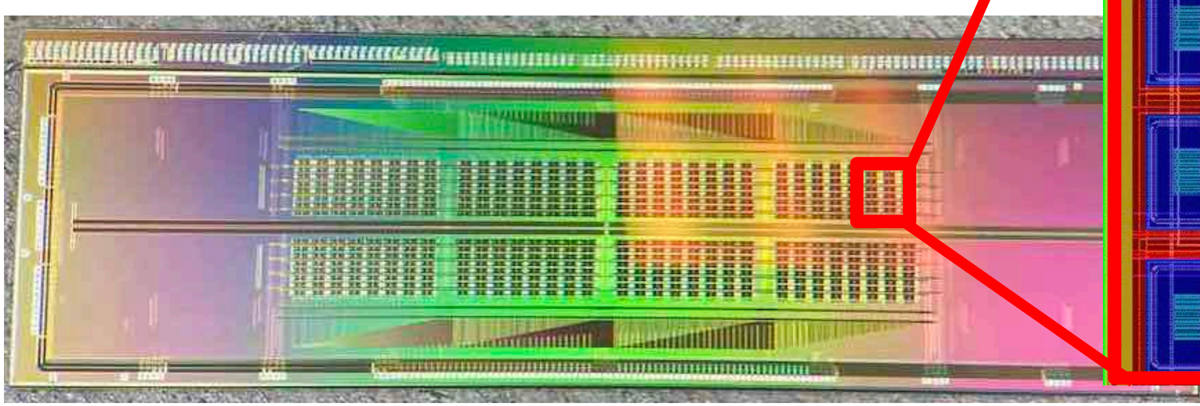
- Add-on p-gain implant underneath the n+ collecting electrode to push the timing performances
- Productions on ARCADIA-ER3 (25 wafers), ER4 (16 wafers) and ER5 (16 wafers, just delivered)

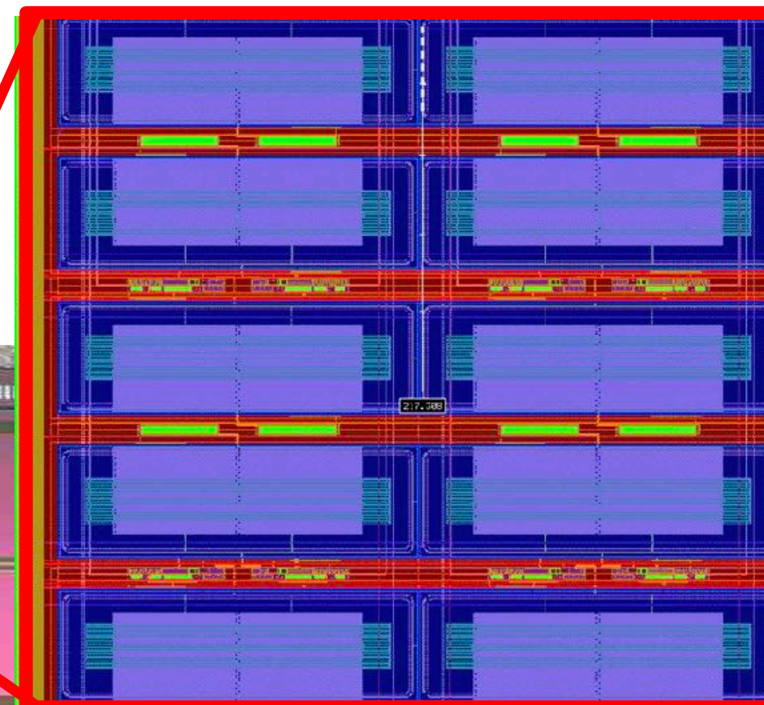
MadPix CMOS LGAD multi-pixel prototype

- MadPix prototype with gain layer and integrated electronics
- first small-scale demonstrator 4 x 16 mm^2;
- 8 matrices (64 pixel pads each) implementing different sensor and front-end flavours;
- 250 x 100 μm^2 pixel pads;
- 64 analogue outputs on each side, rolling shutter of single matrix readout;

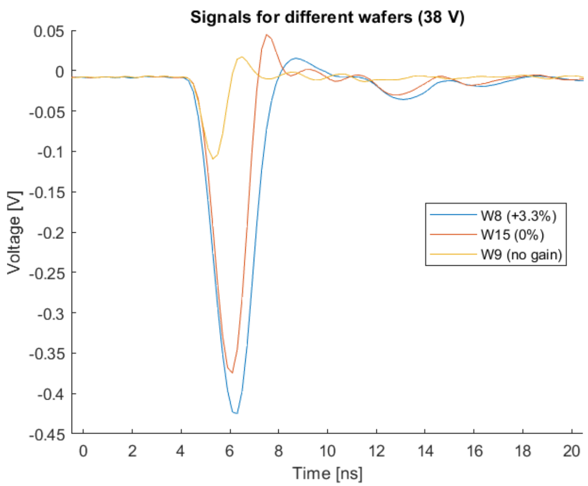


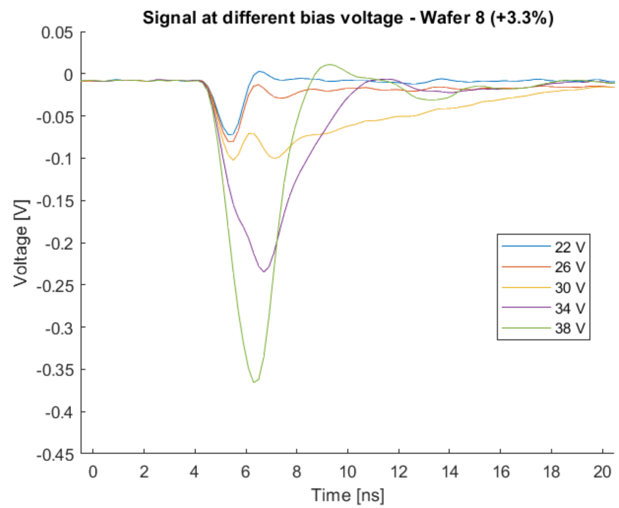
U. Follo, S. Durando, G. Gioachin, C. Ferrero

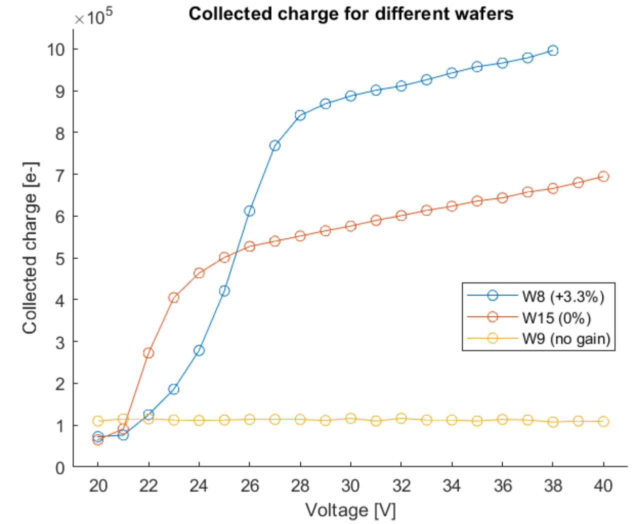




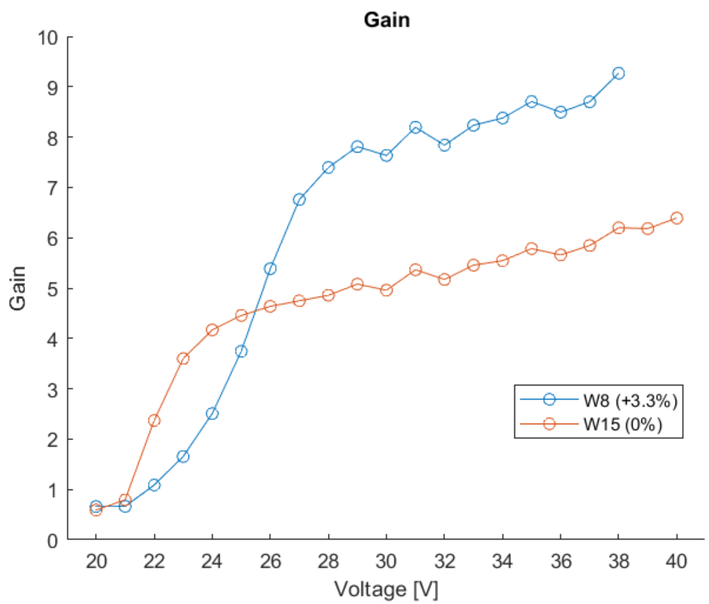
ARCADIA: R&D for fast timing





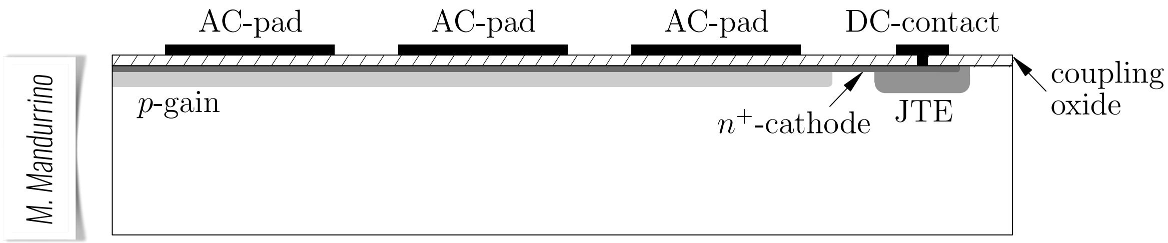


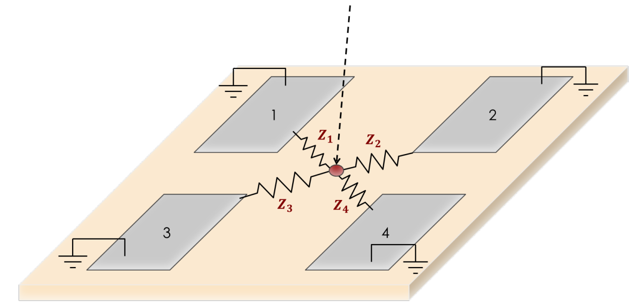
More results on ARCADIA monolithic CMOS detector with internal gain: https://indico.cern.ch/event/1415726/contributions/6144007/attachments/2942716/5170665/Pancheri_ALICE_UpgradeWeek_8Oct2024_v2.pdf



- Gain layer implemented (5-15) with very good matching with TCAD simulation framework
- 48 μm thick active layer on a p+ substrate
- MadPix Test-beam ongoing this week, timing resolution measured < 75 ps (very preliminary results)
- Up next: new short-loop with ARCADIA mask set and thinner n-epi active layer, start full-chip IP design

ARCADIA: R&D for fast timing



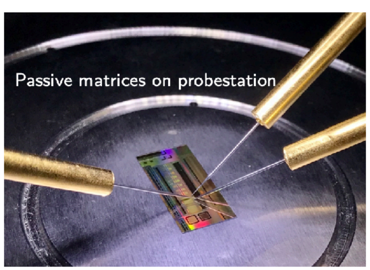


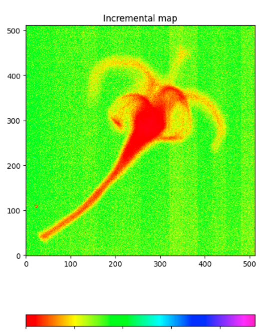
More info on RSD: project, 10.48550/arXiv.2003.04838, 10.1016/j.nima.2021.165319

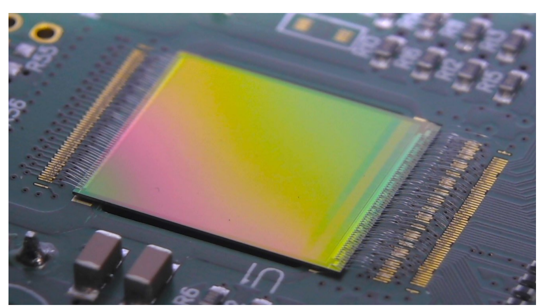
- LGAD detector with continuous gain layer (RSD), charge collection through resistive n-layer and readout by induction on AC coupled pads, for a
- fully active detector, avoiding inefficient regions due to the insulation between pixels in LGAD sensors
- Sharing is deterministic (in low pitch pixel detectors sharing is dominated by Landau fluctuations)
- Timing resolution approximatively independent from pixel pitch
- CMOS integration of the LGAD technology already demonstrated (in LF11is) with the ARCADIA project
- Up next for CMOS AC-LGAD: demonstrate the compatibility between the RSD readout scheme and the LF11is CMOS process flow

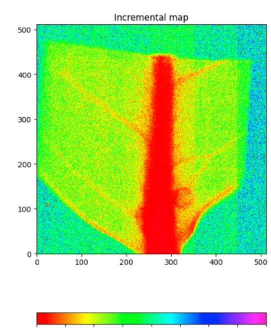
ARCADIA FD-MAPS: Status and Perspectives

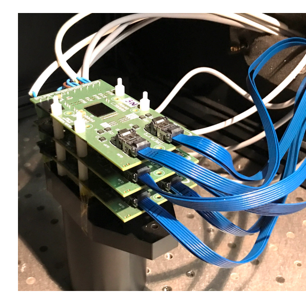
- **ARCADIA:** CMOS sensor design and fabrication platform on LF11is technology
  - Scalable FDMAPS architecture with very low-power: **10 mW/cm²**
  - Custom BSI process allow to develop fully-depleted thick sensors (400μm) for soft X-ray imaging
- INFN has secured 600k€ funding for production of ARCADIA FDMAPS in '25 - '26:
  - New FSI and BSI mask sets: IP development (shunt LDOs, chip-to-chip data transmission blocks), optimisation towards system-grade I/O interface, optimisation of the front-end intrinsic timing performance
- Ongoing R&D for the implementation of monolithic CMOS sensors with gain layer for fast timing, candidate technology for the ALICE3 Time-of-Flight detector
- ARCADIA LF11is FD-MAPS technology support through **DRD7.6a** (*Common Access to selected imaging technologies*)











LF11is FDMAPS development through DRD7

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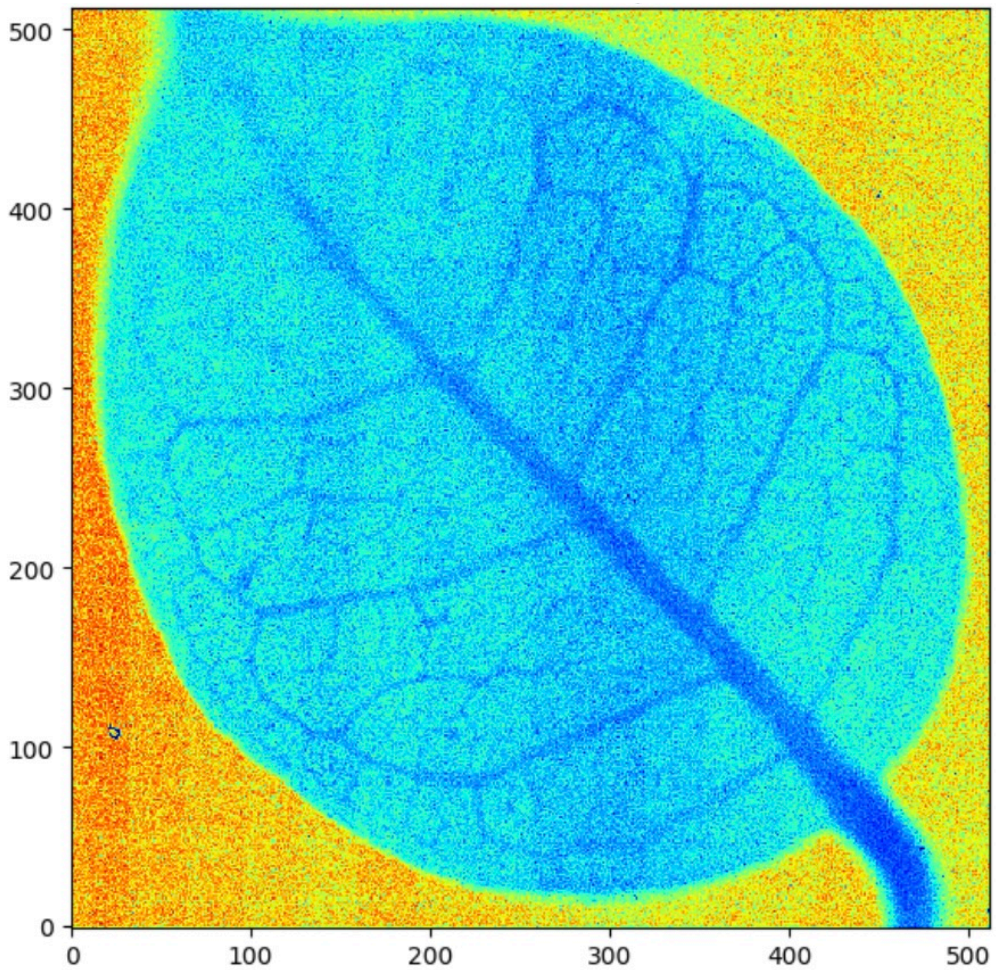
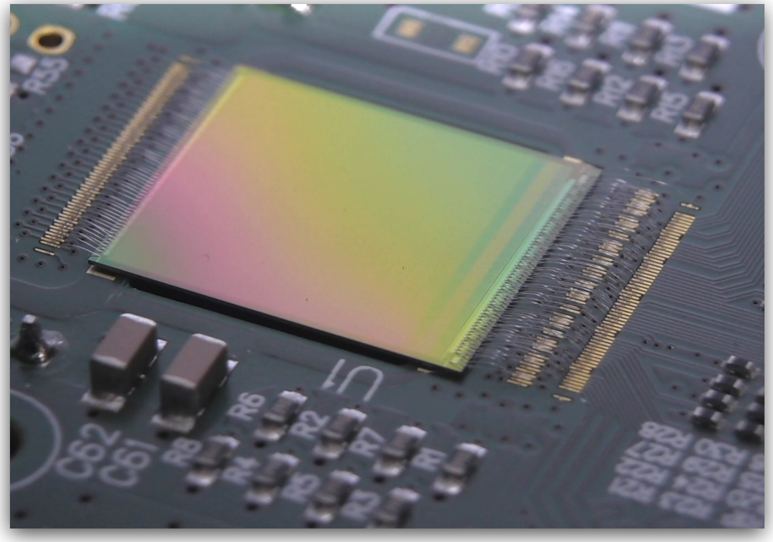
DRD7.6 – Complex Imaging ASICs and Technologies

- Possibility to explore multiple wafer splits: n-epi thickness, n-type or p-type starting substrate, substrate resistivity, FSI or BSI process on different wafer thicknesses, use of a gain layer for the implementation of monolithic CMOS LGADs.
- INFN and LFoundry agree on the terms to allow for the participation of third-party design groups to joint LF11is production runs, enabling straightforward and low-risk ramp-up of the R&D on FDMAPS using LF11is technology for new design teams.
- Silicon-proven IP available (Serialisers, c-LVDS Transceivers, bandgap/LDO, SPI, DAC/ADCs).

Further information on DRD7 workshop 25-26 September 2023: https://indico.cern.ch/event/1318635/





ARCADIA

Manuel Rolo (INFN),
on behalf of the **ARCADIA Collaboration.**

INFN
Istituto Nazionale di Fisica Nucleare

Thank you for your time!

CEPC