

Status of drift chamber for CEPC

Mingyi Dong

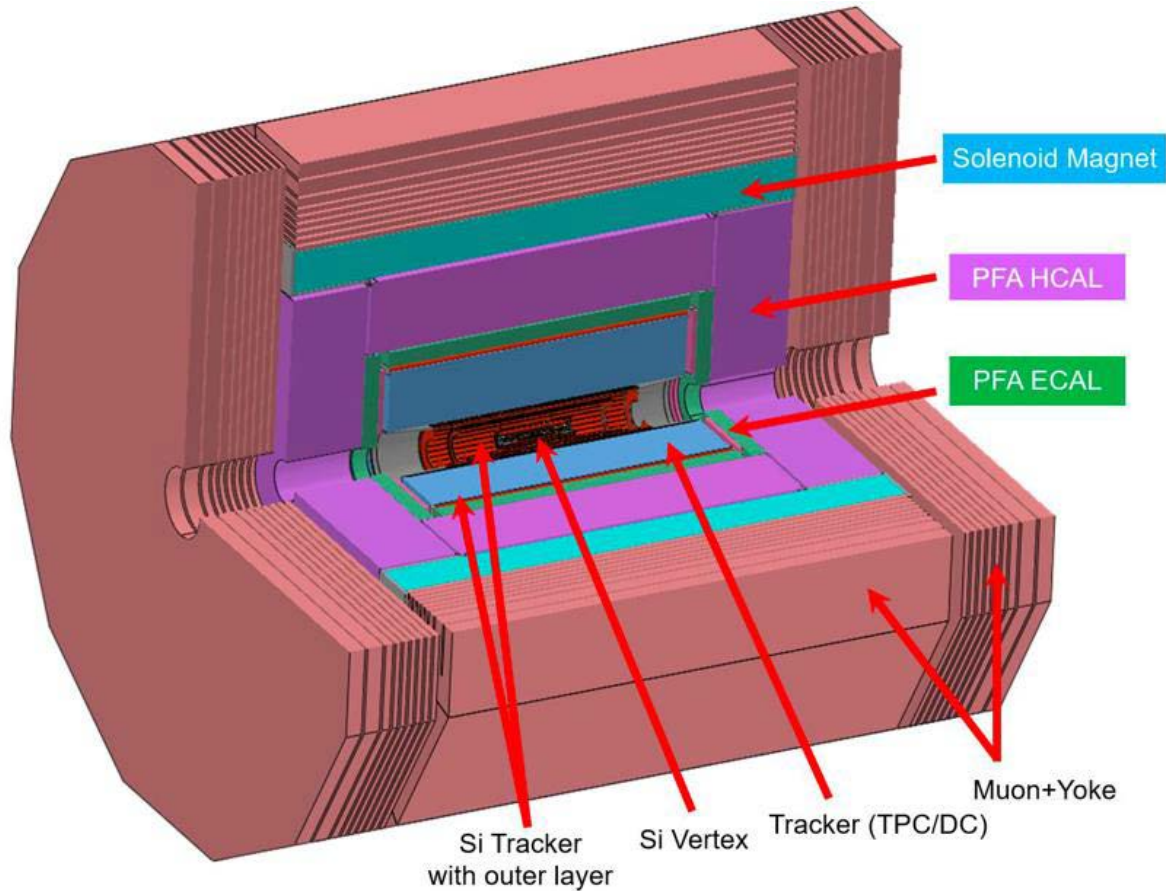
On behalf of CEPC drift chamber group

The 2024 international workshop on the high energy Circular Electron
Positron Collider , Oct 22 – 27, 2024, Hangzhou

Outline

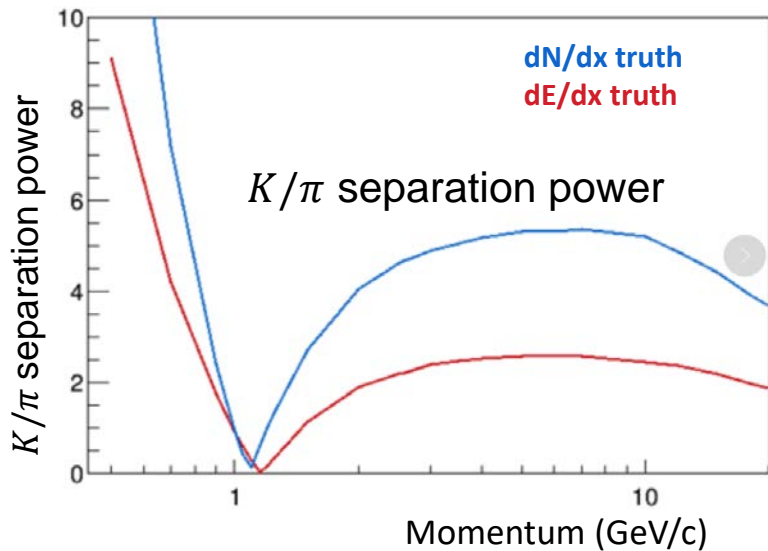
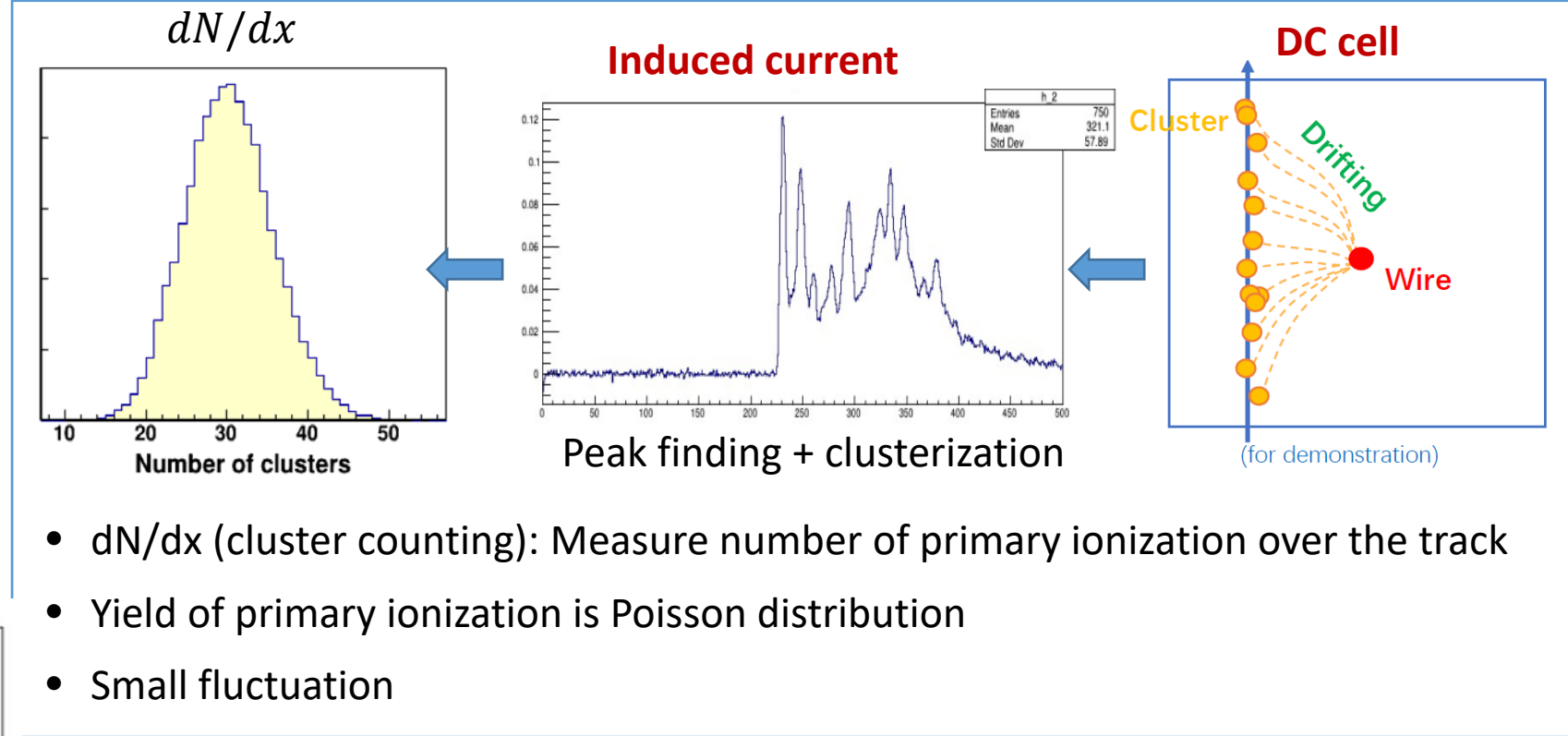
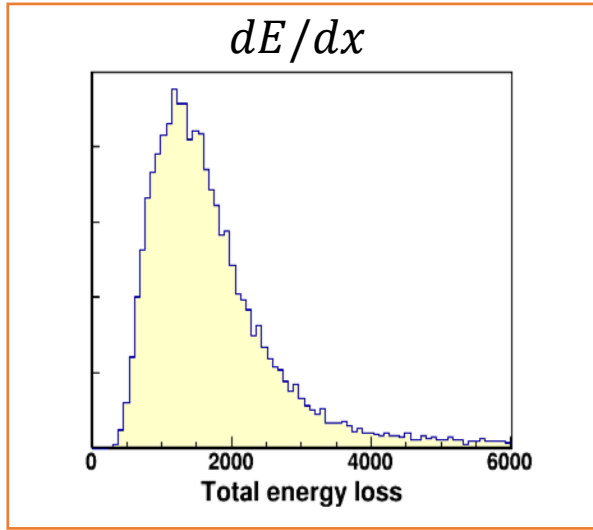
- Introduction of drift chamber for CEPC
- Performance study
- Preliminary design of mechanics and Readout scheme
- R & D progress
- Summary

Drift Chamber for CEPC reference detector



- PID is essential for CEPC, especially for flavor physics
- Combined tracking system that includes a silicon tracker and a drift chamber is an important option.
- Drift chamber will be optimized for its PID capability
- Provides better than 3σ separation power for K/π with momentum up to $20\text{GeV}/c$
- Benefits tracking and momentum measurement

Ionization measurement with dN/dx



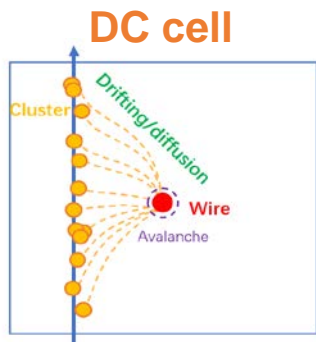
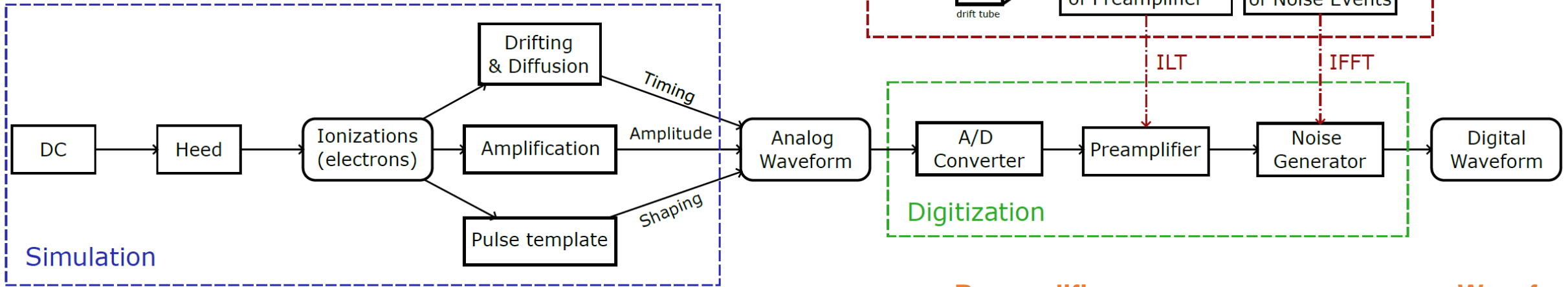
dN/dx has a much better (2 times) K/π separation power up to 20 GeV/c compared to dE/dx (Simulation)

Key issues with dN/dx measurement

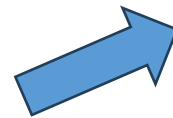
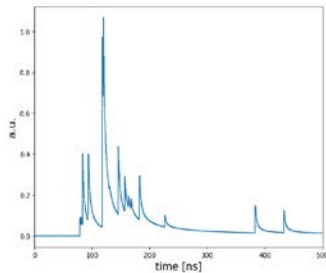
- Detector optimization and performance study (dN/dx resolution and PID capability)
 - Geometry of the detector
 - Mechanical structure, material budget
 - Gas mixture: low drift velocity, suitable ionization density gas with low diffusion and low multi electron ionization
- Precise testing of waveforms
 - Fast and low noise electronics
- dN/dx reconstruction algorithm
 - Identifying primary and secondary ionization signals
 - Reducing noise impacts
 - Improve the reconstruction efficiency

Waveform-based full simulation

Developed sophisticated software tools for DC PID simulation
(Garfield++-based simulation + data-driven digitization)

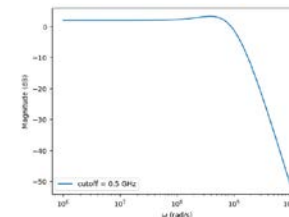


Induced signal

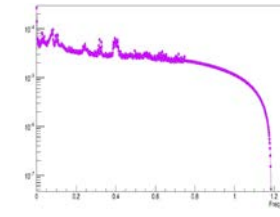


Tuned MC is comparable to data

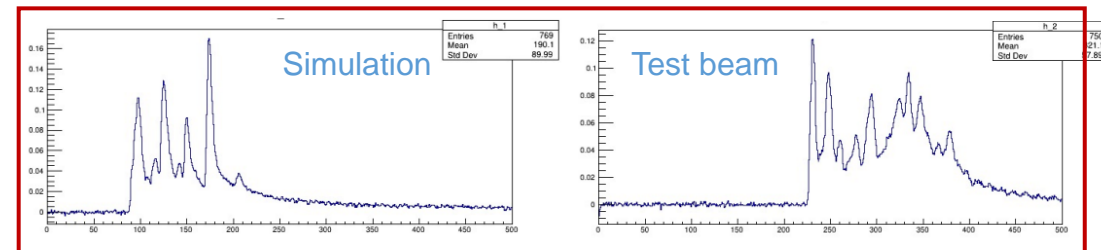
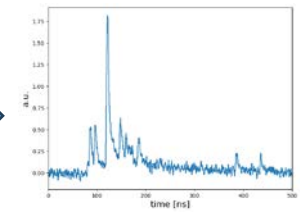
Preamplifier



Noise



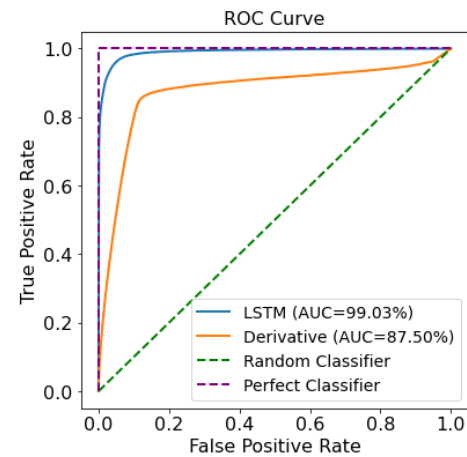
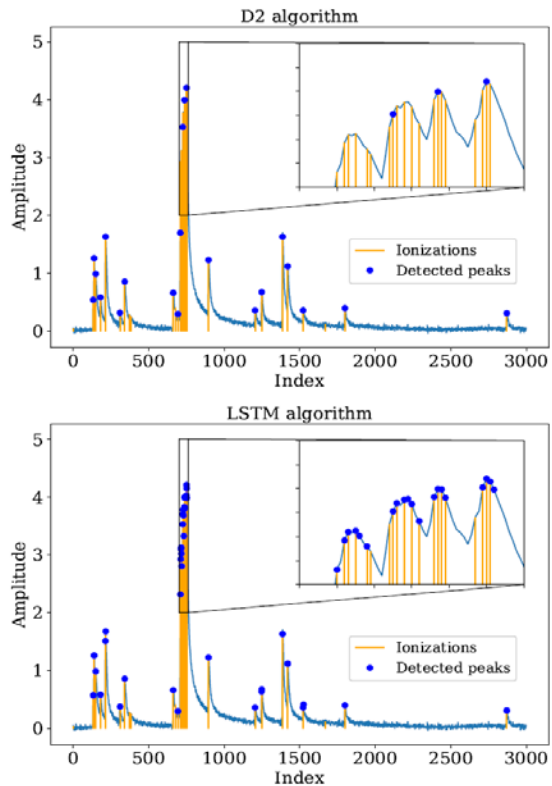
Waveform



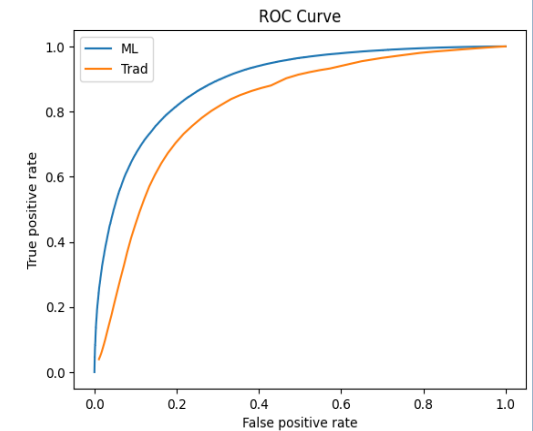
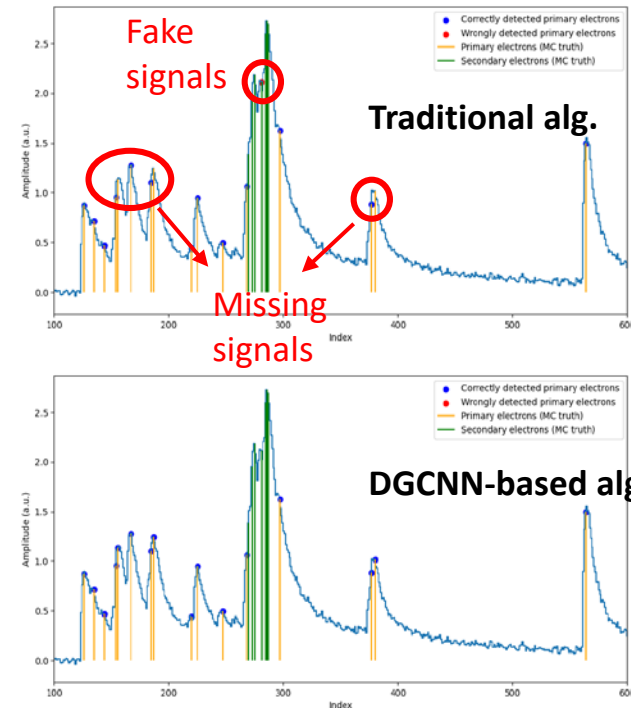
Machine learning reconstruction algorithm

- LSTM-based peak finding and DGCNN-based clusterization
- ~ 10% improvement of PID performance with ML

Long Short-Term Memory (LSTM)-based peak finding
higher efficiency than the derivative-based algorithm,
especially for the pile-up recovery

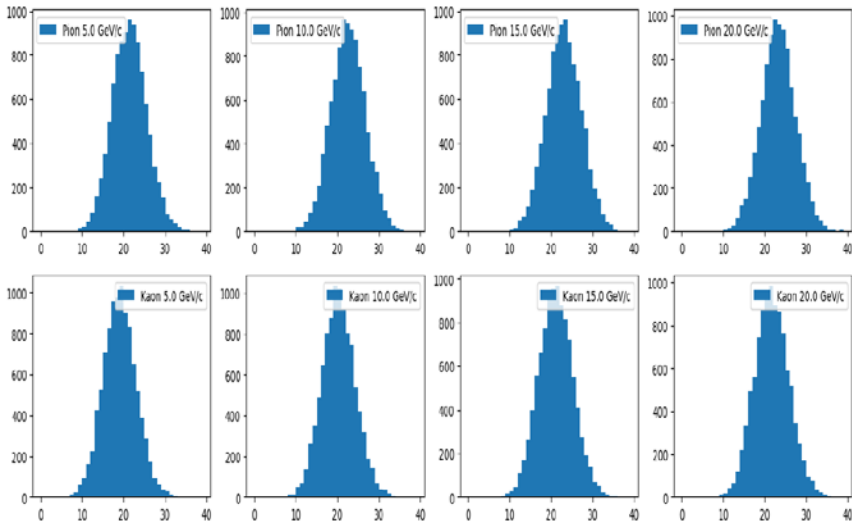


Dynamic Graph CNN (DGCNN)-based clusterization
higher efficiency, and lower fake rate

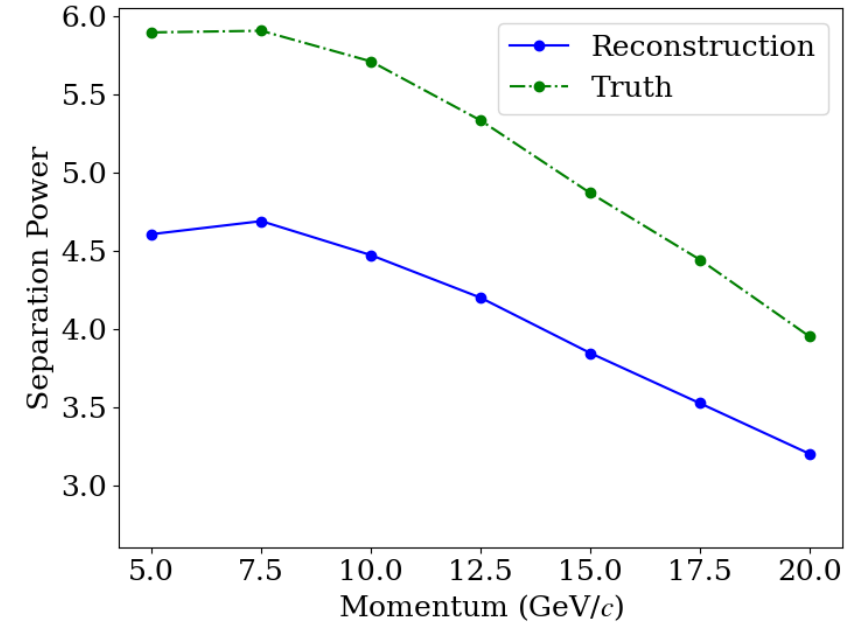
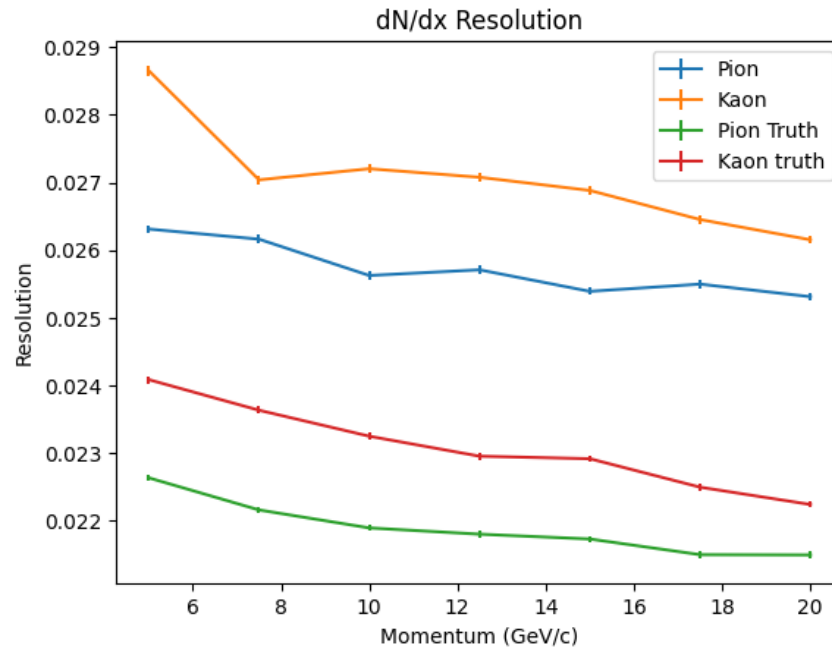


dN/dx Resolution

Reconstructed # of clusters distributions



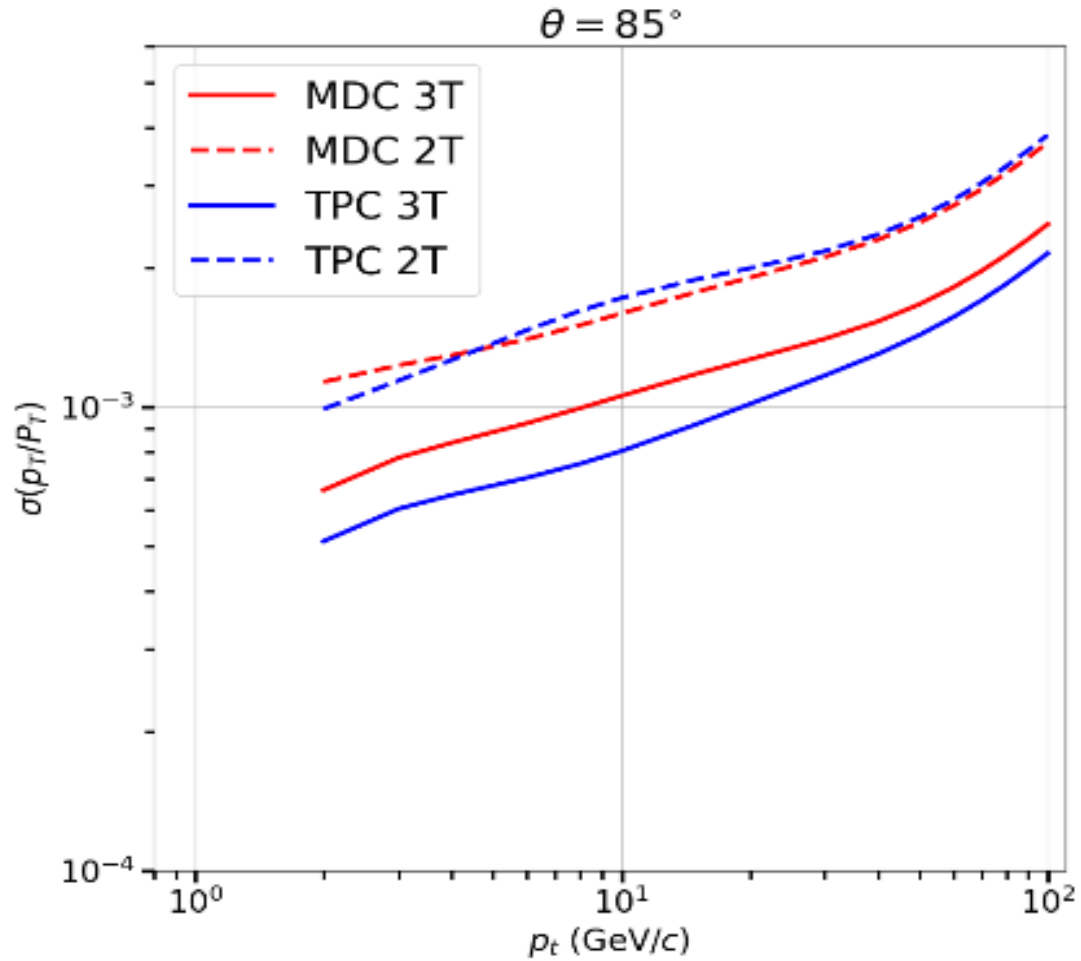
The reconstructed n_{cls} distributions are very well Gaussian-like



- dN/dx resolution (1.2 m track length):
 - 2.5%-2.6% for Pion
 - 2.6%-2.7% for Kaon

- 1.2 m track length
- For 20 GeV/c K/π , Separation power: 3.2σ

Momentum Resolution



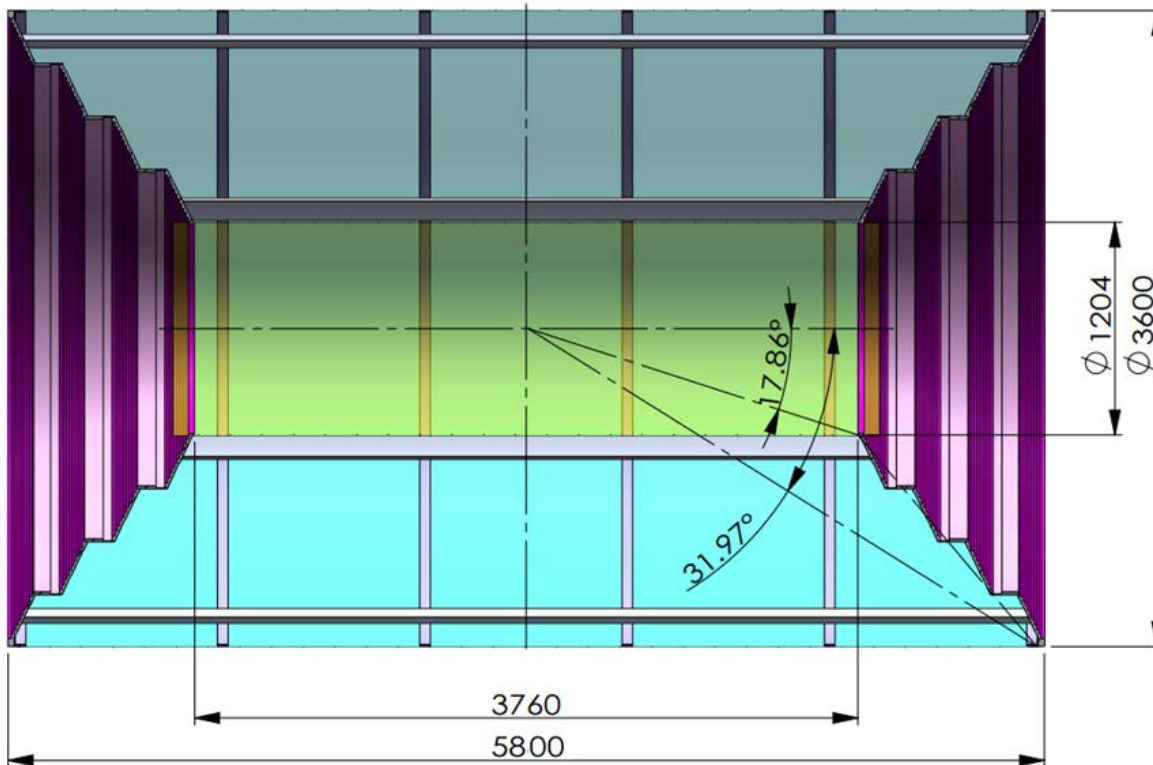
$$\sigma(1/p_t) = a \pm b/p_t$$

	Higgs	Z-pole
a (1/GeV)	2.1×10^{-5}	3.2×10^{-5}
b	0.77×10^{-3}	1.16×10^{-3}

Momentum resolution is comparable with TPC at Higgs and Z mode

Overall mechanical design

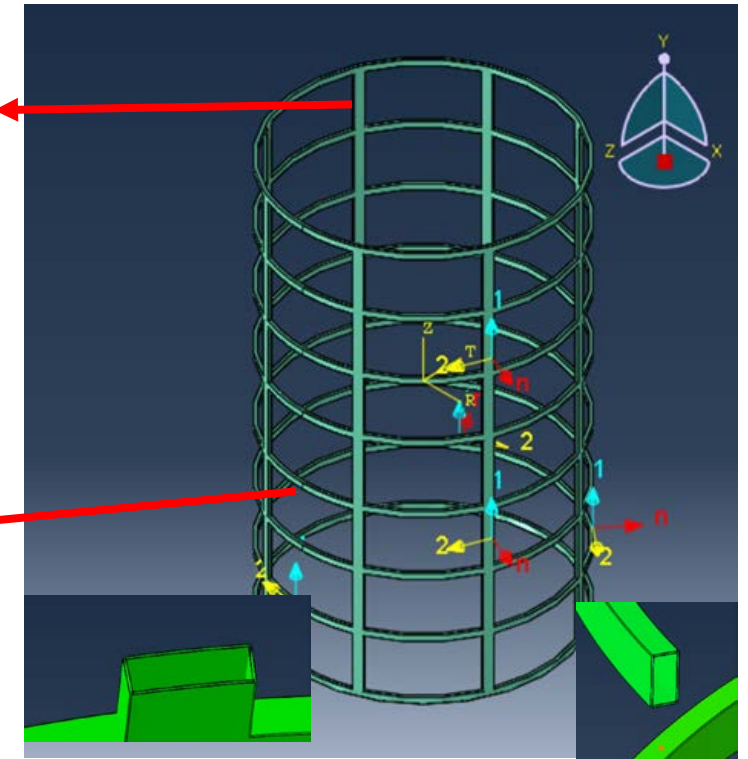
End plates + CF frame structure



CF frame structure

Cross section of longitudinal HB :
80mm*40mm,
thickness: 3.2mm

Cross section of annular HR :
40*10mm
Thickness: 3.2mm



- CF frame structure: 8 longitudinal hollow beams + 8 annular hollow rings + inner CF cylinder and outer CF cylinder
 - Length: 5800 mm
 - Inner diameter: 1200 mm, Outer diameter: 3600 mm
- Each End plate: including 4 steps, thickness: 20 mm, weight: 880 kg

Wire tensions

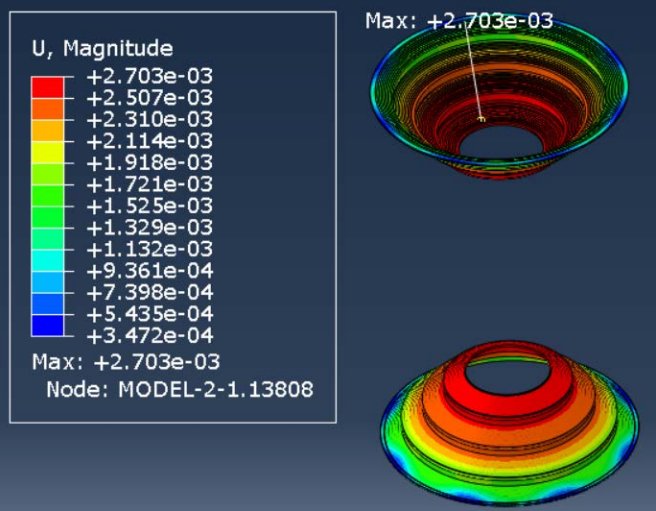
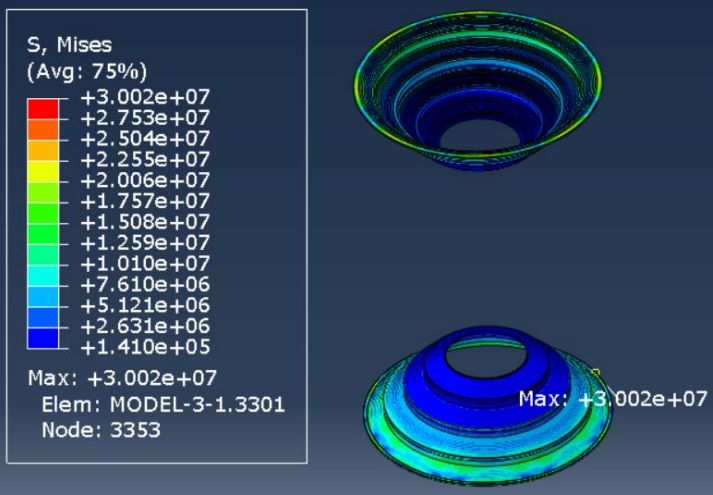
	Cell number/step	Average length (mm)	Single sense wire tension (g)	Single field wire tension (g)	Total tension/step (kg)
step1	9172	5668	86.92	133.56	4472.08
step2	7528	5122	70.98	109.07	2997.38
step3	5845	4526	55.43	85.16	1817.14
step4	3939	3928	41.75	64.14	922.46
total	26483				10209

Diameter of field wire (Al coated with Au) : 60 μ m
 Diameter of sense wire (W coated with Au): 20 μ m
 Sag = 280 μ m

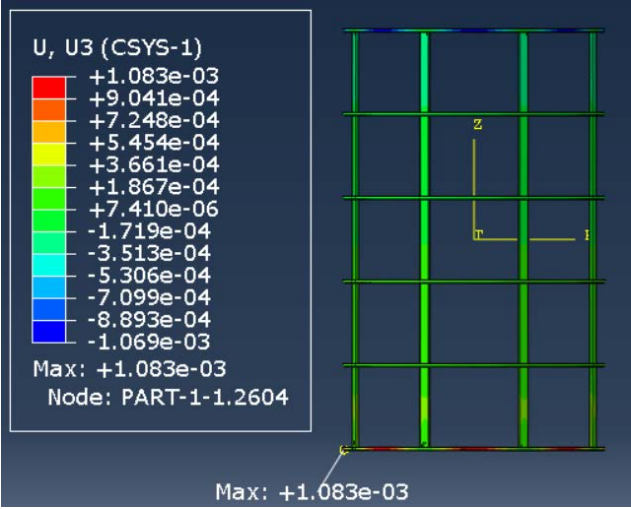
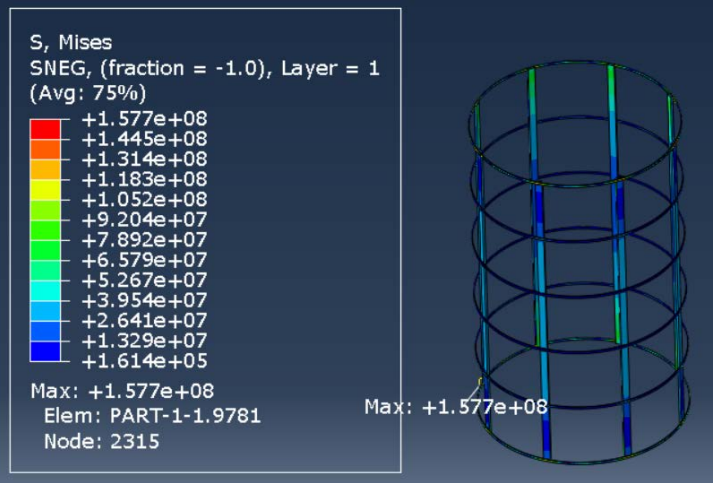
Meet requirements of stability condition:

$$T > \left(\frac{VLC}{d}\right)^2 / (4\pi\epsilon_0)$$

Finite element analysis



- Max Mises stress of End plate : 30MPa
- Endplate deformation 2.7mm



- Max Mises stress of CF frame : 235MPa
- CF frame deformation 1.1mm

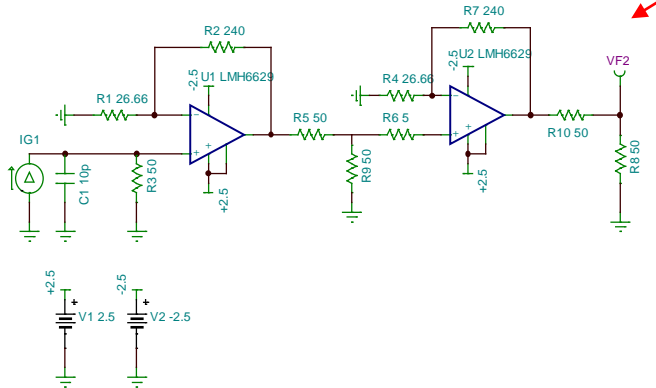
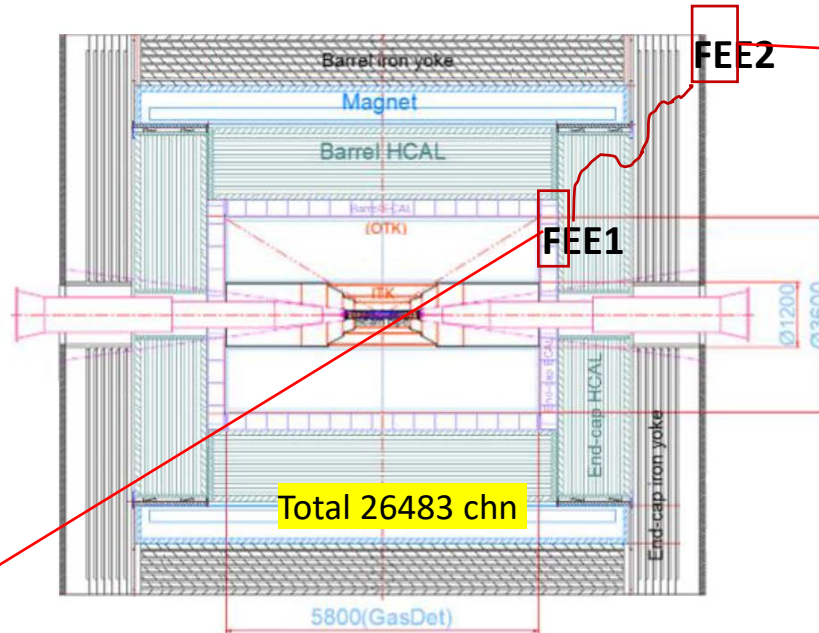
The structure is stable

Preliminary readout scheme of drift chamber

Considering : radiation hardness
Power consumption,
Material budget

FEE-1:
Rad-hard analog preamps

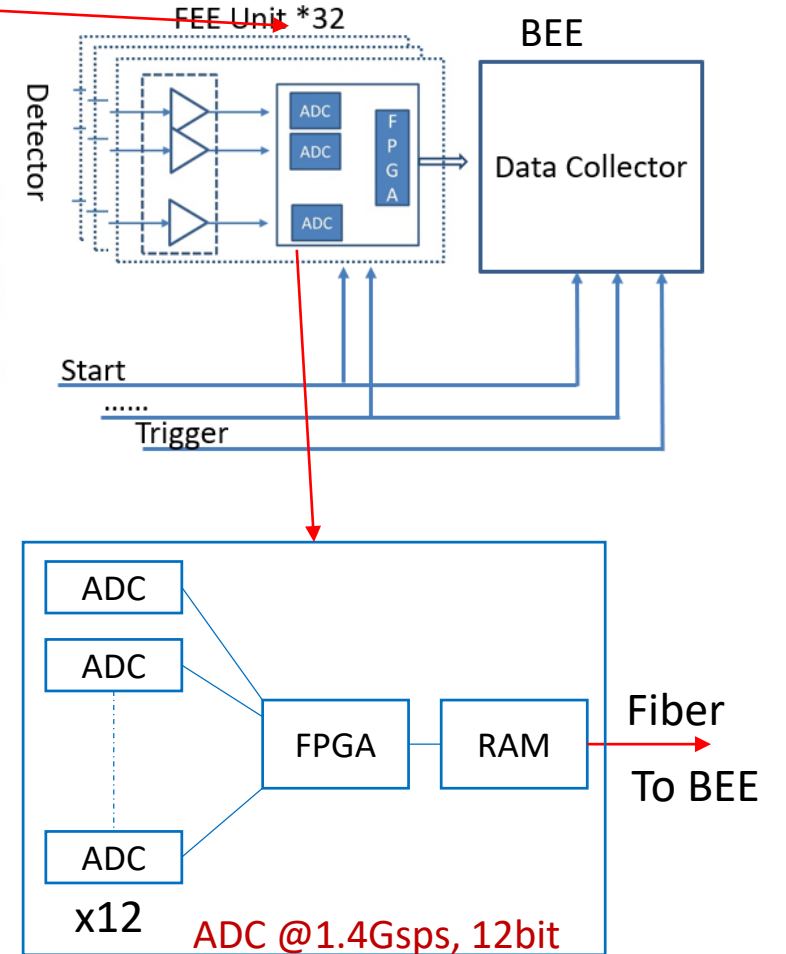
FEE-2:
ADC and FPGA board for data readout
and buffering, put in low dose region



High Bandwidth Preamp
100mW/ch -> ~2.6kW in total
1.3kW for each end plate, air cooling is OK
no additional material budget



Analog signal on Cable
2.8mm per co-ax
12 signals + 1 Power
3dB attenuation @ 280MHz

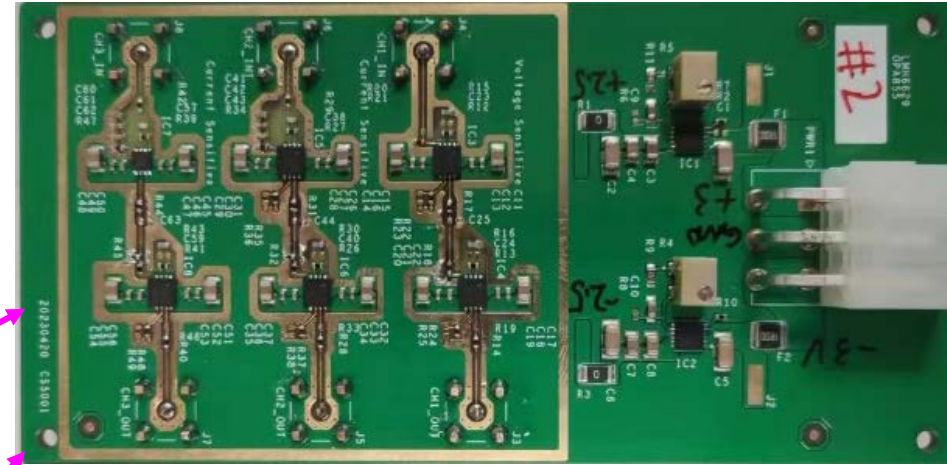
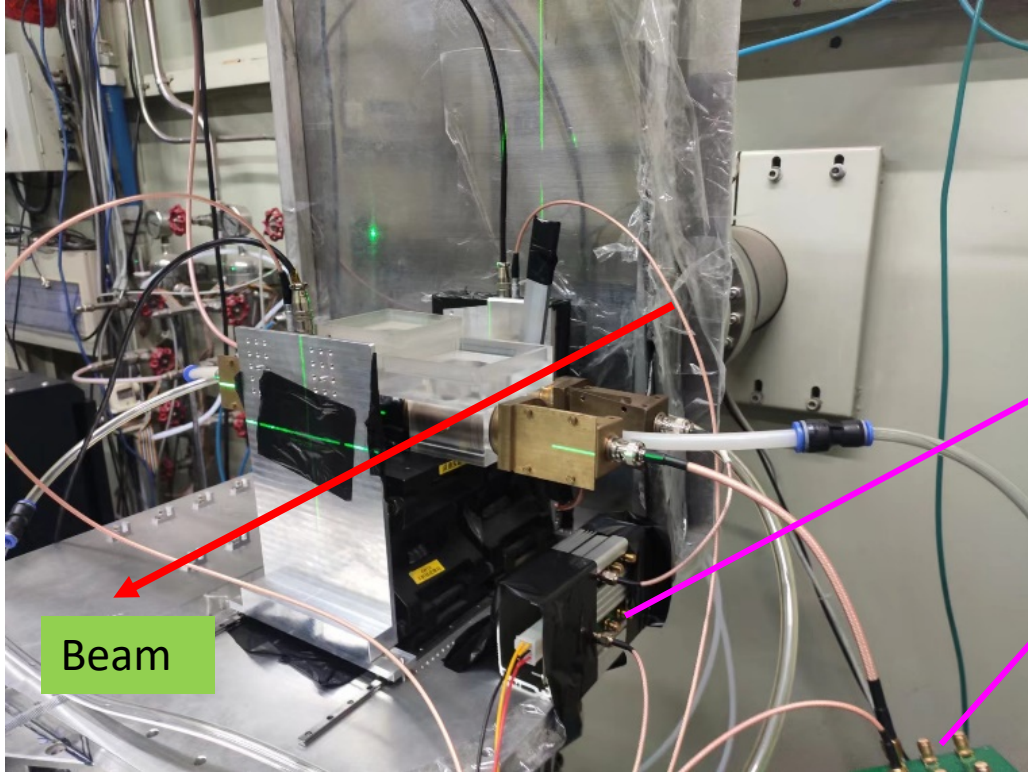


0.5Gbps/12 channels--
compatible with requirement of
CEPC overall readout scheme

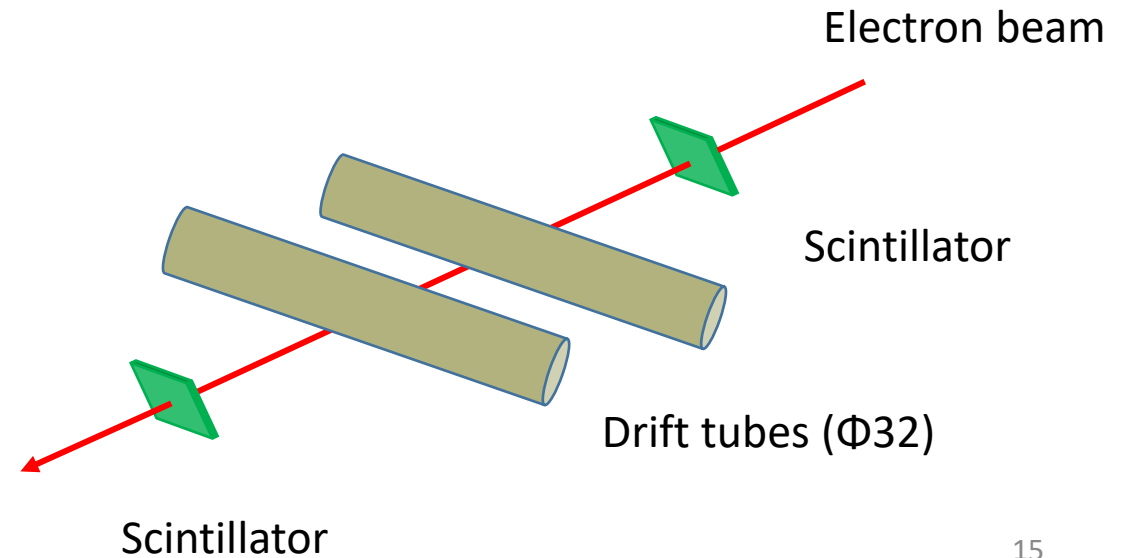
Preliminary design parameters

R extension	600-1800mm
Length of outermost wires ($\cos\theta=0.85$)	5800mm
Thickness of inner CF cylinder: (for gas tightness, without load)	200 μ m
Thickness of outer CF cylinder: (for gas tightness, without load)	300 μ m
Outer CF frame structure	Equivalent CF thickness: 1.8 mm
Thickness of end Al plate:	20mm
Cell size:	$\sim 18 \text{ mm} \times 18 \text{ mm}$
Cell number	26483
Ratio of field wires to sense wires	3:1
Gas mixture	He/ $i\text{C}_4\text{H}_{10}$ =90:10

Detector R&D and test

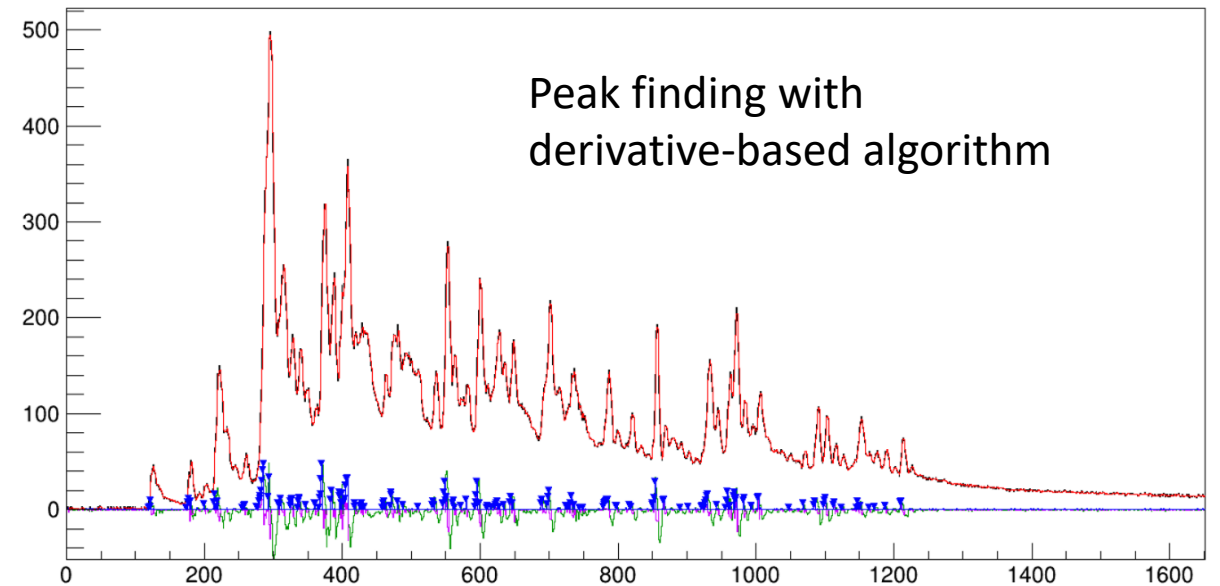
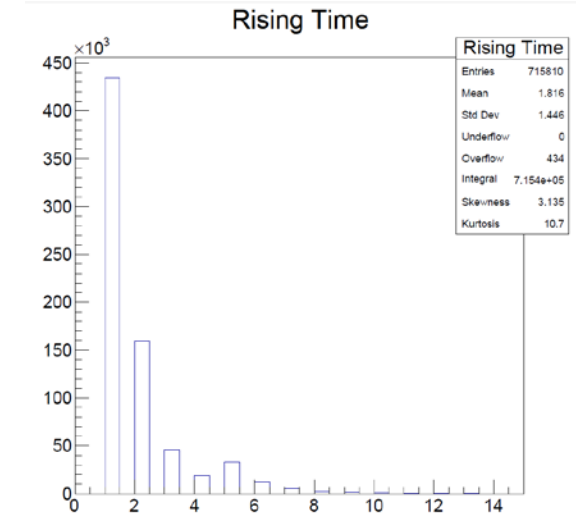
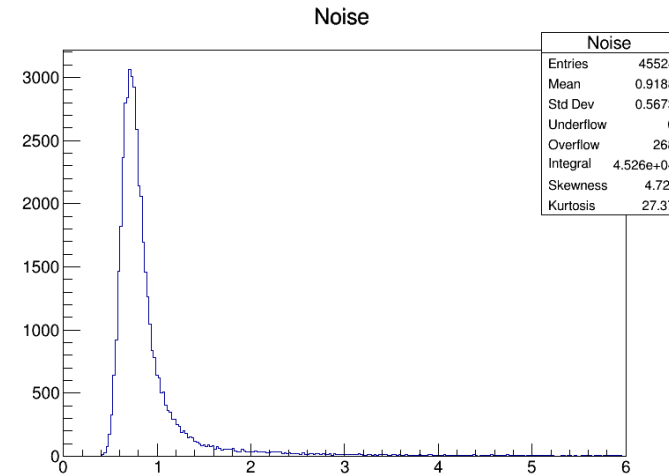
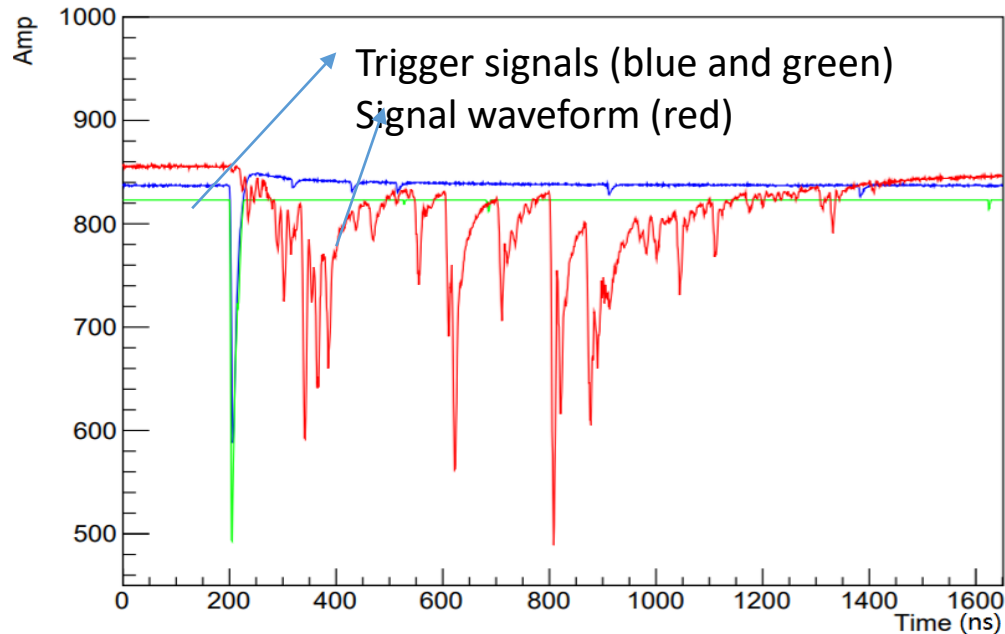


- Developed fast and high bandwidth preamps
- Set up a test system and tested with electron beam at IHEP
 - Two drift tubes + preamps + ADC (DT 5751 digitizer with 1GHz sampling rate)
 - Two scintillators provide trigger signals



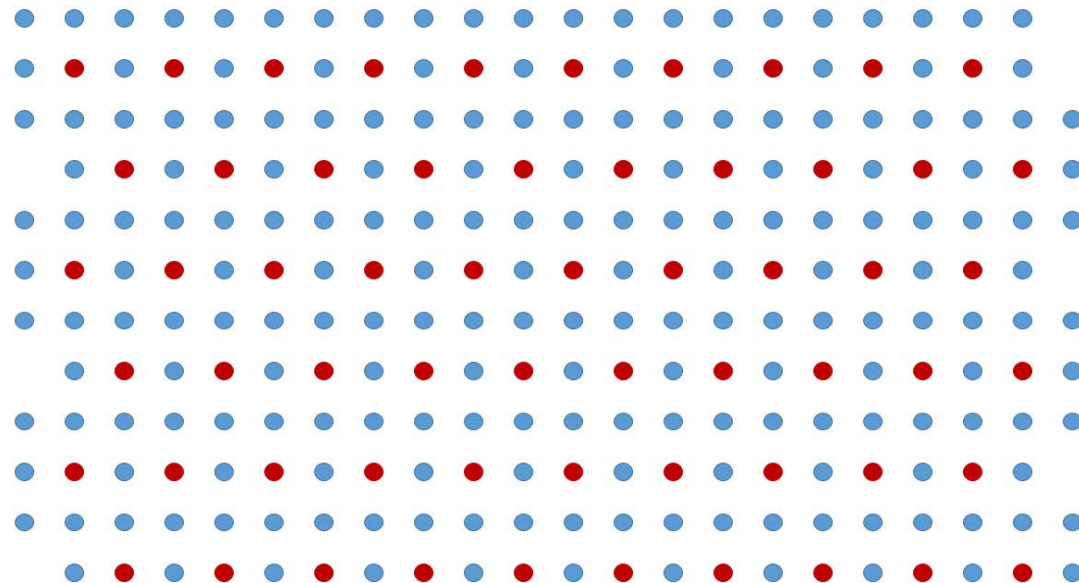
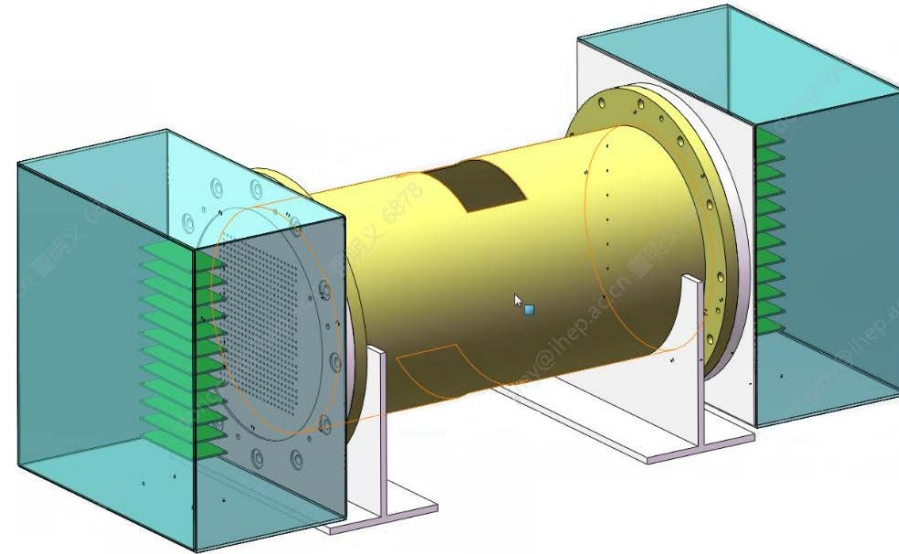
Preliminary results

- Clear peaks
- Rise time : \sim ns
- The performance of preamplifiers:
 - Low noise
 - high bandwidth



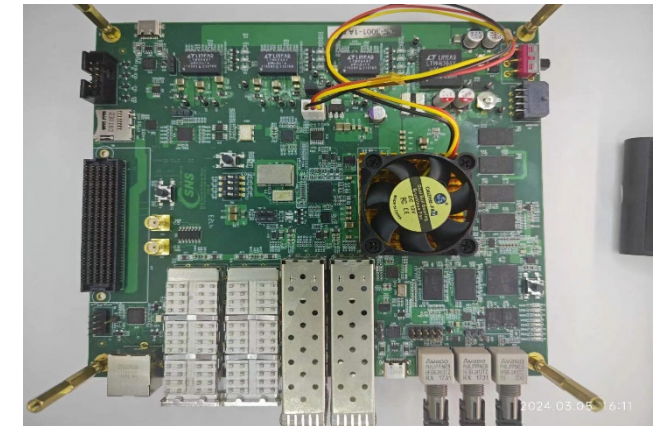
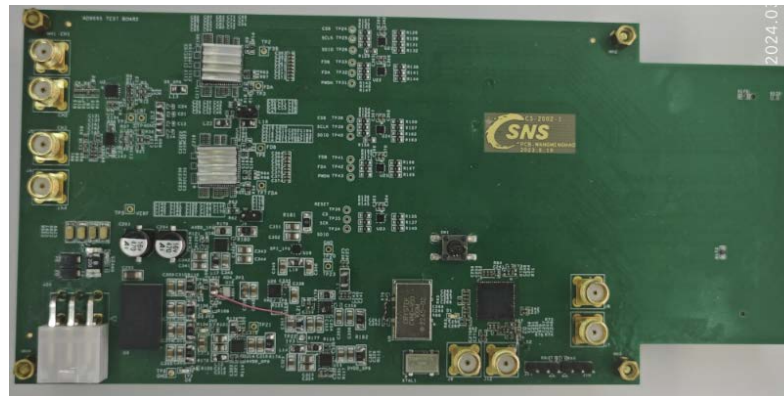
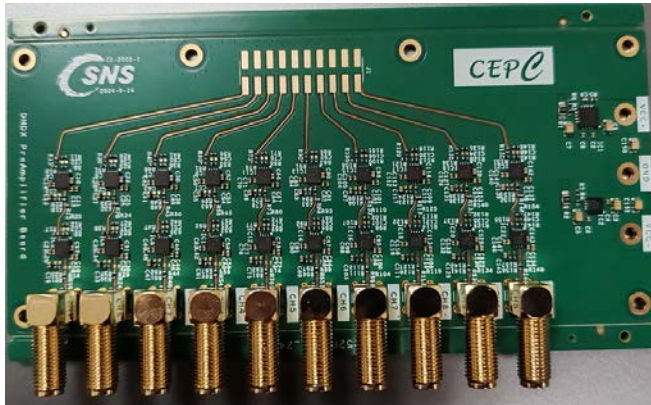
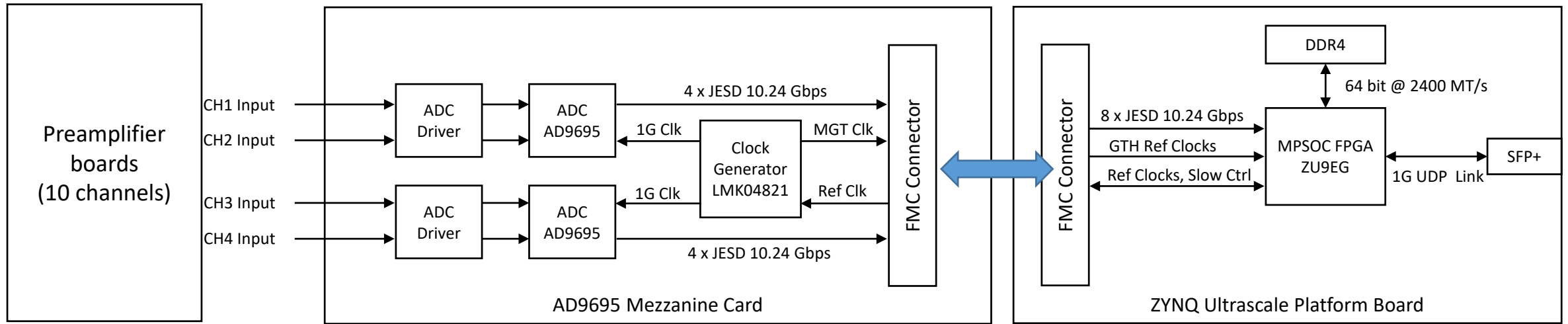
Multi-layer prototype design

- Prototype with 12 layers (120 cells) was designed for dN/dx resolution study
- Components (wires, feedthroughs, connectors) were prepared
- Cell size : $18 \text{ mm} \times 18 \text{ mm}$
- Sense wire: $20 \mu\text{m}$ Au-plated tungsten
- Field wire: $60 \mu\text{m}$ Aluminum or $80 \mu\text{m}$ Au-plated Aluminum



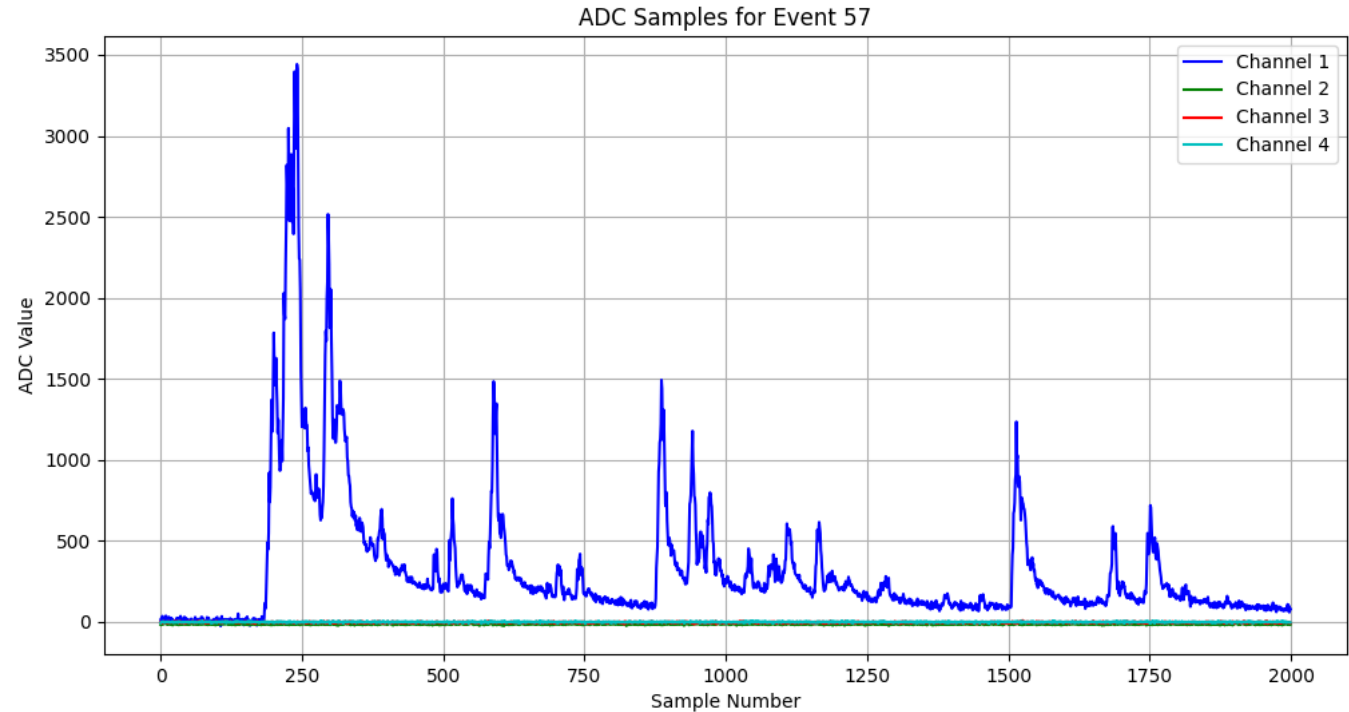
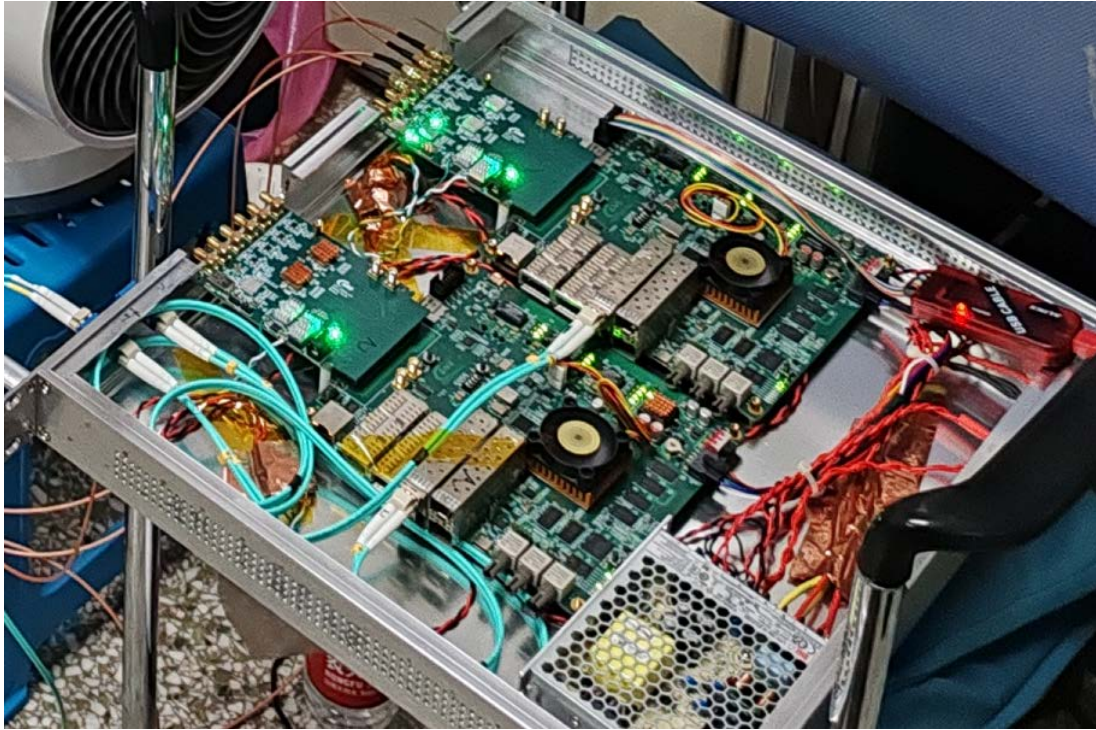
- Field wire
- Sense wire

Readout electronics design



- A readout prototype system is developed, consisting of a preamplifier board, an ADC board and an FPGA board
- The ADC board is based on two high-speed ADCs (ADI AD9695), 14 bit resolution, and a maximum sampling of 1.4 Gbps

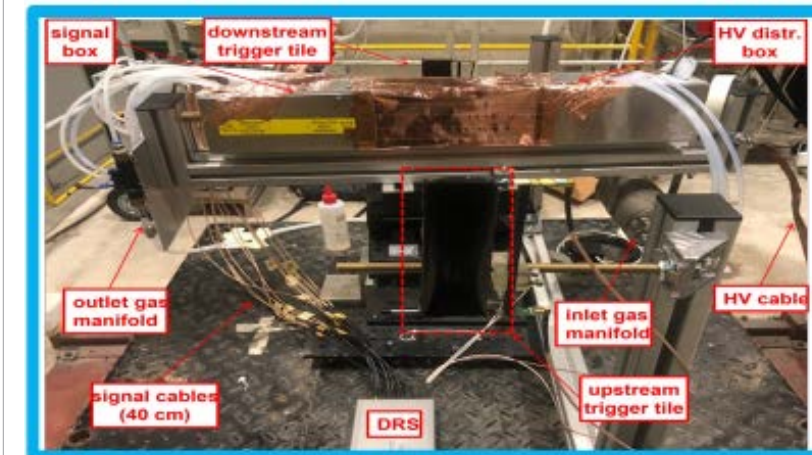
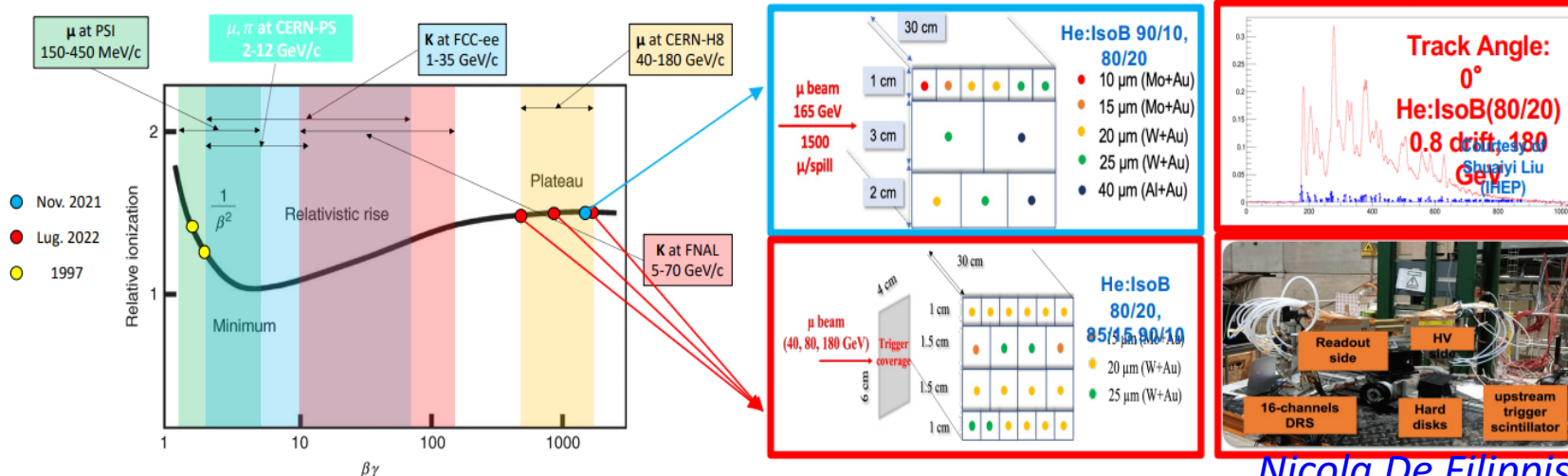
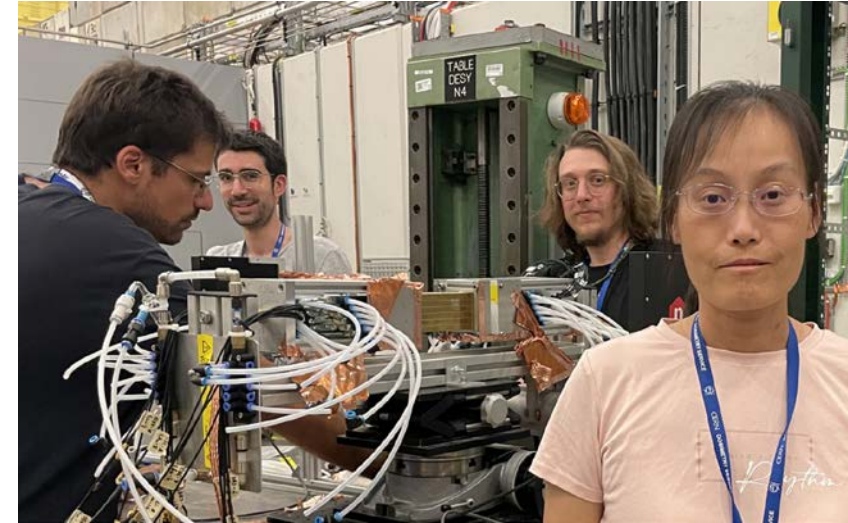
Test of the readout electronics



- The readout system was tested with a detector prototype
- The tested waveforms seem ok. Clear peaks and low noise
- The ADC board and an FPGA board will be integrated into one board in next version

Collaboration with INFN (IDEA DC group)

- Beam tests organized by INFN group:
 - Two muon beam tests performed at CERN-H8 ($\beta\gamma > 400$) in Nov. 2021 and July 2022
 - A muon beam test (from 4 to 12 GeV/c) in 2023 performed at CERN
 - Test in July 2024 aimed to fully exploit the relativistic rise
- Contributions from IHEP group:
 - Participate data taking and collaboratively analyze the test beam data
 - Develop the machine learning reconstruction algorithm



Nicola De Filippis, 2023 CEPC workshop, Nanjing 23-27, 2023

Summary

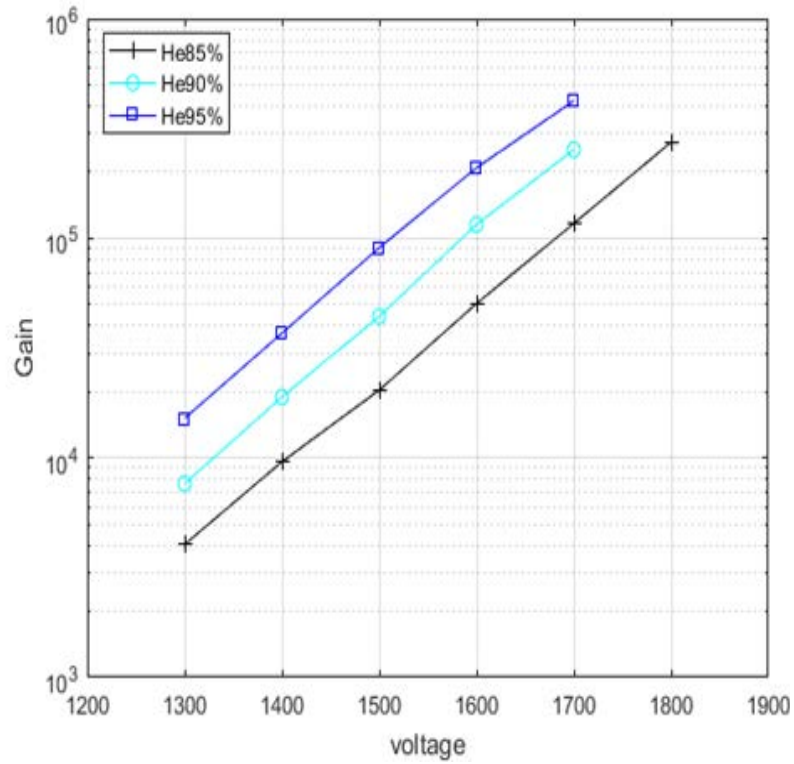
- R&D progress of CEPC drift chamber:
 - Simulation studies show that 3.2σ K/ π separation at 20GeV/c can be achieved with 1.2m track length
 - Preliminary mechanical design and FEA show the structure is stable, and global electronics scheme is reasonable
 - Fast electronics development is under progress. Preliminary tests validated the performance of the readout electronics and the feasibility of dN/dx method
- Further study plan
 - Detector prototyping and testing
 - Fine detector optimization
 - Optimize deep learning algorithm and FPGA implementation

Thanks for your attention

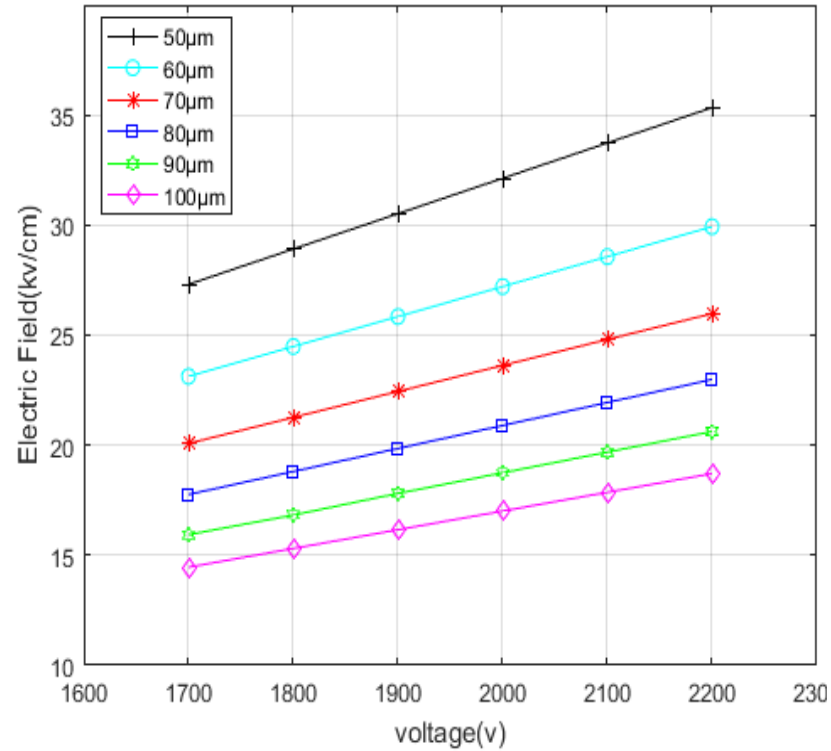
Backup

Garfield++ simulation

Gain vs HV



Electric field on the surface of field wires vs HV



Electric field on the surface of sense wires vs diameter of field wires

