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Design of COFFEE2: a pixel sensor prototype in 55nm high-voltage CMOS process

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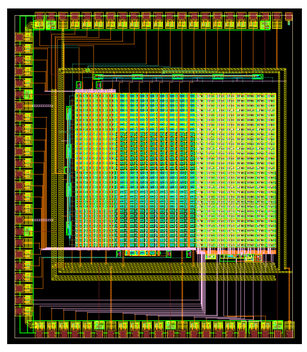
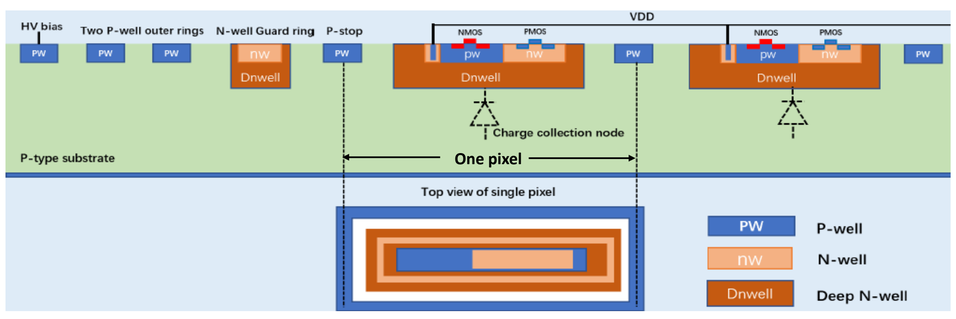
Introduction

To explore HV-CMOS processes with smaller design nodes and meet the requirements of the CEPC inner tracker, a series of chips named "COFFEE" is currently under development. This report presents the design and simulation results for COFFEE2 , which is the first prototype developed to verify the process and circuit module in SMIC High-voltage 55 nm technology. COFFEE2 features a small scale (2.2 × 2.7) mm^2 chip divided into (20 × 32) pixels with 3 variations of pixel design.



HV-55nm process

- Large electrodes: Dnwell-Psub junction as collection electrode
- Triple-well process: N-well/P-well/Deep n-well
- Low P-type substrate resistivity: 10 Ω·cm
- Guard ring: one inner N-well ring, with two P-well outer rings
- Substrate breakdown Voltage > 50V with frontside HV bias



COFFEE2 architecture & design

To quantitatively evaluate the "X-talk" issue of HV-CMOS pixel sensor technology in the new process and guide the overall design of the future detector chip, COFFEE2 includes both analog and digital readout pixel designs. The digital readout pixels incorporate two different comparator structures for comparative verification. The schematics are shown below, peripheral modules including bandgap, analogue buffer, DACs and row/column selection.

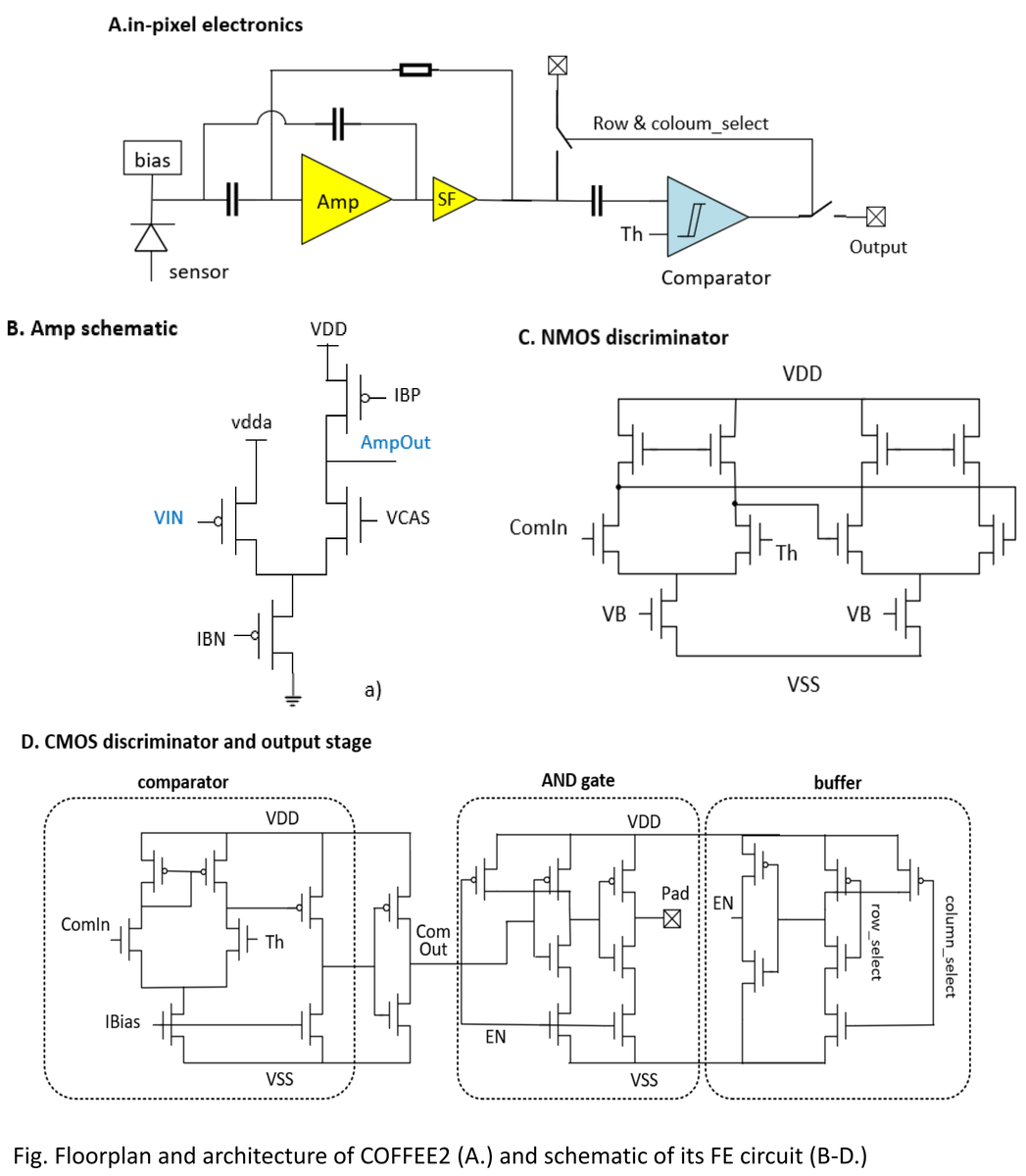


Fig. Floorplan and architecture of COFFEE2 (A.) and schematic of its FE circuit (B-D.)

Simulation results

CSA: noise and gain

Simulated noise and gain for preamplifier, as a function of detector capacitance. The estimated sensor capacitance, derived from TCAD for the three different pixel designs, ranges from 80 to 100 fF. Due to discrepancies between actual fabrication and simulation, also to provide a reference for future modifications, the simulation range has been expanded to 50-150 fF. The bias current is approximately 4.6 μA for the preamplifier.

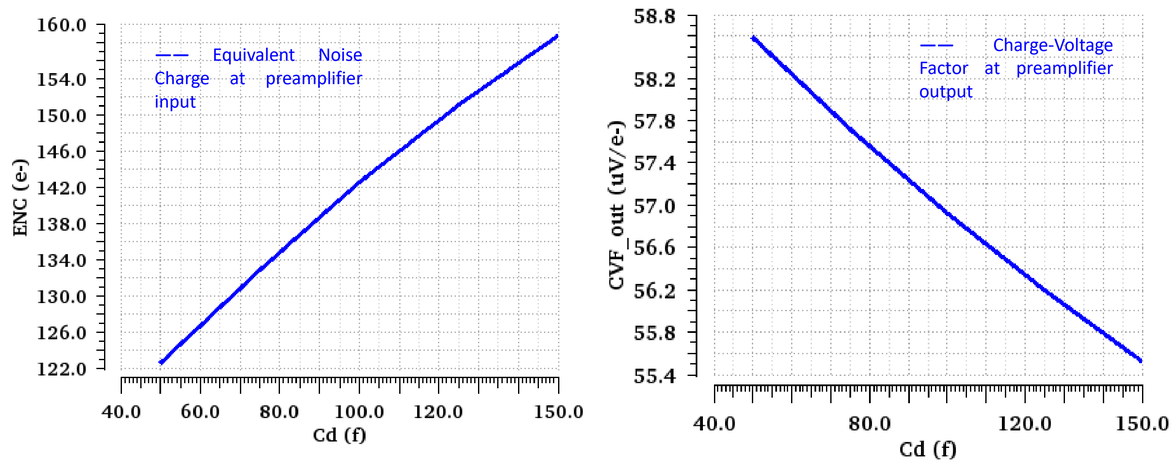


Fig. The input equivalent noise (ENC) of the preamplifier (left) and the gain in CVF (right)

CMOS/NMOS Comparator: time-walk

Figure shows the simulated waveforms of the comparator output (“ComOut”) and the CAS output (“PreAmp”), with the input charge ranging from 2k e− to 20k e−. The simulated time-walk of CMOS comparator is ~ 2 ns, for NMOS comparator has a larger value of ~ 9 ns. The bias current are ~ 15 μA and 8.5 μA, for the CMOS and NMOS comparator, respectively.

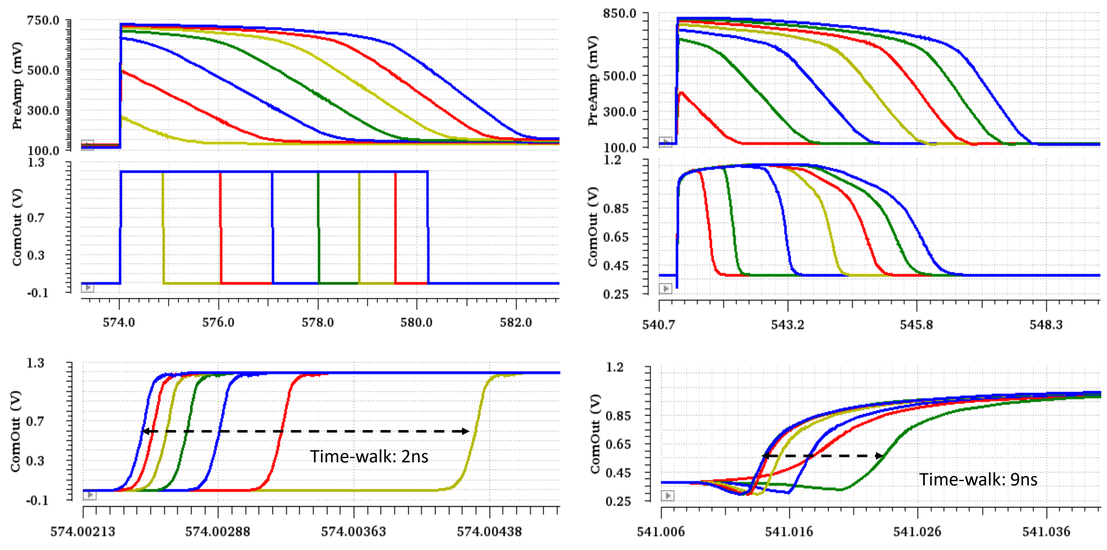


Fig. Simulated waveform of CMOS comparator (left) and NMOS comparator (right) output and time-walk

Summary & outlook

A pixel sensor prototype, COFFEE2, was designed using SMIC's 55 nm HV-CMOS technology to explore next-generation process nodes. COFFEE2 includes various in-pixel preamplifier and comparator designs. Simulations show the preamplifier’s gain and noise as functions of the input detector capacitance, while the time-walk for the two comparators is 2 ns and 9 ns, respectively, across a signal range from 2 ke^- to 20 ke^-. The testing and verification of the COFFEE2 chip are still ongoing, with preliminary test results in Zhiyu Xiang’s poster. The design of the next version, COFFEE3, is also underway, with the submission for fabrication planned for early next year.

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