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HVCMOS (COFFEE2) Design

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Sub-100nm processes are becoming a critical trend in the development of HV-CMOS pixel detector technology. To evaluate the impact of in-pixel electronics design on HV-CMOS pixel sensor performance at these advanced process nodes, we have designed and submitted a prototype chip named COFFEE2, fabricated using a 55nm HV-CMOS process. This chip features a pixel array of 32 rows by 20 columns, divided into three regions, each with distinct in-pixel amplifier and comparator structures. Additionally, the chip includes a bandgap reference, row/column configurations, and digital-to-analog converters (DACs) integrated into the peripheral circuitry surrounding the pixel matrix. We will present detailed electronic designs, simulation results, and preliminary test results.

Primary author: 李, 乐怡 (中国科学院高能物理研究所（IHEP）)

Presenter: 李, 乐怡 (中国科学院高能物理研究所（IHEP）)

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