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TCAD Simulations of HV-CMOS

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Abstract

Technology Computer-Aided Design (TCAD) simulations were conducted on High Voltage CMOS (HV-CMOS) sensors with varying substrate resistivities. The simulations investigated how changes in substrate resistivity affect leakage current, breakdown voltage, the depletion region, and the distribution of high electric field areas within the sensor. The effects of pixel gap and p-stop on capacitance were evaluated, with simulation results agreeing with experimental measurements. Furthermore, Allpix2 simulations provided insights into the sensor's response to Minimum Ionizing Particles (MIPs), facilitating an analysis of signal collection and charge sharing phenomena across different substrate resistivities.

Structure of HV-CMOS (COFFEE2)

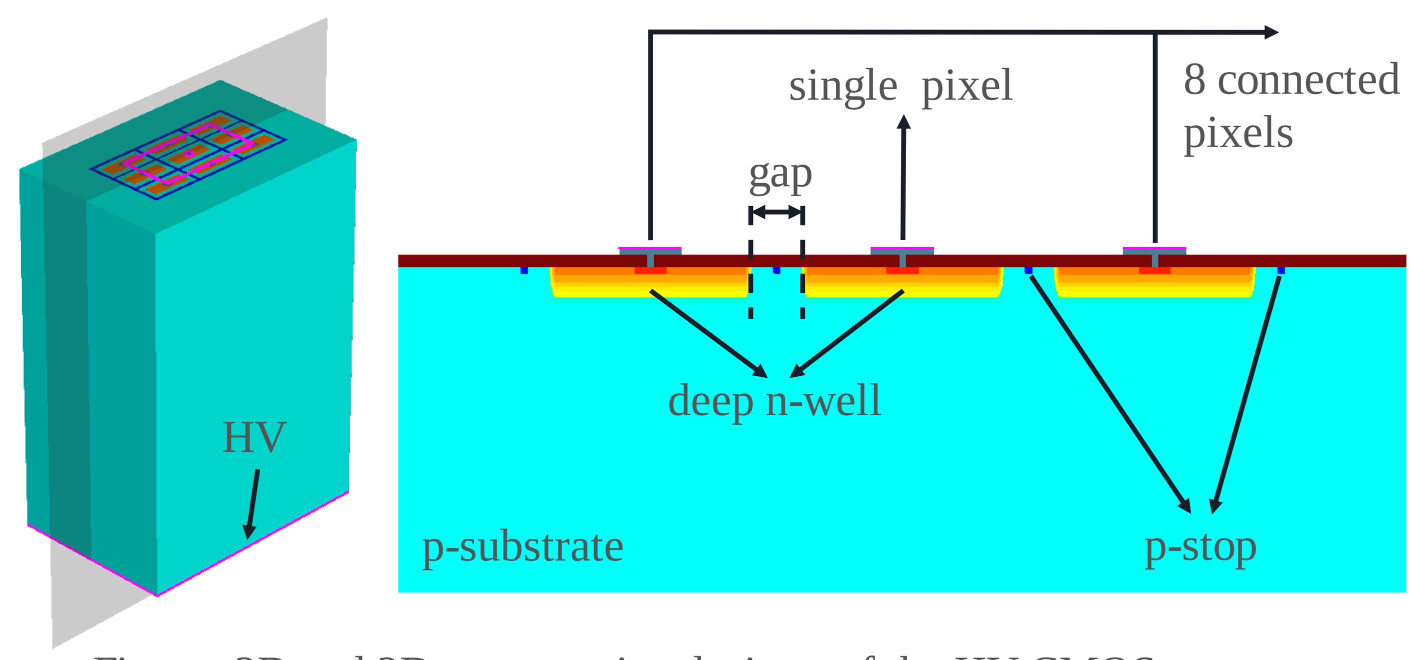

Figure: 3D and 2D cross-sectional views of the HV-CMOS structure.

- **gap**: 10/20/30 μm
- **p-substrate**
  Resistivity: 10/100/500/1000/2000 Ωcm
  Depth: 500 μm
- **deep n-well**
  Gauss profile: $5*10^{17} \sim 1*10^{17}$ cm^{-3}
  Depth: 5 μm
- **p-stop isolation**
  Concentration: $1*10^{19}$ cm^{-3}
  Depth: 2 μm

A simplified three-dimensional structure based on COFFEE2 (CMOS sensOrs in Fifty-FivE nanometer procEss) is simulated with varying substrate resistivities. The diode configurations include 3 gap sizes and the presence or absence of p-stop between pixels. The 8 peripheral pixels are connected in parallel for output, with HV bias applied from the bottom in the simulations.

Depletion Depth and Breakdowm Voltage

Resistivity (Ωcm) / N_A (cm^{-3})	10	100	500	1000	2000
HV (V)	1.36e15	1.33e14	2.66e13	1.33e13	6.64e12
-10	3.0	9.0	16.1	21.3	35.6
-50	6.1	19.2	37.6	53.8	76.8
-100	--	31.3	55.7	77.2	100.3
-200	--	--	--	100.3	147.1

Table: Depletion depth (μm) for varying substrate resistivities and voltages.

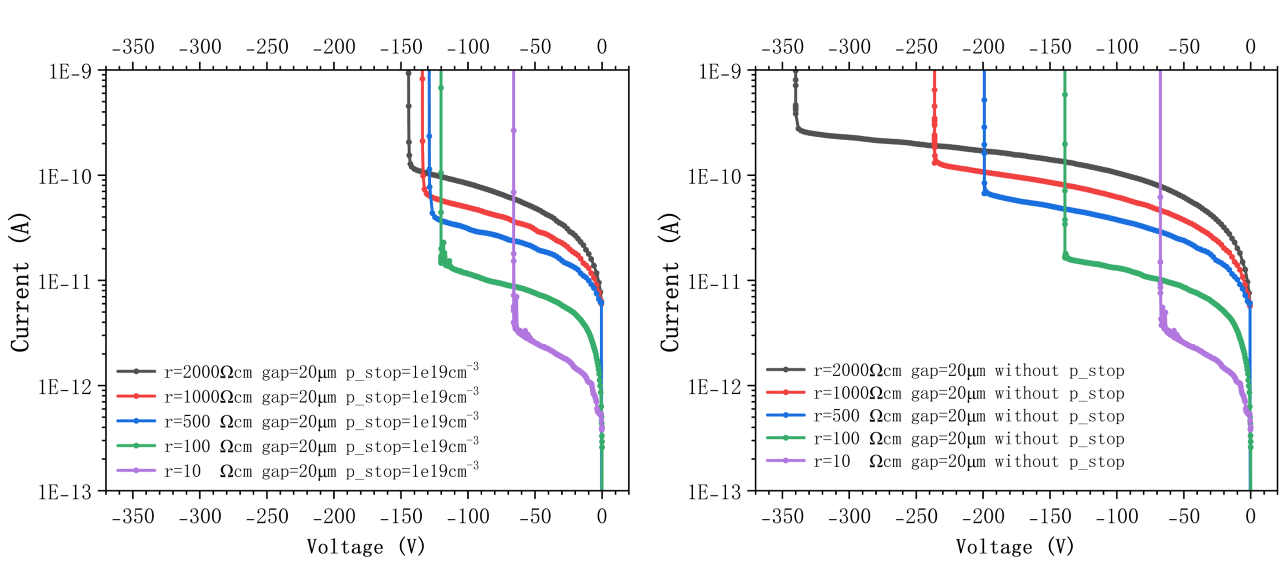

Figure: IV curves for varying resistivities, with and without p-stop.

The Depletion region depth generally follows the formula $D \propto \sqrt{V_{bias}\frac{N_A+N_D}{N_A \cdot N_D}}$. The IV curves indicates that increasing resistivity results in higher leakage current and breakdown voltage. Since this simplified model lacks complete structures like guard rings, the presence of p-stop may cause an earlier breakdown voltage.

Effects of Gap and P-stop on Capacitance

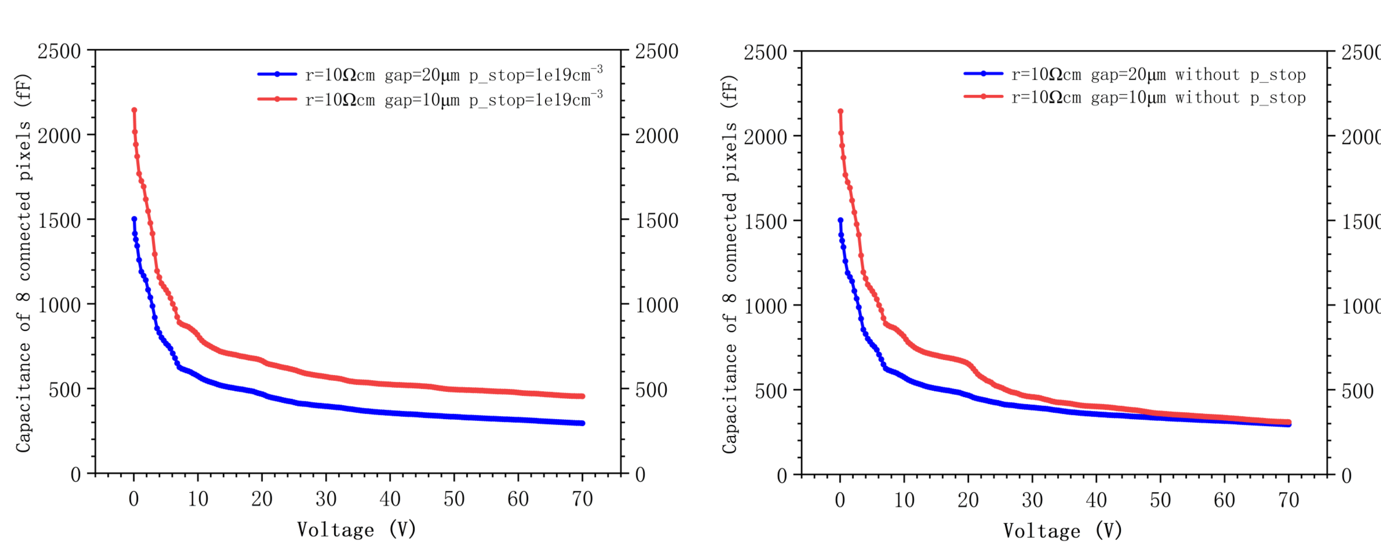

Figure: CV curves for r = 10 Ω·cm, gap = 10/20 μm, with and without p-stop.

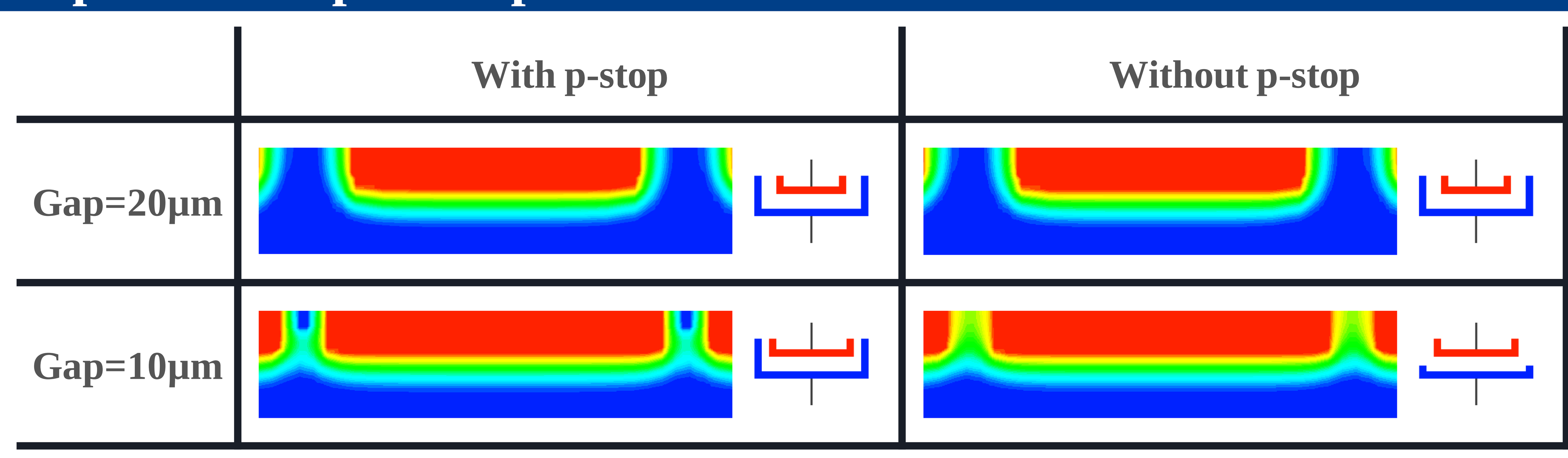

Figure: Electric potential diagram for gap sizes 10/20 μm, with and without p-stop, at HV = -70 V

The figures above are based on a substrate resistivity of 10 Ω·cm. At low bias voltages, pixels with smaller gaps have greater bottom and side areas of the DNW, resulting in higher capacitance, unaffected by p-stop. However, as bias voltage increases and the depletion region extends into the adjacent pixel, p-stop prevents a decrease in side capacitance, leading to a higher capacitance than pixels without p-stop.

MIP Test and Charge Sharing Simulation

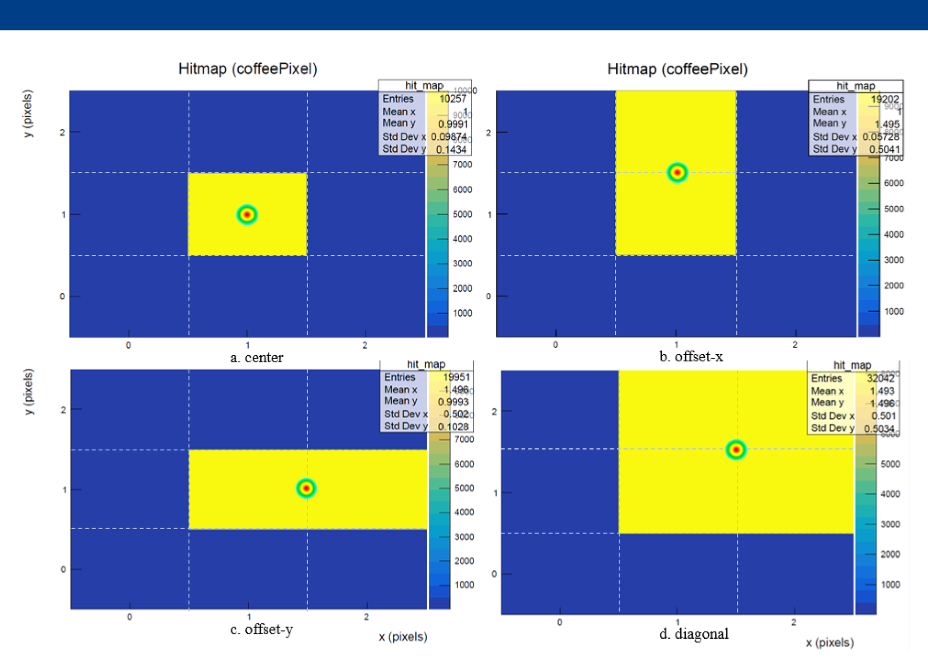

Figure: Hitmap at 4 different incident positions.

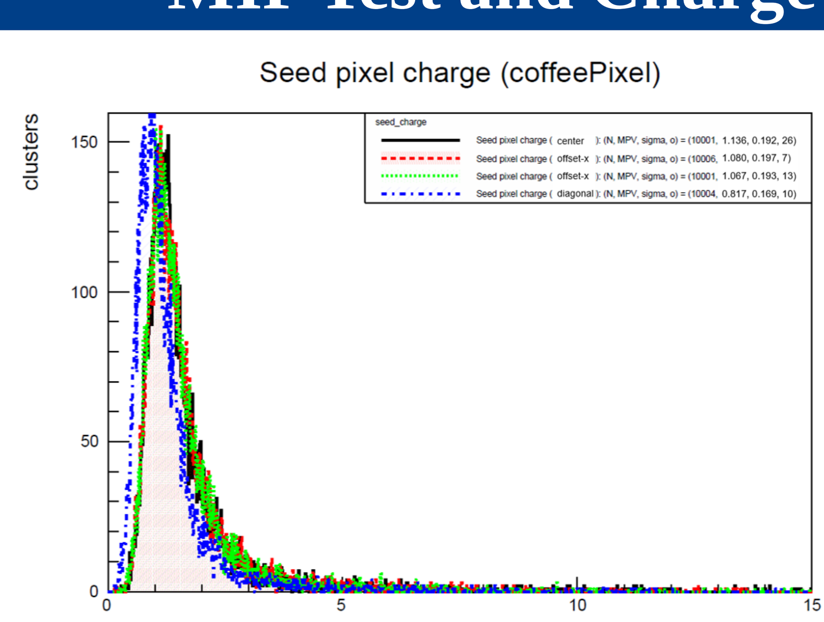

Figure: Distribution of the seed pixel signal.

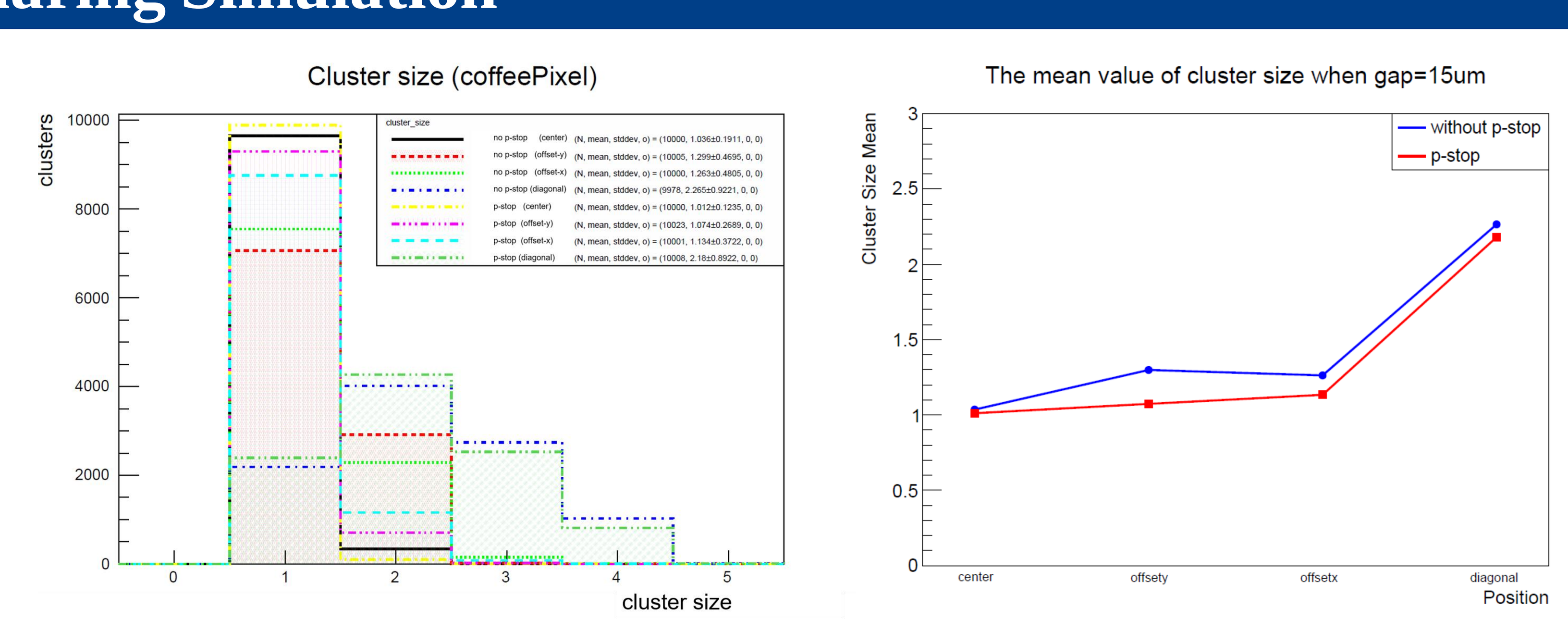

Figure: The distribution of cluster size at a threshold of 120 e-, and the mean value of cluster size.

A 3x3 pixel array on a 10 Ω·cm resistivity substrate (gap=15μm) is simulated by integrating a detailed TCAD electric field model into the Allpix2 framework. A 4 GeV proton beam (MIPs) incident on the array is modeled, and the seed pixel signal for different impact positions (center, offset-x, offset-y, diagonal) is shown. The MPV of the Landau distribution ranges from 0.8 to 1.1 ke-. The cluster size is approximately 1 for center incidence, reaching 2.3 for diagonal incidence. The average cluster size indicates that the p-stop structure effectively reduces charge sharing.

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