Test of HVCMOS sensor using 55nm process [1]
(Poster 21)

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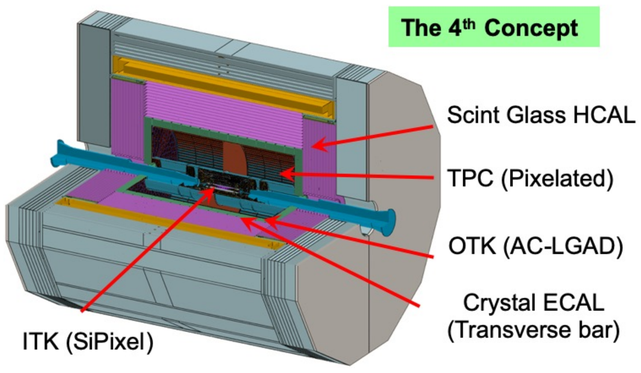
1 Introduction

CEPC plans to utilize a large-area and economic silicon-based tracker to achieve exceptional spatial resolution.

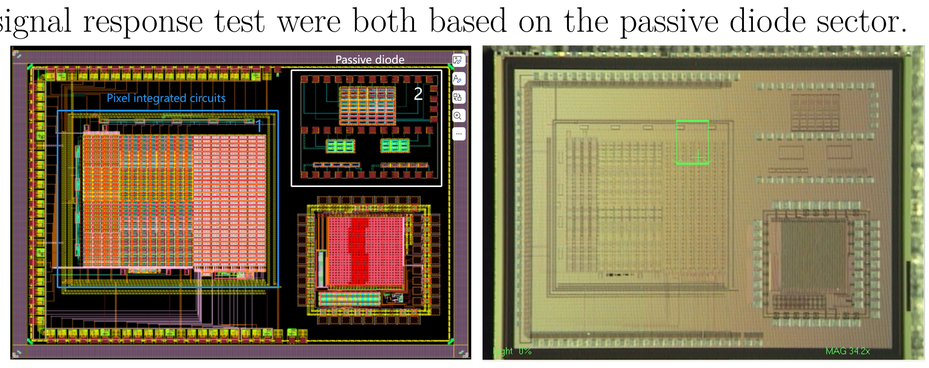


The CEPC tracking system conceptual design.

CMOS technology presents an appealing solution due to its high performance and cost-effectiveness. The commercially available high resistance wafer based High Voltage CMOS (HVCMOS) is intrinsically radiation hard and has large capacitance for signal acquisition, it has been used in such as Mu3e or ATLASPix. Current research and development mainly focus on 150/180nm processes while 55nm helps integrate more functions and reduce power consumption within the same pixel area.

2 COFFEE2 chip

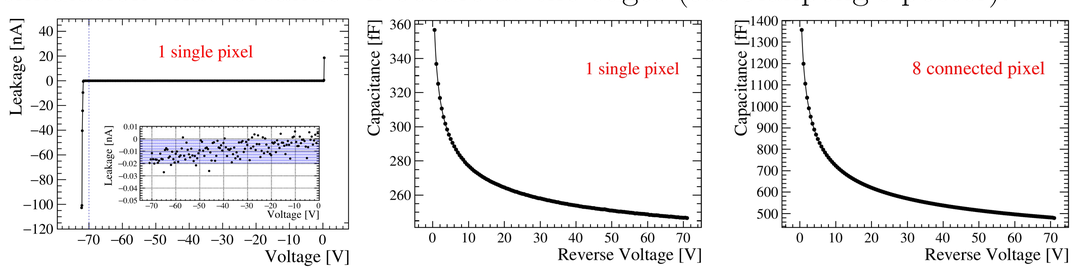
The CMOS sensOr in Fifty-FivE nm procEss (COFFEE) has been designed and evolved. COFFEE2 chip, size of 4×3 mm^2, consists of a passive array sector and a pixel array (40×80 μm^2 for each pixel) with integrated circuits. Though the high resistance substrate was not yet available, the pixel array is already a true verification of the complete structure. The analog amplifier, switch circuit and variant diode structures were integrated in sector 1 while sector 2 only contains passive diode. The following IV/CV and signal response test were both based on the passive diode sector.



The layout of design (left) and photo (right) of COFFEE2 chip

3 IV/CV test

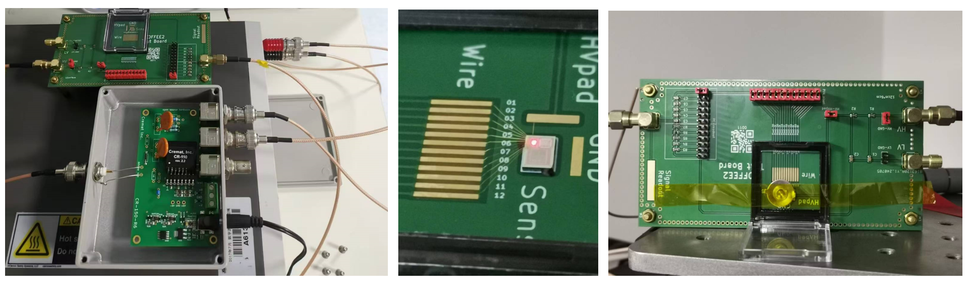
For COFFEE2 chip, the IV test results show very good diode behavior with low leakage $\sim$ 10 pA for different pixel array. Clear positive conduction and gradually reverse breakdown begins as voltage increases to 70V. Under the same voltage, the capacitance variation of 8 pixels array is 8 times that of a single pixel. Considering deducting parasitic parameters of metal routing wire, the capacitance of single pixel is about 30-50 fF. It is evident that the pixel have not been completely depleted and it can be inferred from the simulation that breakdown occurs at the edges (see Jianpeng's poster).



The typical IV result (left) and CV curves for single pixel (middle) and 8-pixel parallel structure (right)

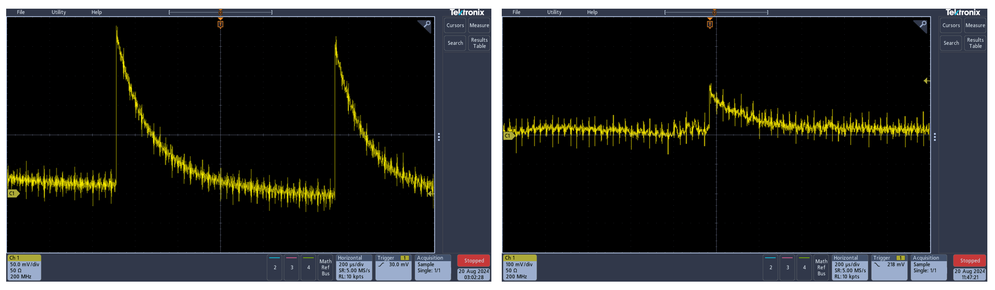
4 Signal response test

The signal response test was performed with laser or radioactive sources to verify the reliability of the COFFEE2 CMOS sensor with 55nm process. An external charge sensitive amplifier, with the gain of 1mV/fC, was used to test the passive diode array response to red laser ($\lambda \sim 650$nm) or radioactive sources (i.e. α, β source).



The setup for external CSA connect to COFFEE2 (left), the red laser focusing on chip (middle) and illuminate the chip with an α source

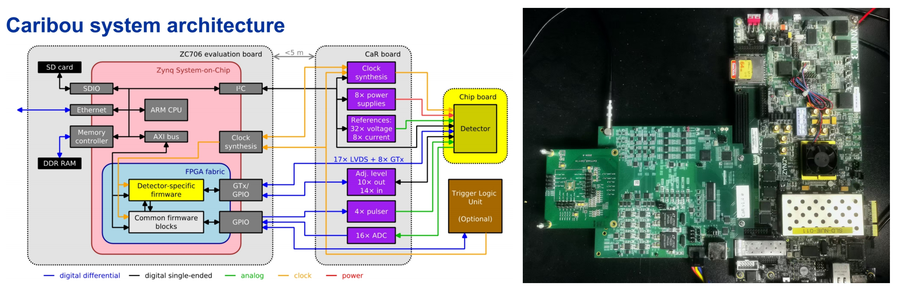
With the high voltage applied, the response of pixel array (54 pixels) to red laser is proportional to the magnitude of the high voltage. Under 70V, on average, each pixel is excited by 5fC charge due to red laser energy deposition. For α source, the signal response of pixel can reach up to 100fC due to the α complete deposition. The β and X-ray source also tried, ^{90}Sr and ^{55}Fe, but no clear signal was found at existing noise level. Due to the high noise level of the external amplifier, the pixel integrated amplifier will be used in the next to observe the signal.



Under 70V, the response of an array consisting of 54 pixels to red laser (left) and α source (right)

5 Circuit test

The ZC706 + Caribou boards form the circuit testing system and a dedicated carrier board is designed for COFFEE2 chip. The circuit test verified the expected digital circuit functionality (row-column gating and DAC unit), demonstrating the feasibility of the digital circuit design.



The Caribou system architecture (left) and the circuit test setup (right)

6 Summary & plan

Promising test results from CMOS chip using 55nm process indicate the possibility of future applications. For the verification of radiation resistance, nucleon beam in SNS, DESY or CERN can be chosen. The results of COFFEE2 testing provide important input for future chip design.

[1] Zhuojun Chen, Ruoshi Dong, Leyi Li, Yiming Li, Weiguo Lu, Yunpeng Lu, Ivan Peric, Jianchun Wang, Zhiyu Xiang, Kunyu Xie, Zijun Xu, Hui Zhang, Mei Zhao, Yang Zhou, Hongbo Zhu **and** Xiaoyu Zhu. "Feasibility study of CMOS sensors in 55 nm process for tracking". **in***Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*: 1069 (2024), **page** 169905. ISSN: 0168-9002. DOI: https://doi.org/10.1016/j.nima.2024.169905.