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Test of CMOS chip using 55nm process

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The CEPC plans to utilize a high spatial resolution, low-material, fast-readout, large-area, and cost-effective silicon-based tracker system. CMOS technology is a promising solution. Compared to hybrid silicon pixel sensors, CMOS processes enable smaller sensor sizes while maintaining a lower material budget. CMOS technology is also a potential candidate for future upgrades to other experiments, such as the LHCb Upstream Tracker.

Unlike many CMOS processes that require modifications to achieve sufficient signal generation, commercially available high-resistance wafer-based High Voltage CMOS (HVCMOS) is intrinsically radiation-hard and offers substantial capacitance for signal acquisition. While HVCMOS may have higher noise and power consumption compared to small-electrode CMOS, these factors are manageable for large-area trackers. Recent advancements in the HVCMOS production process at domestic foundries make it commercially customizable.

We will present promising test results from preliminary CMOS sensors, including those from the 55nm process (COFFEE), COFFEE1, and COFFEE2.

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