CMOS Strip Development for CEPC ITK

Xin Shi

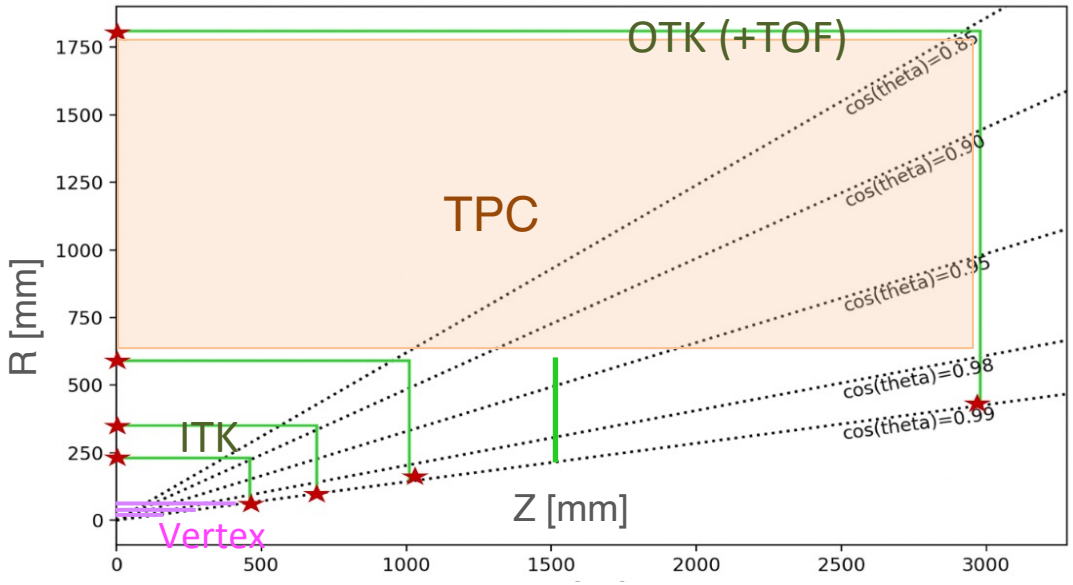
On behalf of CEPC Silicon Tracker Team

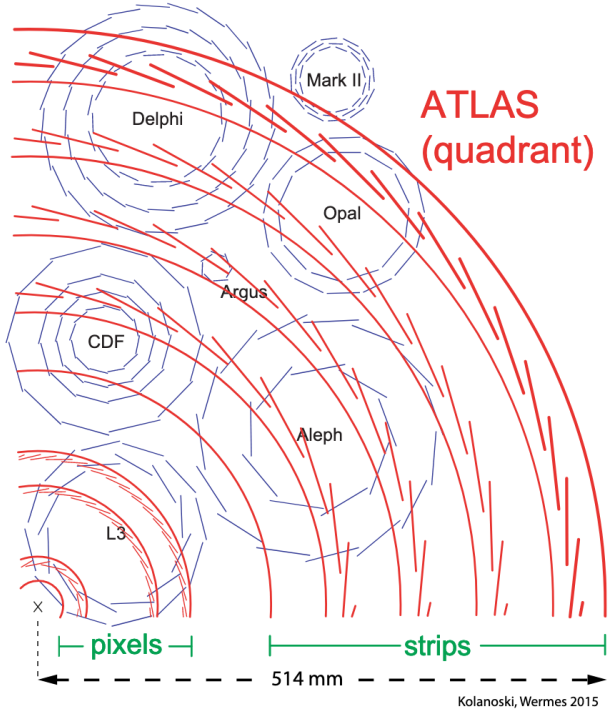
2024.10.24

2024 CEPC International Workshop

Why Strips for CEPC Inner Tracker?

- CEPC physics requirements impose technical challenges on silicon tracker
  - Spatial resolution $\sigma_\varphi < 10$ μm, $\sigma_z < 50$ μm (barrel) and $\sigma_z < 100$ μm (endcap)
  - Low material budget: < 1% X_0 per layer
  - A few nano-seconds timing resolution to tag 23 ns bunch crossing
  - Cost effective area to cover ~20 m^2

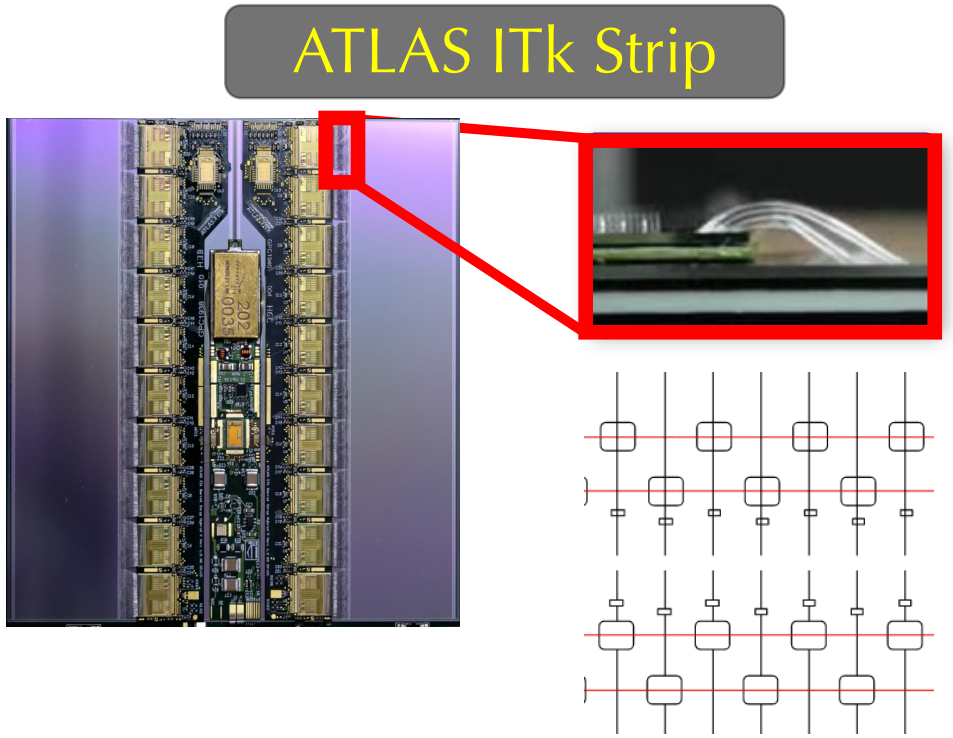




- Silicon strip is mature and widely used in HEP experiments
  - HERA, H1, ATLAS, CMS, ALICE, LHCb …
- Largely used for the HL-LHC upgrade
  - ATLAS ITk strip, CMS Outer Tracker …
- Rich experience on strip detector development at IHEP
  - Complete production facility and team members at IHEP
  - Experience in sensor, ASIC, strip module **construction,** and testing

Why CMOS Strip? (vs Hybrid silicon strip + ASICs)

- High spatial resolution impose challenging pitch size for strip detector design and fabrication
  - Less than 30 μm pitch to reach <10 μm spatial resolution
  - Wire bonding will be a nightmare
  - ATLAS ITk Strip: 4 layers of wires / chip
- CMOS Strip can combine active detection layer and readout electronics into a single structure
  - no wire bonding for each channel
  - Industrial standard to reduce cost eventually
  - ATLAS ITk strip: all in one company > 3 years production of strip sensors

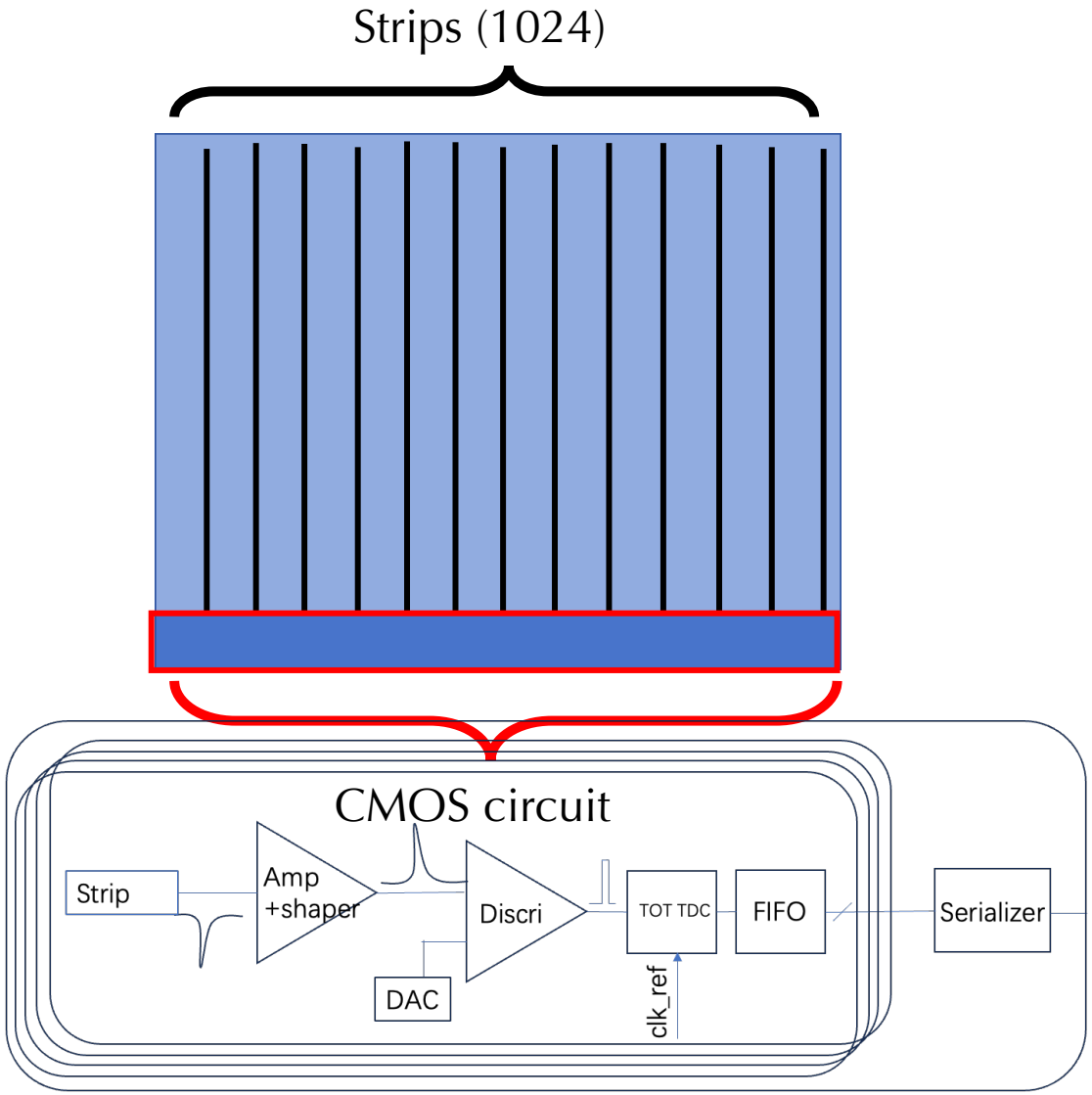


Complicated bonding structure

- 4 layers of wires / chip
- 5k wire bonds / module

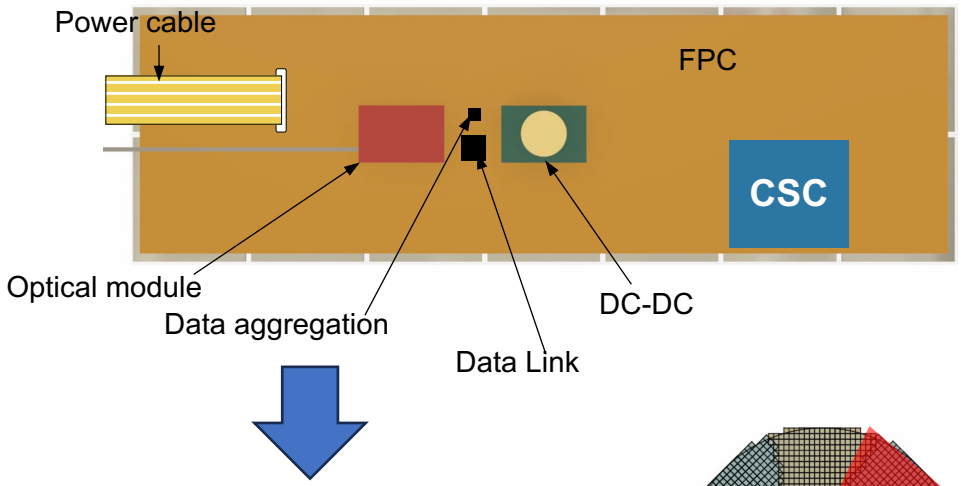
CMOS Strip Chip - CSC

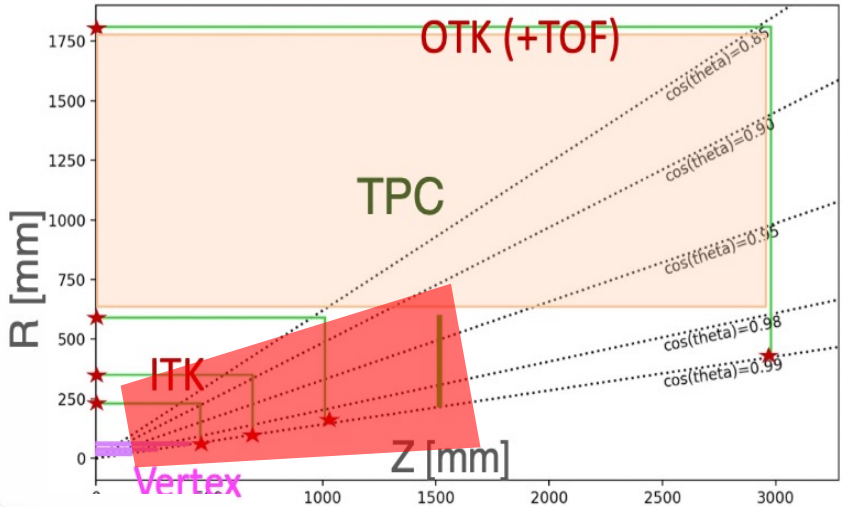
Version 1.3

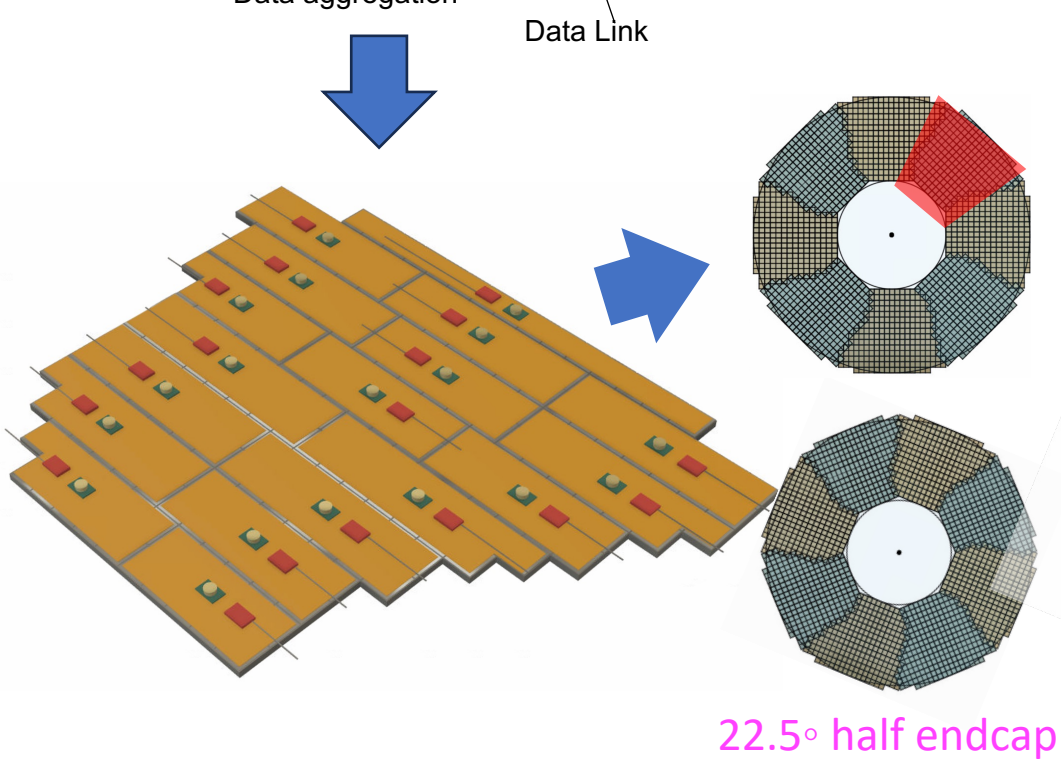


CSC Parameters	
Strip width	10 μm
Strip pitch	20 μm
Strip number / chip	1,024
Chip size	2.1×2.3 cm^2 (active area: 2.05 cm x2.05 cm)
Spatial resolution	σ~5 μm
Time resolution	~3 ns
Power consumption	~80 mW/cm^2
Data size per hit	32 bits (10b BXID, 10b address, 6b TOT + other 6 bits)
Event rate / chip	Maximum ~0.25 Gbps (CEPC Endcap note)
LV / HV	1.8 V / 200 V
Wafer resistivity	2k Ω cm
Technology Node	180 nm

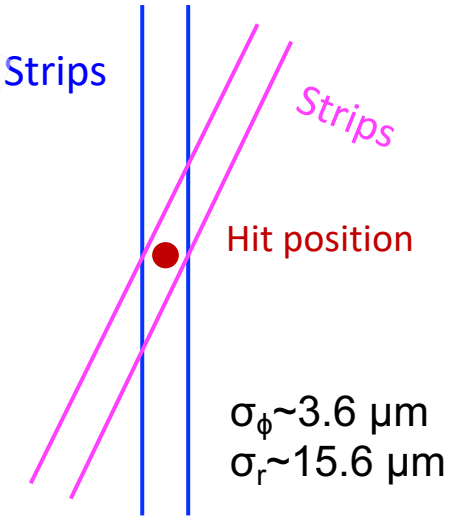
CEPC ITK Endcap Design – CMOS Strips







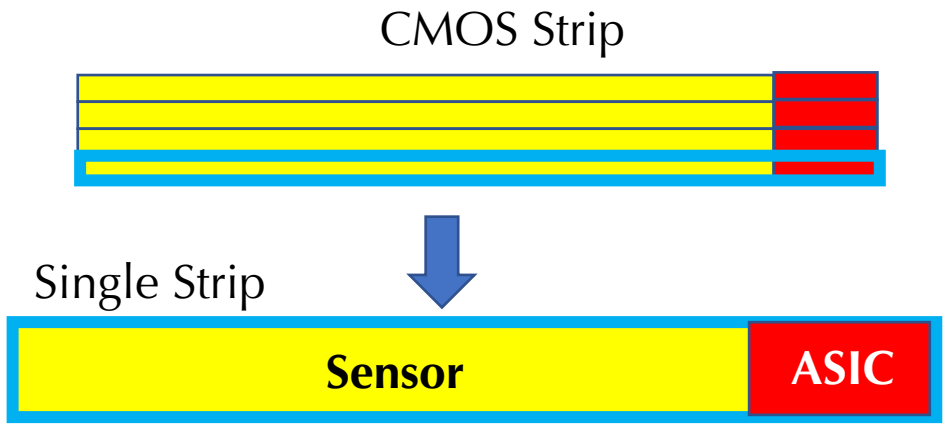
22.5◦ half endcap



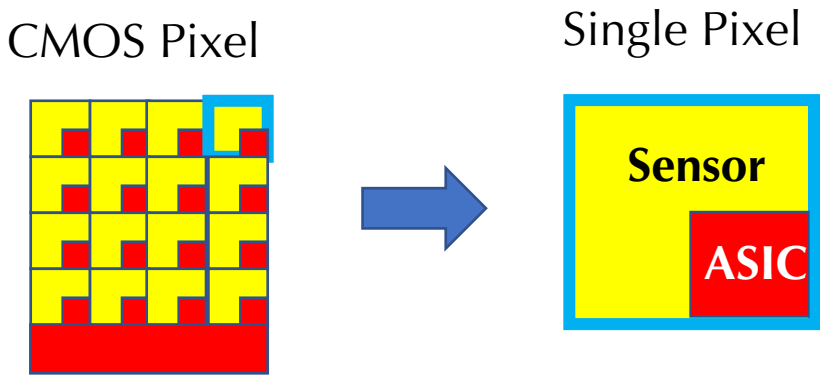
σ_ϕ~3.6 μm
σ_r~15.6 μm

CMOS Strip Chip – Basic Concept

- CMOS **strip** is different than CMOS **pixel**



- Pros: simple readout / ASIC only located at the end of strip / facilitate the design of ASIC / negligible interference between sensors and ASIC
- Cons: large capacitance of strip sensor

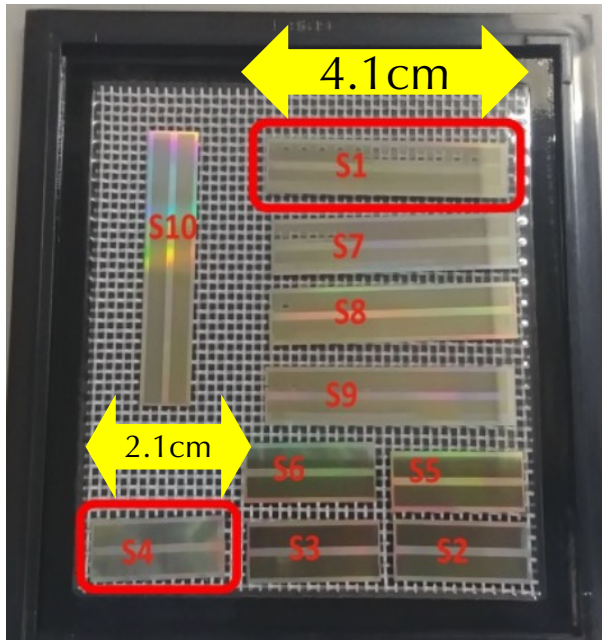


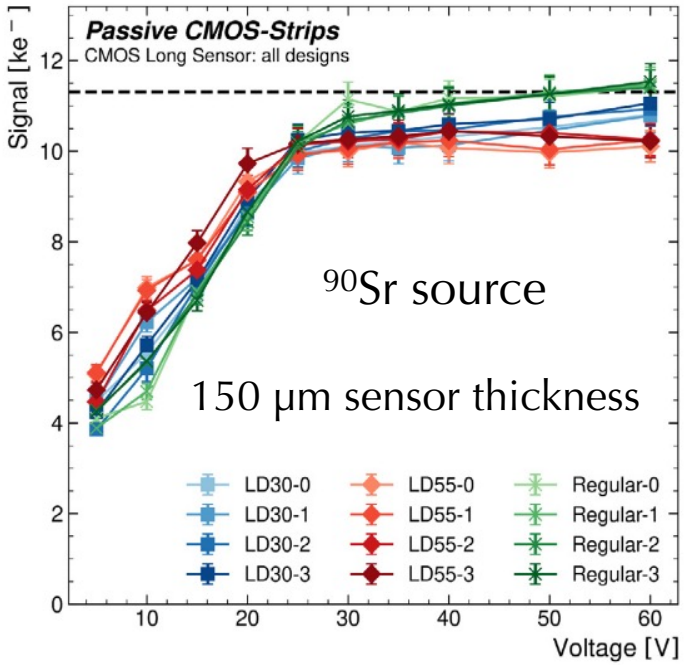
- Pros: small capacitance of sensor
- Cons: ASICs and sensors share same area with interference between sensor and ASIC

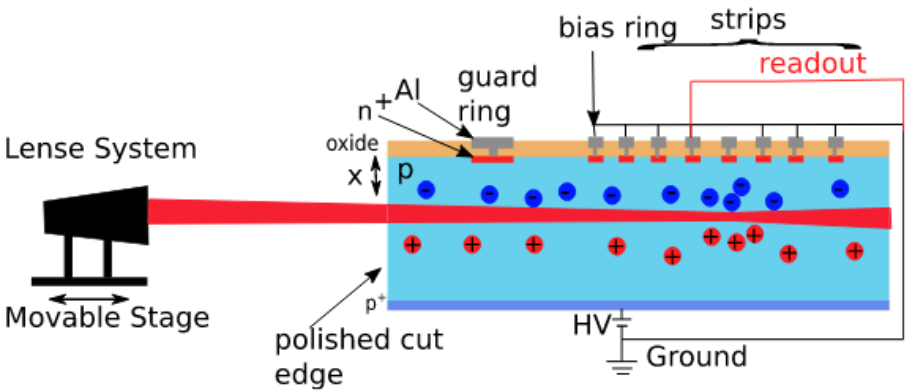
Existing passive CMOS sensor

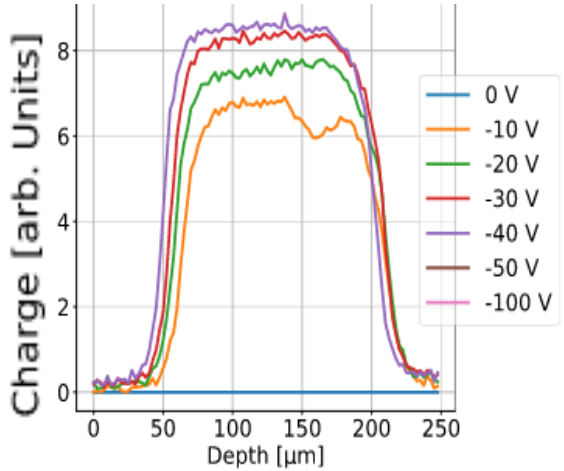
Diehl et. al, Characterization of passive CMOS strip sensors, NIMA 1033 (2022) 166671

- First large sized CMOS passive sensor (> 4 cm)
  - 75.5µm pitch on 6-inch, 3-5 kΩ wafer with LFoundary 150 nm
- Successfully tested of strip sensor behavior
- Confirmed feasibility of CMOS strip sensor path
- Passive CMOS without ASIC design, no integrated chip yet



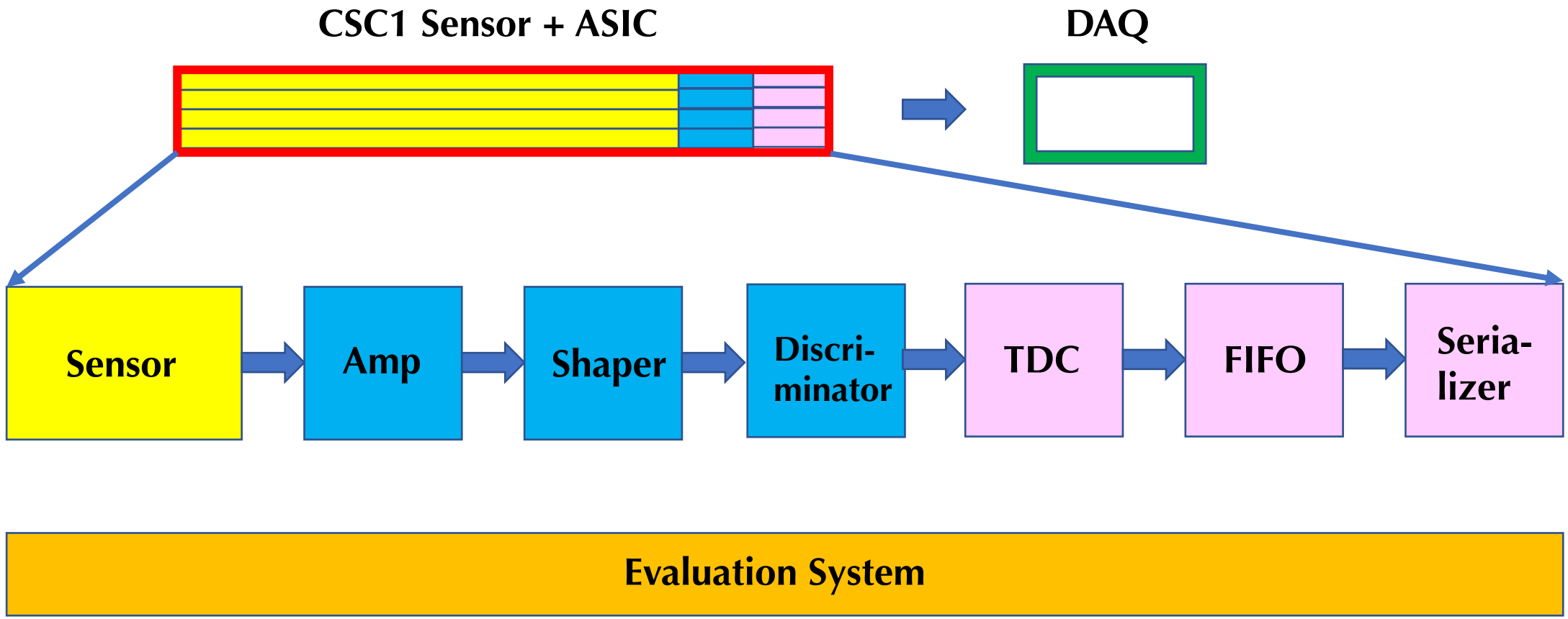






- CSC Target: 20 µm pitch, 2cm sensor + ASIC , 2kΩ, 180 nm

CSC1 Design Diagram



CSC Participating Institutes

CONVe-YI

北京科维泰信科技有限公司

IFT

山东高等技术研究院

SHANDONG INSTITUTE OF ADVANCED TECHNOLOGY

中国科学院微电子研究所

INSTITUTE OF MICROELECTRONICS OF THE CHINESE ACADEMY OF SCIENCES

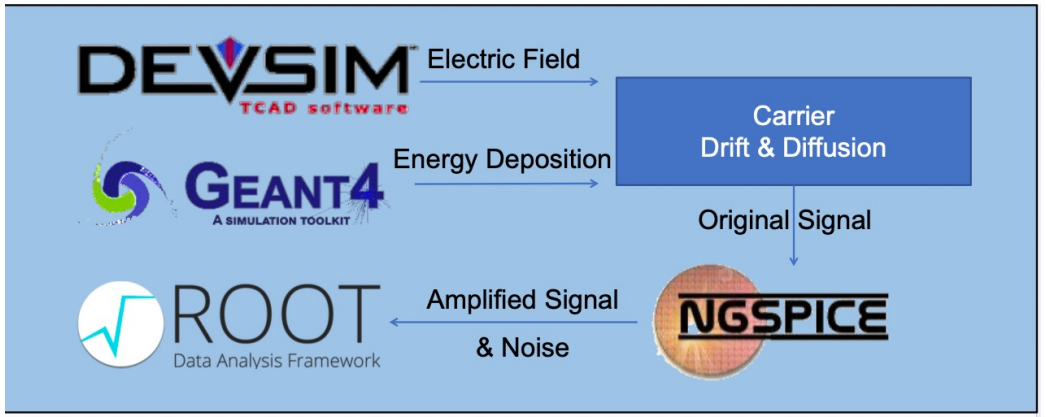
张江实验室

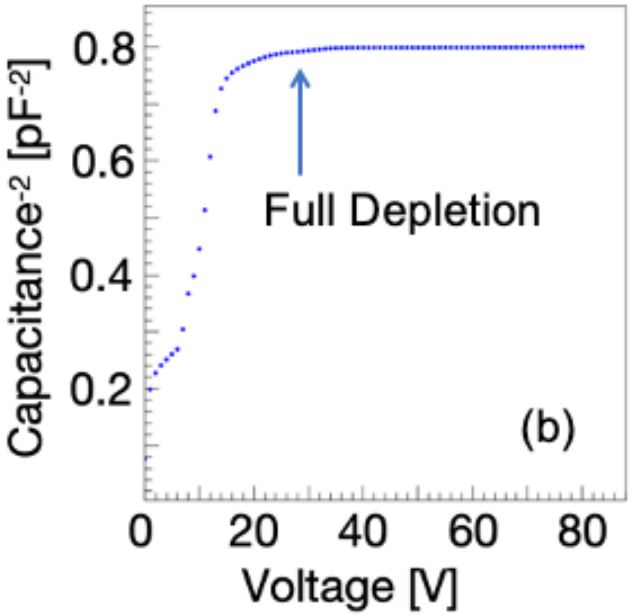
ZHANGJIANG LABORATORY

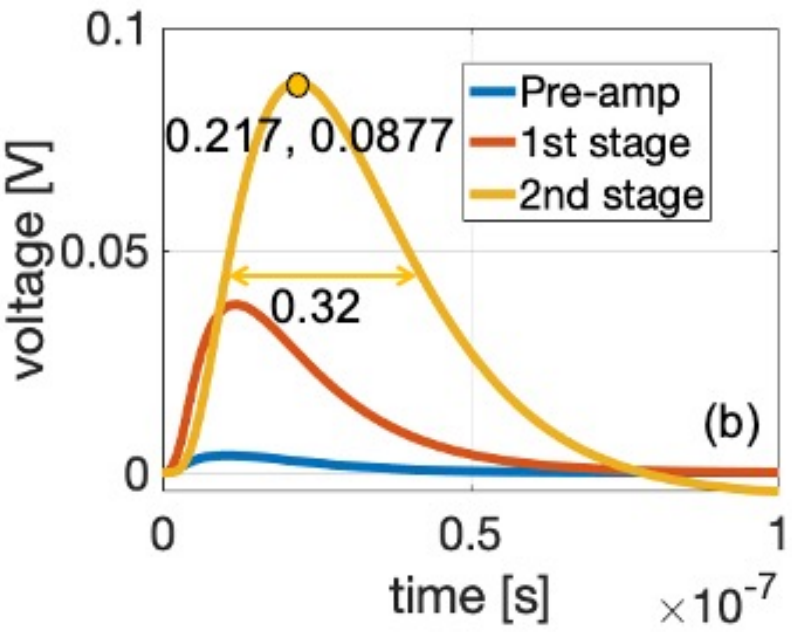
- All institutes are members of RASER Team

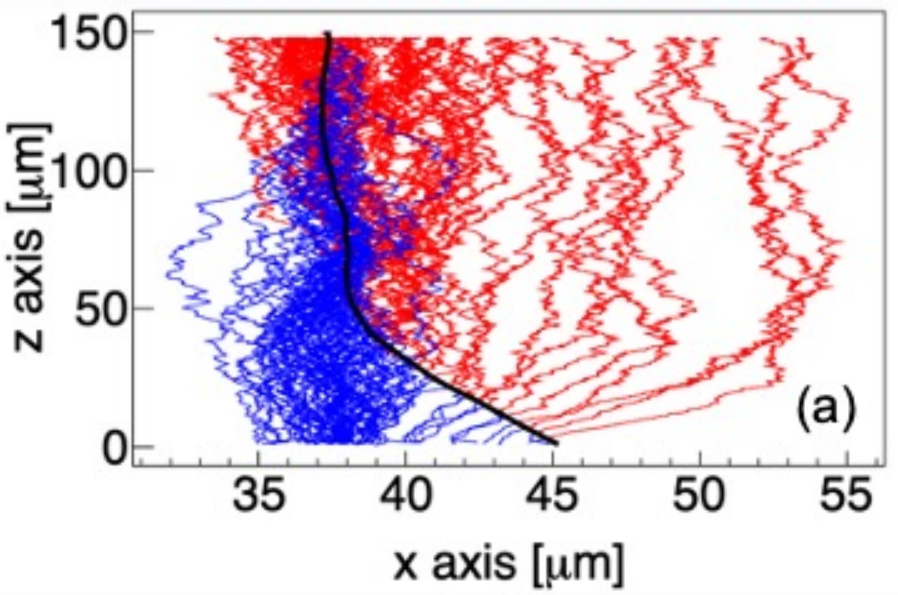
CSC Simulation with open source RASER

- Simulation based on RASER code [1]
- CMOS sensor / electronics / response to laser and MIP





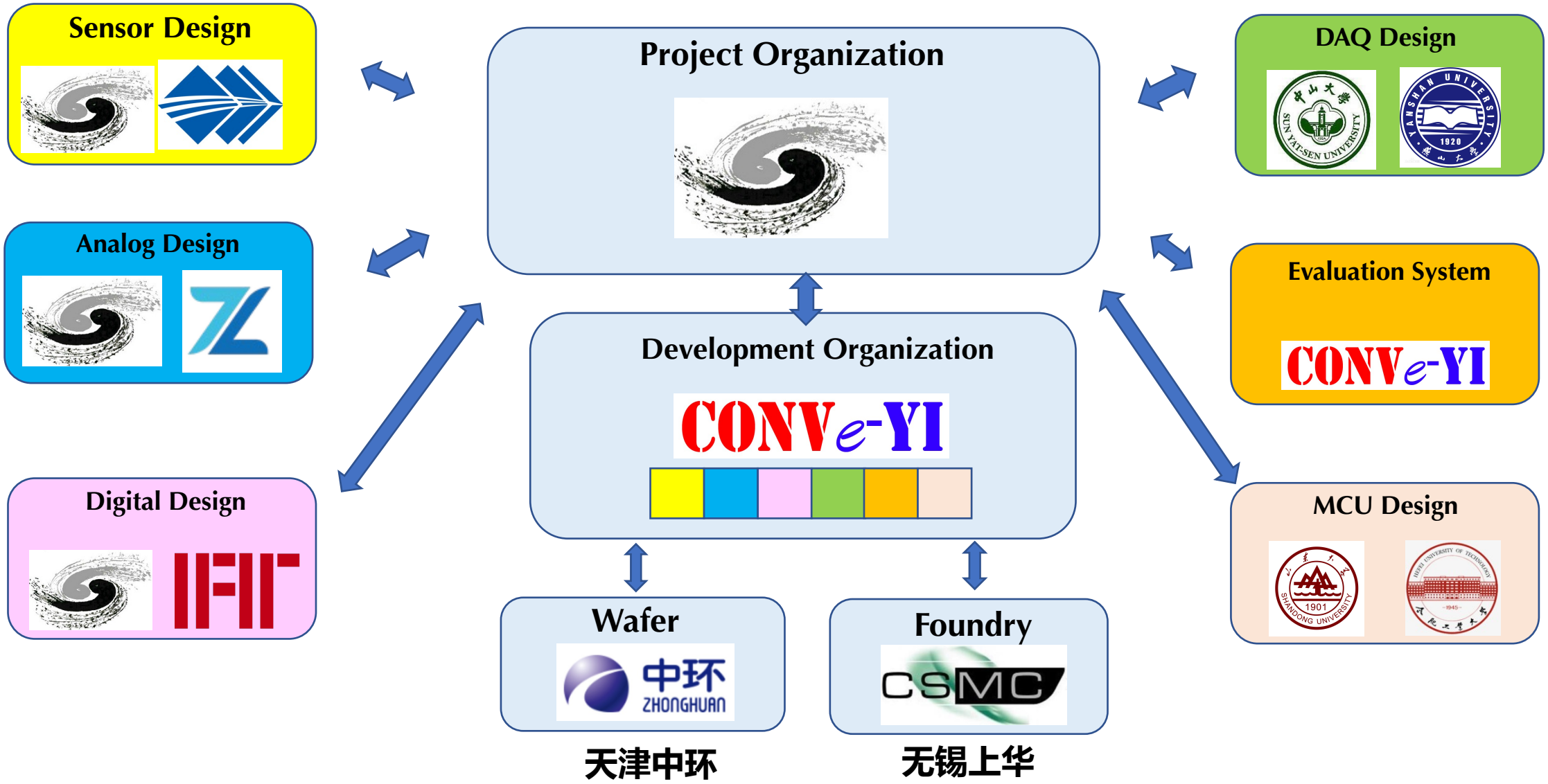




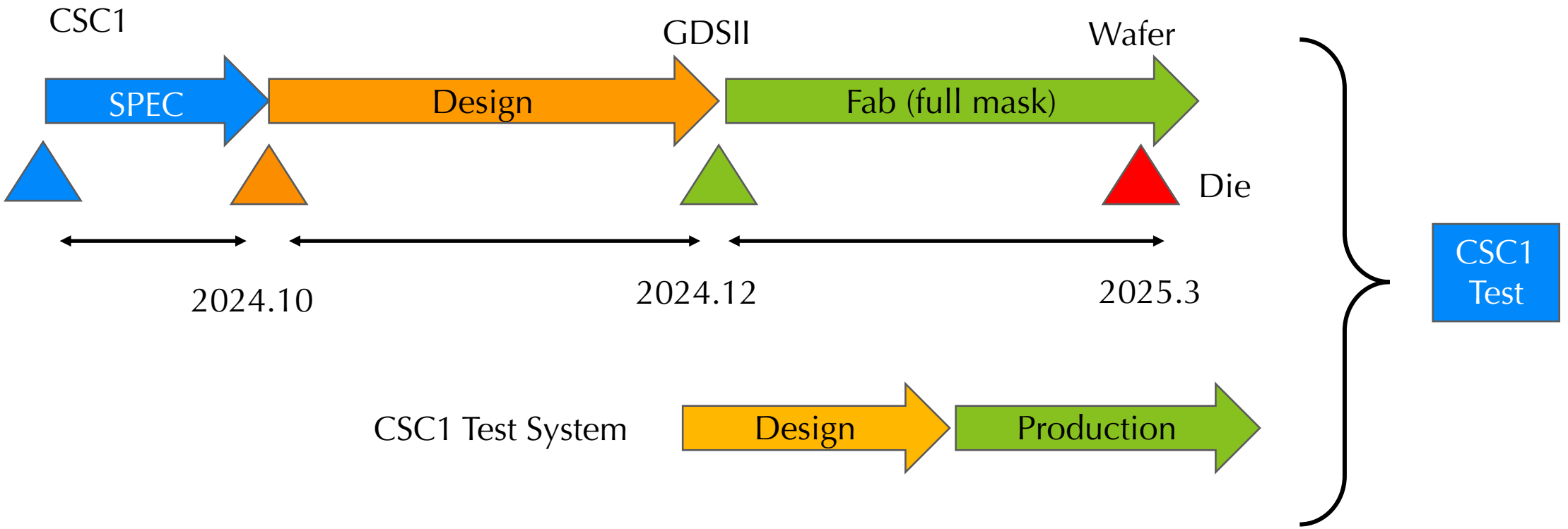
[1] https://pypi.org/project/raser/

Please see C. Fu and S. Zhao's Poster (ID 43) for more detail.

CSC Developer Orgnization

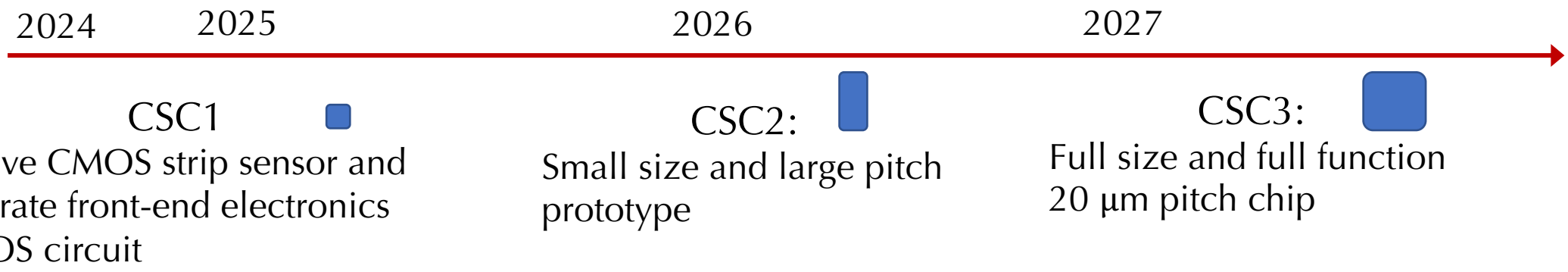


Timeline for CSC1



Summary and Plan

- Hybrid silicon strip is mature and widely used technology in HEP experiment.
- Our target is to develop CMOS strip, which integrates active detection layer and readout electronics into a single chip to achieve ultimate spatial resolution better than **5 μm**.
- CEPC ITK choose CMOS Strip as one baseline for endcap.
- CMOS Strip Chip (CSC) development is steadily progressing.



Welcome to join us!

中国科学院高能物理研究所

Institute of High Energy Physics
Chinese Academy of Sciences