Introduction on ATLAS Phase-II Global Trigger and GCM design

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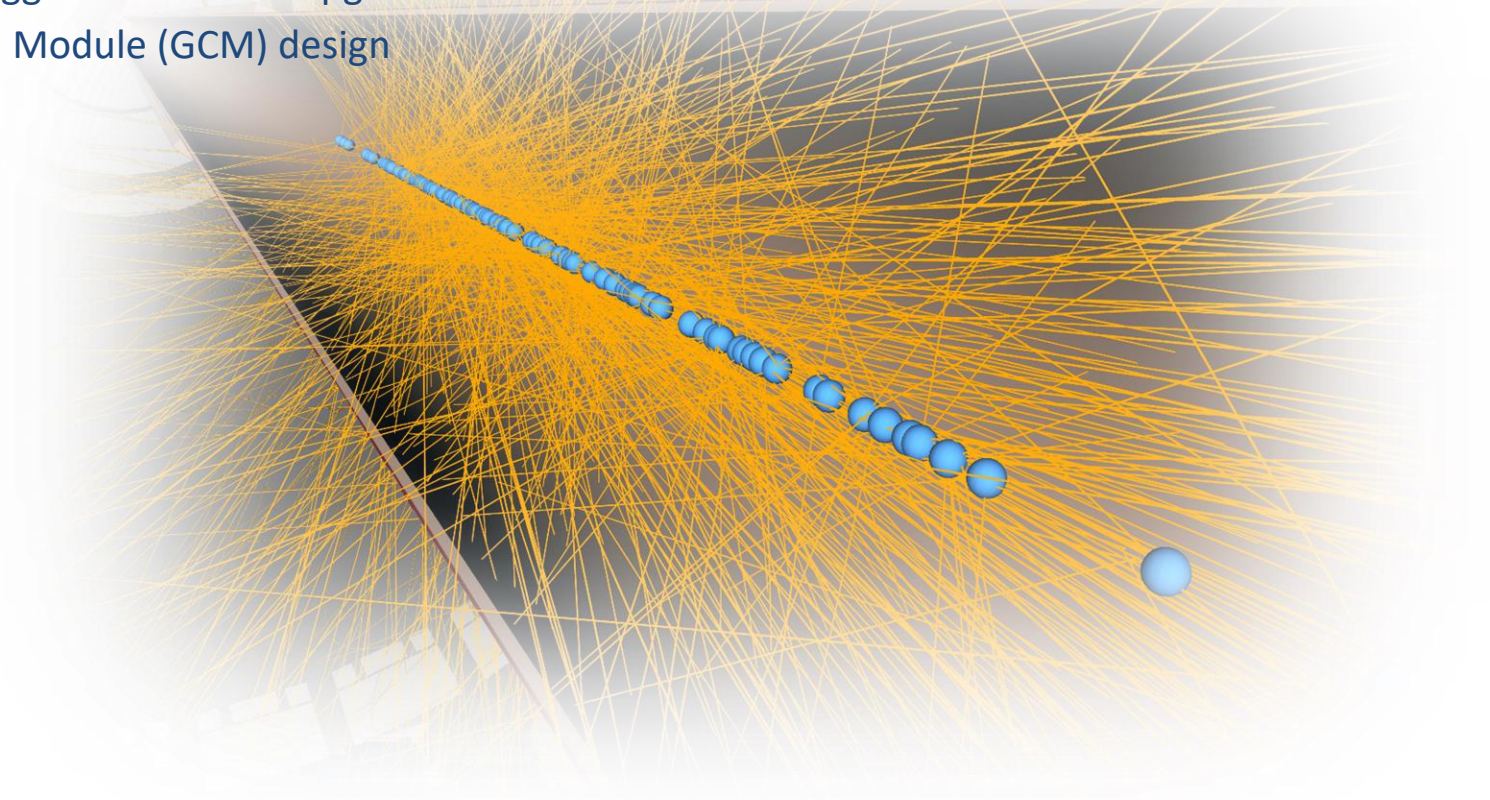
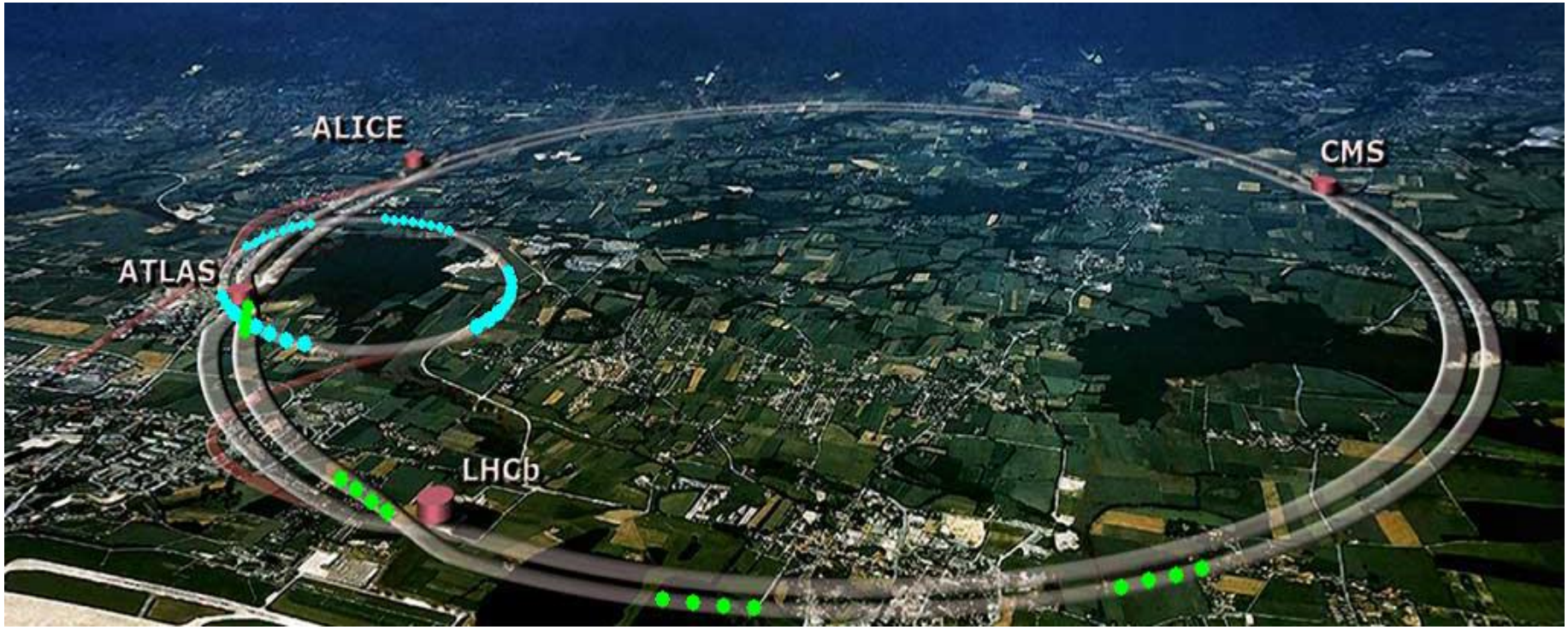
Outline

- Brief introduction on LHC and ATLAS
- Brief introduction on Trigger concept
- ATLAS Global Trigger for Phase-II Upgrade
- Global Common Module (GCM) design
- Summary



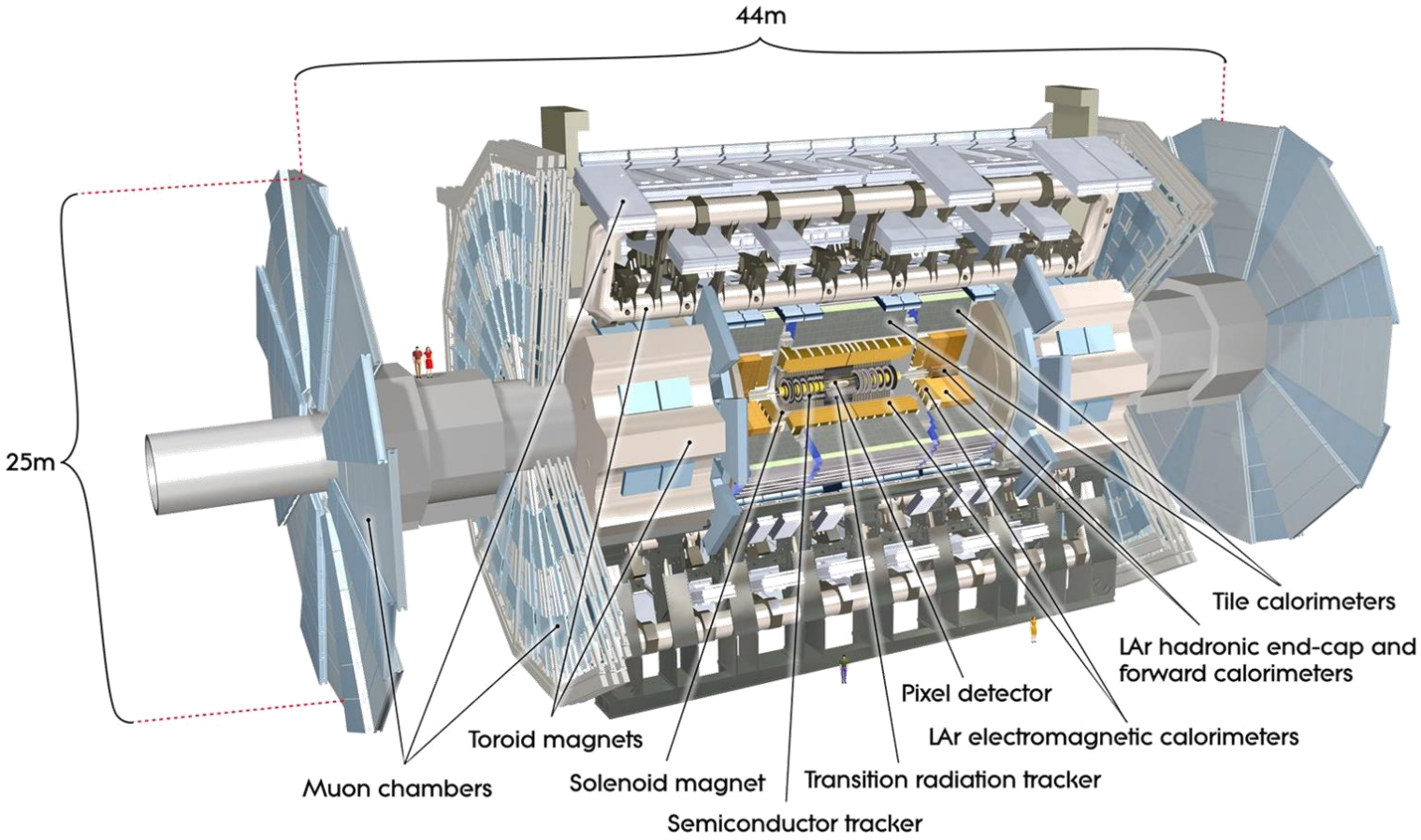
Large Hardon Collider

- Circumference ~27km
- Nominal energy, protons 7 Tev, 99.9999991% of *c*
- Magnetic dipole field 8.3T, 100,000 times of earth's



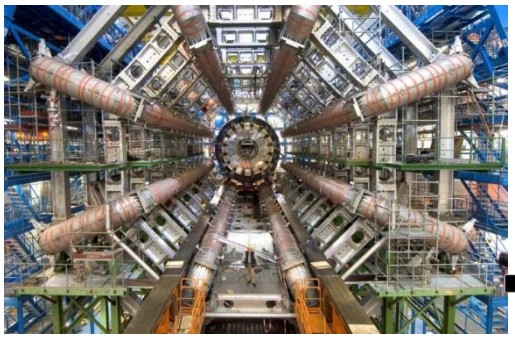
A Toroidal LHC ApparatuS

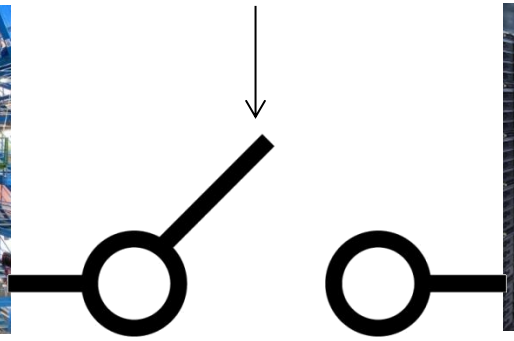
- ~180 institutes, >3000 authors
- Total detector channels ~100,000,000



ATLAS data volume and trigger

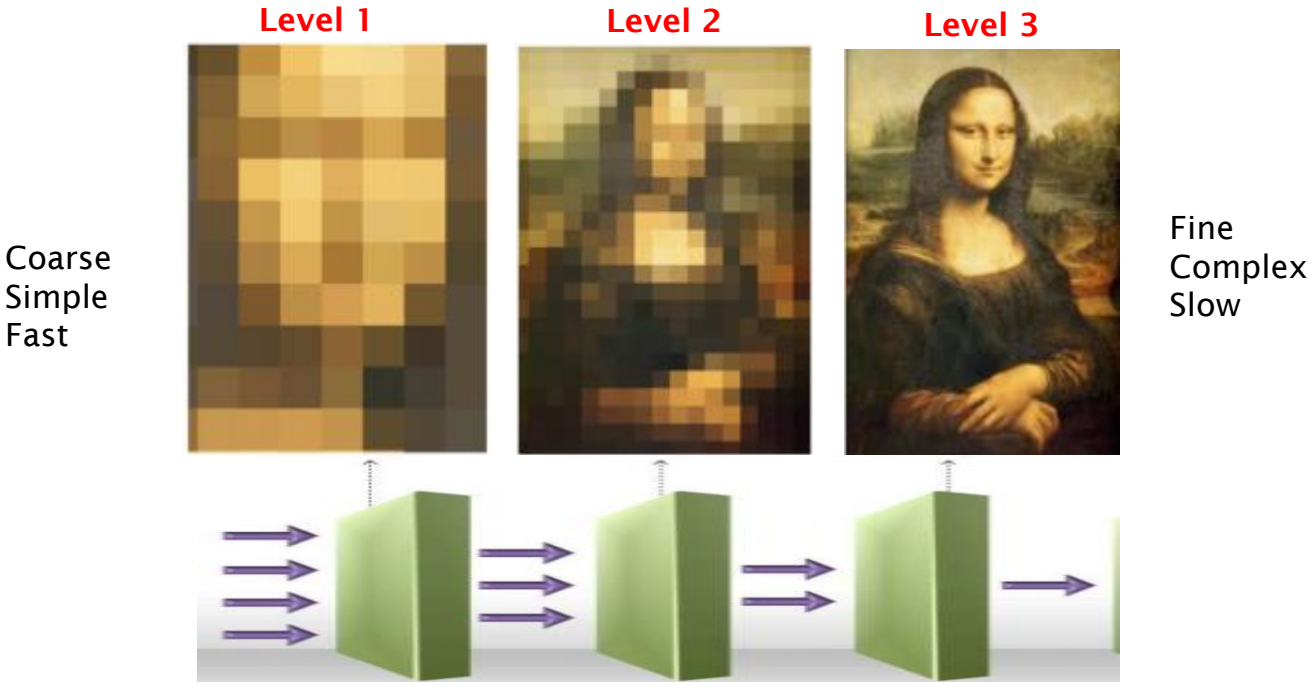
- Total data volume generated by ATLAS
  - Collision rate 40MHz x 100 million channels ~ $4x10^{15}$ bytes/s
- Trigger concept
  - The role of the trigger is to select bunch collisions containing potential interesting physics
  - What is “interesting”?
    - Define what is signal and what is background
  - Which is the final affordable rate of the DAQ system?
    - Define the maximum allowed rate





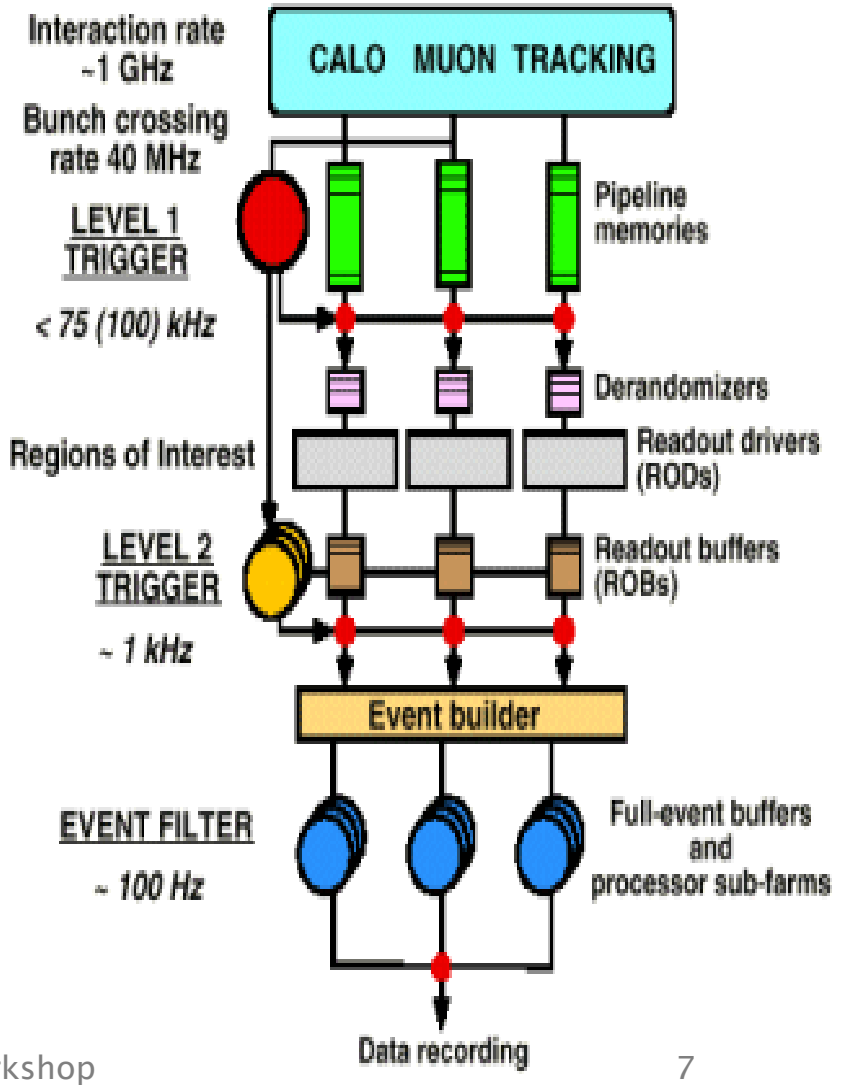
Multi-level trigger concept

- Adopted in large experiments, successively more complex decisions are made on successively lower data rates
  - First level with short latency, working at higher rates
  - Higher levels apply further rejection power, with longer latency (more complex algorithms)



Original ATLAS TDAQ Architecture

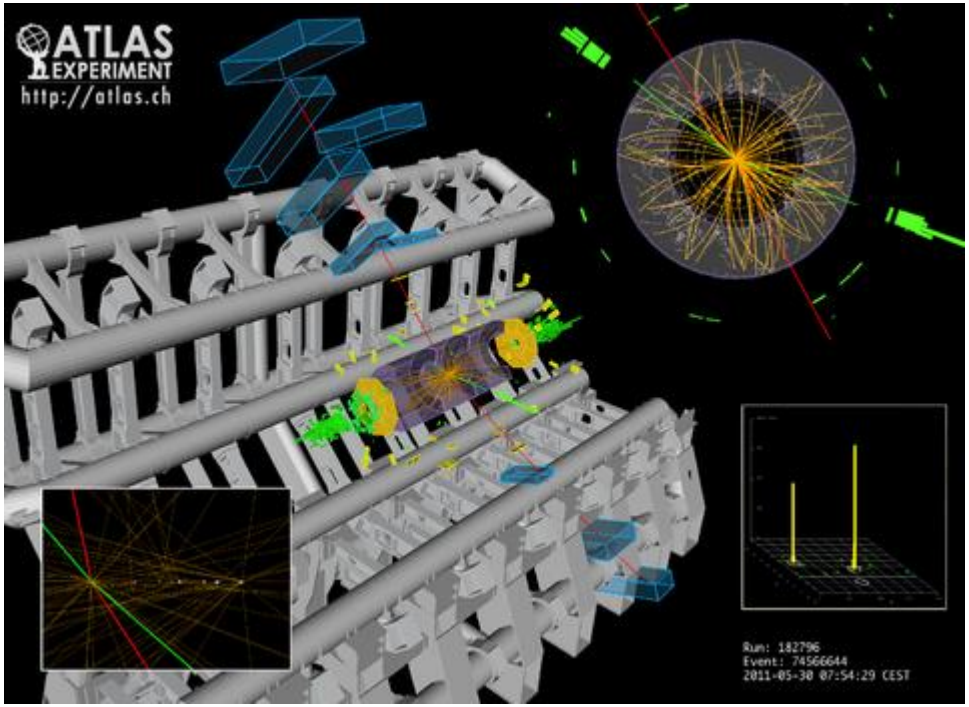
- Level 1 trigger
  - Rapid rejection of high-rate backgrounds
  - Fast custom electronics
    - Real-time @40MHz
  - Coarse calorimeter info
- High lever trigger
  - Event selection
  - Software running on computer farm
  - Access to full event data
    - Full granularity
    - Full precision



Very successful

- Higgs boson discovery 2012
  - ATLAS together with CMS

Higgs → 2mu2e

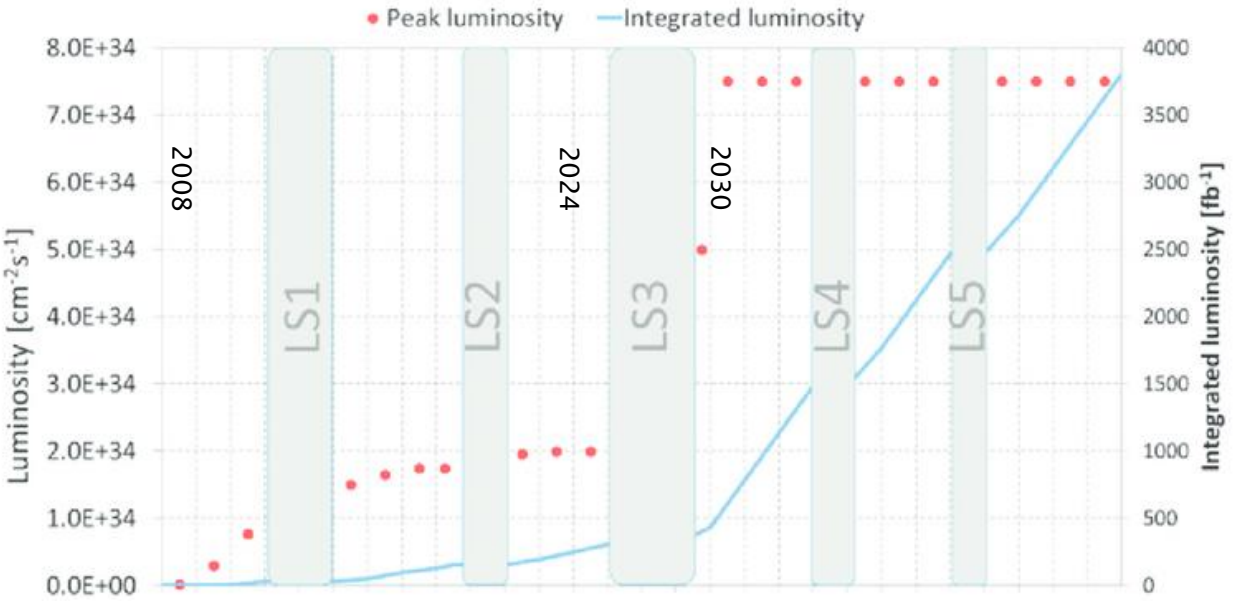


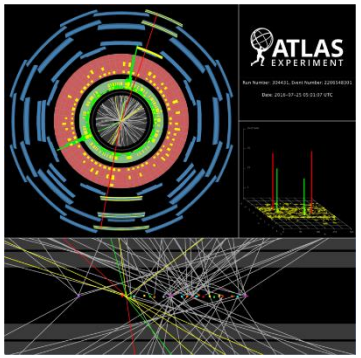
The Nobel Prize in Physics 2013

Photo: A. Mahmoud
François Englert
Prize share: 1/2

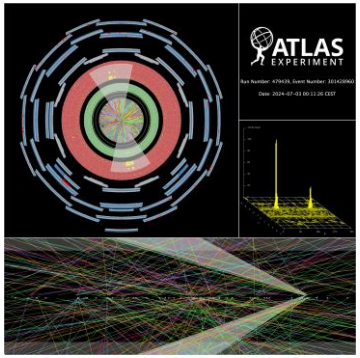
Photo: A. Mahmoud
Peter W. Higgs
Prize share: 1/2

LHC Luminosity profile and pileup

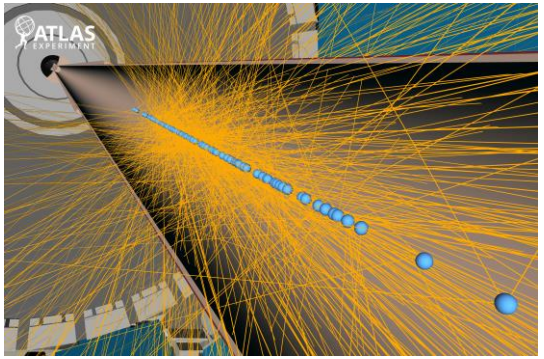




μ=20



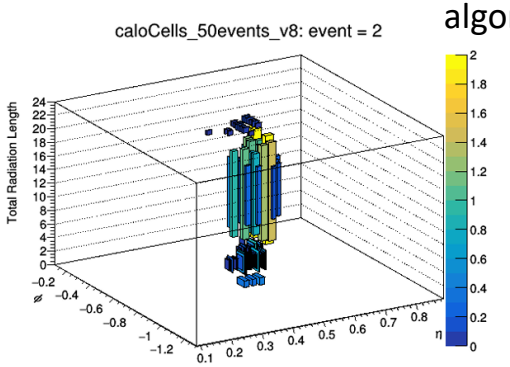
μ=65

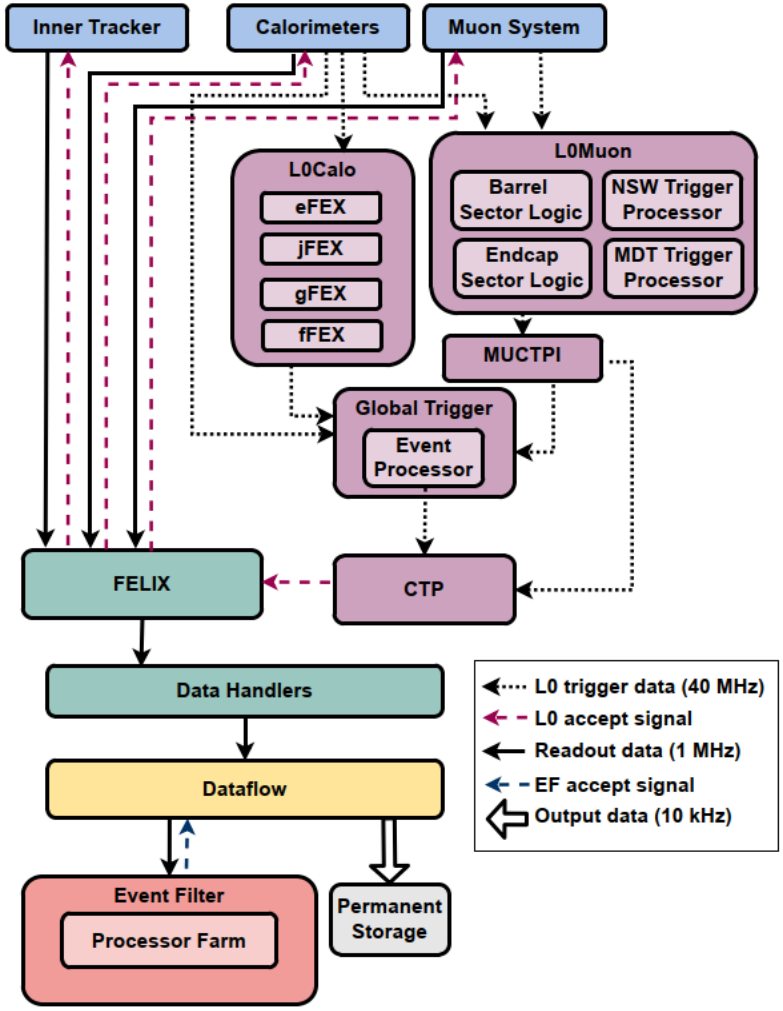


μ=200

ATLAS TDAQ Phase-II Architecture

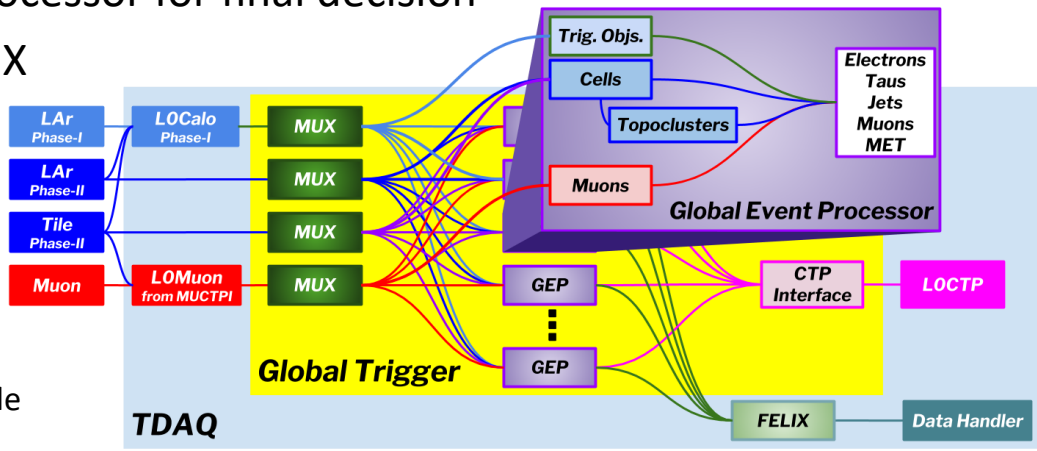
- L0 Trigger
  - Real-time
    - 10 μs latency
    - 1 MHz trigger rate
  - L0Calo, L0Muon, CTP
  - Global Trigger
    - Running complex full event algorithms inside FPGA at real time
      - E.g. TopoCluster algorithm
      - Similar to phase-I offline algorithms running on PC farm





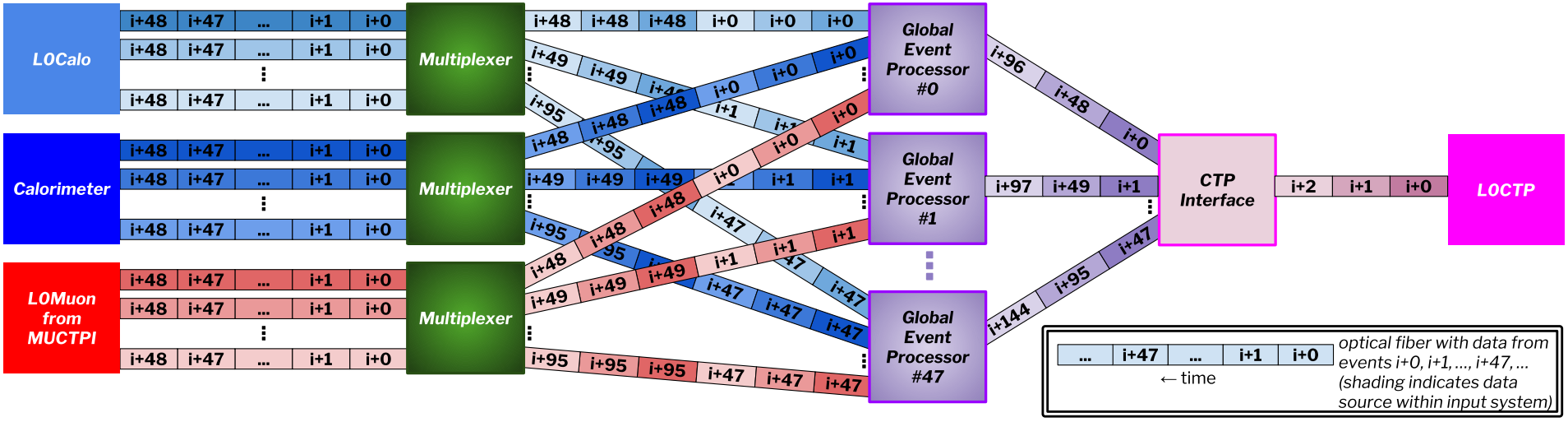
Global Trigger system overview

- Maximize physics potential by concentrating full event data onto single processing unit
  - Inputs from LAr, Tile, L0Calo, L0Muon at 40 MHz
  - ~ 50 Tb/s into Global Trigger
  - Data aggregation to single node with time multiplexing
  - Object-level and event-level reconstruction and analysis
  - Outputs to Central Trigger Processor for final decision
  - Readout on L0 Accept to FELIX
- Farm of FPGA-based processing units
  - Different functions implemented in firmware
    - Common hardware platform
      - The Global Common Module



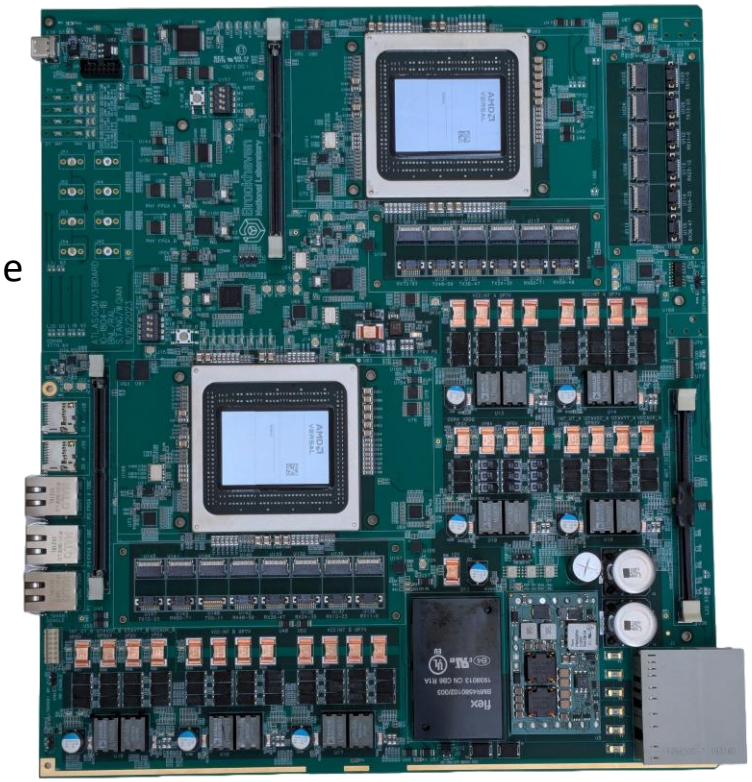
Global Trigger system realization

- Three-layer system with synchronous interface to rest of ATLAS
  - Nominal 49 node MUX layer
    - captures incoming data from Calorimeters, L0Calo and MuCTPi every BC and streams consecutive events to Global Event Processors in turn
  - Nominal 49 node GEP layer
    - each node receives a new event every 49 BC, performs trigger algorithms, streams results to gCTPi interface
  - Single node gCTPi interface
    - receives list of trigger items from Global Event Processors and sends results to CTP every BC with fixed latency
  - Interconnected by full mesh optical fibre exchange



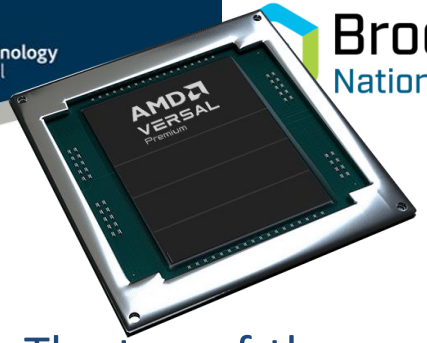
GCM prototype v3

- Main Features
  - ATCA form factor
  - AMD/Xilinx Versal Adaptive SoCs
    - 1 versal premium VP1802 for MUX node
    - 1 versal premium VP1802 for GEP/gCTPi node
  - Samtec Firefly 25Gx12ch optical modules
    - 8 for GEP/gCTPi node
    - 12 for MUX node
    - 240 optical links in total
  - Power design capacity 540W
    - 1 PIM4328/ 1 BMR458 (-48V/12V)
    - 7 LTM4681/1 LTM4638 (POL)
  - Clock chips
    - 2 Si5395A
  - 26-layer PCB with backdrill and via-in-pad technology
  - Ultralow loss PCB material EM890K

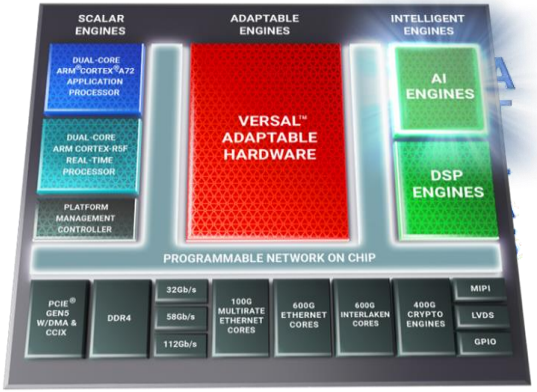


Science & Technology Facilities Council

Brookhaven National Laboratory



VP1802 FPGA

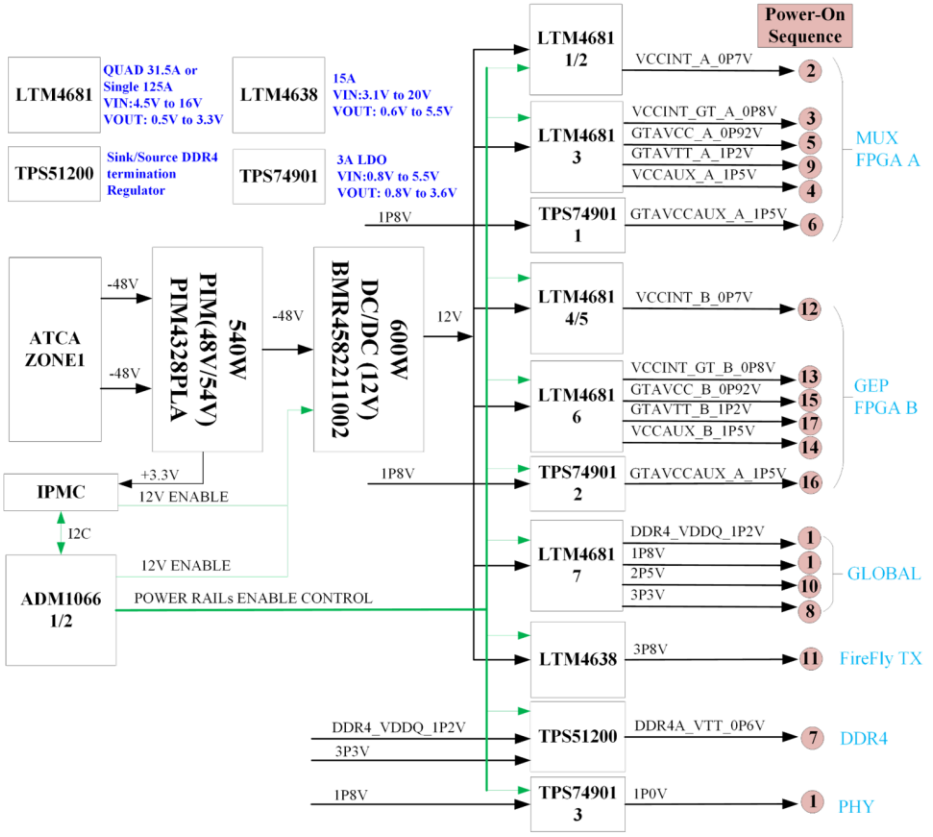


- The top-of-the-range AMD/Xilinx versal premium

		VP1002	VP1052	VP1102	VP1202	VP1402	VP1502	VP2502	VP1552	VP1702	VP1802
Adaptable Engines	System Logic Cells (K)	833	1,186	1,575	1,969	2,233	3,763	3,738	3,837	5,558	7,352
	LUTs	380,800	542,080	719,872	900,224	1,020,928	1,720,448	1,708,672	1,753,984	2,540,672	3,360,896
	NoC Master / NoC Slave Ports	22	22	30	28	42	52	52	52	76	100
	Super Logic Regions (SLRs)[1]	-	-	-	-	-	2	2	2	3	4
	Distributed RAM (Mb)	12	17	22	27	31	53	52	54	78	103
Memory	Block RAM (Mb)	19	26	49	47	70	89	89	89	132	174
	UltraRAM (Mb)	97	138	127	190	181	366	366	366	541	717
	Multiport RAM (Mb)	80	80	-	-	-	-	-	-	-	-
	Total PL Memory (Mb)	208	261	198	264	282	508	507	509	751	994
	DDR Memory Controllers	2	2	3	4	3	4	4	4	4	4
	DDR Bus Width	128	128	192	256	192	256	256	256	256	256
Intelligent Engines	DSP Engines	1,140	1,572	1,904	3,984	2,672	7,440	7,392	7,392	10,896	14,352
	AI Engines Tiles	-	-	-	-	-	-	472	-	-	-
	AI Engine Data Memory (Mb)	-	-	-	-	-	-	118	-	-	-
Scalar Engines	APU	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC									
	RPU	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC									
	Memory	256KB On-Chip Memory w/ECC									
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)									
Serial Transceivers	GTY Transceivers (32.75Gb/s)	20	20	-	-	-	-	-	-	-	-
	GTYP Transceivers (32.75Gb/s)	-	-	8	28[2]	8	28[2]	28[2]	68[2]	28[2]	28[2]
	GTM Transceivers (58G (112G))	24 (12)	48 (24)	64 (32)	20 (10)	96 (64)[3]	60 (30)	60 (30)	20 (10)	100 (50)	140 (70)
Integrated Protocol IP	PCIe® w/DMA & CCIX (CPM4)	2 x Gen4x4	2 x Gen4x4	-	-	-	-	-	-	-	-
	PCIe w/DMA & CCIX (CPM5)	-	-	-	2 x Gen5x8	-	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8
	PCI Express	1 x Gen4x8	1 x Gen4x8	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	8 x Gen5x4	2 x Gen5x4	2 x Gen5x4
	100G Multirate Ethernet MAC	3	5	6	2	6	4	4	4	6	8
	600G Ethernet MAC	2	3	7	1	11	3	3	1	5	7
	600G Interlaken	1	2	0	0	0	1	1	0	2	3
	400G High-Speed Crypto Engine	1	1	3	1	4	2	2	2	3	4

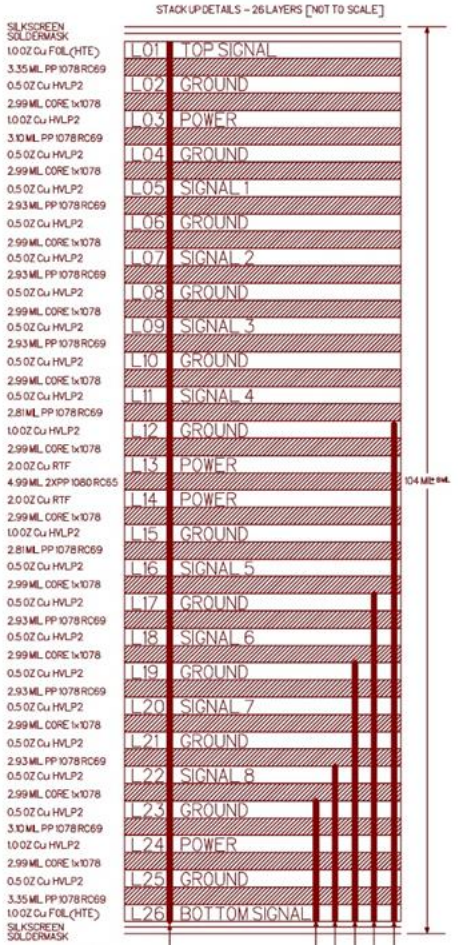
Power Design

- Worst-case scenario (540W)
  - FPGA ~ 200 W each
  - FireFly ~ 100 W (for 20 modules)
  - Misc ~40 W
- 10 POL DC-DC for ~20 power rails
  - 7 LTM4681
  - 1 LTM4638
  - 2 TPS74801
  - 1 TPS51200
- Independent and symmetric power solution for MUX and GEP
- Two ADM1066 for power sequencing



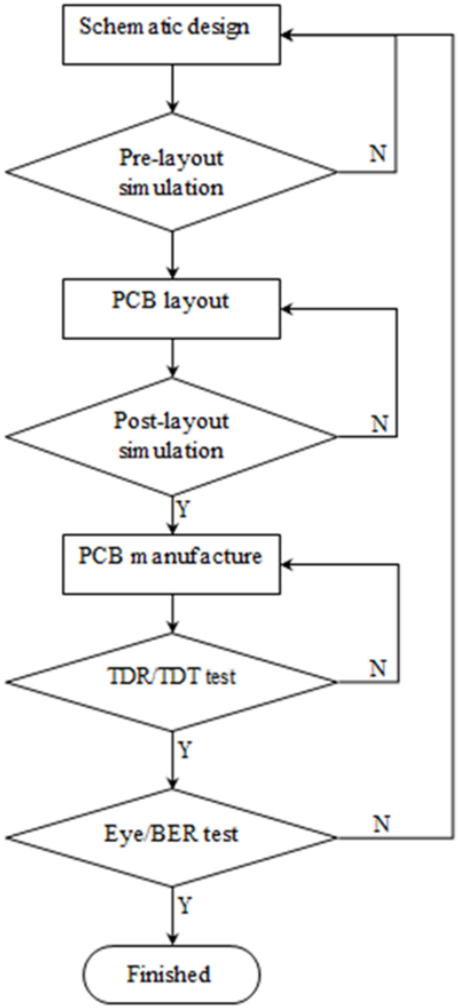
PCB technology

- **Material**: EM890K, Halogen free.
- **Total thickness 2.65mm** ± 0.2 mm, milled down on bottom edge
- **5 Backdrill** (stub less than 8 mil):
  - L26 - L23, DO NOT BREAK L22
  - L26 - L21, DO NOT BREAK L20
  - L26 - L19, DO NOT BREAK L18
  - L26 - L17, DO NOT BREAK L16
  - L26 - L12, DO NOT BREAK L11
- **Minimum via for non-backdrill**: 8 mil hole / 18 mil pad
- **Minimum via for backdrill**: 8 mil hole /22mil pad
- **IPC Class II**
- **Impedance tolerance** ± 10% for 50/93/100 ohm



PCB Design Methodology

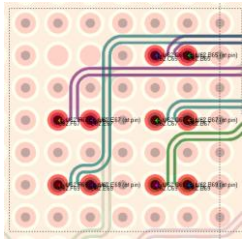
- Why
  - High-speed, high-power and high-density board
    - Too many rule of thumbs
      - Sometimes conflicting each other
      - Impossible to follow all of them
  - Compatibility to standards
    - Maximize margins
  - Help understand and debug
  - Goal
    - Reducing the number of board iterations
      - Dream – first time pass
- How
  - Simulation integrated into design flow
    - Iterative processes
  - Validation of simulation
    - Integrated PCB test coupon
    - Special test launch points

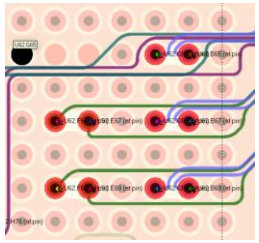


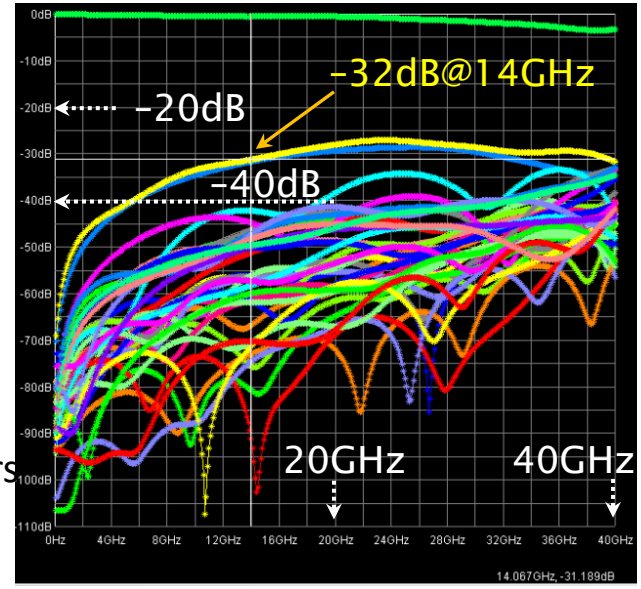
GCM v3 SI Simulation Example

https://iopscience.iop.org/article/10.1088/1748-0221/19/02/C02049/pdf

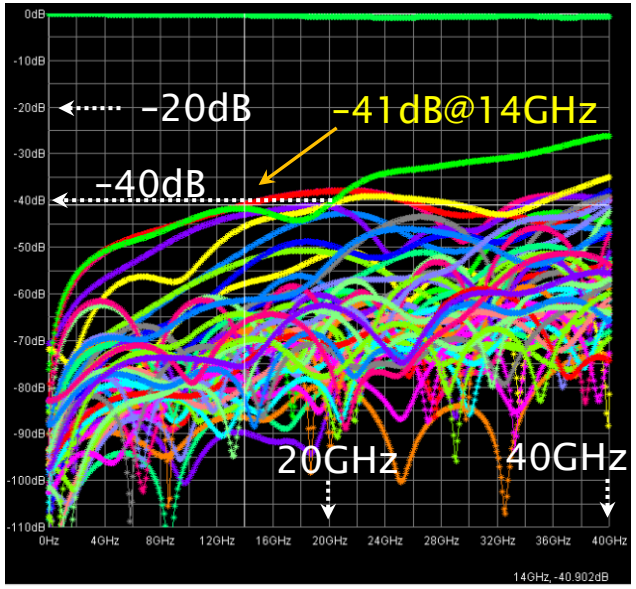
- Xilinx Crosstalk Requirement for CEI-28G-VSR
  - Rx-Rx
    - < -40dB
- GCM Rx-Rx
  - Majority
    - < -42dB
  - But one
    - ~32dB
  - Optimization
    - Swapping routing layers







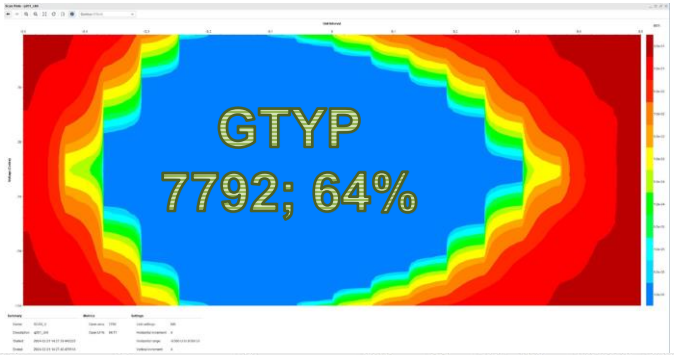
Before optimization

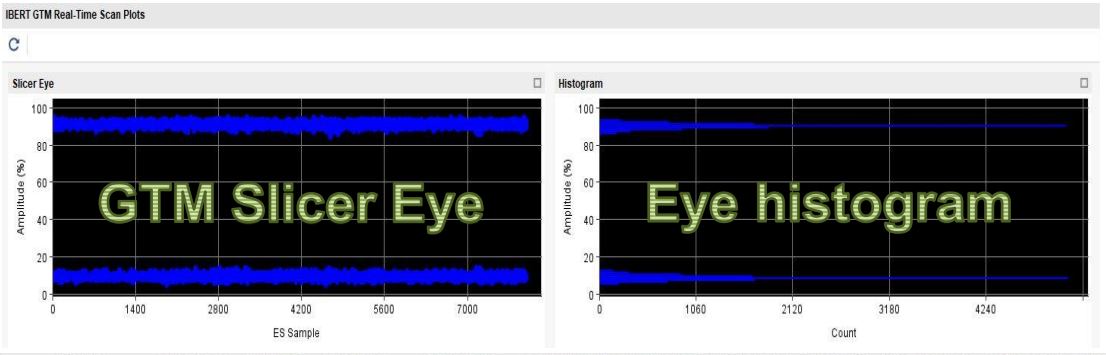


After optimization

Link Test Results - 25.7 Gb/s NRZ

- All optical links error free with good margin
  - BER < 1E-15



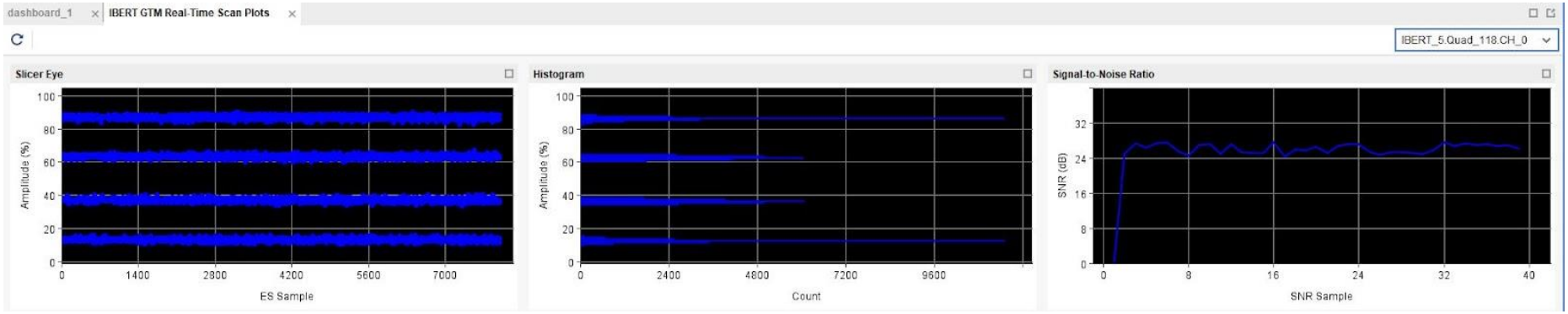


Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Main-Cursor	TX Diff Swing	TX Pre-Cursor	TX Post-Cursor	TXUSERCLK Freq	RXUSERCLK Freq	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
Ungrouped Links (0)																					
GTYP (4)							Reset	PRBS 31	PRBS 31		13	0	0			Inject	Reset	Reset			None
Link 0	IBERT_0.Quad_201.CH_0.TX	IBERT_0.Quad_201.CH_0.RX	25.777 Gbps	1.022E14	0E0	9.786E-15	Reset	PRBS 31	PRBS 31		13	0	0	402.759	402.759	Inject	Reset	Reset	Locked	Locked	None
Link 1	IBERT_0.Quad_201.CH_1.TX	IBERT_0.Quad_201.CH_1.RX	25.777 Gbps	1.022E14	0E0	9.786E-15	Reset	PRBS 31	PRBS 31		13	0	0	402.759	402.759	Inject	Reset	Reset	Locked	Locked	None
Link 2	IBERT_0.Quad_201.CH_2.TX	IBERT_0.Quad_201.CH_2.RX	25.777 Gbps	1.022E14	0E0	9.787E-15	Reset	PRBS 31	PRBS 31		13	0	0	402.759	402.759	Inject	Reset	Reset	Locked	Locked	None
Link 3	IBERT_0.Quad_201.CH_3.TX	IBERT_0.Quad_201.CH_3.RX	25.777 Gbps	1.022E14	0E0	9.789E-15	Reset	PRBS 31	PRBS 31		13	0	0	402.759	402.759	Inject	Reset	Reset	Locked	Locked	None
GTM (8)							Reset	PRBS 31	PRBS 31	0.502 Vdd		0 dB	0 dB			Inject	Reset	Reset			None
Link 4	IBERT_1.Quad_205.CH_0.TX	IBERT_1.Quad_202.CH_0.RX	25.775 Gbps	1.022E14	0E0	9.788E-15	Reset	PRBS 31	PRBS 31	0.502 Vdd		0 dB	0 dB	322.192	322.192	Inject	Reset	Reset	Locked	Locked	None
Link 5	IBERT_1.Quad_205.CH_1.TX	IBERT_1.Quad_202.CH_1.RX	25.775 Gbps	1.022E14	0E0	9.788E-15	Reset	PRBS 31	PRBS 31	0.502 Vdd		0 dB	0 dB	322.192	322.192	Inject	Reset	Reset	Locked	Locked	None
Link 6	IBERT_1.Quad_205.CH_2.TX	IBERT_1.Quad_202.CH_2.RX	25.775 Gbps	1.022E14	0E0	9.788E-15	Reset	PRBS 31	PRBS 31	0.502 Vdd		0 dB	0 dB	322.192	322.192	Inject	Reset	Reset	Locked	Locked	None
Link 7	IBERT_1.Quad_205.CH_3.TX	IBERT_1.Quad_202.CH_3.RX	25.775 Gbps	1.022E14	0E0	9.789E-15	Reset	PRBS 31	PRBS 31	0.502 Vdd		0 dB	0 dB	322.119	322.192	Inject	Reset	Reset	Locked	Locked	None
Link 8	IBERT_1.Quad_206.CH_0.TX	IBERT_1.Quad_203.CH_0.RX	25.775 Gbps	1.021E14	0E0	9.79E-15	Reset	PRBS 31	PRBS 31	0.502 Vdd		0 dB	0 dB	322.192	322.192	Inject	Reset	Reset	Locked	Locked	None
Link 9	IBERT_1.Quad_206.CH_1.TX	IBERT_1.Quad_203.CH_1.RX	25.775 Gbps	1.021E14	0E0	9.79E-15	Reset	PRBS 31	PRBS 31	0.502 Vdd		0 dB	0 dB	322.192	322.192	Inject	Reset	Reset	Locked	Locked	None
Link 10	IBERT_1.Quad_206.CH_2.TX	IBERT_1.Quad_203.CH_2.RX	25.775 Gbps	1.021E14	0E0	9.791E-15	Reset	PRBS 31	PRBS 31	0.502 Vdd		0 dB	0 dB	322.192	322.119	Inject	Reset	Reset	Locked	Locked	None
Link 11	IBERT_1.Quad_206.CH_3.TX	IBERT_1.Quad_203.CH_3.RX	25.775 Gbps	1.021E14	0E0	9.792E-15	Reset	PRBS 31	PRBS 31	0.502 Vdd		0 dB	0 dB	322.192	322.192	Inject	Reset	Reset	Locked	Locked	None

Link Test Results - 58Gb/s PAM4

- 8 on-board electric GTM links between MUX and GEP
  - 4 Tx from MUX to GEP
  - 4 Tx from GEP to MUX

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TXUSERCLK Freq	RXUSERCLK Freq	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode	TX Main-Cursor
Ungrouped Links (0)																		
Link Group 0 (8)							Reset	PRBS 31	PRBS 31			Inject	Reset	Reset			None	User Design
Link 0	IBERT_5.Quad_118.CH_0.TX	IBERT_7.Quad_204.CH_0.RX	60.891 Gbps	3.238E13	0E0	3.088E-14	Reset	PRBS 31	PRBS 31	380.566	380.566	Inject	Reset	Reset	Locked	Locked	None	User Design
Link 1	IBERT_5.Quad_118.CH_1.TX	IBERT_7.Quad_204.CH_1.RX	60.891 Gbps	3.238E13	0E0	3.088E-14	Reset	PRBS 31	PRBS 31	380.493	380.566	Inject	Reset	Reset	Locked	Locked	None	User Design
Link 2	IBERT_5.Quad_118.CH_2.TX	IBERT_7.Quad_204.CH_2.RX	60.891 Gbps	3.236E13	0E0	3.09E-14	Reset	PRBS 31	PRBS 31	380.566	380.493	Inject	Reset	Reset	Locked	Locked	None	User Design
Link 3	IBERT_5.Quad_118.CH_3.TX	IBERT_7.Quad_204.CH_3.RX	60.879 Gbps	3.233E13	0E0	3.093E-14	Reset	PRBS 31	PRBS 31	380.493	380.566	Inject	Reset	Reset	Locked	Locked	None	User Design
Link 4	IBERT_7.Quad_204.CH_0.TX	IBERT_5.Quad_118.CH_0.RX	60.891 Gbps	3.232E13	0E0	3.094E-14	Reset	PRBS 31	PRBS 31	380.566	380.566	Inject	Reset	Reset	Locked	Locked	None	User Design
Link 5	IBERT_7.Quad_204.CH_1.TX	IBERT_5.Quad_118.CH_1.RX	60.891 Gbps	3.232E13	0E0	3.094E-14	Reset	PRBS 31	PRBS 31	380.566	380.566	Inject	Reset	Reset	Locked	Locked	None	User Design
Link 6	IBERT_7.Quad_204.CH_2.TX	IBERT_5.Quad_118.CH_2.RX	60.891 Gbps	3.231E13	0E0	3.095E-14	Reset	PRBS 31	PRBS 31	380.566	380.566	Inject	Reset	Reset	Locked	Locked	None	User Design
Link 7	IBERT_7.Quad_204.CH_3.TX	IBERT_5.Quad_118.CH_3.RX	60.879 Gbps	3.23E13	0E0	3.096E-14	Reset	PRBS 31	PRBS 31	380.566	380.566	Inject	Reset	Reset	Locked	Locked	None	User Design



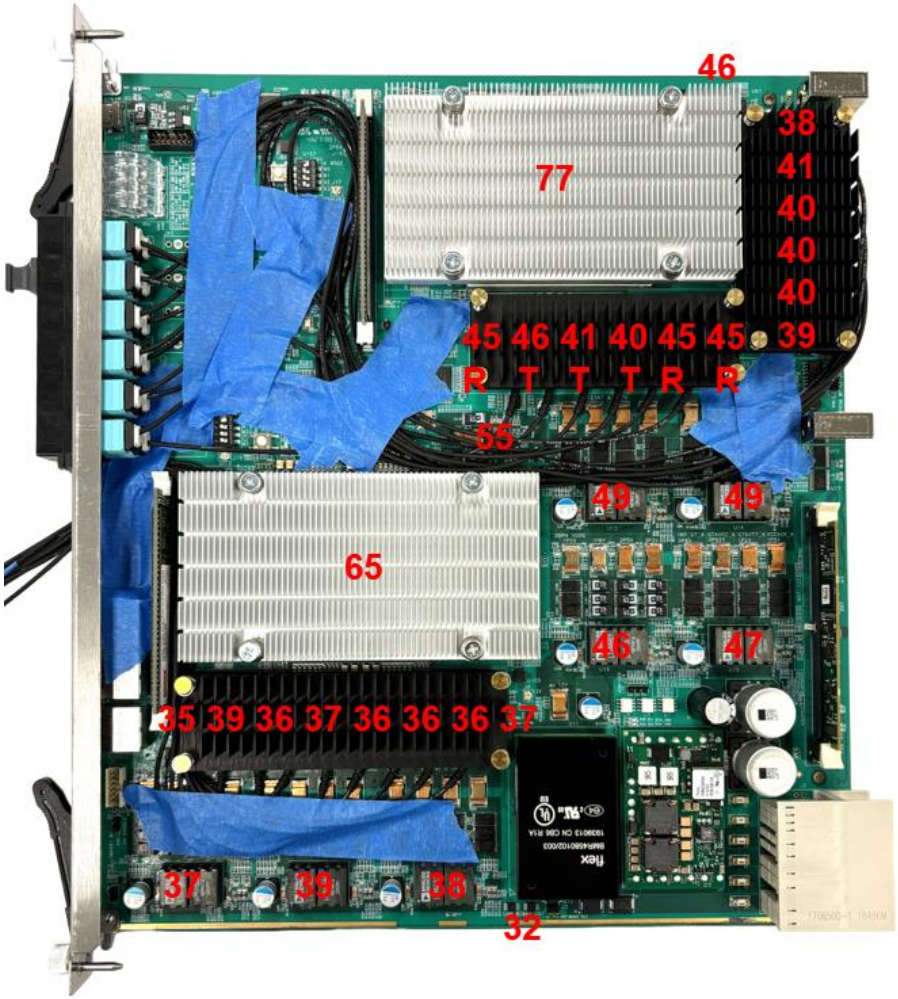
GTM Slicer Eye

Eye Histogram

Eye SNR

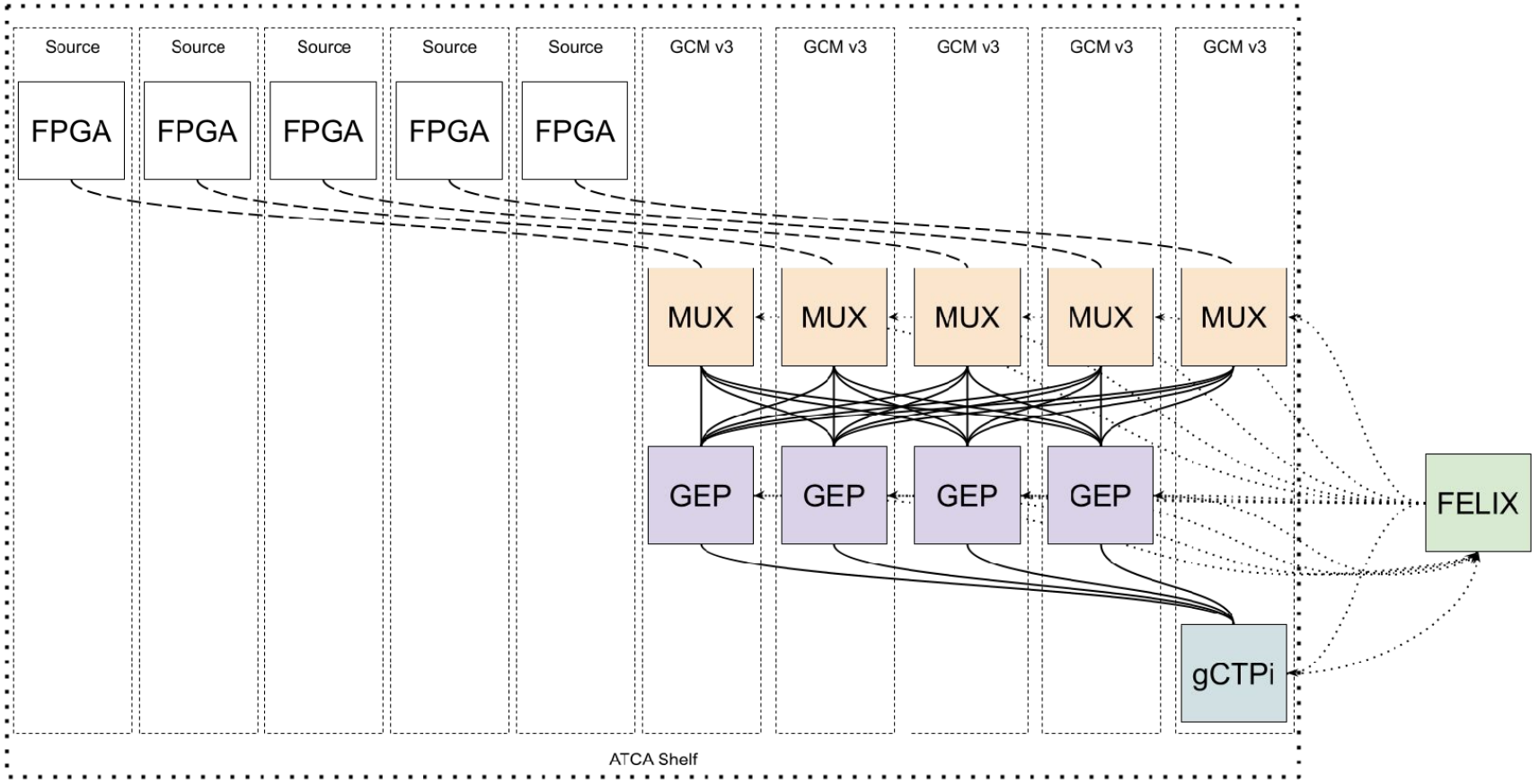
Power/Thermal stress test

- Worst Case scenario
  - Both FPGA firmware resource usage 70% + 22 GTM Quads
- ATCA Fan Level 10
- Total power: 402W
  - MUX 152 W
  - GEP 144 W
- Temperature:
  - MUX 77 °C
  - GEP 65 °C
  - All Firefly modules below 50 °C
  - All power modules < 55 °C
  - Inlet airflow on board 32 °C
  - Outlet airflow on board 46 °C



Next step

- Slice test with 5 GCMv3 modules at CERN
  - To demonstrate the data flow through the slice (10%) system

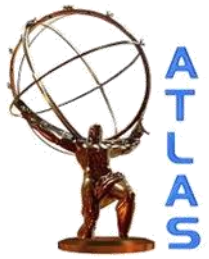


Summary

- ATLAS TDAQ phase-II upgrade will be installed during the LHC LS3 in preparation for the High-Luminosity LHC era.
- The new Global Trigger is the core of the real-time L0 trigger of ATLAS TDAQ phase-II upgrade.
- The Global Trigger is based on FPGA farm of three layers.
  - MUX, GEP and gCTPi
- A full function Global Common Module prototype has been developed to support the functionalities of all nodes in all three layers with different firmware loads.
- GCM is a state-of-the-art high-speed high-density high-power ATCA board designed with a systematic methodology.
- 5 GCM prototype modules have been made and achieved first time pass successfully.

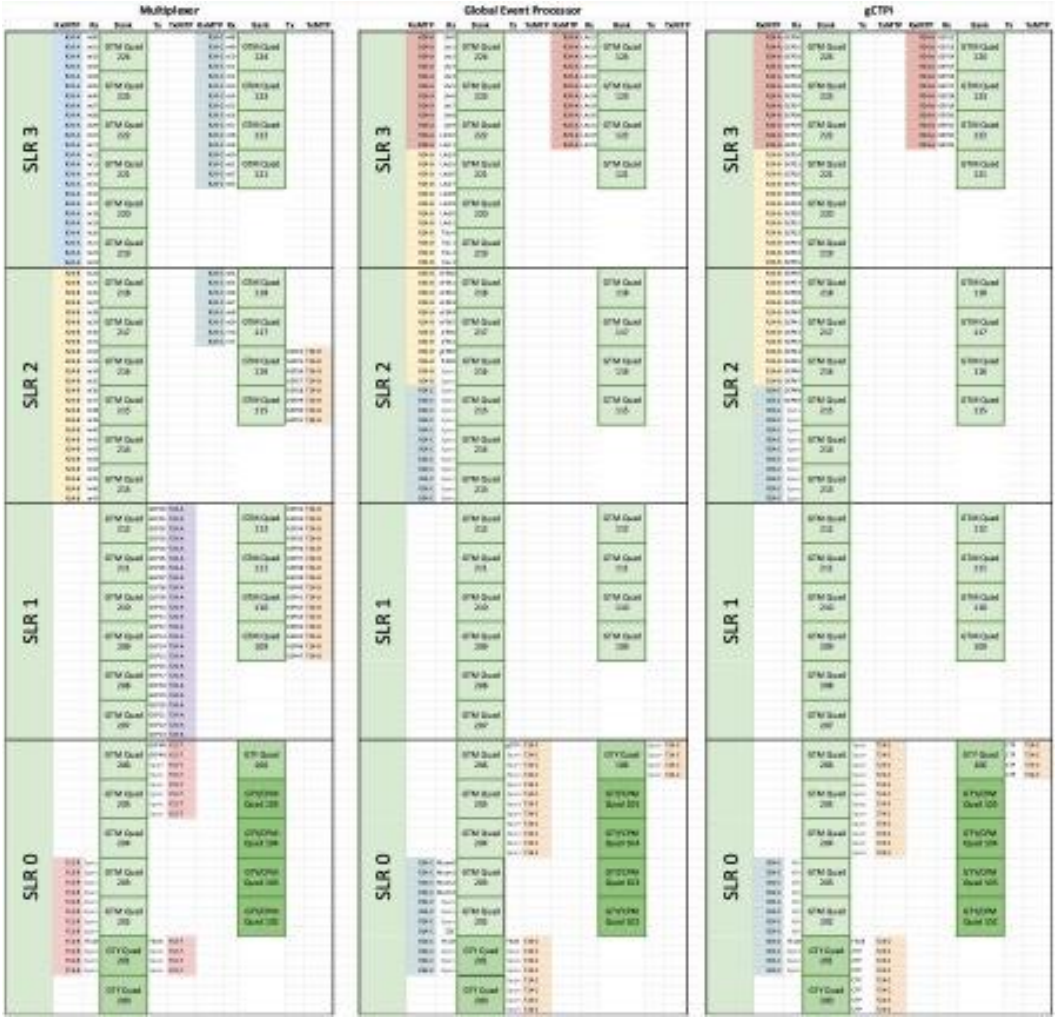
Science & Technology Facilities Council

Brookhaven National Laboratory



Backup

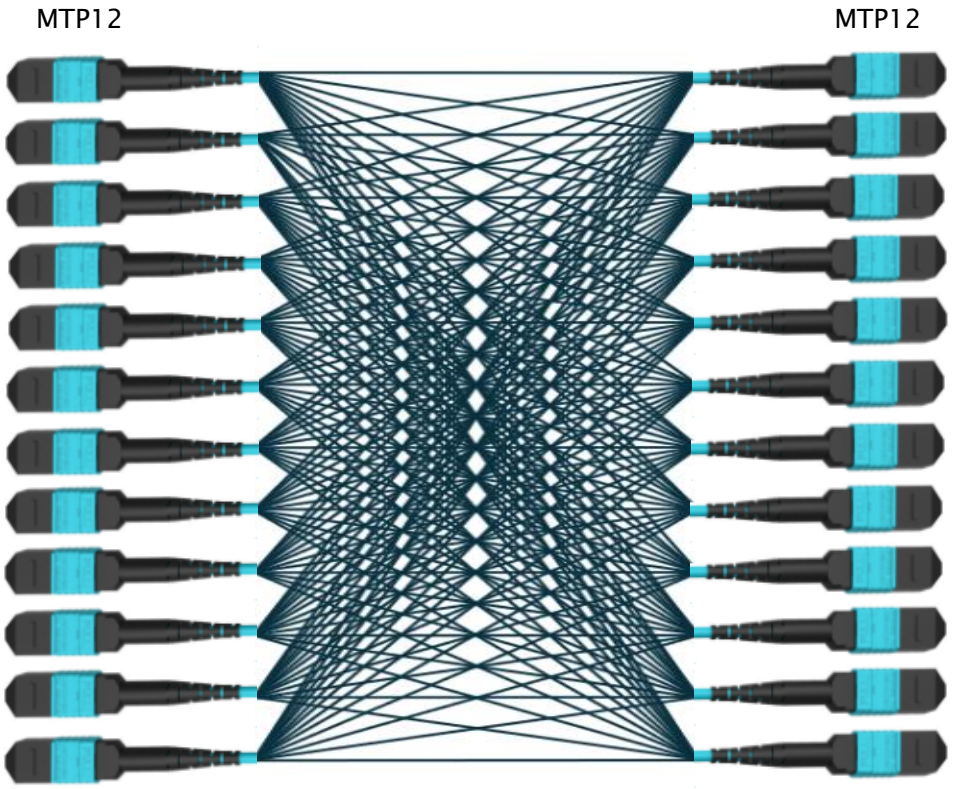
VP1802 GT mapping



Optical fibre full mesh exchange

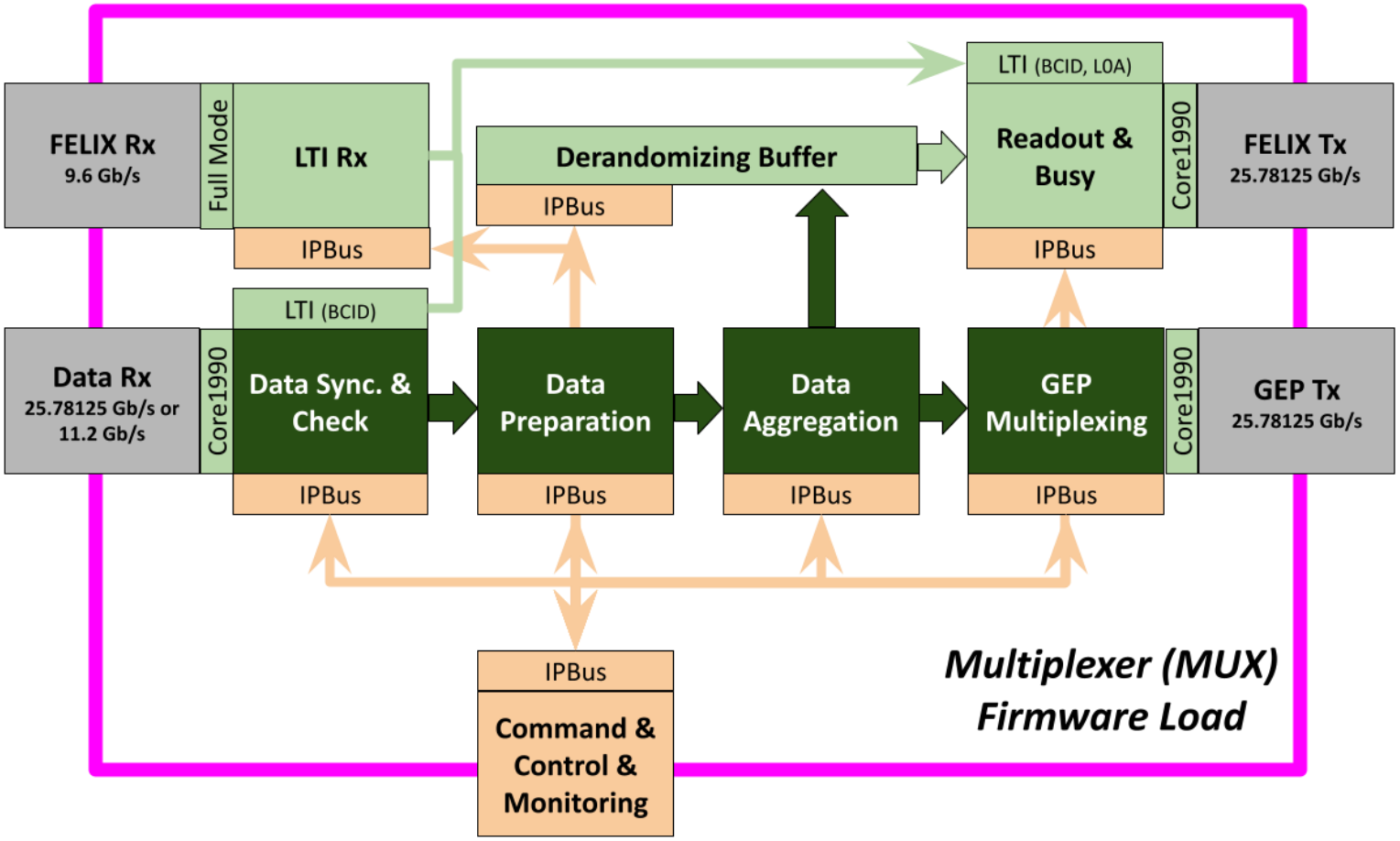
12 MTP12 x 12 MTP12

COTS product

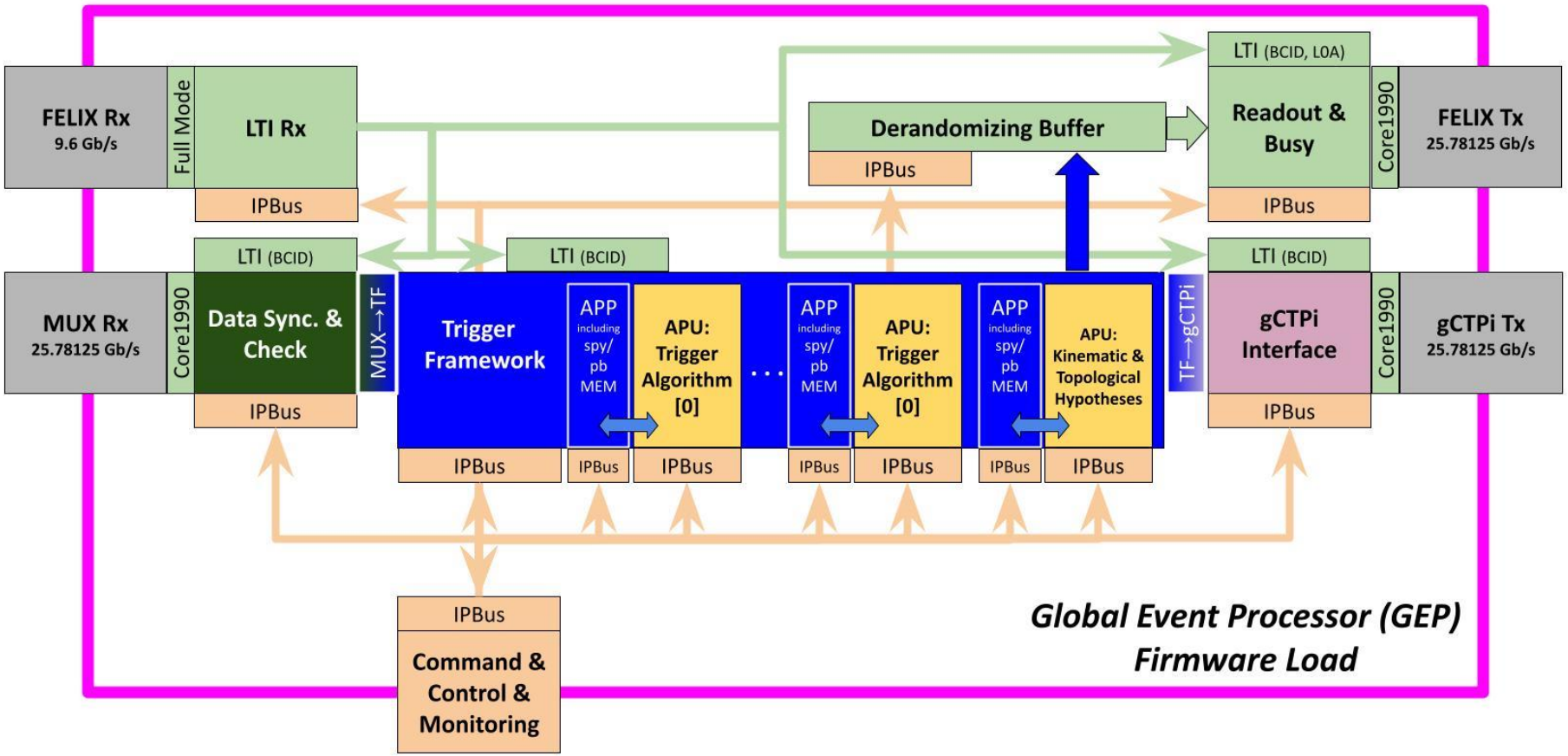


A 60 MUX nodes to 60 GEP nodes full mesh optical fibre exchange can be constructed from above COTS product easily.

Global firmware MUX/gCTPi

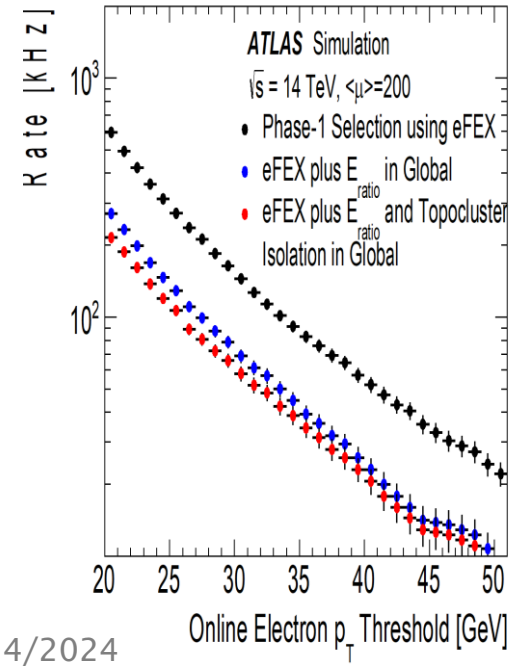


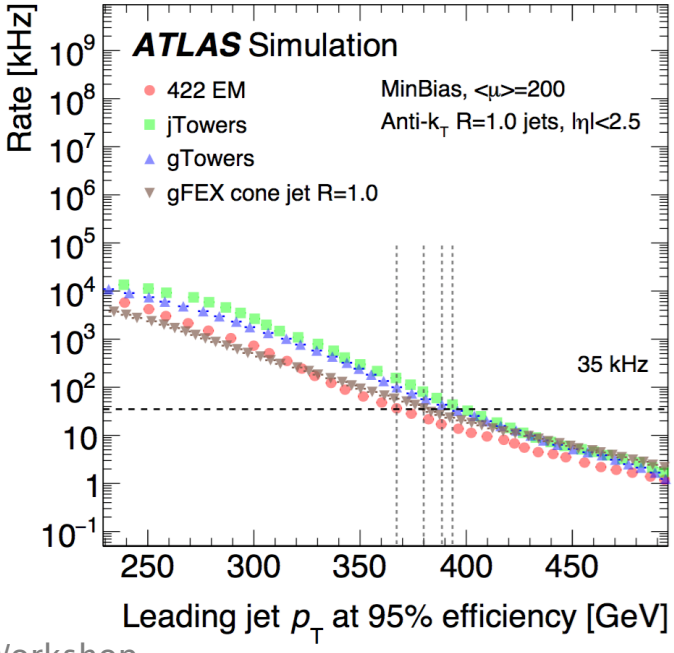
Global firmware GEP framework



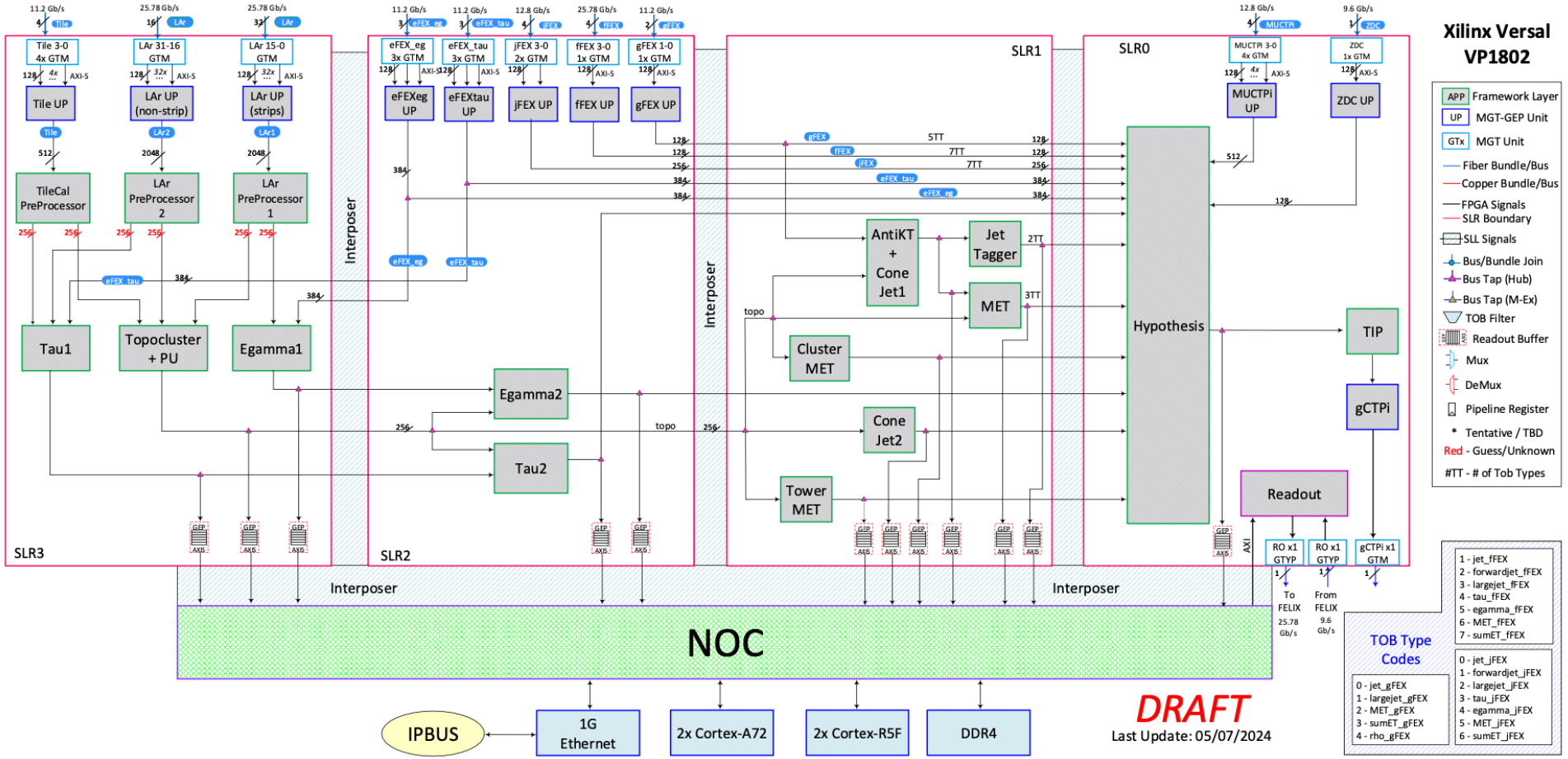
Algorithms on Global Trigger

- Combine FEX TOB seeds with full calorimeter cell information above 2 σ noise cut
  - Full calorimeter event-based
    - jets using topoclusters, finer calibration and a closer approximation to anti-k_T jets
    - jet substructure, E_T and E_T^miss
  - RoI-based
    - *e/γ* using strips and finer granularity to calculate shower shape – *E_ratio* or BDT
    - Tau using strips and topoclusters
    - wide area around electron and tau for background for isolation (eFEX 0.3×0.3 in η×φ)





Global GEP firmware floor plan



Global firmware management

- Release Management and Continuous Integration based on HoG
  - Guarantees reproducibility and traceability (even locally!)
    - Continuous Integration with minimal additional effort
    - multiple Release branches plus develop branch
    - automatic checking of software and firmware register maps
      - version and SHA cross-checked and written in XMLs and firmware
      - critical for achieving reliability in complex system!

https://hog.readthedocs.io/en/latest/#