中國科學院高能物理研究所
Institute of High Energy Physics Chinese Academy of Sciences

The development of HV-CMOS pixel sensors for silicon tracker in 55 nm process

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On behalf of the CEPC ITK HV-CMOS pixel collaboration

- R&D Objectives: CEPC ITK & LHCb UT upgrade
- Status of HV-CMOS pixel sensors
- Design & test results of COFFEE2
- Summary and Outlook

The International Workshop on CEPC, Hangzhou，Oct 23-27, 2024

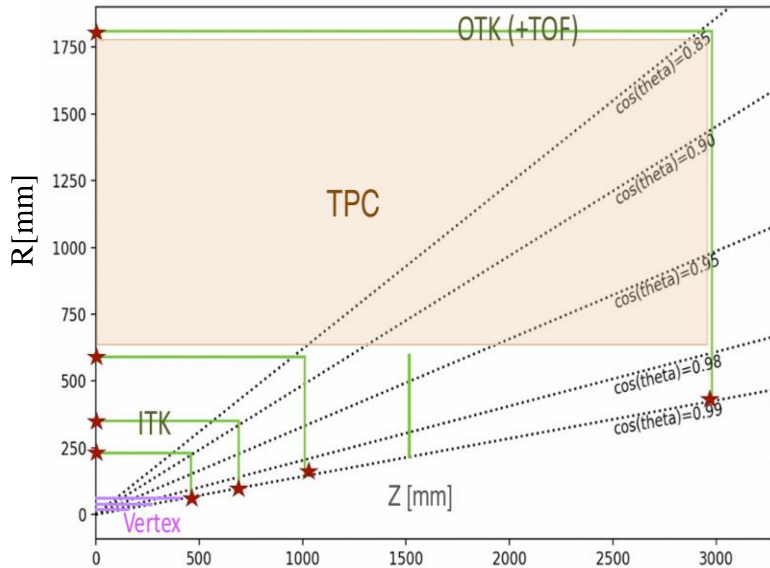
Collaboration group

> 30 people from 8 institutes:

- **IHEP：** Weiguo LU, Mei ZHAO, Zhiyu Xiang, Kunyu Xie, Leyi Li, Xiaoyu ZHU, Xiaoxu ZHANG, Ruoshi DONG, Congcong Wang， Yang ZHOU, Zijun Xu, Yiming Li, Jianchun Wang;
- **KIT：** Hui ZHANG, Ruoshi DONG, Ivan PERIC，
- **Zhejiang University:** Jianpeng DENG, Pengxu LI, Hongbo ZHU；
- **Northwestern Polytechnical University:** Zexuan ZHAO， XiaoMin WEI；
- **Dalian Minzu University:** Yang CHEN， Yujie WANG， Xuekang LI， Xinyang GUO， Zhan SHI，
- **Shandong University:** Leyi LI, Meng WANG,
- **NanJing University:** Xiaoxu ZHANG, Lei ZHANG
- **Hunan University:** Zhuojun CHEN

R&D Objectives: CEPC inner silicon tracker (ITK)

To achieve precise position measurements for accurate particle trajectory determination:



Required ITK performances:

- Spatial resolution:

  Barrel: $\sigma_\Phi < 10$ µm, $\sigma_z < 50$ µm;
  Endcap: $\sigma_\Phi < 10$ µm, $\sigma_z < 100$ µm;
- Low material budget: <1% X_0 per layer
- Luminosity: ~115×10^{34} $cm^{-2}s^{-1}$ (Z-pole)

  Maximum hit rate ~10^6 Hz/cm^2
  A few ns timing resolution to tag 23ns bunches;
- Cost effectiveness:

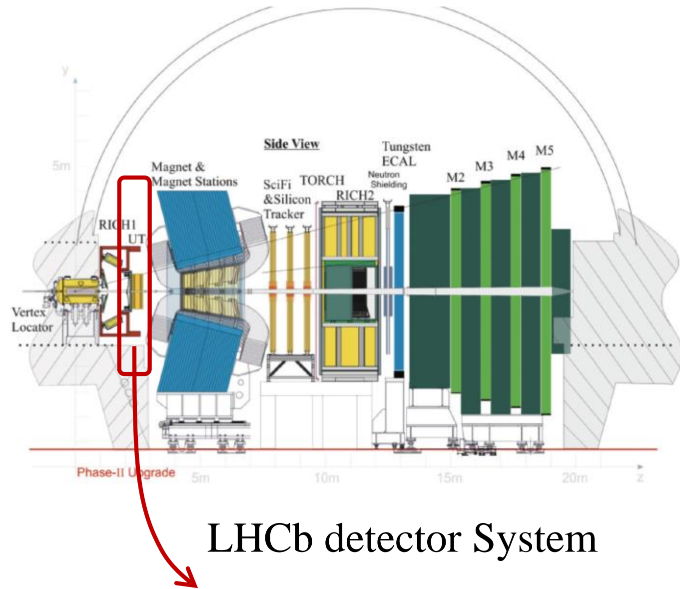
  ~ 15 m^2 area;

Sensor Design specifications:

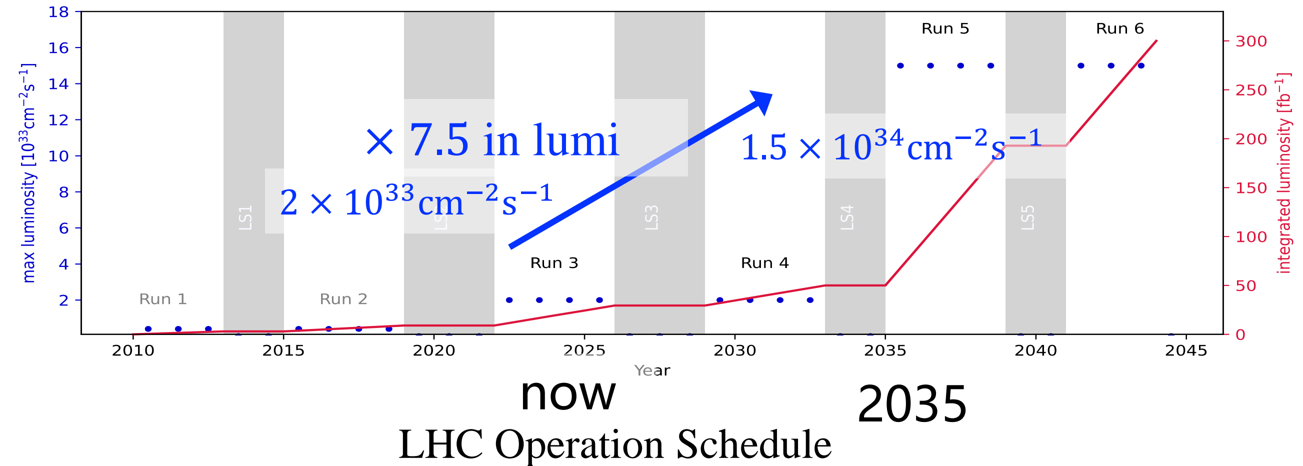
	Monolithic HVCMOS pixels
Pixel Size (Strip Pitch Size)	34 µm × 150 µm
Sensor size	2 cm × 2 cm (active area: 1.92 cm x 1.74 cm)
Array size (Strip number)	512 rows × 128 columns
Spatial resolution	σ_φ ~8 µm (bending), σ_z~40 µm
Timing resolution	~3-5 ns
Data size per hit (1 readout)	42 bits (14b BXID, 7b+9b address, 6b TOT, 5b fine TDC, 1 polarity)
Data rate per sensor	Maximum ~0.1 Gbps* (pair production)
LV / HV	1.2 V / 150 V

**Please see Yiming Li's report "CEPC Inner Silicon Tracker towards Ref-TDR"*

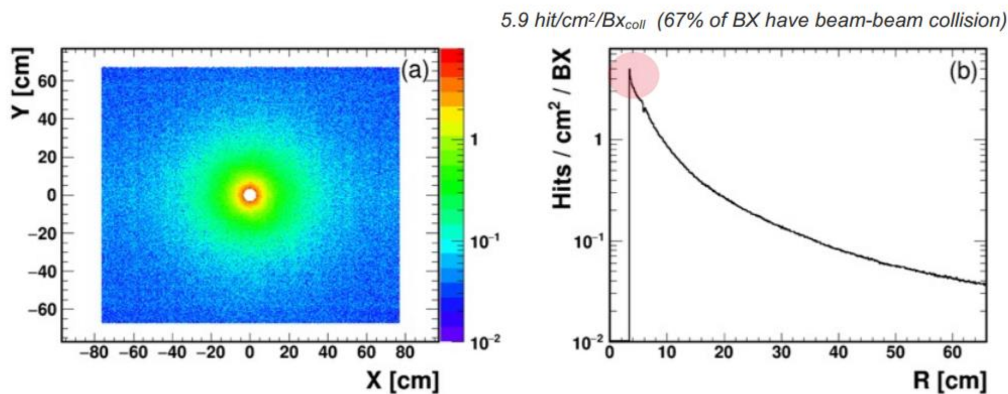
R&D Objectives: LHCb Upstream Tracker (UT) upgrade



LHCb detector System



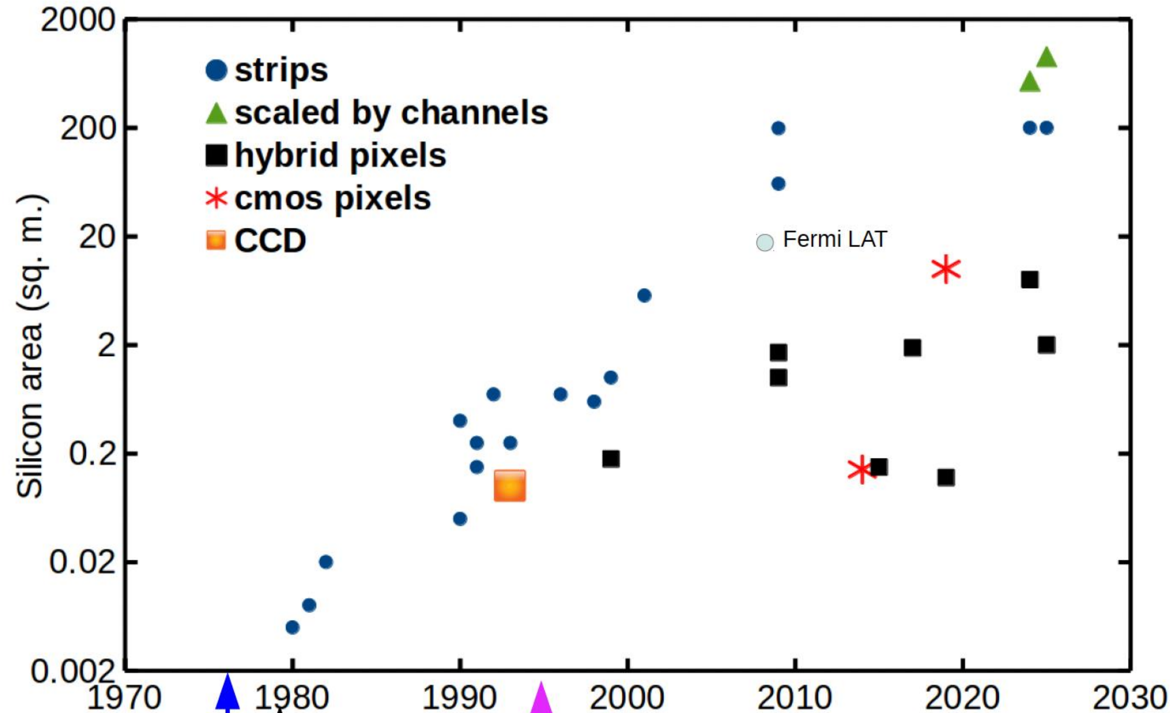
LHC Operation Schedule



The estimated hit density at the UT location after the LHCb upgrade

- Detector upgrade at ~2032 （**L**ong **S**hutdown4） to meet the requirement of 7-fold increase in luminosity；
- Maximum hit density : ~6 hits/cm²/BX (25 ns);
- Time resolution of a few ns, low pile-up, and high radiation tolerance (3×10^{15} n_{eq}/cm^2, 240 Mrad TID), with low power consumption (100-300 mW/cm²)

Silicon Tracking Detectors developed for HEP



Year of first data taking

First CCD digital cameras

Start of HEP IC design

CMOS sensors used in webcams

Strip Detectors

Year	Detector
1980	NA1
1981	NA11
1982	NA14
1990	MarkII
1990	DELPHI
1991	ALEPH
1991	OPAL
1992	CDF SVX
1993	L3
1996	CDF SVX'
1998	CLEO III
1999	BaBar
2001	CDF SVXII+ISL
2009	ATLAS SCT
2009	CMS tracker
2025	ATLAS ITK
2025	CMS upgrade

Hybrid Pixels

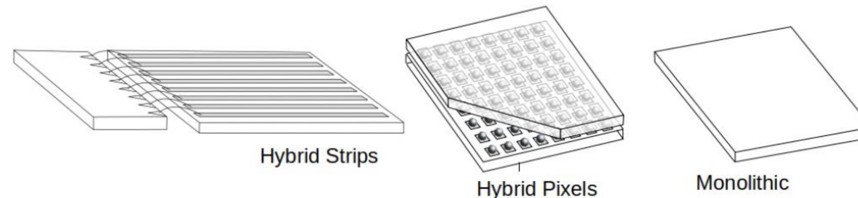
Year	Detector
1999	Delphi
2009	ATLAS
2009	CMS
2015	ATLAS IBL
2017	CMS
2019	velopix
2025	ATLAS
2025	CMS

CMOS Pixels

Year	Detector
2014	STAR
2019	ALICE

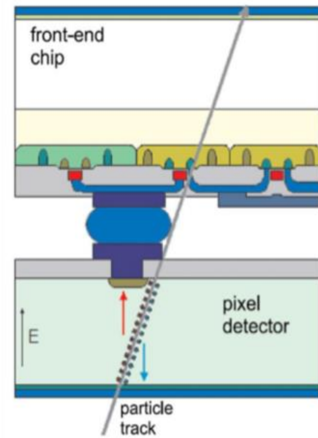
CCDs

Year	Detector
1993	VXD



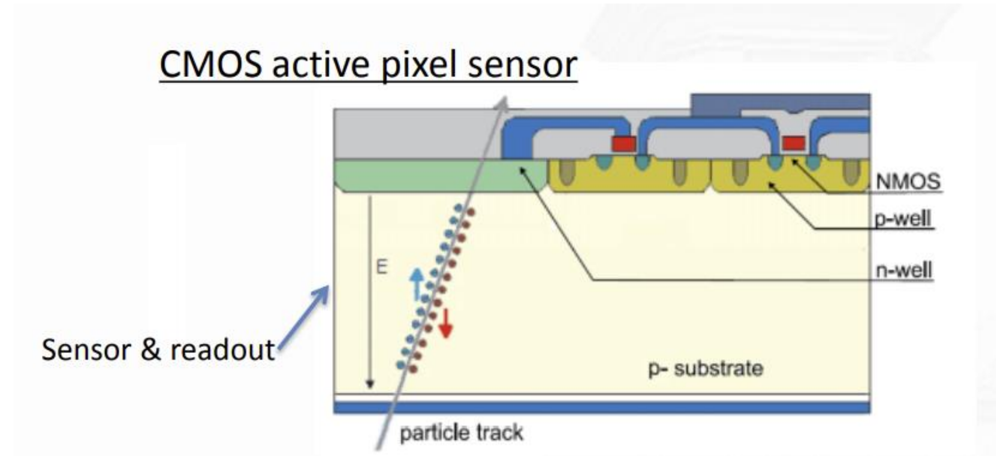
M. Garcia-Sciveres @ HSTD13, Dec 2023

Hybrid vs Monolithic



Readout
ASIC chip

The sensor



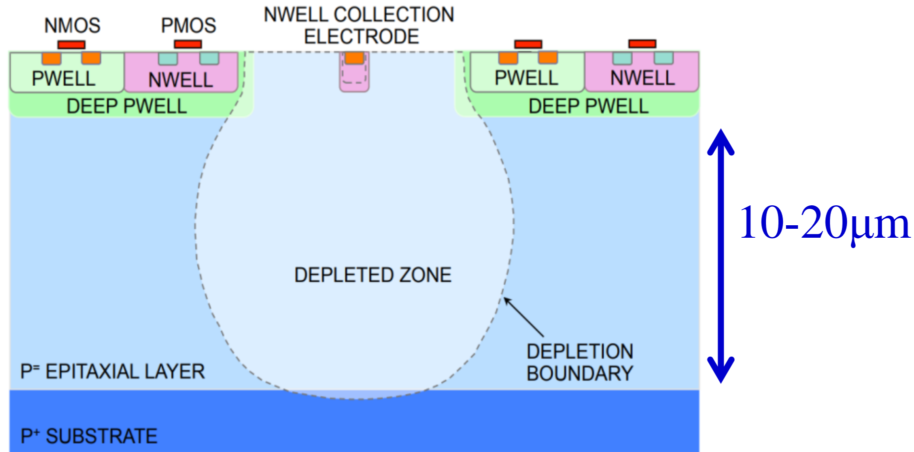
Hybrid detectors

Monolithic pixel sensors (MAPS)

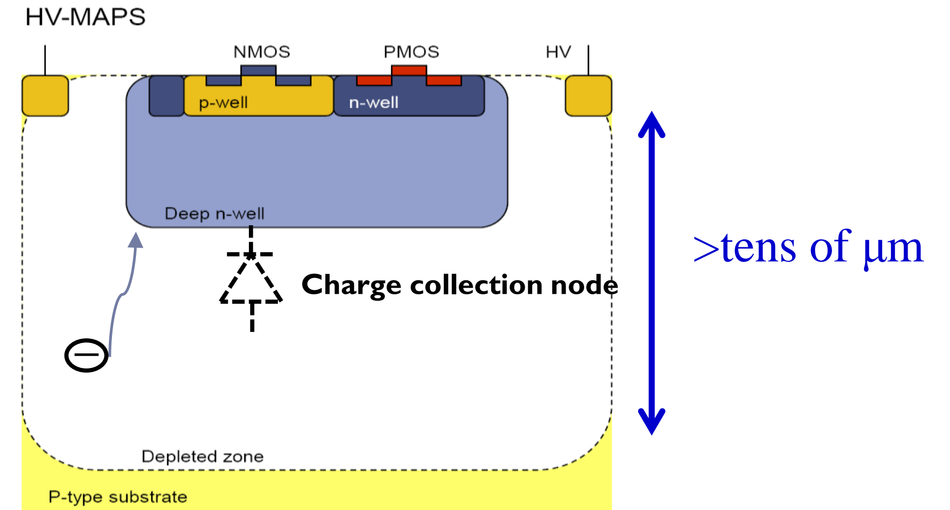
- The sensor and the readout ASIC optimized separately;
- Connected via Flip-chip bonding;

- The sensor and ASIC integrated on the same wafer,
- Easier to achieve low power consumption and low material budget;

Monolithic pixel sensor： small vs large charge sensing diode



Small sensing diode

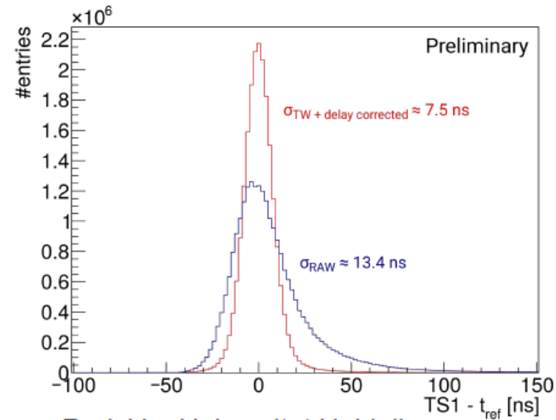


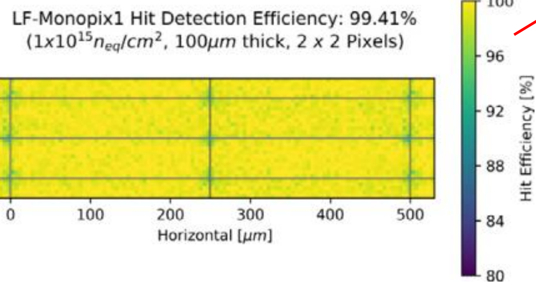
Large sensing diode

- Smaller input C--» low power， low noise;
- Higher biasing voltage: fast charge collection， high radiation tolerance (NIEL);

It is also called the "HV-CMOS pixel sensor"

Status of HV-CMOS Pixel Tracking Detectors





Chip	Pixel size [μm^2]	Array size	Noise [e-]	Power density [mW/cm^2]	Fluence [n_{eq}/cm^2]
AMS/TSI 180 nm					
ATLASPix1	60 × 50	56 × 320	~200	170	1×10^{15}
ATLASPix3	50 × 150	372 × 132	~60	~150	1.5×10^{15}
MuPix10	80 × 80	256 × 250	75	190	
MightyPix1	55 × 165	29 × 320			
LFoundry 150 nm					
LF-Monopix1	50 × 250	129 × 36	~200	~288	10^{15}
LF-Monopix2	50 × 150	340 × 56	~100	~400	
RD50-MPW1	50 × 50	40 × 78			2×10^{15}
RD50-MPW2	60 × 60	8 × 8	~50		2×10^{15}
RD50-MPW3	62 × 62	64 × 64	~900		
RD50-MPW4	62 × 62	64 × 64	480	~600	3×10^{16}
CACTUS	1000 × 1000	7 × 6	~2k		

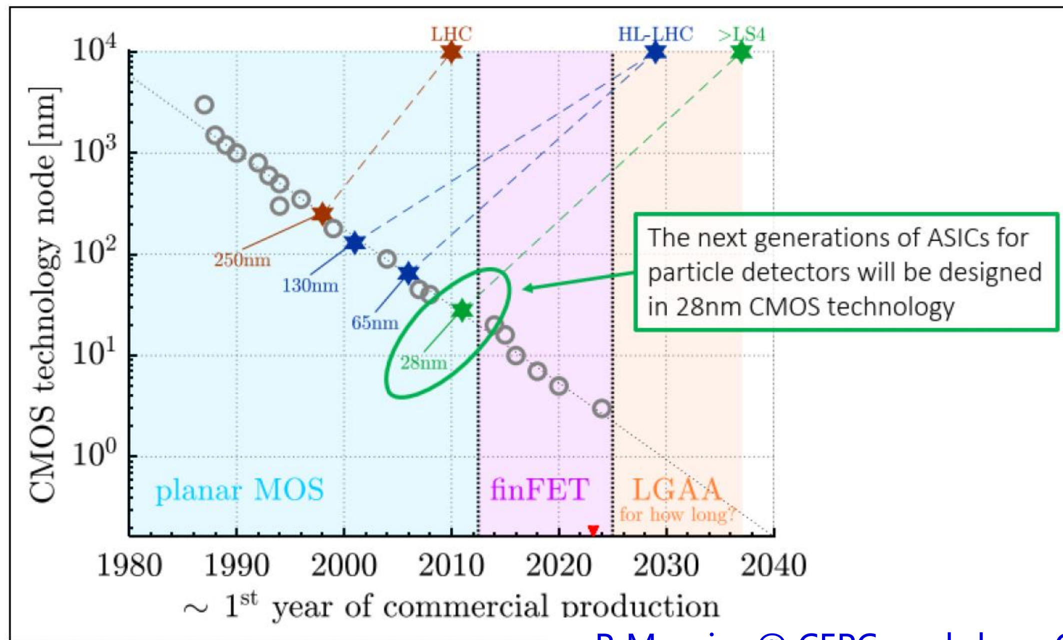
The HV-CMOS pixel sensor has been selected for Mu3e experiment (The only HV-CMOS detector used in current experiment).

- ~ns time resolution;
- NIEL >10^{15} n_{eq}/cm^2;
- Validated in 180 nm/ 150 nm process;

Why 180nm → 55nm?

The primary reason is **safety concern:**

- TSI stopped services for the HV-CMOS 180nm process at the end of 2023, directly impacting the production of the Mu3e and LHCb MT upgrade chips. Installation delayed, sensor design and validation has to move to AMS technology;
- The process should provide stable support for mass production in next 10 years.



P. Moreira @ CEPC workshop, Oct 2023

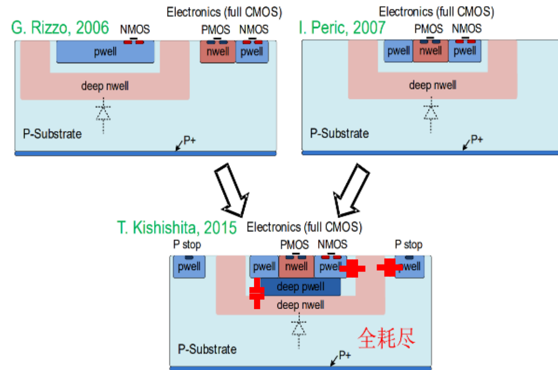
The second reason is **the drive of technological development:**

Better readout ASIC performances:

- ✓ **lower Power/function;**
- ✓ **Higher speed;**
- ✓ **Higher TID;**
- ✓ **Smaller dead area;……**

Main development steps to do from 180nm - > 55nm

1. Process exploration and modifications: for sensor optimizations

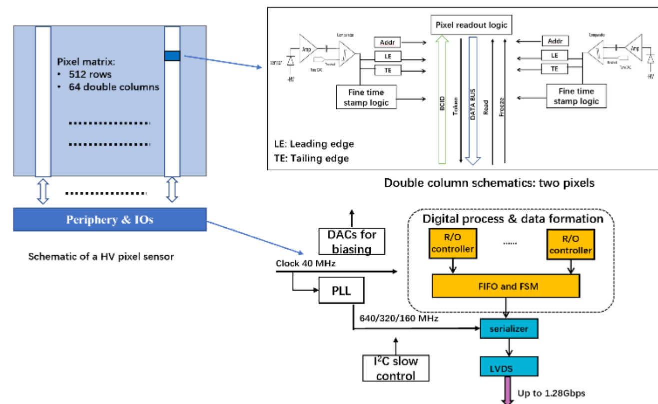


Example of the process development in the history: 2well -> 4 wells in-pixel, substrate resistance ~Ω·cm -» several k Ω·cm

- Well structures, injection concentration, depth;
- Sensor pitch size, gaps, p-stops;
- Resistance of the substrate;
- Guard ring structures;

……

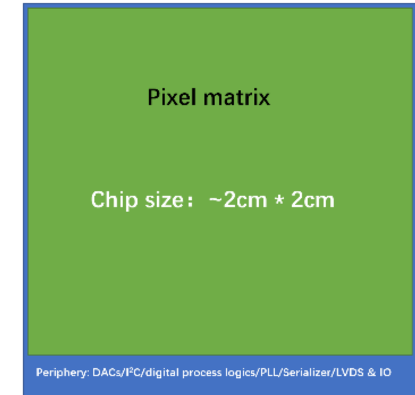
2. Pixel array readout scheme and necessary functional modules design：



- In-pixel electronics;
- Organization for matrix readout;
- Periphery digital logics and functional IPs;
- Slow control & Fast control….
- Data/Power/CLK interfaces……

……

3. Full-size full-function sensor performances optimization



- Time resolution;
- Power dissipation;
- Detection efficiency & fake hit rate;
- Radiation Influences (NIEL, TID, …);
- Yield;
- Material;

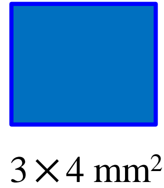
……

Prototypes in 55nm HV-CMOS Process

CMOS SENSOR IN FIFTY-FIVE NM PROCESS

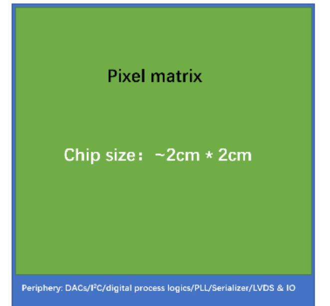
2023 Several MPWs to reach the full-size full-function sensor 2027

Time line



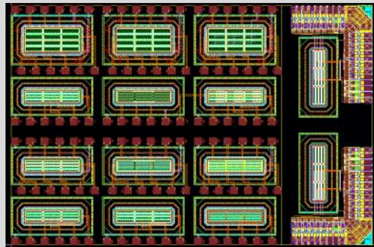
3×4 mm^2

¼ of the full size



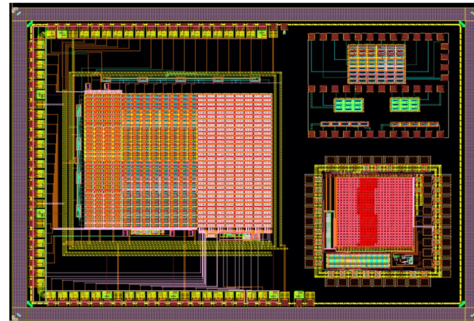
HV process

COFFEE1

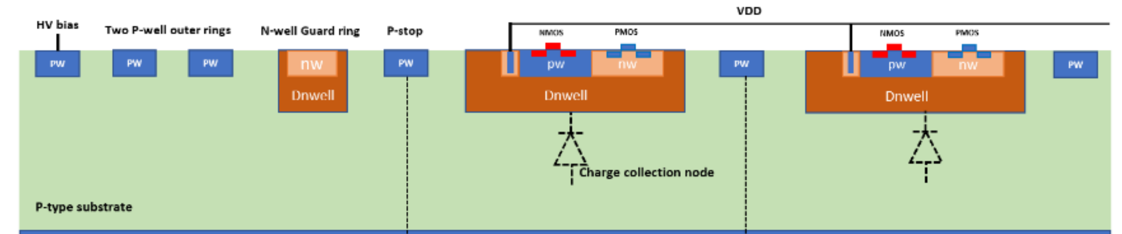


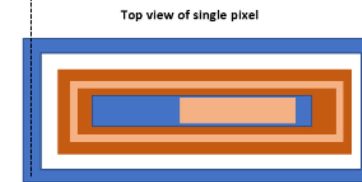
Submitted 2022.10

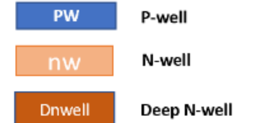
COFFEE2



Submitted 2023.8/received 2023.12







- In 55nm Low-leakage process;

  Verified not a suitable process for this development.

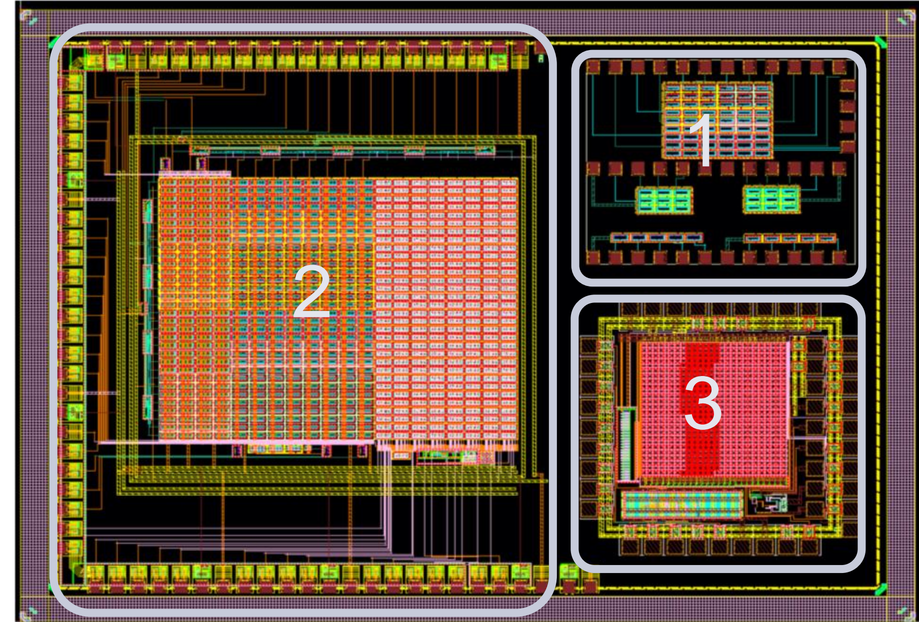
The fist prototype in 55nm HV-CMOS process, which is dedicated to the validation of "the new process" & "a new pixel array readout architecture"

HV-CMOS process cross-section diagram showing the guard ring and pixel structure.

COFFEE2: design overview

Three independent regions in COFFEE2:

1. **Passive diode arrays:**
   - Various sensing structures: DNW size, distances, with/without P-stop ;
2. **An active pixel matrix including 3 variations of pixel design:**
   - To quantitatively evaluate the “cross-talk" issue of HV-CMOS pixel sensor technology in the new process and guide the overall design of the future detector chip
3. **An active pixel matrix with a new readout architecture:**
   - Very small pixel size $25 \times 25 \mu m^2$ (for a HV-CMOS pixel sensor);
   - New matrix readout architecture;
   - Digital peripheral data processing included;



The COFFEE2 design includes three independent regions.

Published paper: NIMA Volume 1069 P169905 (2024)
https://doi.org/10.1016/j.nima.2024.169905

1st region: passive diode arrays

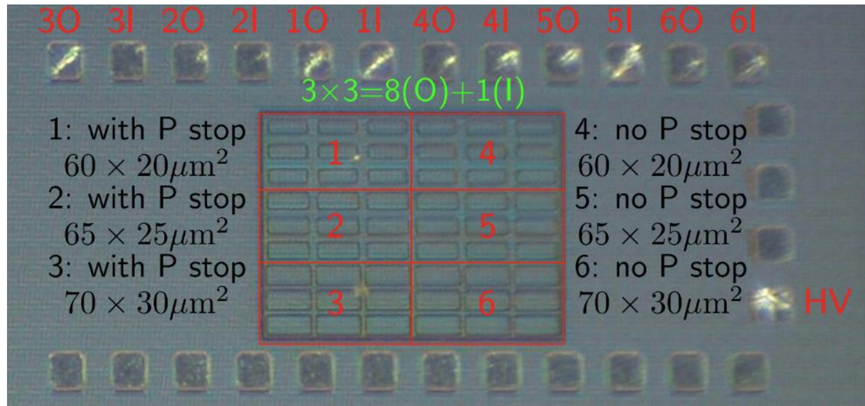


Photo of passive diode array in COFFEE2：

- pixel size 40μm×80μm;
- 6 sub-arrays of different design structure；

Table: details of 6 sub-arrays: various of DNW size, distance, with/without P stop

Diodes flavor	Specifications	
Pix_D10core	Single DNW size: 30μm×70μm, distance between two diodes 10μm	With P stop
Pix_D10core_wps		Without P stop
Pix_D15core	Single DNW size: 25μm×65μm, distance between two diodes 15μm	With P stop
Pix_D15core_wps		Without P stop
Pix_D20core	Single DNW size: 20μm×60μm, distance between two diodes 20μm	With P stop
Pix_D20core_wps		Without P stop

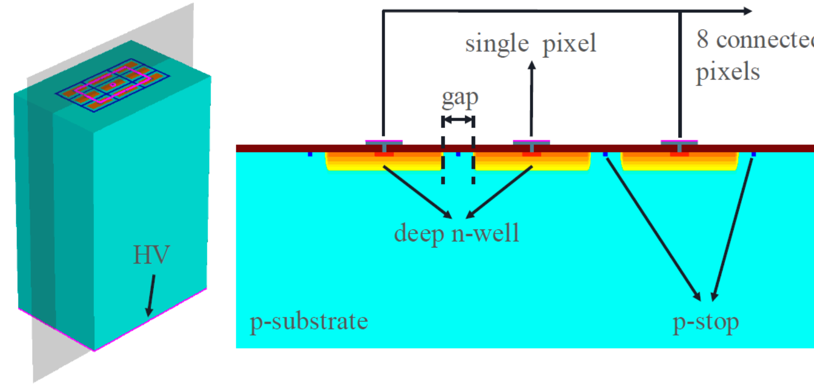


Figure: 3D and 2D cross-sectional views of the HV-CMOS structure.

- **gap**: 10/20/30 μm
- **p-substrate**
  Resistivity: 10/100/500/1000/2000 Ωcm
  Depth: 500 μm
- **deep n-well**
  Gauss profile: $5*10^{17} \sim 1*10^{17}$ cm^{-3}
  Depth: 5 μm
- **p-stop isolation**
  Concentration: $1*10^{19}$ cm^{-3}
  Depth: 2 μm

* Process profiles are from experience not the foundry

TCAD simulations are conducted.

- *About simulation, please see Jianpeng Deng's poster (ID:55) "TCAD Simulations of HV CMOS";*
- *About test, please see Zhiyu Xiang's poster (ID: 21)"Test of CMOS chip using 55nm process";*

1st region: TCAD simulation Vs test results

TCAD simulation

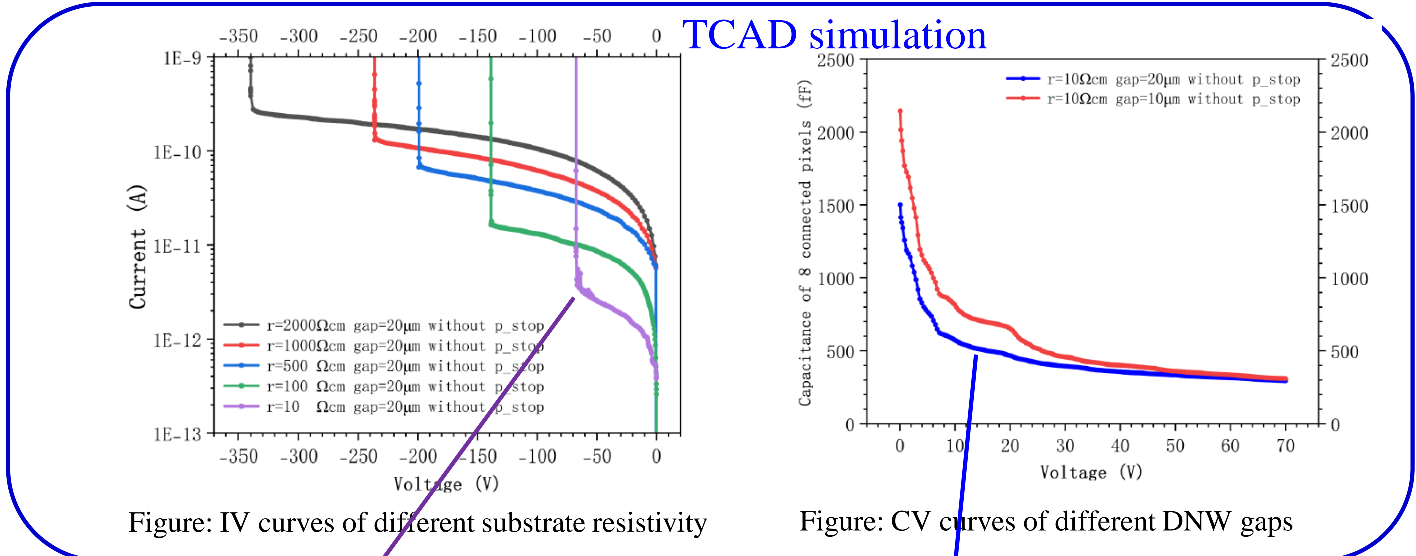
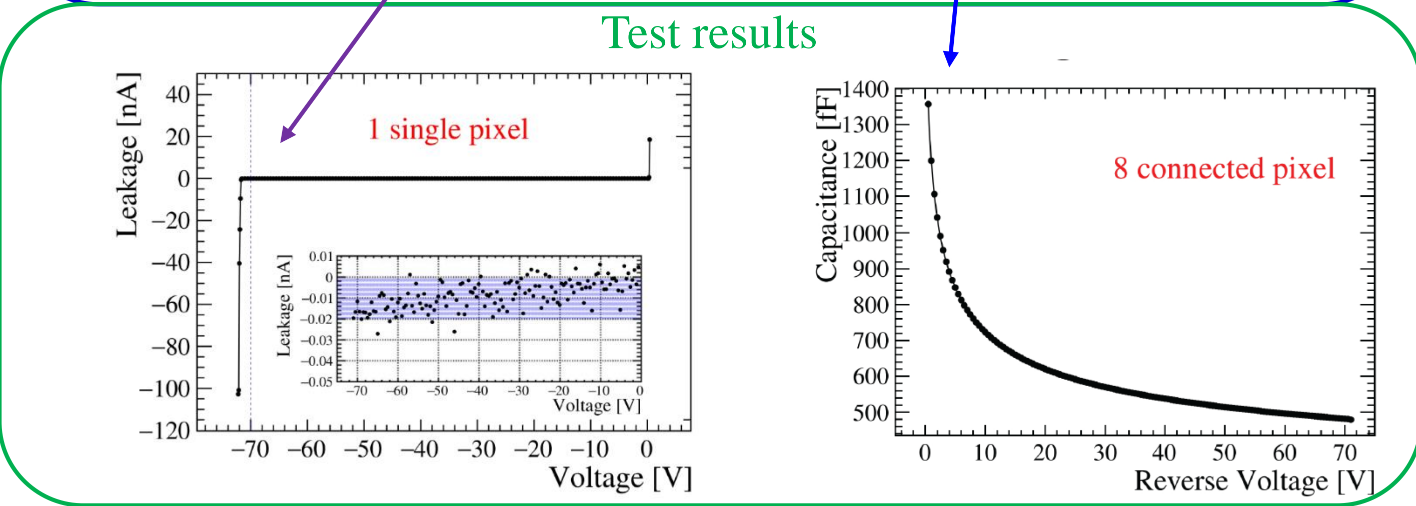


Figure: IV curves of different substrate resistivity

Figure: CV curves of different DNW gaps

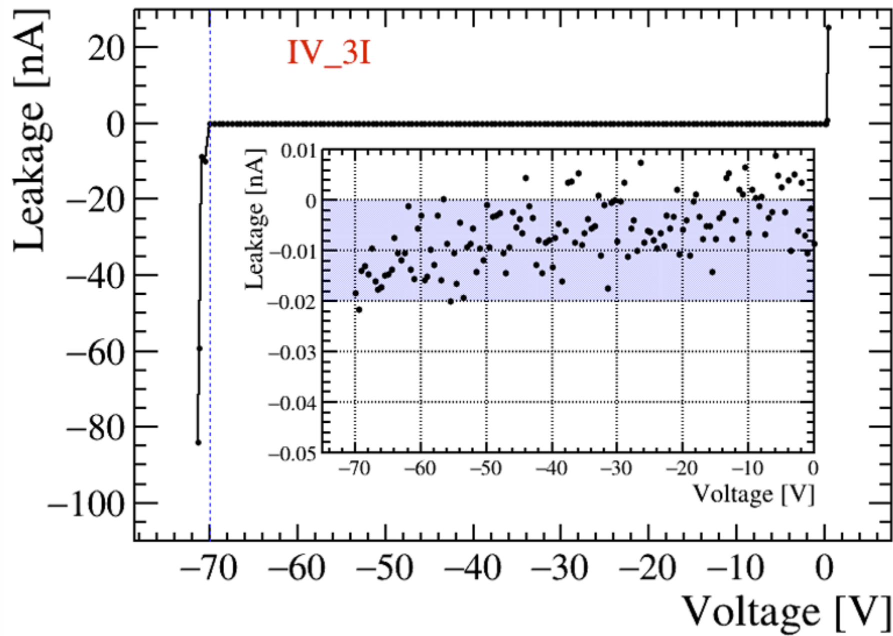
Test results

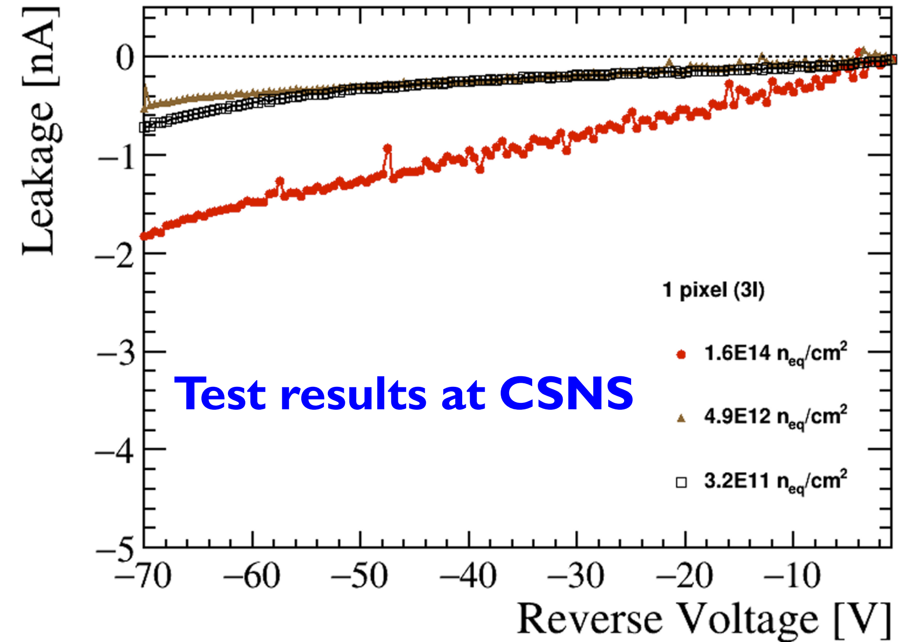


TCAD simulation results are confirmed through testing.

- Current substrate resistivity (10 Ω·cm) limits the break down voltage of the sensor at ~70 V. (Could be significantly increased for a substrate with higher resistivity)
- The diode equivalent capacitance reaching ~40 fF/pixel at ~70V. (Decreases as the bias voltage increases)

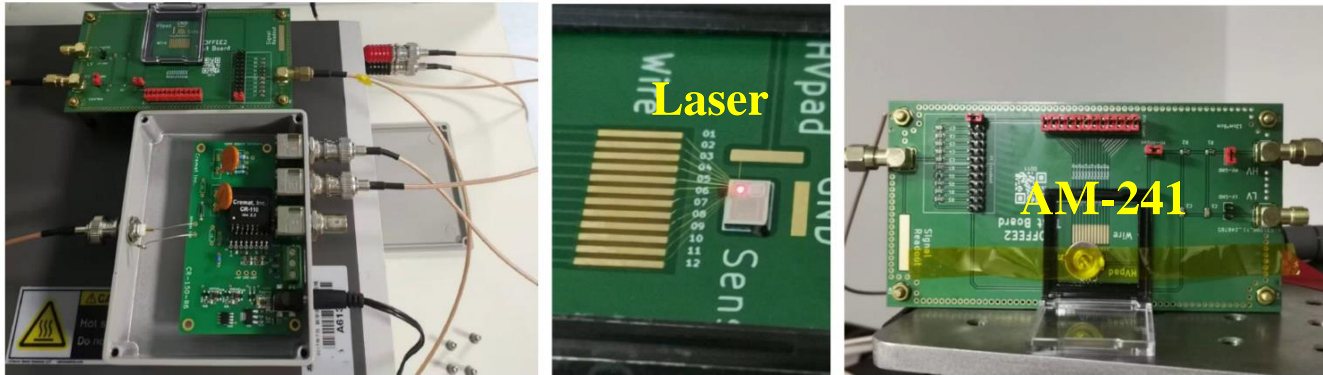
1st region: leakage current after radiation



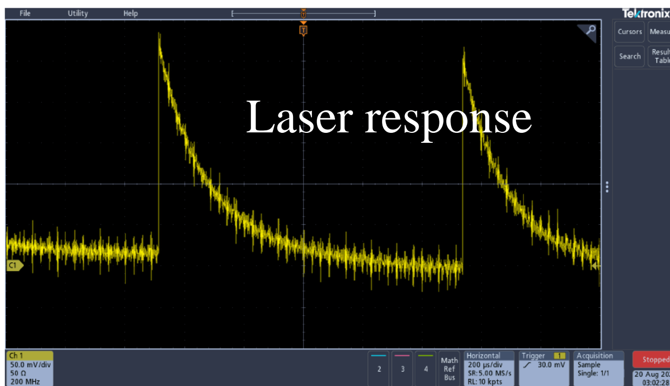


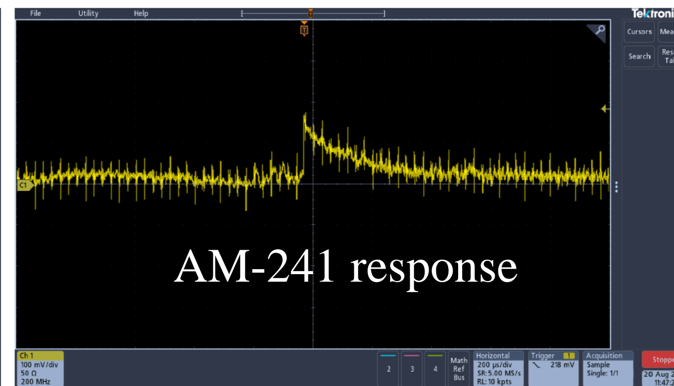
- Leakage current increased from 0.01 nA / pixel to ~1 nA /pixel （Biasing at 50V） after 10^{14} n_{eq}/cm^2 radiation.

1st region: test results of signal response



The test setup





Passive diodes are connected to an external Charge Sensitive Amplifier:

- sensor responses to both a laser and AM-241 source have been observed.
- Further calibration tests are pending for the active pixels.

1st region: Allpix² simulations for pixel response to MIP

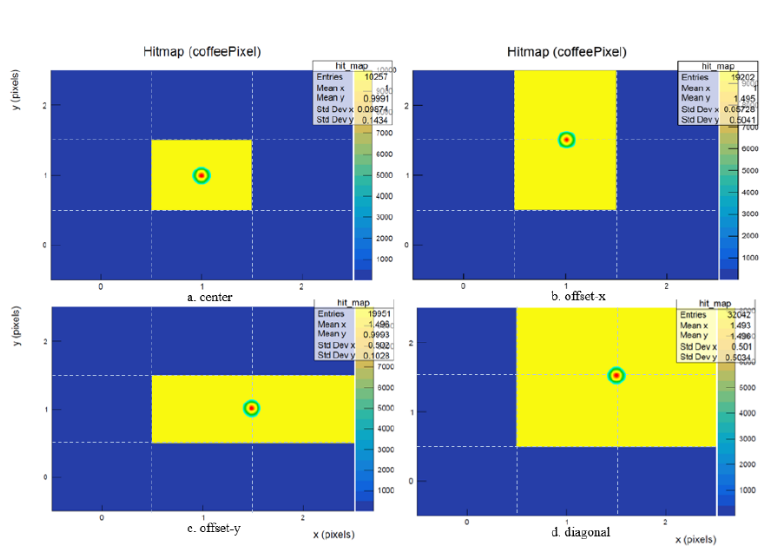
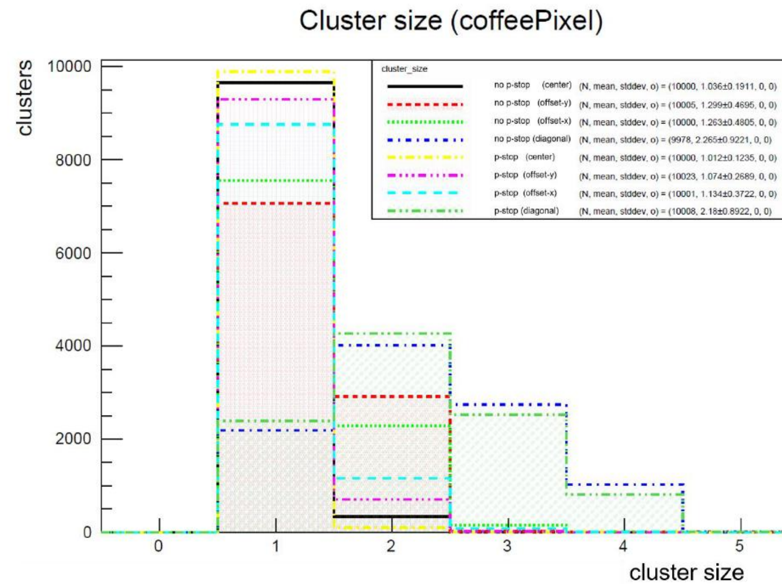


Figure: Hitmap at 4 different incident positions.



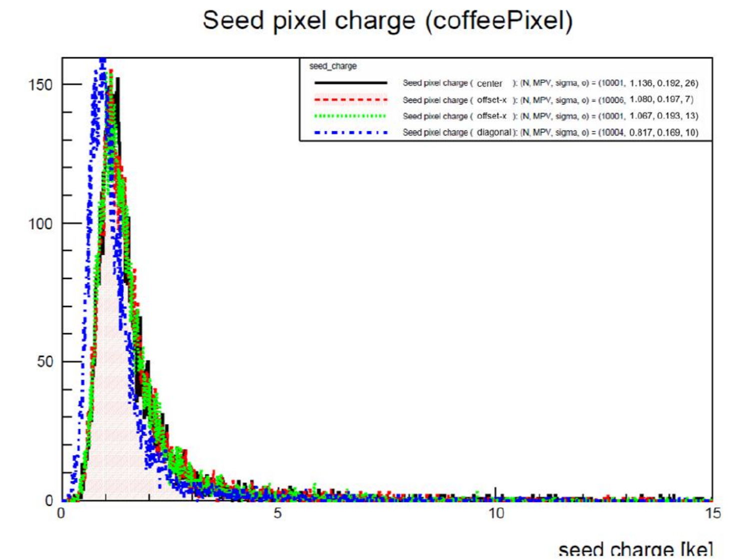


Figure: Distribution of the seed pixel signal.

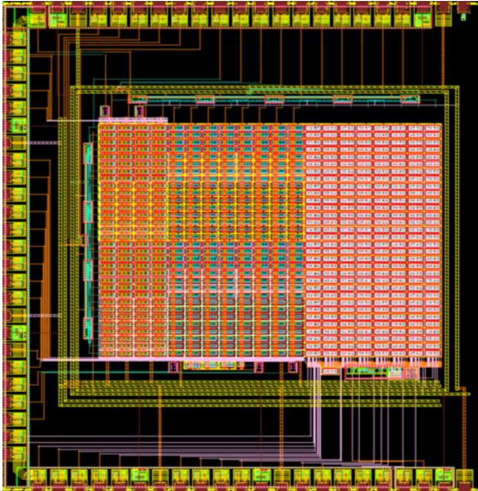
Simulation configuration details：

- 3×3 pixel array；
- 10 Ω·cm substrate resistivity；
- Electric filed model from TCAD；
- 4 GeV proton beam (MIPs) used for simulation；

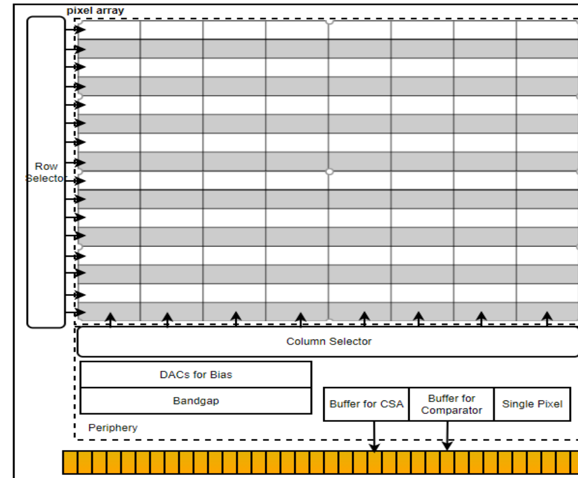
Simulation results ：

- Cluster size ~1 for the center incidence, ~2.3 for the diagonal incidence;
- MPV of the landau distribution for seed pixel ranges from 0.8 – 1.1 ke⁻;
- The P-stop structure effectively reduces charge sharing;

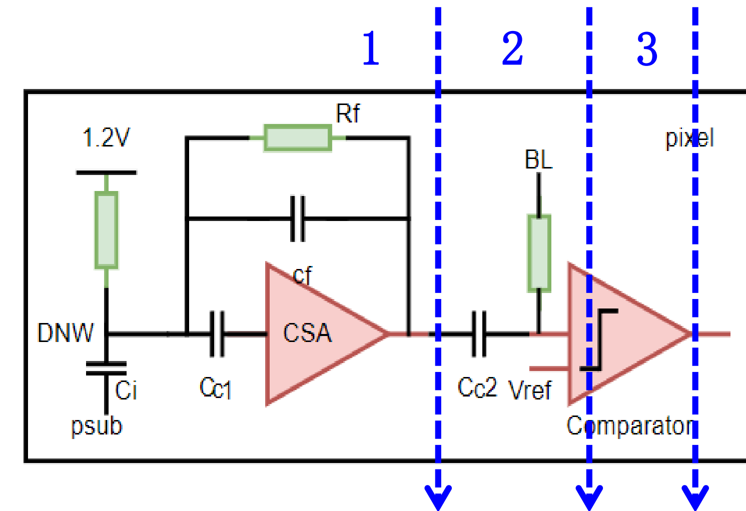
2nd region: an active pixel matrix



Layout of the 2nd region



Floor plan of the 2nd region

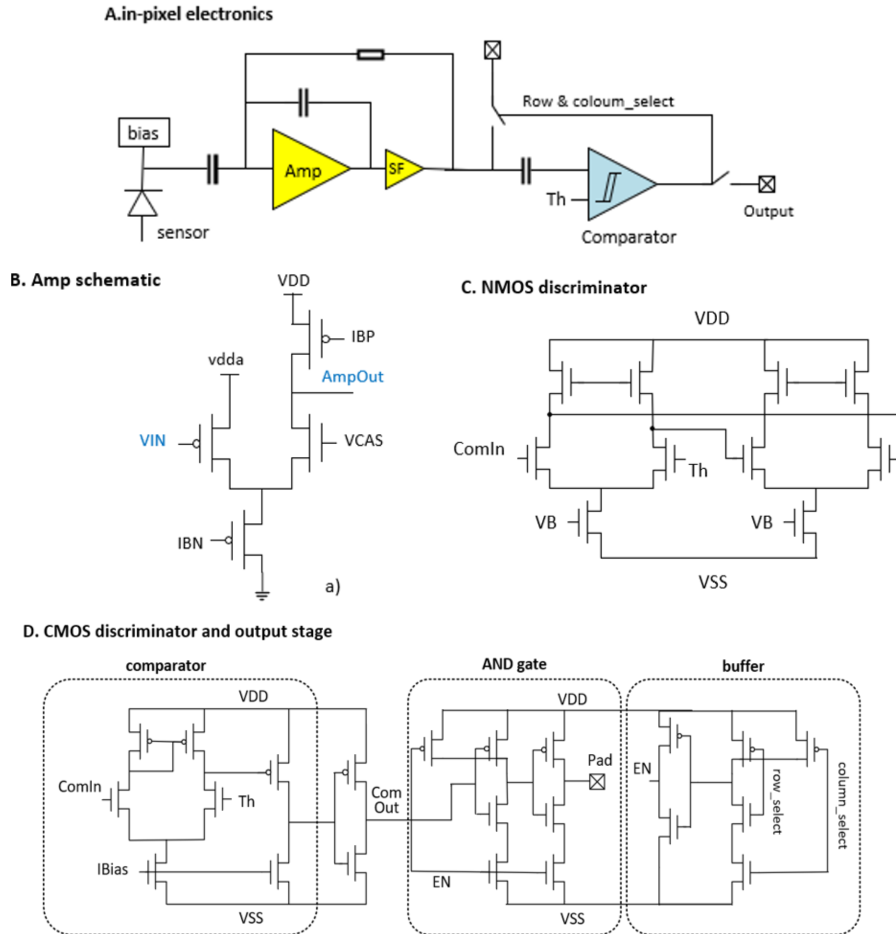


3 variations of in-pixel electronics

- A 32×20 active pixel matrix, peripheral modules including bandgap, analogue buffer, DACs and row/column selection;
- Three sub-arrays with different in-pixel electronics are included；
  1. Only CSA inside;
  2. CSA + NMOS Comparator;
  3. CSA + CMOS Comparator;

To evaluate the "cross-talk" issue in this new process and guide the overall design of the next detector chip.

2nd region: in-pixel design



Schematic of the in-pixel electronics

Simulation performances:

- CSA(for in-put capacitance ~100fF):

  ~ 140 e- Equivalent Noise Charge; ~57µV/e^- Charge to Voltage factor;

  4.6µA power dissipation;

- CMOS comparator:

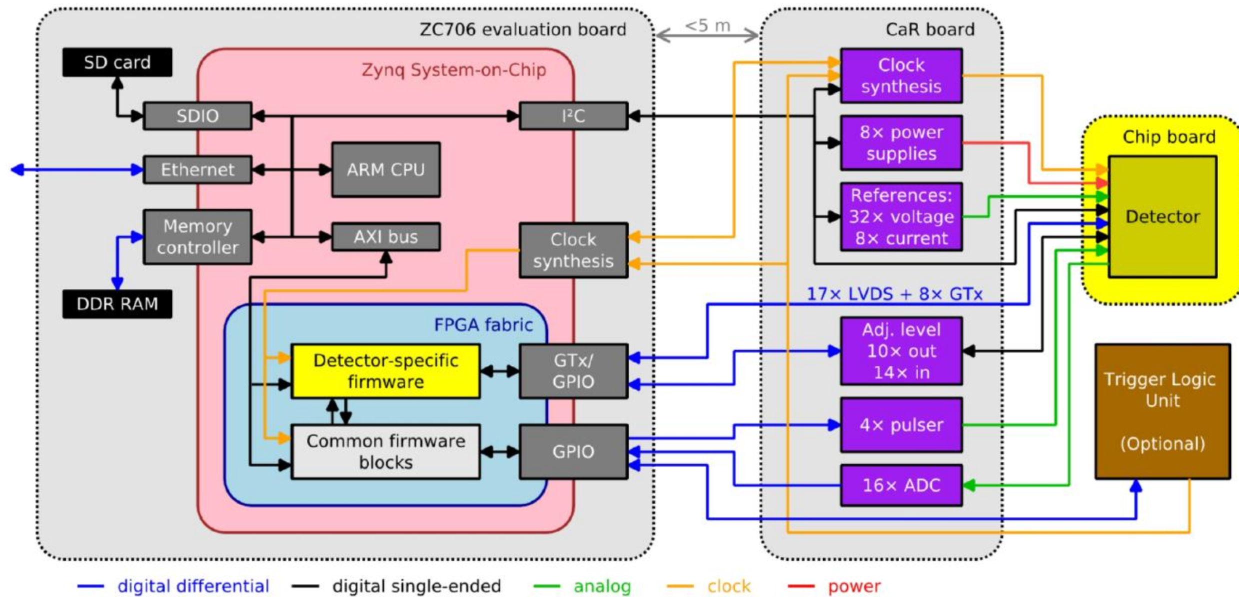
  Time-walk ~2ns; time over threshold ~5µs; 15µA power dissipation;

- NMOS comparator:

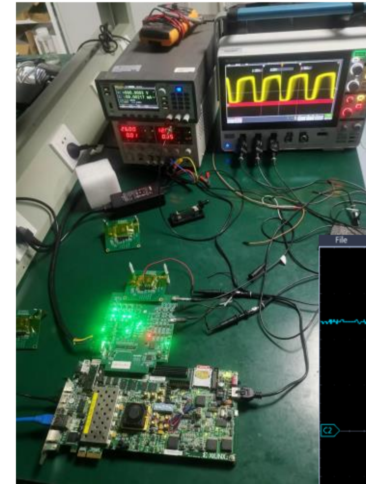
  Time-walk ~9ns; time over threshold ~5µs; 8.5µA power dissipation;

**About design details, please see Leyi Li's poster (ID: 53) "Design of coffee2: a pixel sensor prototype in 55nm high-Voltage CMOS process ";*

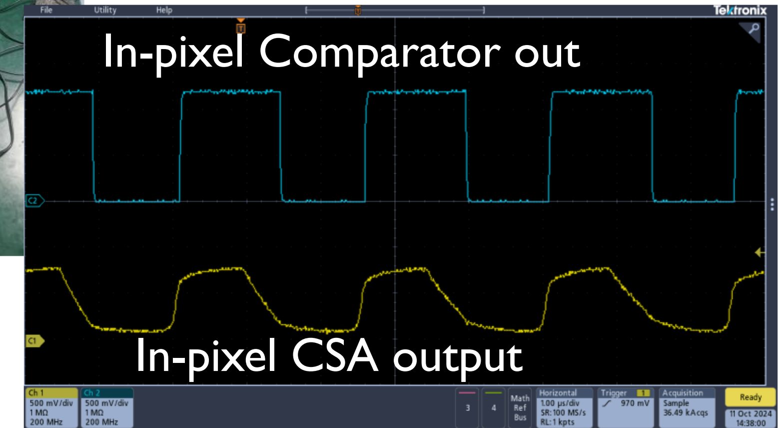
2nd region: test system



Test system block diagram: COFFEE2 chip carrier board – CaR board - ZC706 - PC



Picture of the test system

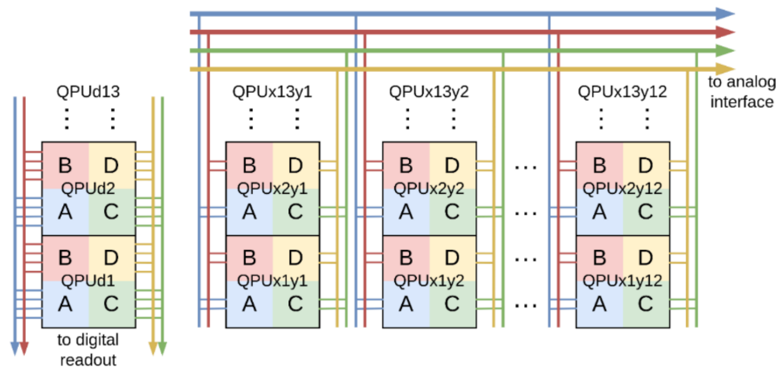


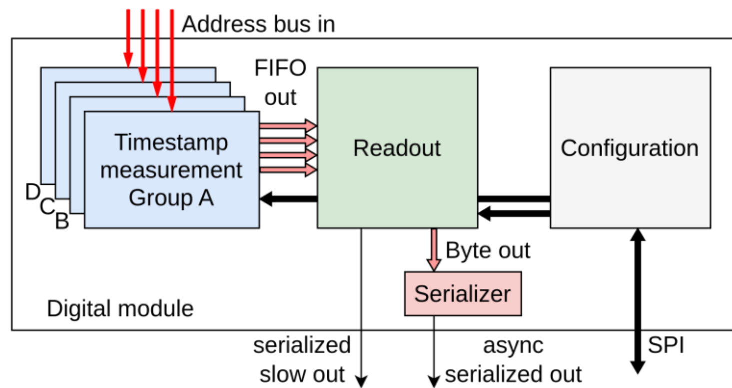
Pixel analogue & digital output

The adjustment of the test system and interpretation of the preliminary test results is in progress.

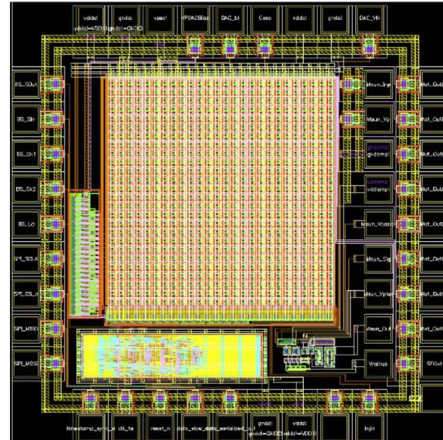
3rd region: design

Karlsruhe Institute of Technology

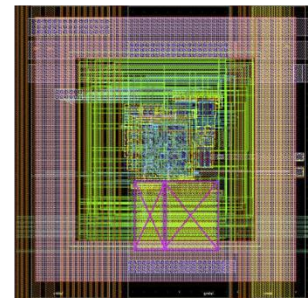




Floor plan of the 3rd region



Prototype Layout



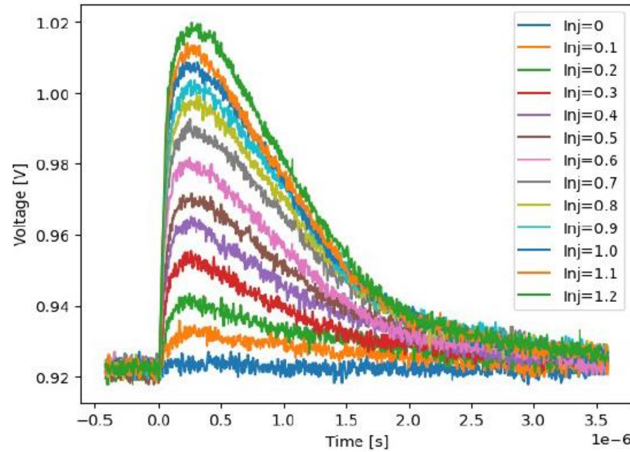
Pixel layout:25×25μm^2

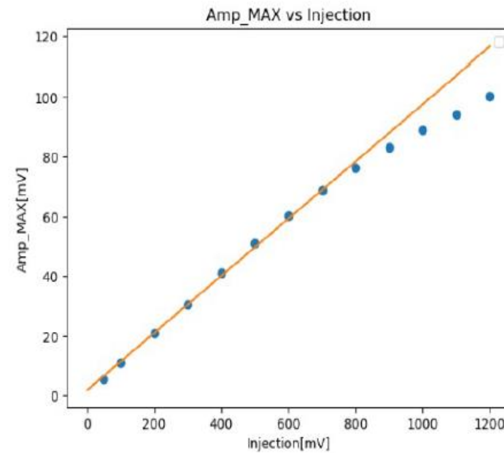
@ designed by KIT group

1. A 26×26 pixel matrix with very compact pixel size was realized: 25×25μm^2
   - In-pixel CSA + NMOS comparator; *(no cross-talk issues)*
2. A new matrix readout scheme was used:
   - Address encoded in pixel matrix; significantly decrease number of lines required for routing (*compared with ALTASpix solutions, where each pixel has an independent readout)*
3. A Digital periphery also included:
   - Bin size for time stamp : 5ns
   - Data information 3

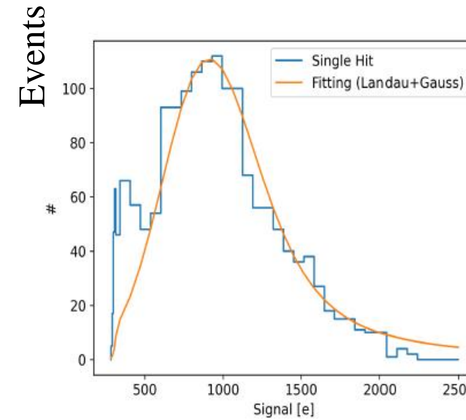
error_bit	addr[3:0]	hit_id[7:0]	lead_ts[11:0]	trail_ts[11:0]

3rd region: preliminary test results

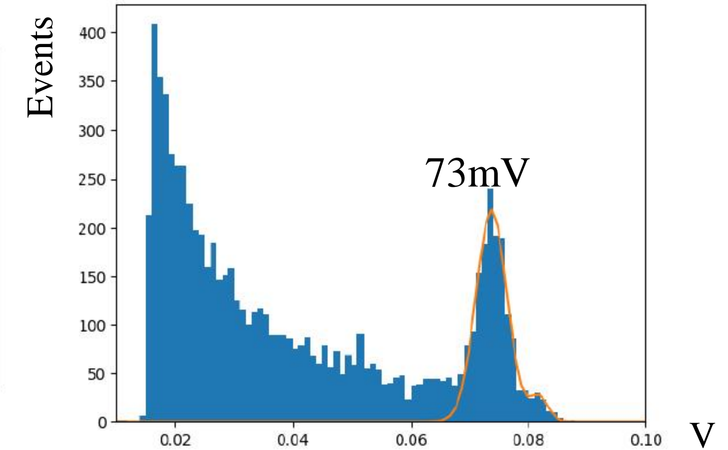




CSA outputs with different inject charges



Test results of Sr-90, MPV ~1000 e⁻



Test results with ^{55}Fe source

Sensor biasing condition: 30 V

Noise: ~50 e^-

** Reported by Hui Zhang "High voltage monolithic pixel sensor in 55nm technology", 30/9 - 4/10 , TWEPP 2024*

Summary & Outlook

- We are developing the HV-CMOS pixel detector technology roadmap in the 55nm process (COFFEE), with CEPC ITK and LHCb UT upgrades as application targets.
- COFFEE2 is the first prototype based on HV-CMOS 55nm process， the sensing diode break down voltage > 70V；
- Testing and evaluation progressing well, and the preliminary test results are promising.
- Some process adjustments can improve detector performances, such as using a higher substrate resistivity. Optimization of the sensor, in close cooperation with the foundries, is also ongoing.
- The next prototype, COFFEE3, is currently in design, primarily aimed at validating the pixel array readout architecture and the necessary peripheral functional modules required for a fully functional chip. The tape-out is planned for spring 2025.

谢谢！