Versal FPGA based development for HEP

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Outline

- Introduction to our organization and the Versal project
- Progress on fundamental studies.
  - PAM4 data link, PCIe, AI engine, DPU.
- HLS, ML, AI engine: roadmap of FPGA methodology
- International collaborations
  - TYL/FJPPN: Japan-France collaboration project
  - DRD7.5a

Introduction to Collider Electronics Forum (CEF)

- Collide Electronics Forum (CEF):
  - Within Instrumentation Technology Development Center (ITDC) of KEK IPNS.
  - Motivated to provide a platform of common development on the electronics devices with new technologies for future collider experiments.
  - Established by M. Tomoto-san, M. Tanaka-san and Y. Ushiroda-san in 2022, mainly within E-sys, Belle II, and Energy Frontier groups of KEK IPNS.
  - Research proposal from each group can be made and discussed.
    Then the works of the project will be shared with the members in the forum.

- We will also promote the collaboration with other experimental groups.
  - Communication with SPADI-A: Unified DAQ system design for nuclear experiments in Japan.

- Our activities can be found at https://kds.kek.jp/category/2369/

- Core members: from ATLAS, E-sys, Belle II and ALICE/EIC
  - ATLAS: M. Tomoto (KEK), K. Nagano (KEK), J. Maeda (Kobe), Y. Horii (Nagoya)
  - E-sys: R. Honda, M. Tanaka, Y.-T. Lai
  - Belle II: T. Koga, S. Yamada, Y. Ushiroda (KEK)
  - ALICE/EIC: T. Gunji (CNS)

Application of FPGA in HEP experiments

- Belle II Central Drift Chamber (CDC):

CDC

Sense wire

Front-End Electronics

- Collect TDC and ADC waveform info.
- Zero suppression.

Optical link

Optical link

L1 Trigger signal

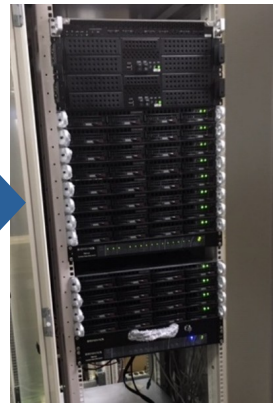
DAQ

Data readout / collector

PCIe / GbE

- Data collection.
- Data formatting.
- (Pre-)event building.

HLT / storage



L1 Trigger

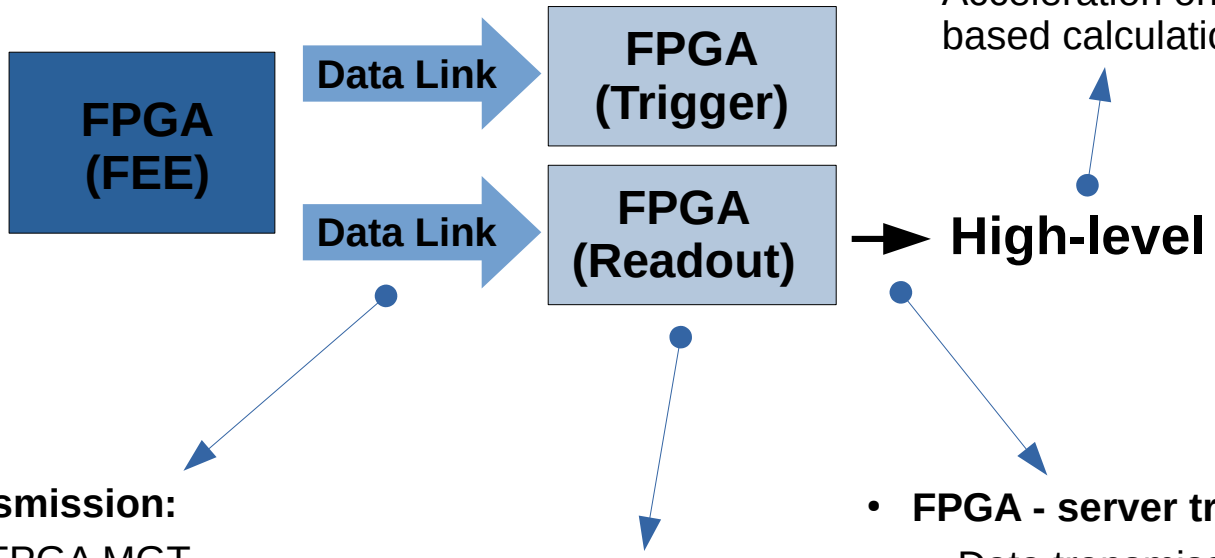
- Real-time complicated trigger algorithm for tracking / clustering / decision.

- For these application of FPGA device:
  - New technology for data transmission?
  - New technology for logic design in FPGA?
  - Impact on each aspect for experimentalists? For TRG, DAQ, or FEE?

Application of FPGA in HEP experiments (cont'd)

- **Our target:** Study the latest COTS FPGA devices and their associated new technologies for possible application and upgrade in different aspects of HEP experiments.

- **Hardware acceleration:**
  - Not only CPU, but also GPU and FPGA.
  - Acceleration on software-based calculation.



- **FPGA - FPGA transmission:**
  - Optical link with FPGA MGT and optical modules.
  - Non-Return-to-Zero (NRZ).
  - Different encoding based on protocol design purposes. e.g. 8B/10B and 64B/66B.
    - <10 Gbps for DAQ.
    - <25 Gbps for TRG.

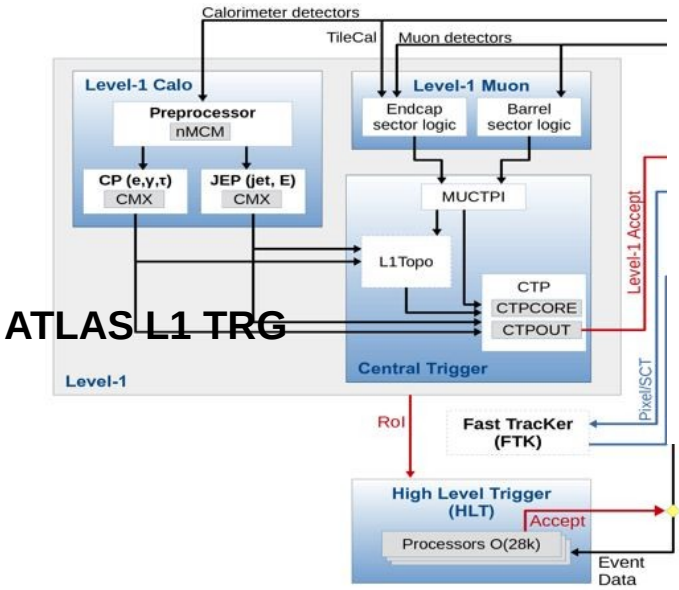
- Strong **FPGA devices** with:
  - Larger number of cells.
  - Larger data bandwidth.

  are critical for the usage in:
  - **TRG**: complicated algorithm implementation.
  - **DAQ**: collect and process large data.

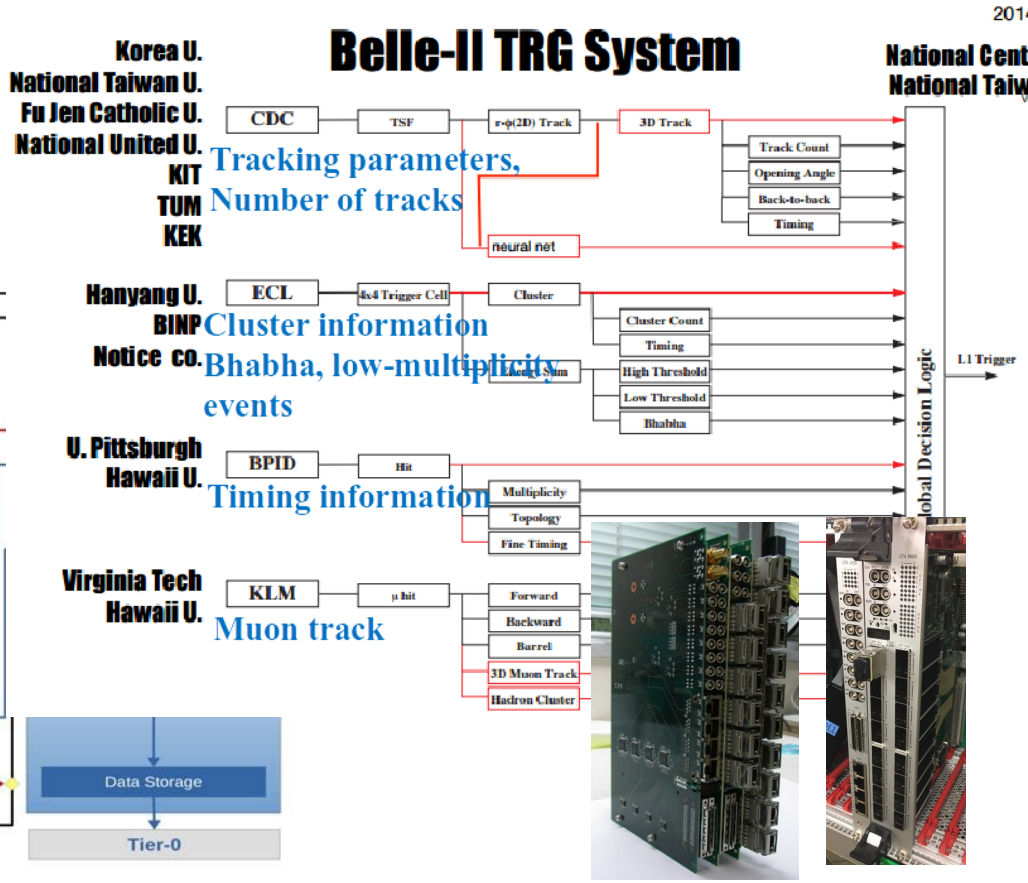
- **FPGA - server transmission:**
  - Data transmission and system slow control.
  - GbE, PCI-express, VME, etc.
  - PCI-Express is the most popular one nowadays: PCIe40 in ALICE, LHCb, and Belle II.

L1 Trigger system

- For TRG purpose, complicated algorithm is implemented to process detector raw data in real-time.
- Larger number of cells: improve the logic itself, resolution of triggering, and reduce the background rate.
- Utilization of machine-learning in the logic design.



ATLAS L1 TRG



Belle II TRG boards

Trigger device for Belle II and ATLAS

- For TRG purpose, complicated algorithm is implemented to process detector raw data in real-time. Utilization of machine-learning in the logic design became a trend recently.
- Strong FPGA with large resource: improve the logic itself, resolution of triggering, reduce the background rate, and perform everything within a latency limit.

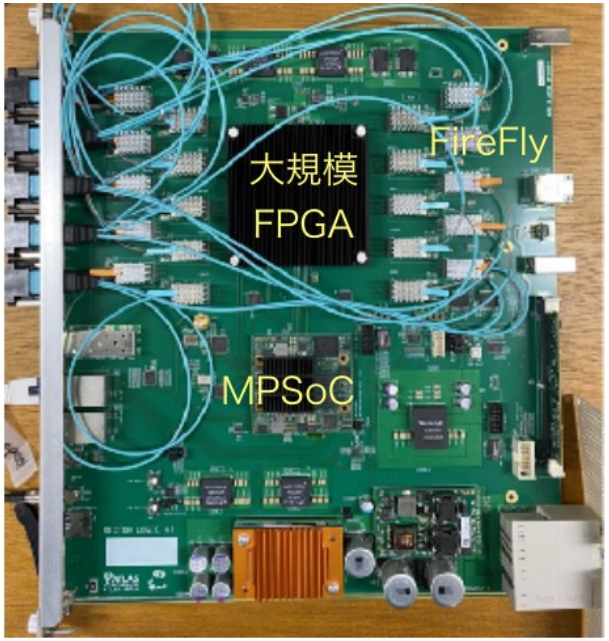
Belle II UT3

Xilinx Virtex-6
xc6vhx380t, xc6vhx565t
11.2 Gbps with 64B/66B

Belle II UT4

Xilinx UltraScale
XCVU080, XCVU160
25 Gbps with 64B/66B

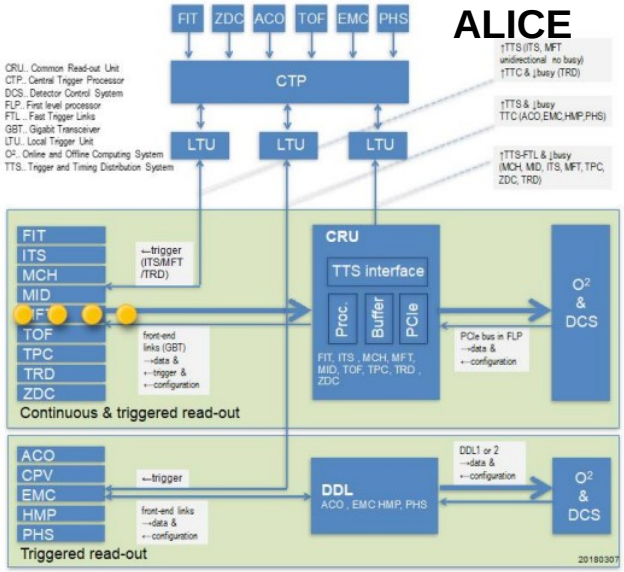
ATLAS Muon Trigger processor

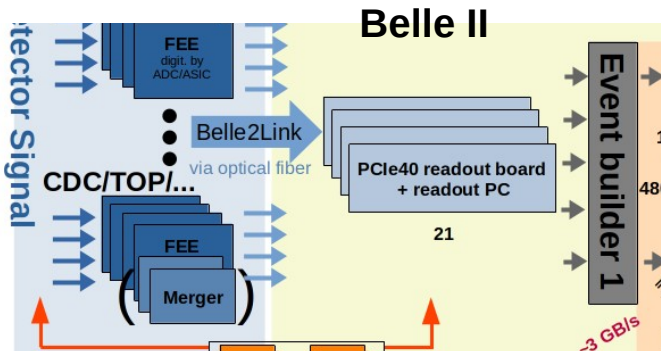


Xilinx UltraScale+
XCVU13P XCZU5EV
GTH,GTY: 16.8 Gbps
with 64B/66B

DAQ system

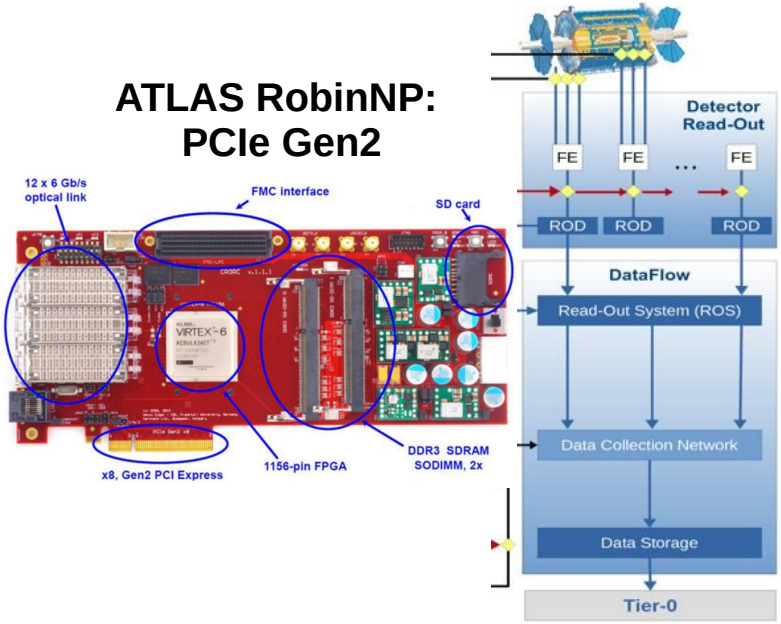
- Readout:
  PCIe has been the most popular solution for electronics → server interface.

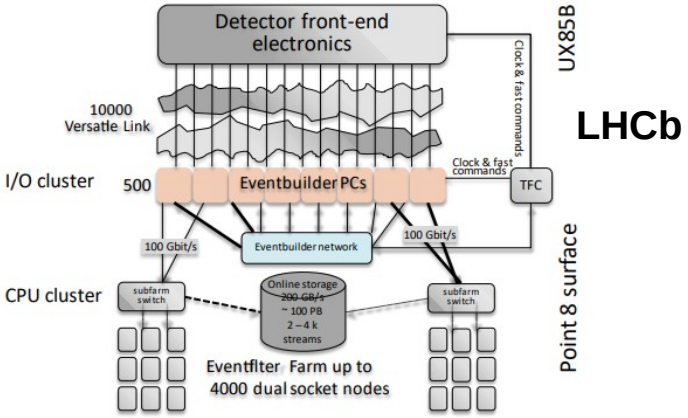




PCIe40: PCIe Gen3

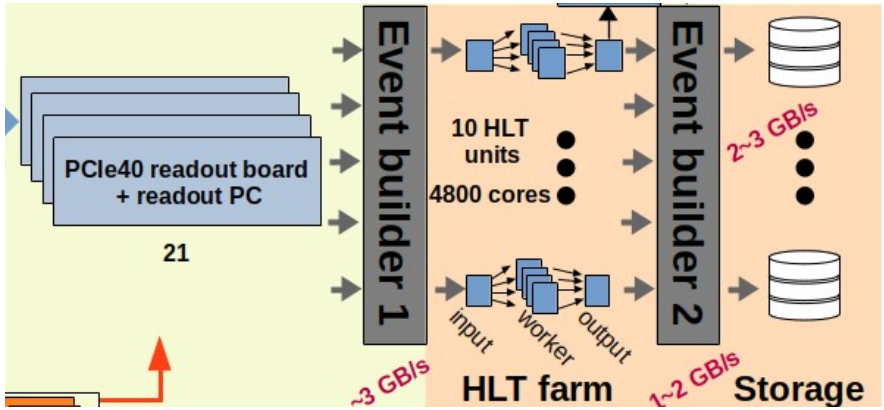
ATLAS RobinNP: PCIe Gen2





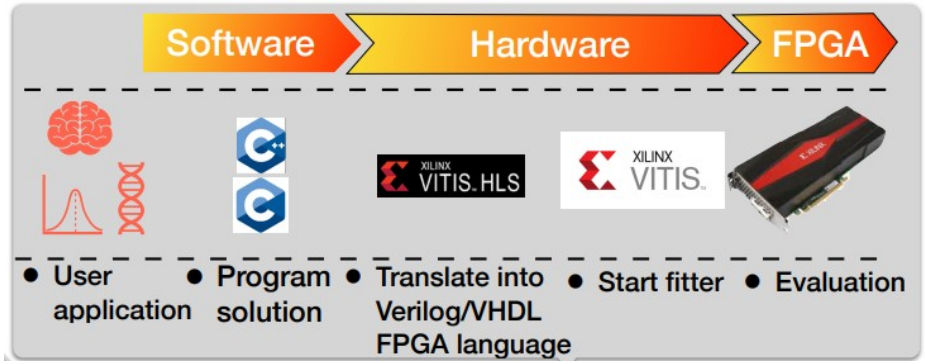
HLT (Belle II)

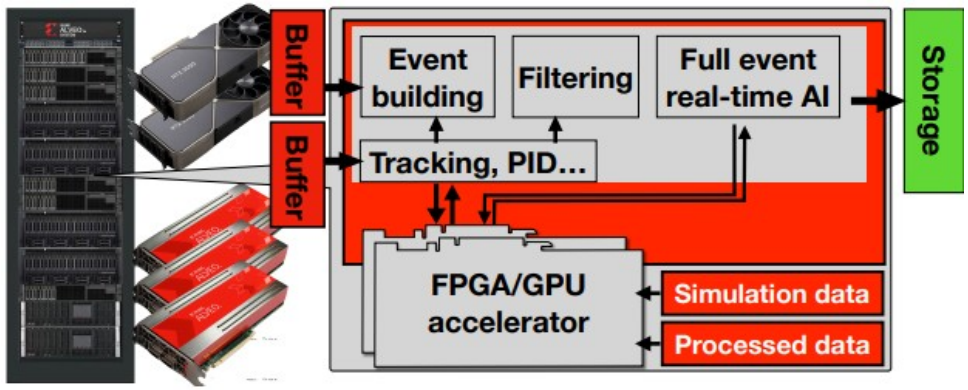
- HLT: Computing servers with reconstruction software.
  - In Belle II: HLT software = offline software.
- How about the options other than CPU?
  - GPU?
  - FPGA hardware acceleration?



source: Qi-Dong Zhou, Shandong Univ.

System	Processing power / HLT unit	Price (¥) / HLT unit	Ratio
CPU (Intel Xeon E5 2660)	480 cores	18,000,000	~6.5
GPU (GeForce RTX 3090)	12 GPU GPU : CPU ~ 40 : 1	GPU: ~180,000 x 12 = 2,160,000 Server: 600,000 x 3 = 1,800,000 Total : 3,960,000	~1.5
FPGA (VCK5000, Versal ACAP VC1902)	5 FPGA card Versal : CPU ~ 100 : 1	FPGA card : ~300,000 x 5 = 1,500,000 Server: 600,000 x 2 = 1,200,000 Total : 2,700,000	1





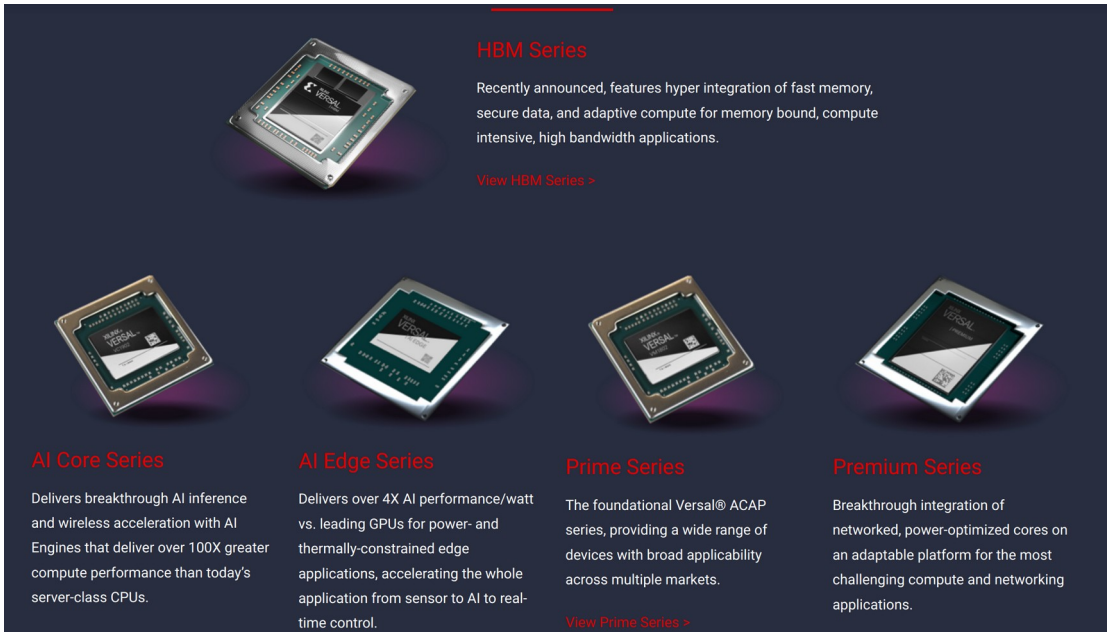
New technologies for TDAQ in HEP

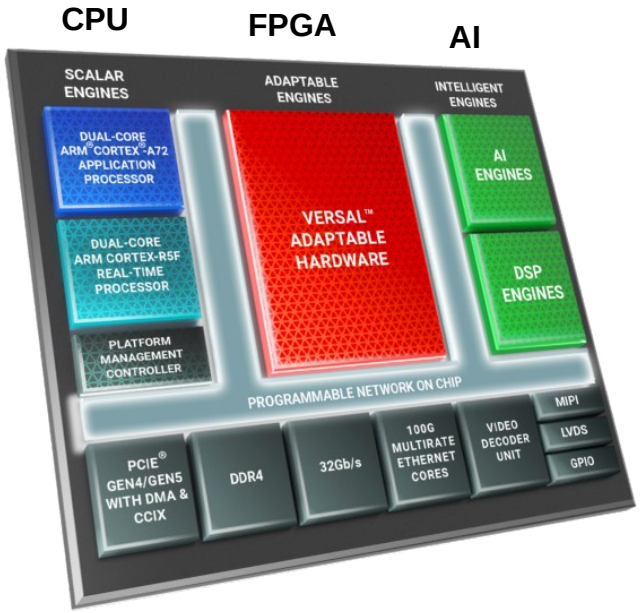
- **FPGA device**:
  - COTs, ACAP, SoC, such as Xilinx Versal, RFSoC, etc.
- **High-speed serial data transmission**:
  - From Non-Return-To-Zero (NRZ) to Pulse-Amplitude-Modulation (PAM4)
  - Optical module: QSFP, FireFly, other EOM.
- **Data readout**:
  - PCI-Express: PCIe40 (Gen3), PCIe400 (Gen5), FELIX (Gen4), Versal (Gen5)
  - Ethernet
- **Algorithm in FPGA**:
  - High-Level-Synthesis (HLS), ML inference, etc.
  - Xilinx Versal AI engine
- **Hardware acceleration**:
  - Xilinx Versal and Alveo acceleration card, Deep Processing Unit (DPU)
  - GPU

Versal project @ CEF

- Our project is mainly based on the Xilinx Versal series of ACAP.
- KEK together with Japanese HEP community purchased a few evaluation kits.
  - Plan: Common and general studies on the new technologies for future electronics device's R&D. Now we plan to use Versal for L1 TRG, DAQ or HLT purpose.

- The features of different Versal series ACAP:
  - AI engine: convenient interface to implement ML core into firmware.
  - High Bandwidth Memory (HBM).
  - Larger number of cells + High transmission bandwidth.





source: Xilinx website

Versal project: General plan

- Our goal: R&D of a new general FPGA device using the Versal ACAP.
  - A L1 TRG, DAQ, or HLT device, and also general for different experiments.
  - One clear target is **UT5 for L1 TRG of both Belle II and ATLAS**.

1st year:

- Study the properties of the **fundamental functionalities** with the kits:
  - GTM (PAM4), PCIe Gen5, AI engine, DPU, etc.
- Prepare basic application for each of them for other members.

Here we are now with VPK120 and VCK190.

2nd year:

- Make general transmission protocols for GTM (PAM4), PCIe Gen5, and do performance study.
- **Implement various Trigger algorithms** (Belle II, ATLAS, etc).
- Connect to existing systems to take real-time data and check performance.

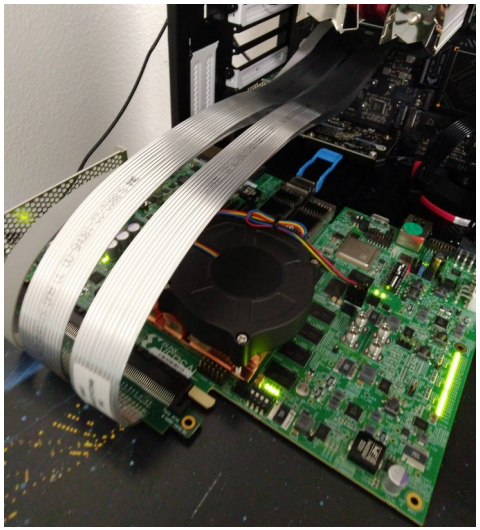
3rd year:

- **Future universal device**: L1 TRG, DAQ readout, or HLT.
  - Discussion.
  - Schematic/PCB design for the prototype boards.
  - Test with experiments people.

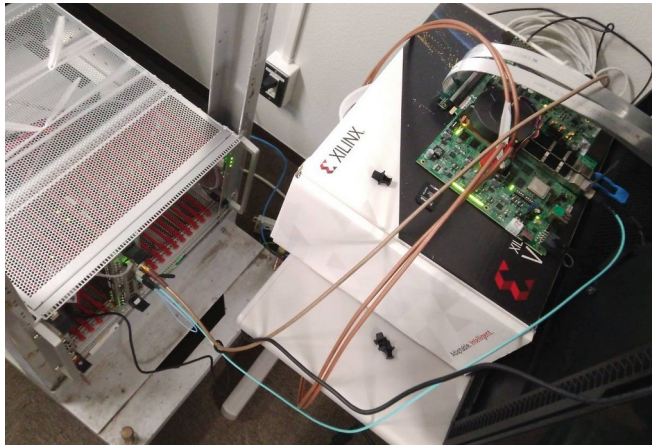
Test benches of Versal kits @ KEK E-sys

- Now we have both VPK120 and VCK190 test benches at KEK E-sys group with host servers.
  - They are opened and shared with our colleagues in CEF.

PC side: PCIe Gen5 x16 slot



VPK120 test bench:
2023 summer



VPK120 connection
to Belle II UT4

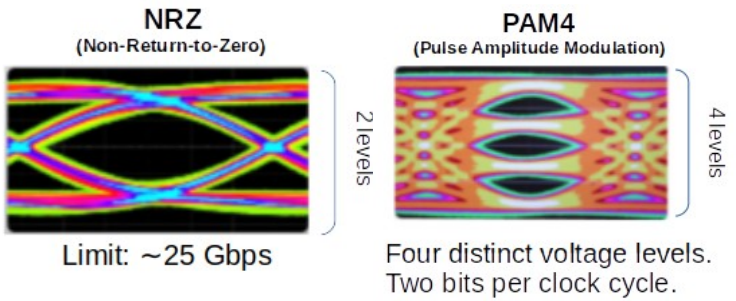
PC side: PCIe Gen4 x8 slot

VCK190 test bench:
2024 March

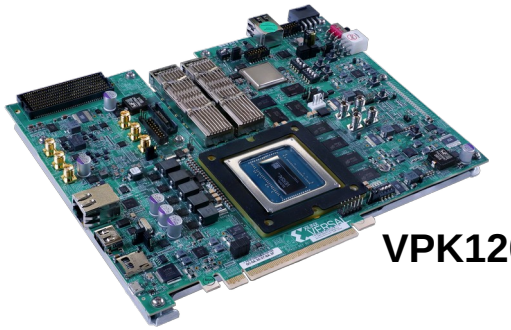
New technology in Versal FPGA: PAM4, PCIe, AI engine

- **Pulse Amplitude Modulation (PAM4):**
  - Four distinct voltage levels to break through the limit of Non-Return-to-Zero (NRZ), which is ~25 Gbps.
  - Using VPK120 to study it.
  - Suitable for high-speed link in L1 TRG.
    Hope to be pioneer to use it in future TRG board.

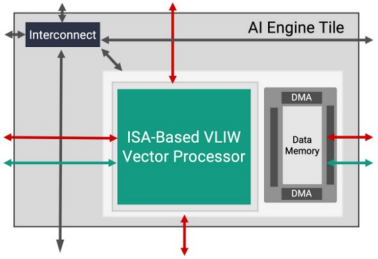
source: Xilinx

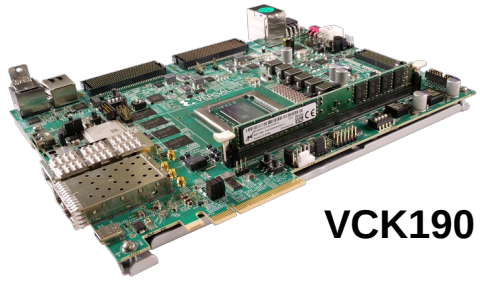


- **PCIe Gen5**:
  - PCIe has been popular option in HEP.
    - ALICE, LHCb and Belle II has been using PCIe40 (Gen3).
  - Study the properties of newer generation of PCIe is beneficial for the future readout device's development.
  - Using VPK120.



- **AI engine**: A new technology for data processing.
  - Help for our algorithm construction in TRG.
  - C programmable.
  - Together, we study many options of HLS and ML inference in FPGA, and their performance in different TRG algorithms.
  - Using VCK190.



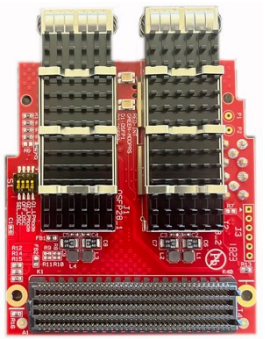


Data transmission with VPK120

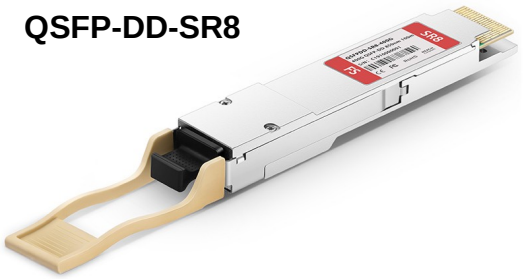
- GTYP: PCIe 5.0 (16) and FMC+ (8)
  - 1.25 ~ 32.75 Gb/s.
  - Various encoder supported.
  - Tested with the dual QSFP28 FMC module from HitechGlobal company.

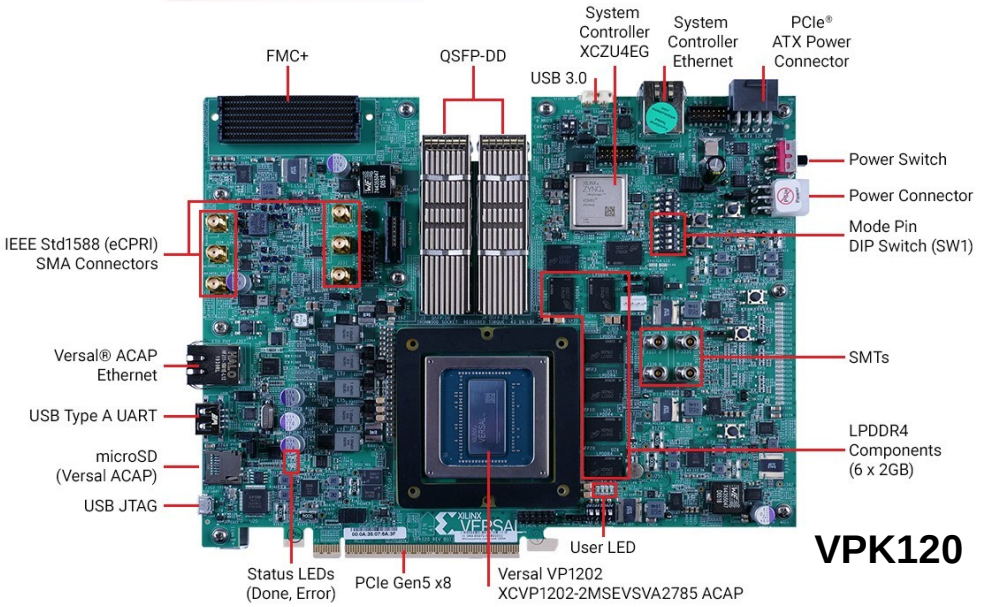
- GTM: QSFPDD (8*2)
  - NRZ:
    - 9.5 ~ 15, 19 ~ 29 Gb/s.
  - PAM4:
    - 19 ~ 30, 38 ~ 60 Gb/s
    - 76 ~ 112 Gb/s: "Half density mode" by combining two lanes.
    - No encoding is supported.
      Need to be make them manually in RTL.
    - Tested with QSGP-DD-SR8 from FS company.

Dual QSFP28 FMC



QSFP-DD-SR8





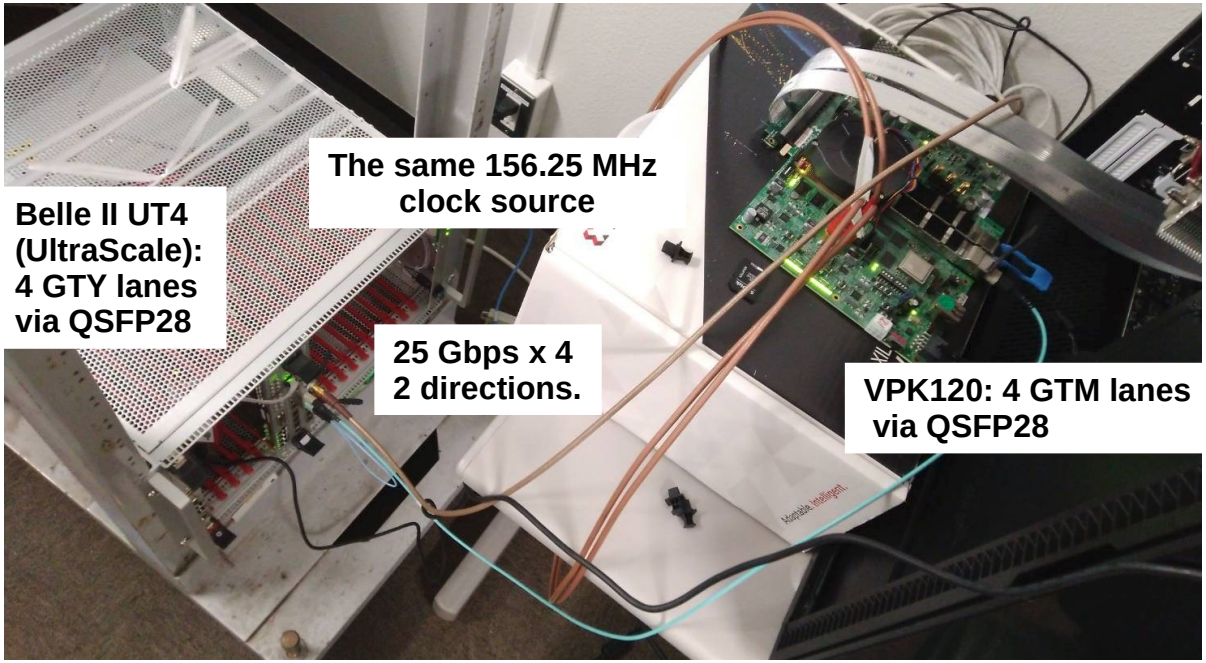
VPK120

Protocol development and connection test

- For GTM, we made a new generalized protocol with raw mode (no encoding).
  - Similar logic to my Belle II TRG protocol design.
  - (de)scrambler for DC balance.
  - Tested to be stable for both NRZ and PAM4.

- Using this new generalized protocol, connection test (25 Gbps x4, NRZ) between Belle II UT4 and VPK120 has been also tested. Stable in few hours.

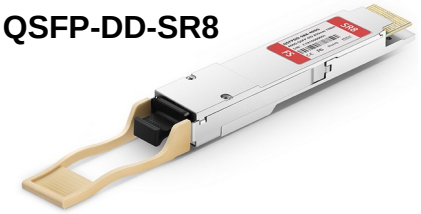
Belle II UT4



Transmission test with PAM4 and QSFPDD

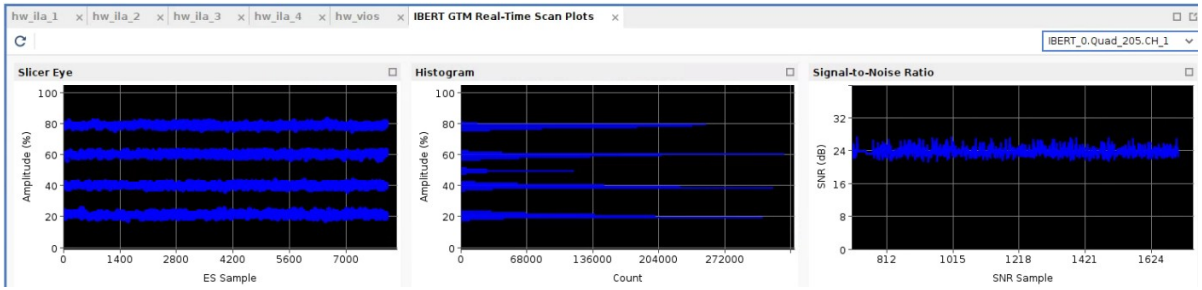
- We have successfully tested the real transmission with PAM4 and QSFPDD:
  - QSFPDD-SR8 with MPO16, from FS company.
  - 53.125 Gb/s x 16 lanes.
    - Only this line rate is supported.

QSFP-DD-SR8

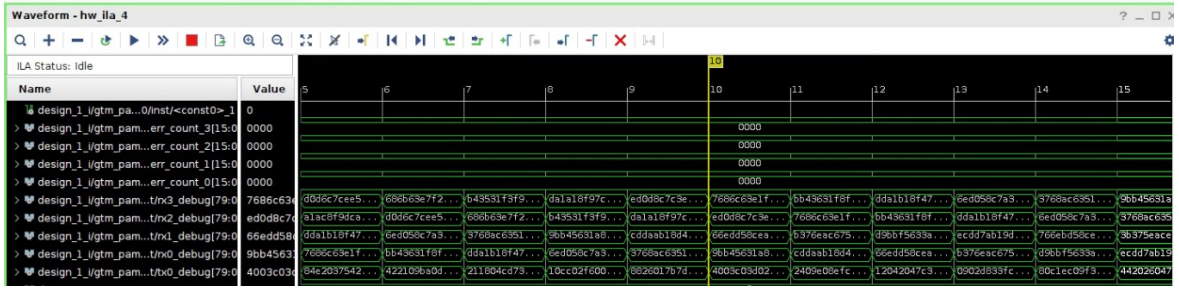


- 3-day BERT, Our self-designed protocol, PRBS16:
  - BER of the worst lane: **9.0×10^{-14}**
  - 16-lane combined BER: **6.7×10^{-15}**
  - Latency: **210~240 ns**

- Based on our experience, NRZ is usually O(10^{-16})
- This BER for PAM4 looksl acceptable.



PRBS16 patterns

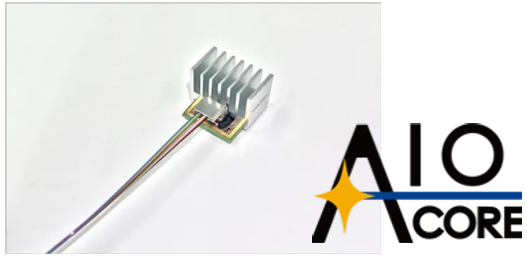


Optical transceiver

- R&D on the new trigger device UT5 is our target, so the options on hardware spec. is important.
  - QSFPDD with MPO-16 is one of the options: 8 pairs of link, so save the space on the circuit.
  - Also, QSFP56 with MPO-8 can be considered: still 4 pairs.
  - To use PAM4, only a fixed data rate is supported.

- Samtec company: FIrefly connector:
  - New product supporting PAM4. Will be released soon.
  - Mainly NRZ products.

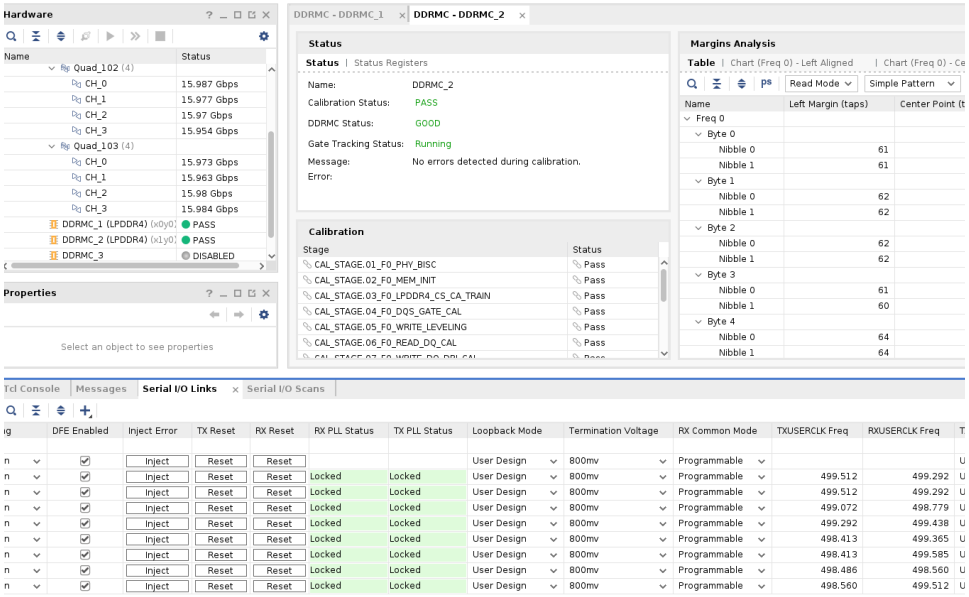
- AIOcore company @ Tokyo:
  - Embedded Optical Module.
  - PAM4 version: under development
  - E-sys group has collaboration with them.
  - Interested in its radiation hardness, and connection to other modules.



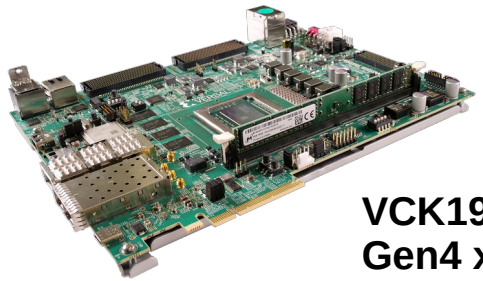
- Versal GTM is a good driver device to probe for other optical devices, so we should try.

PCIe-CPM test with Versal kits

- CPM-PCIe example from Xilinx: XTP712
  - CPM: building block design for PCIe with integrating DMA, CIPS, NOC, etc.
  - PCIe Gen4 x8:
    GTYP links are up. 16 Gbps per lane.
- Driver software: QDMA, also a Xilinx IP.



VPK120
Gen5 x 16

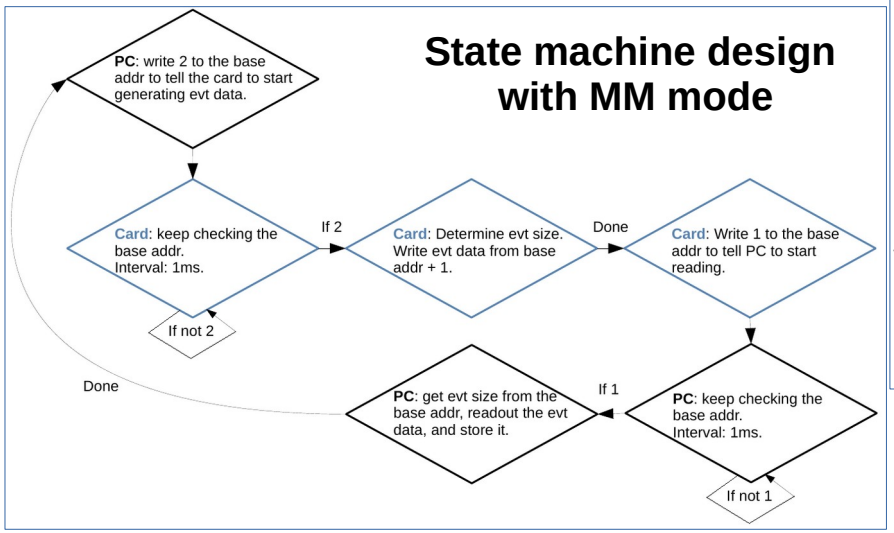


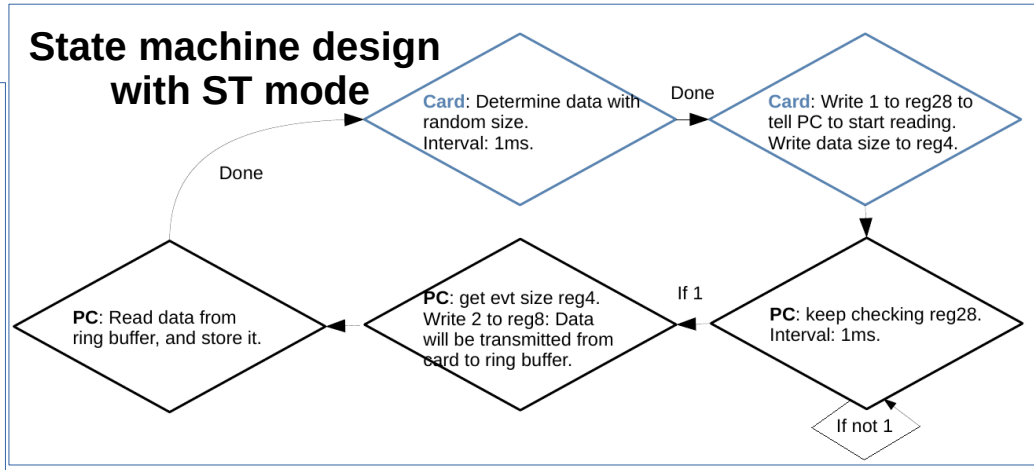
VCK190
Gen4 x 8

```
[root@cef01 linux-kernel]# ./bin/dma-ctl dev list
qdma02000       0000:02:00.0    max QP: 8, 0~7
qdma02001       0000:02:00.1    max QP: 0, -~-
qdma02002       0000:02:00.2    max QP: 0, -~-
qdma02003       0000:02:00.3    max QP: 0, -~-
[root@cef01 linux-kernel]# ./bin/dma-ctl qdma02000 q add idx 0 dir bi
dma-ctl: Warn: Default mode set to 'mm'
qdma02000-MM-0 H2C added.
qdma02000-MM-0 C2H added.
Added 1 Queues.
[root@cef01 linux-kernel]# ./bin/dma-ctl qdma02000 q start idx 0 dir bi
dma-ctl: Info: Default ring size set to 2048
1 Queues started, idx 0 ~ 0.
1 Queues started, idx 0 ~ 0.
[root@cef01 linux-kernel]# ./bin/dma-to-device -d /dev/qdma02000-MM-0 -s 32
size=32 Average BW = 177.377688 KB/sec
[root@cef01 linux-kernel]# ./bin/dma-from-device -d /dev/qdma02000-MM-0 -s 32
size=32 Average BW = 132.445391 KB/sec
[root@cef01 linux-kernel]# ./bin/dma-ctl qdma02000 q stop idx 0 dir bi
Stopped Queues 0 -> 0.
[root@cef01 linux-kernel]# ./bin/dma-ctl qdma02000 q del idx 0 dir bi
Deleted Queues 0 -> 0.
```

PCIe-CPM firmware: Event readout

- State machine of the readout protocol between PC and FPGA.
  - Basically, handshake between PC and FPGA to know when is ready, what is data size, and when to take data.
- Random data size in the data generator.
- Not fully optimized yet: Long waiting time.
  - 1 ms waiting time in idle state to repeat.






```
root@cef01:/home/ytlai/versal/dma_ip_drivers-master_202311/QDMA/linux-kernel/apps/user-readout# ./user-readout -d /dev/qdma02000-MM
-2 -c 10
host buffer 0x1008, 0x5558ab141000.
evt filled
1 192 0 64
evt size:384 bytes
evt taking done
waiting...
waiting...
waiting...
evt filled
3 128 0 64
evt size:832 bytes
```

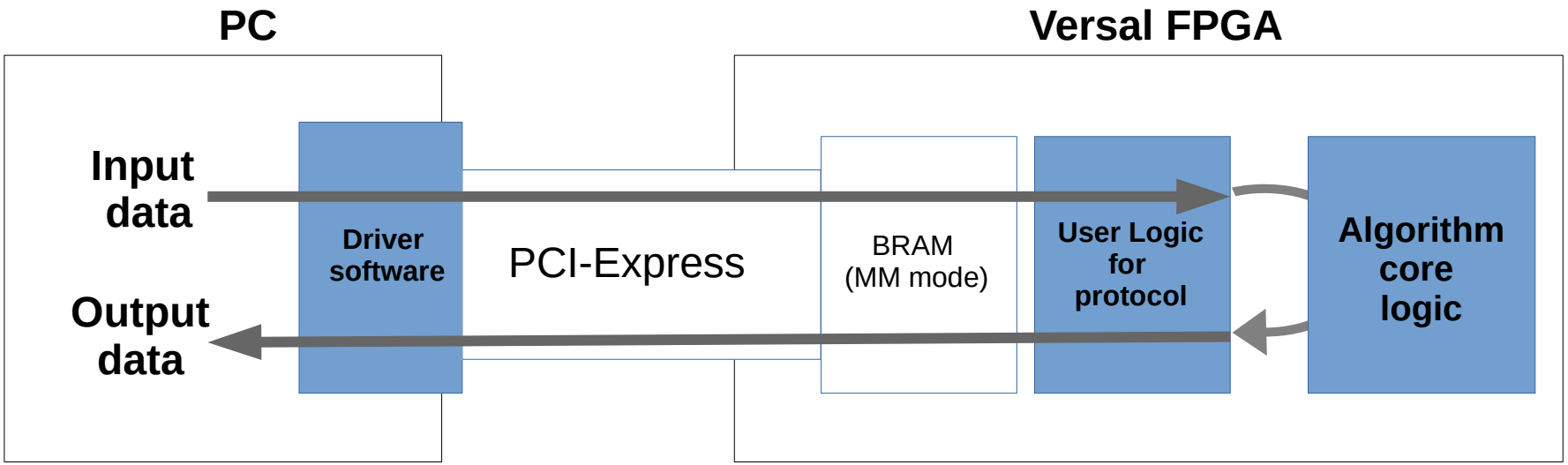
Manual readout software

Store event data with random size

```
512  3月   5 11:01 0.log
192  3月   5 11:01 10.log
512  3月   5 11:01 11.log
448  3月   5 11:01 12.log
384  3月   5 11:01 13.log
128  3月   5 11:01 14.log
  0  3月   5 11:01 15.log
  0  3月   5 11:01 16.log
  0  3月   5 11:01 17.log
576  3月   5 11:01 18.log
512  3月   5 11:01 19.log
448  3月   5 11:01 1.log
448  3月   5 11:01 20.log
```

PCIe-CPM firmware: Event exchange

- A data exchange flow is also made for firmware and software.
  - For both MM and ST modes.
- 1 event in - 1 event out.
- In order to test the algorithm core logic to be implemented in Versal kits.
  - We are going to integrate some algorithms together with this firmware framework to test.

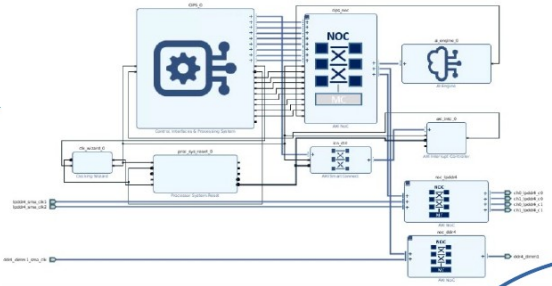


Versal AI engine of VCK190

- Design flow with Vivado/Vitis:
  - C++ programmable design for AI engine.
  - Integrated in PL design.

Vivado

- Open an **example project** for VCK190:
  - Versal Extensible Embedded system. with AI engine.
- Export **platform**



taking this file → **.xsa** file

Vitis

Workspace

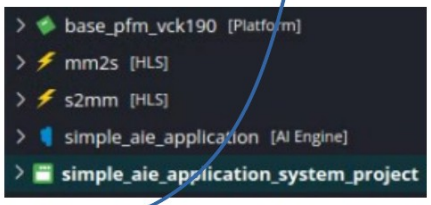
Platform

AI engine component
From example. src, kernel and data.
Algorithm is defined here.

HLS Component: mm2s
with mm2s.cpp

HLS Component: s2mm
with s2mm.cpp

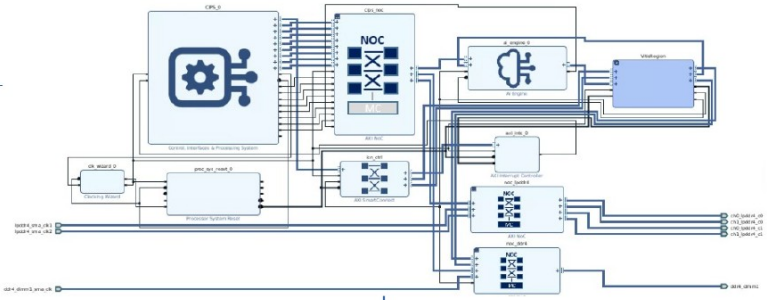
System project Component
for integration



building the hardware

Vivado

Get the final **firmware project**
With AI engine, mm2s, s2mm to NOC

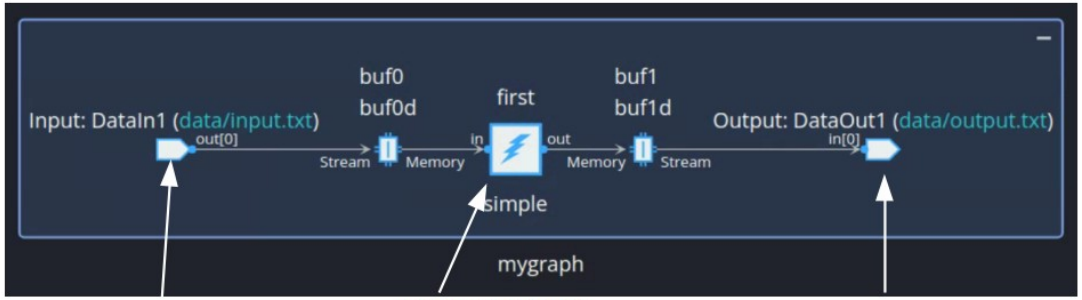


If want to run the system using the Baremetal control application via SD card and UART, need to build up another application in Vitis.

Study on implementation with AI engine

- We have tested with different algorithms implemented on AI engine

Simple arithmetic calculation

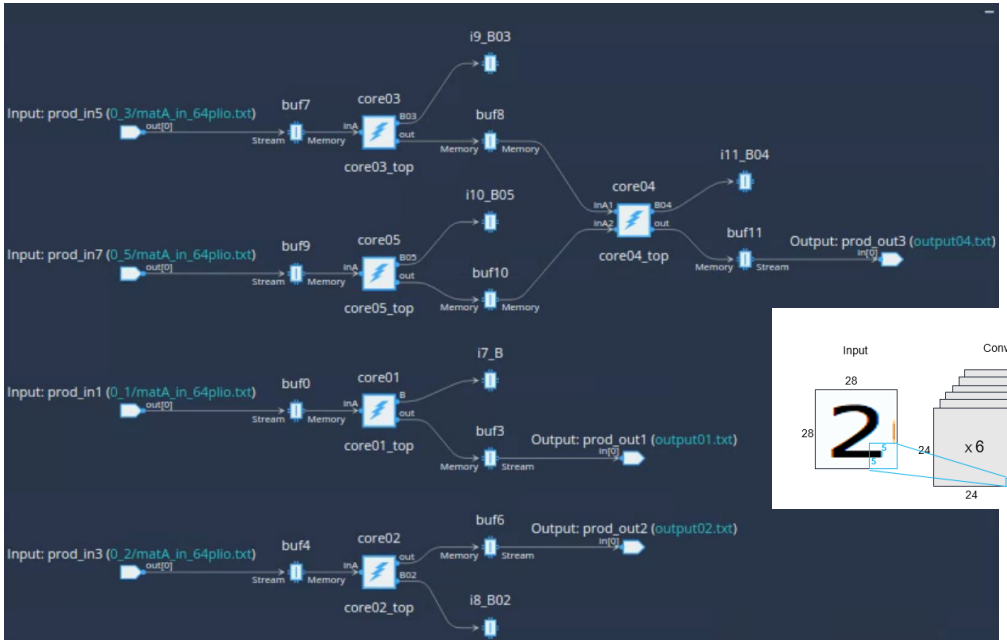


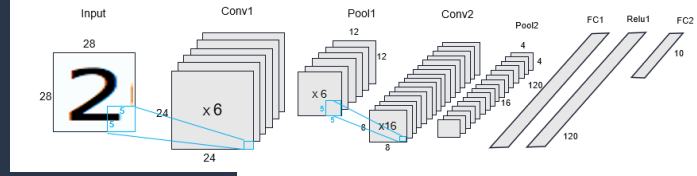
Input: to be connected to PL (AXIS)

"core" of calculation
Multiple core is also fine.

output: to be connected to PL (AXIS)

leNet: a CNN model





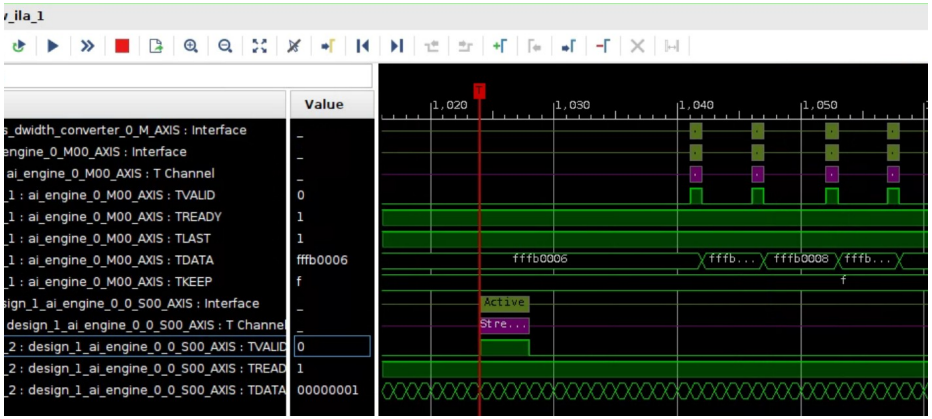
source:
Xilinx git

Study on implementation with AI engine (cont'd)

- Simulation and firmware test.

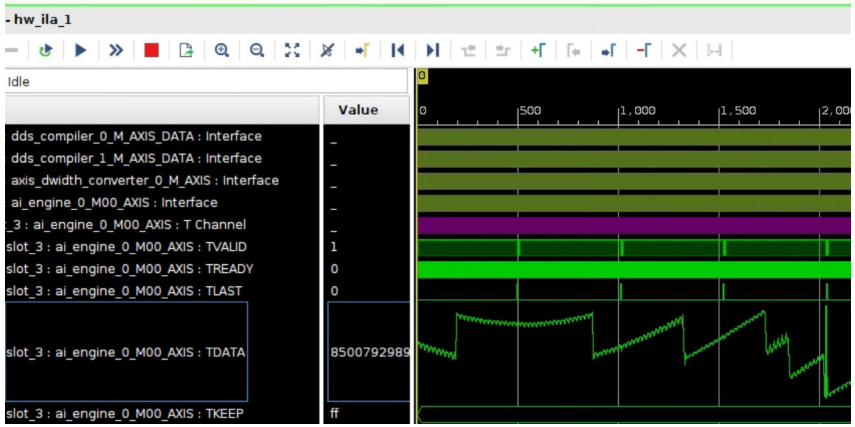
Simple arithmetic calculation

4 separated output

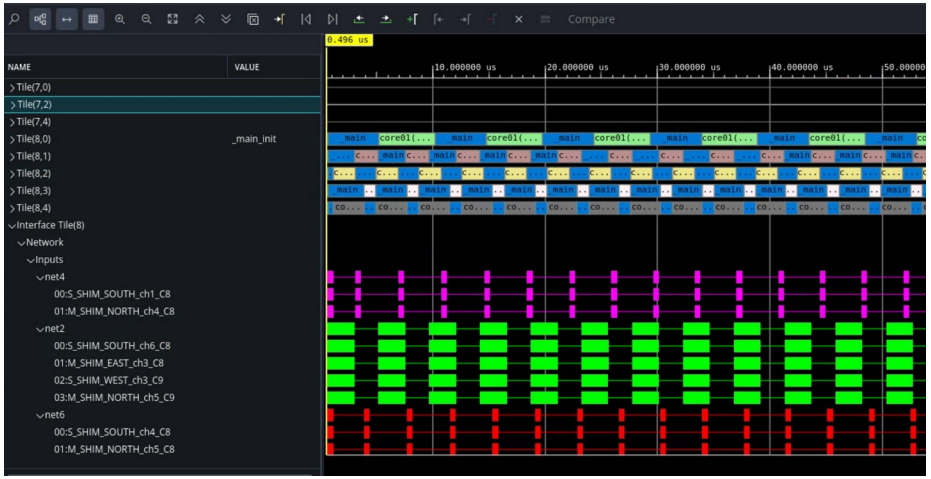


4-clock-cycle input

FIR filter



Simulation for leNet

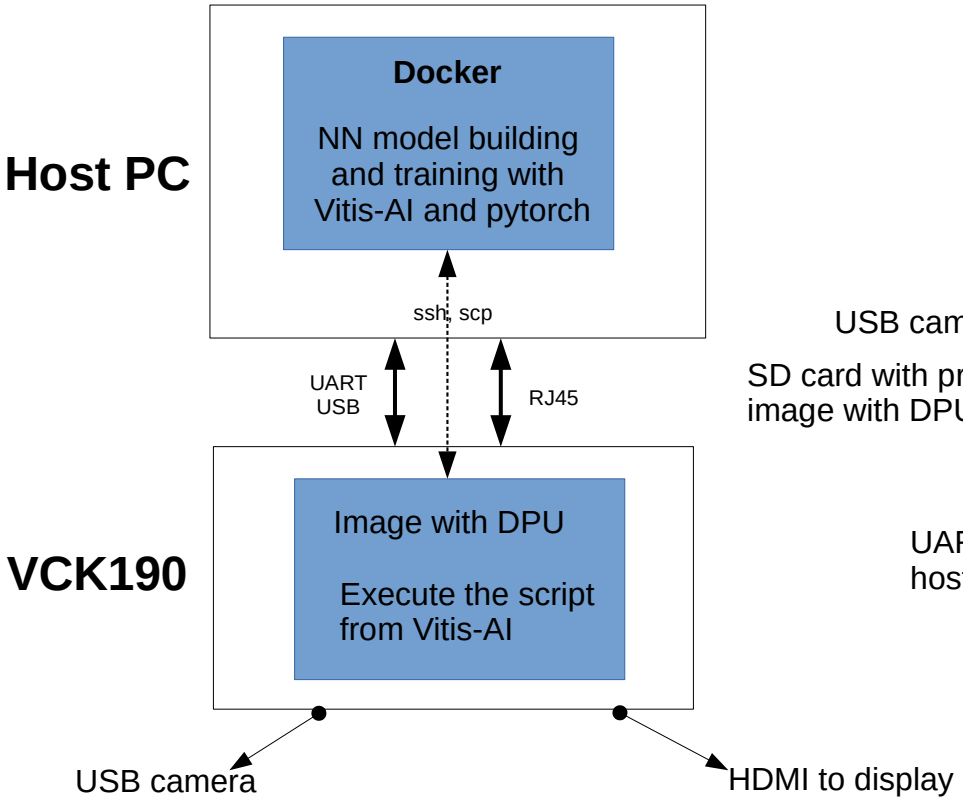


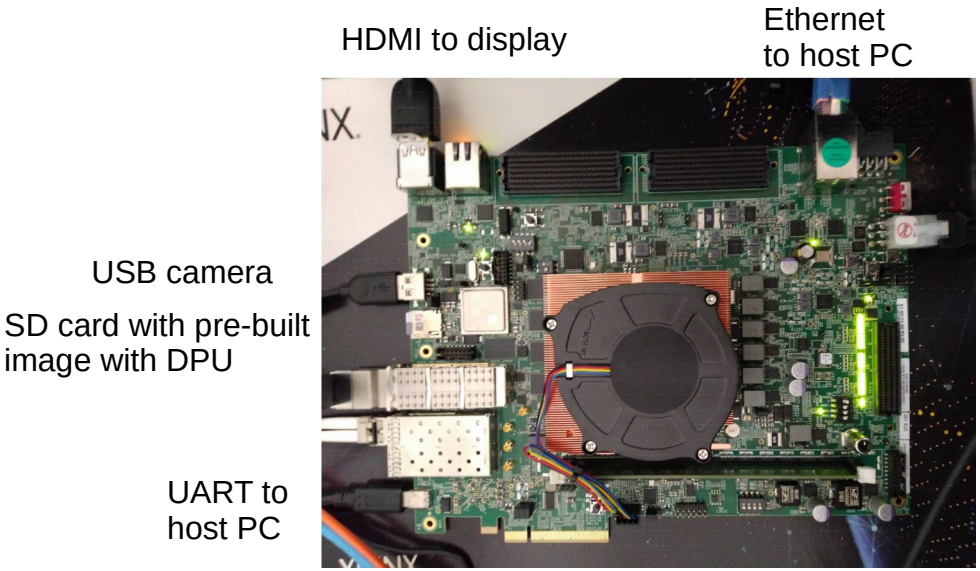
- I/O is based on AXI stream.
- Not exactly pipe-line.
- For a simple calculation:
  - Latency is 10~20 clock-cycles.
  - ~100 ns. (properly mainly I/O)
  - Core logic: processing clock is up to O(GHz).
- More studies will be done.

Vitis-AI with DPU

- VCK190 has another feature of Deep Learning Processor Unit (DPU), which is a a configurable computation engine dedicated to convolutional neural networks.

- The design flow does not involve Vivado for PL design. The device is utilized with a small operation system like a server, and works can be executed in it.
  - A higher-level application.

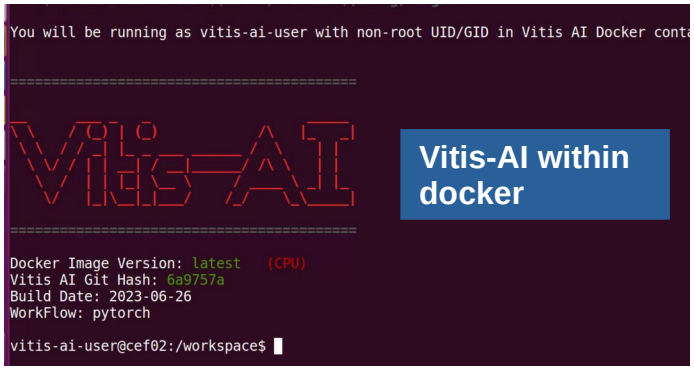




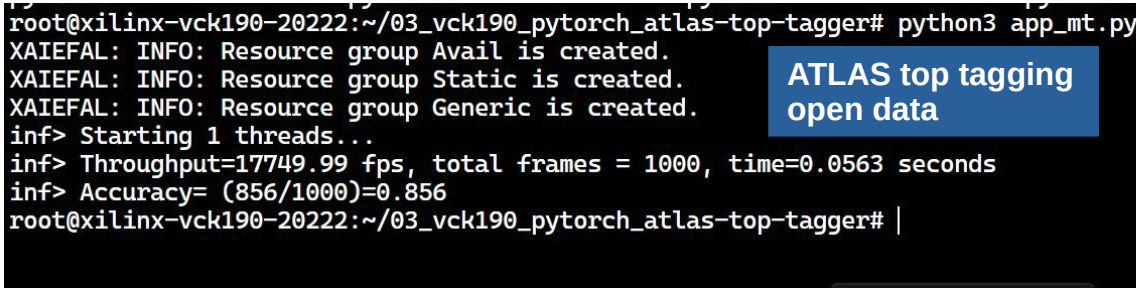
Vitis-AI with DPU: test

- The environment with docker and DPU setup for VCK190 has been ready.
  - GPU quantization.
  - Image and video processing.
  - ATLAS top tagging open data.

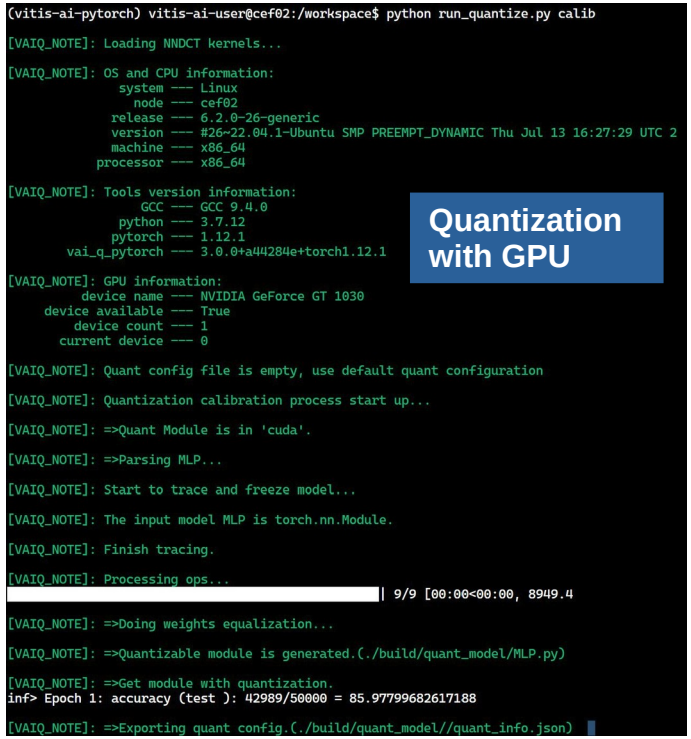
Study by Chaowaroj "Max" Wanotayaroj (KEK IPNS)



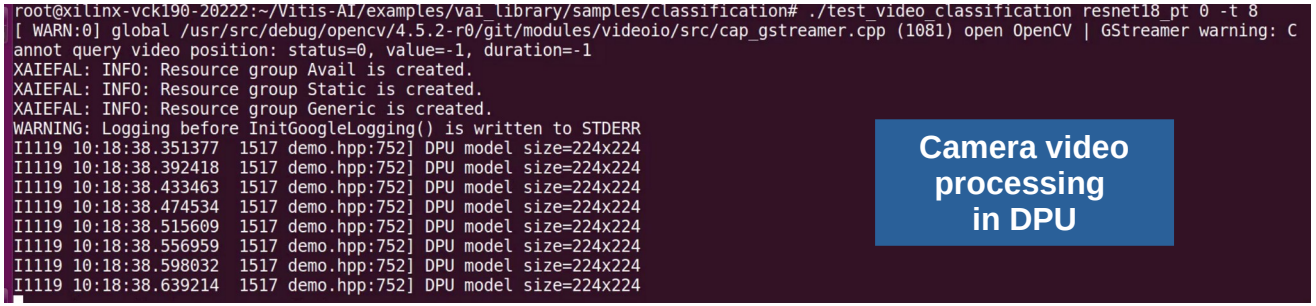
Vitis-AI within docker



ATLAS top tagging open data



Quantization with GPU



Camera video processing in DPU

Algorithm making in FPGA: HLS, ML, AI engine

- Next step, we have many algorithms from Belle II, ATLAS, or so, to play in Versal kits.
  - Before that, let's think about the methodologies to do so.

- Considering algorithm implementation:
  - HDL logic in firmware.
  - HLS: software → firmware.
  - ML inference
  - AI engine.

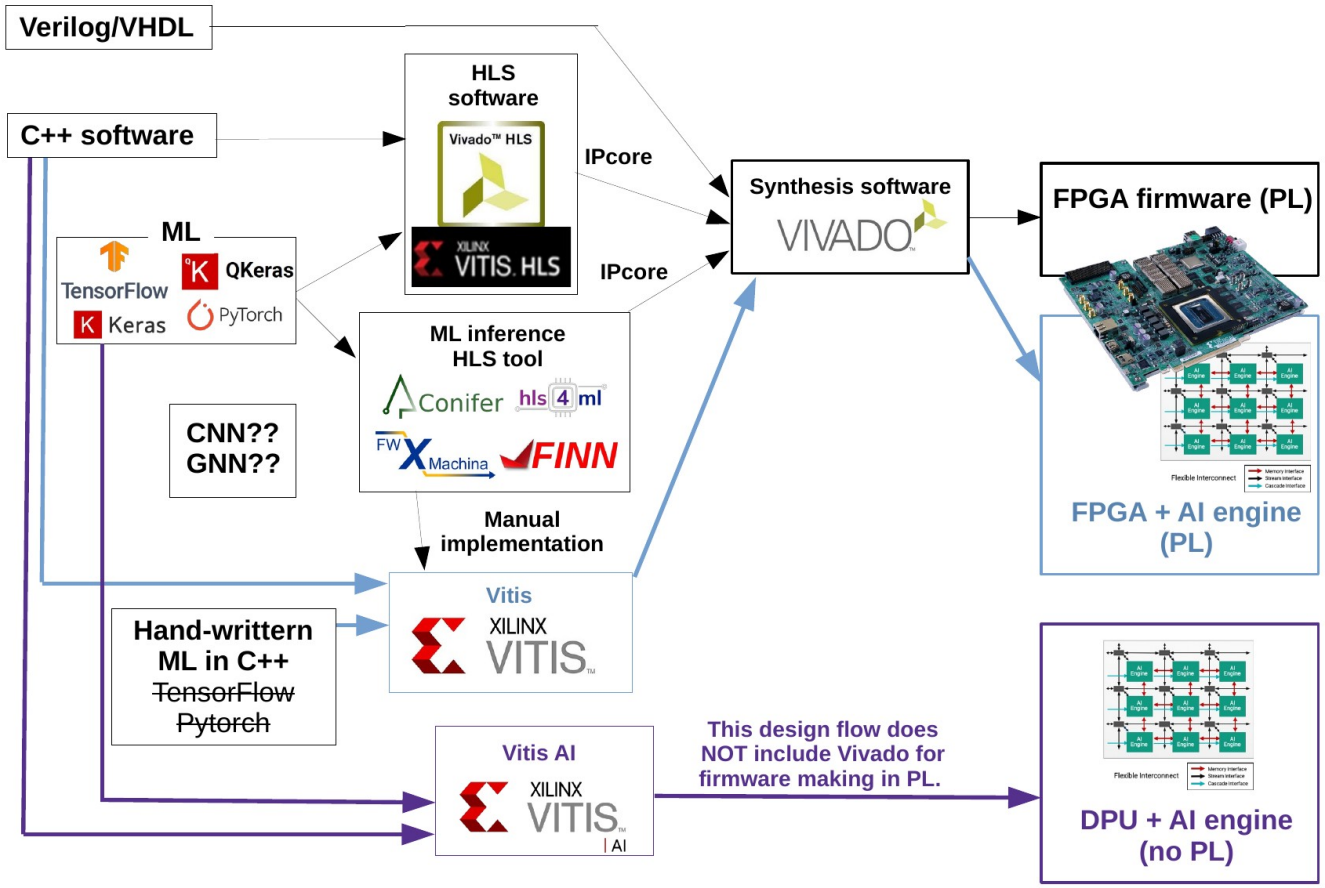
Depend on the different targets, our selection on FPGA differs. A strong FPGA? ACAP with AI engine? DPU?

- Not only the hls4ml, HLS tools has much more for ML and non-ML application.
  - Similarly, Versal AI engine requires a different design flow to make software/firmware.

- For this part of the work, we generalize the work plan into a roadmap in a technical perspective.

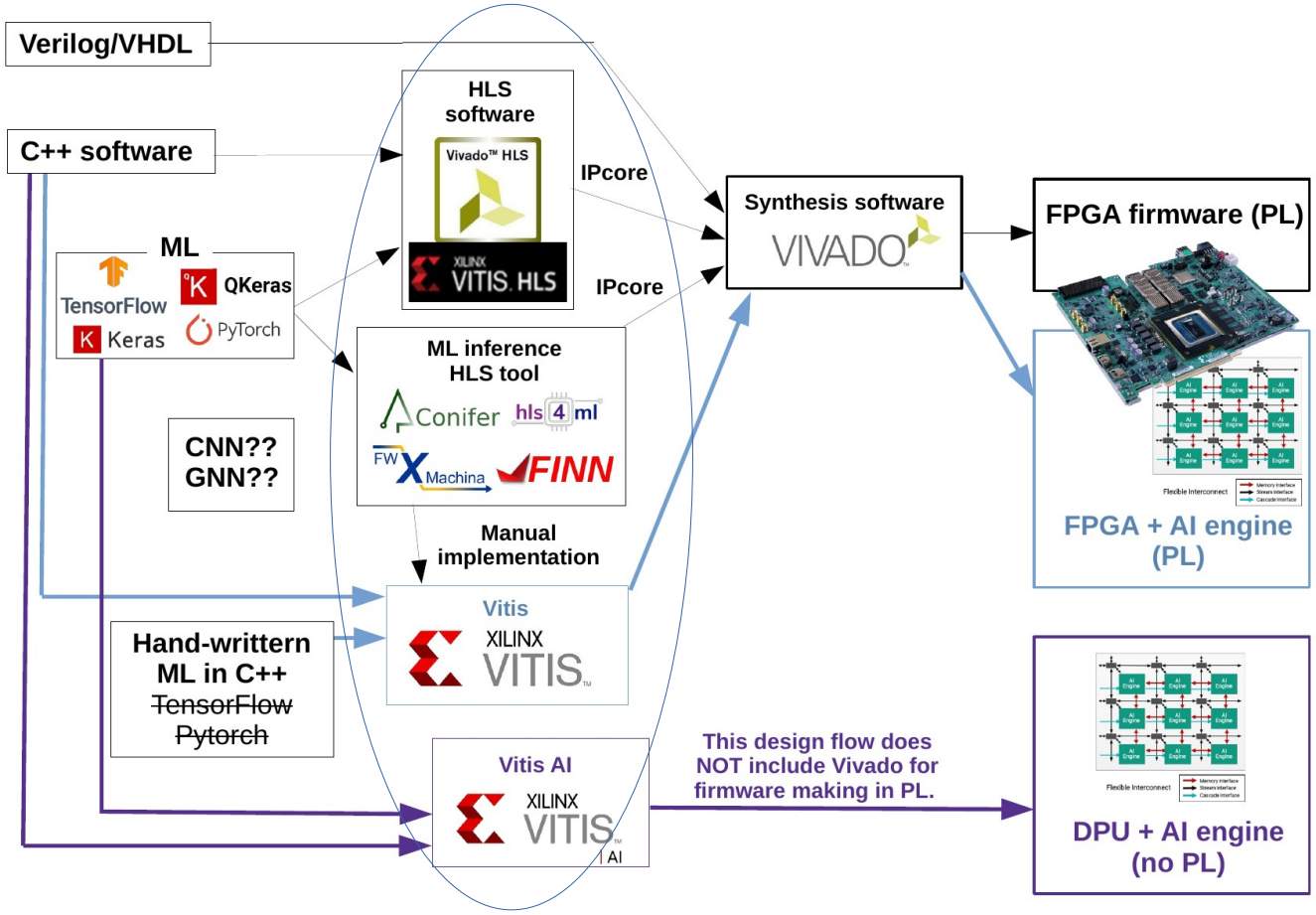
HLS, ML, AI engine: roadmap of FPGA methodology

- Not only what kind of algorithm to design, but also how to design it.
- As a member of KEK E-sys and CEF, we hope to understand the basic utilization on each, and build a database of such technical knowledge, to support our experimental colleagues.



HLS, ML, AI engine: roadmap of FPGA methodology

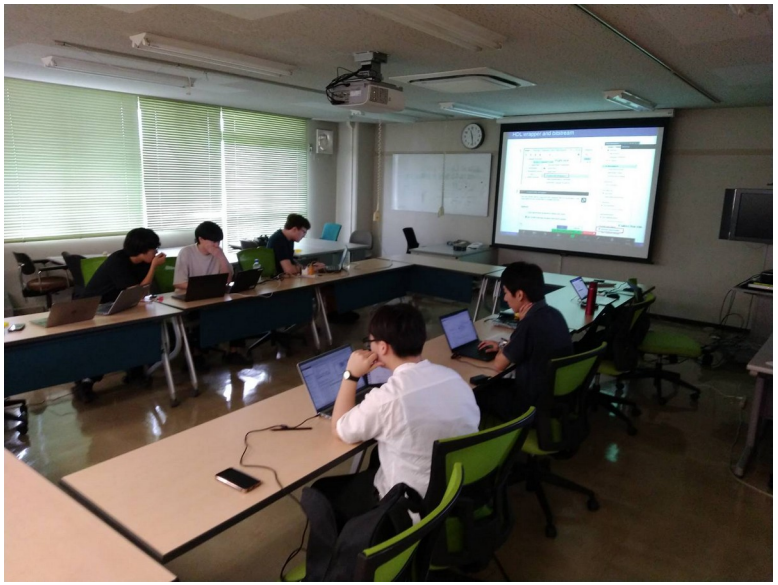
- We are recruiting young student to learn/work with us.
  - Now ~50% of the items have been covered.
  - We also plan to make a series of hand-on lecture for each of them.

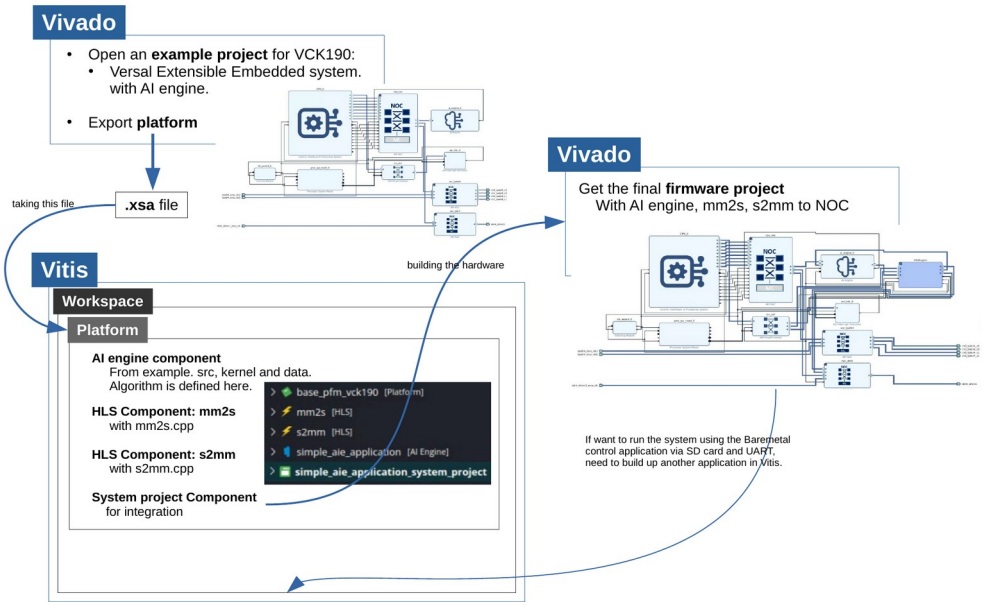


AI engine course @ KEK E-sys, in Aug.

- We tried to hold a course about utilization the AI engine in this Aug. at KEK.
  - Attenders in Japan and other countries remotely.
  - All operations were done using local servers in our laboratory.
  - Almost everything is covered: environment setup, Vivado design flow, Vitis design flow, kernel making, Vitis simulation, hardware test.

- We will try to have more similar course on the other similar FPGA advance skills.

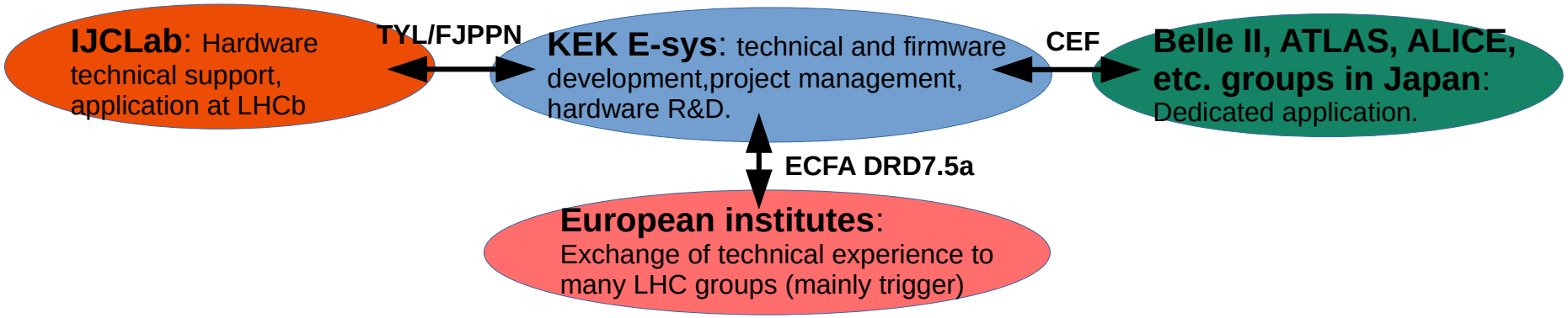




International collaborations

- European Committee for Future Accelerators hosted a Detector R&D Roadmap
  - **ECFA DRD**, where **DRD7 is the Task-Force for electronics**.
  - Our CEF Versal project joined the **7.5a working group: COTs for TDAQ backend**.
  - Y-T. Lai (KEK E-sys) : co-convener of the 7.5a working group

- **"Toshiko Yuasa" France Japan Particle Physics Laboratory (TYL-FJPPL)**:
  - Japan-France research collaboration
  - We have a project with IJCLab Orsay and CPPM Marseille
  - For advance FPGA device application and PCIe related study
  - PI: Y.-T. Lai (Japan) - D. Charlet (France)



Project in TYL/FJPPN: SuperKEK BOR readout

- We plan to prepare a system to readout the waveform of oscillation from the Bunch Oscillation Recorder (BOR)
  - Feature study for sudden beam loss issue.
  - IDROGEN + ADC + WhiteRabbit.

- Work plan:
  - Optical data link
  - PCIe readout.
  - Oscillating waveform analysis, ML prediction
  - Using Versal and PCIe40 system.

- Collaborators:
  - Keisuke Yoshihara (Univ. of Hawaii)
  - Hiroshi Kaji (KEK ACCL)
  - Daniel Charlet (IJCLab)

Versal

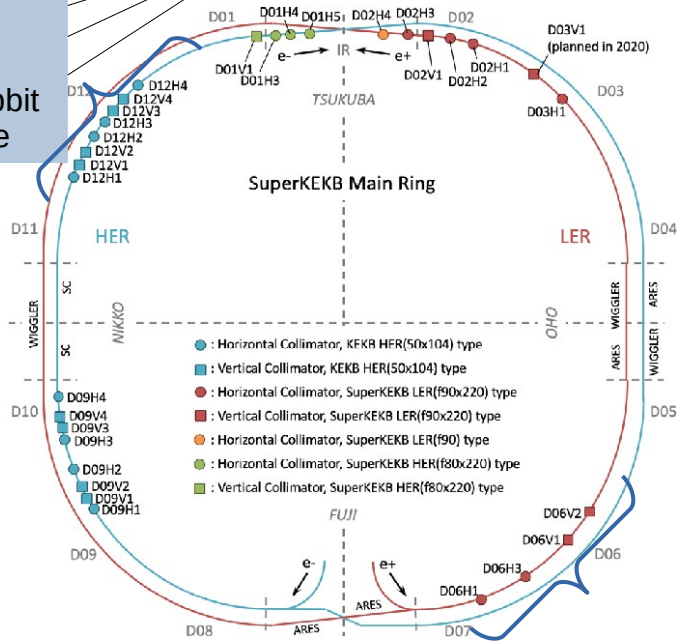
PCIe40

IDROGEN

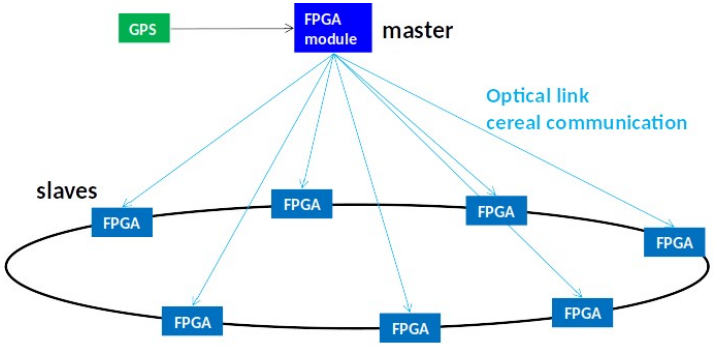
readout (PCIe or so) here

O(km)

Plan to put IDROGEN + ADC + WhiteRabbit around here



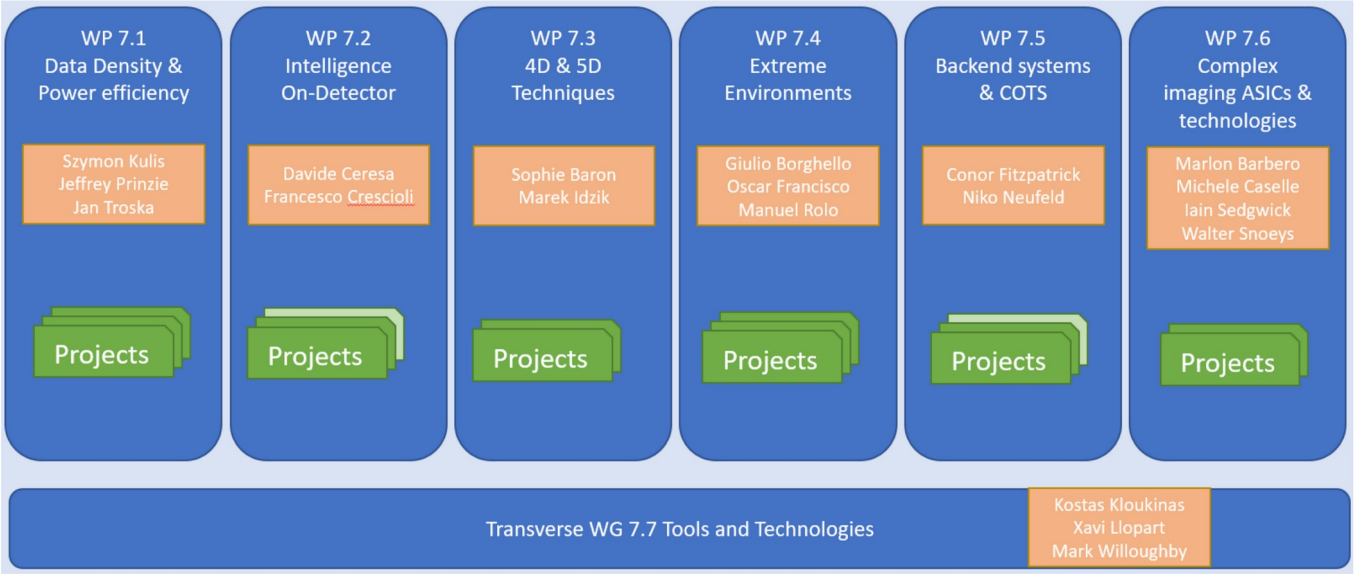
A few RFSoC



WhiteRabbit: clock synchronization system < 100ps accuracy

accelerator beamline ~1km – 10km

DRD7.5a: TDAQ backend with COTs



WP7.4		
Extreme environments	**7.4a** Device modelling and development of cryogenic CMOS PDKs and IP **7.4b** Radiation resistance of advanced CMOS nodes **7.4c** Cooling and cooling plates **Overlap with DRD8 to be clarified**	Harsh environments Dense heat generation and critical extraction
WP7.5		
Backend systems and COTS components	**7.5a** DAQOverflow **7.5b** From FE to BE with 100GbE	DAQ platforms survey and benchmarking Reference implementations Simplified backends
WP7.6		
Complex imaging ASICs and technologies	**7.6a** Common access to selected imaging technologies **7.6b** Shared access to 3D integration	Collaborative effort on complex technologies Common access framework IP blocks

From Francois Vasey, the 3rd DRD7 Workshop

DRD7.5a: TDAQ backend with COTs

- DRD7.5a:
  - TDAQ backend in HEP experiments
  - Hardware device: keep pace with **COTs** technologies (CPU, GPU, FPGA).
  - Software/firmware development: generic algorithms, workflows, or design tools for TDAQ real-time processing
  - Mainly **trigger** development.

- 14 sub-groups in 7.5a

Relatively coupled

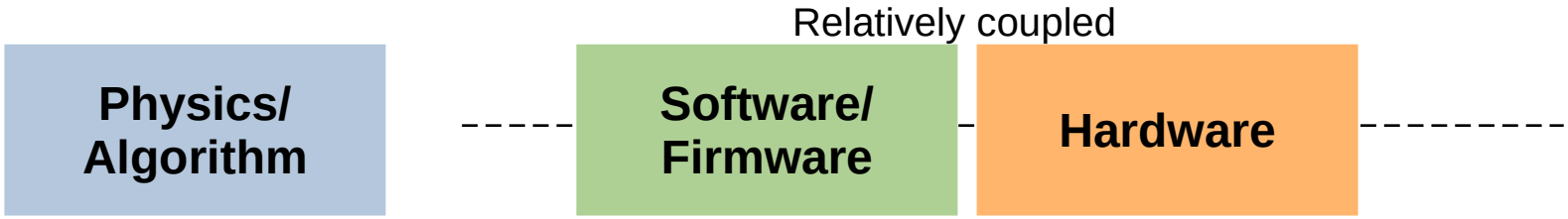
Physics/ Algorithm	Software/ Firmware	Hardware
• Tracking • Calo clustering • Topology • Anomaly detection •	• Software coding • ML framework • HDL • HLS • ML inference •	• CPU • GPU • FPGA

Activities within 7.5a

- Considering the trend, two major types of **Trigger** systems for real-time processing/filter:
  - A very personal point of view, as the boundary in between is getting vague nowadays.

- **Hardware/low-level**: Rely on the FPGA programmable logic (PL) design based on HDL/RTL logics to achieve short-latency quick processing (in O(μs)).

Keywords: FPGA, PL, HDL, RTL, HLS, ML inference (hls4ml, etc), Versal ACAP, Versal AI engine, short latency in O(μs).

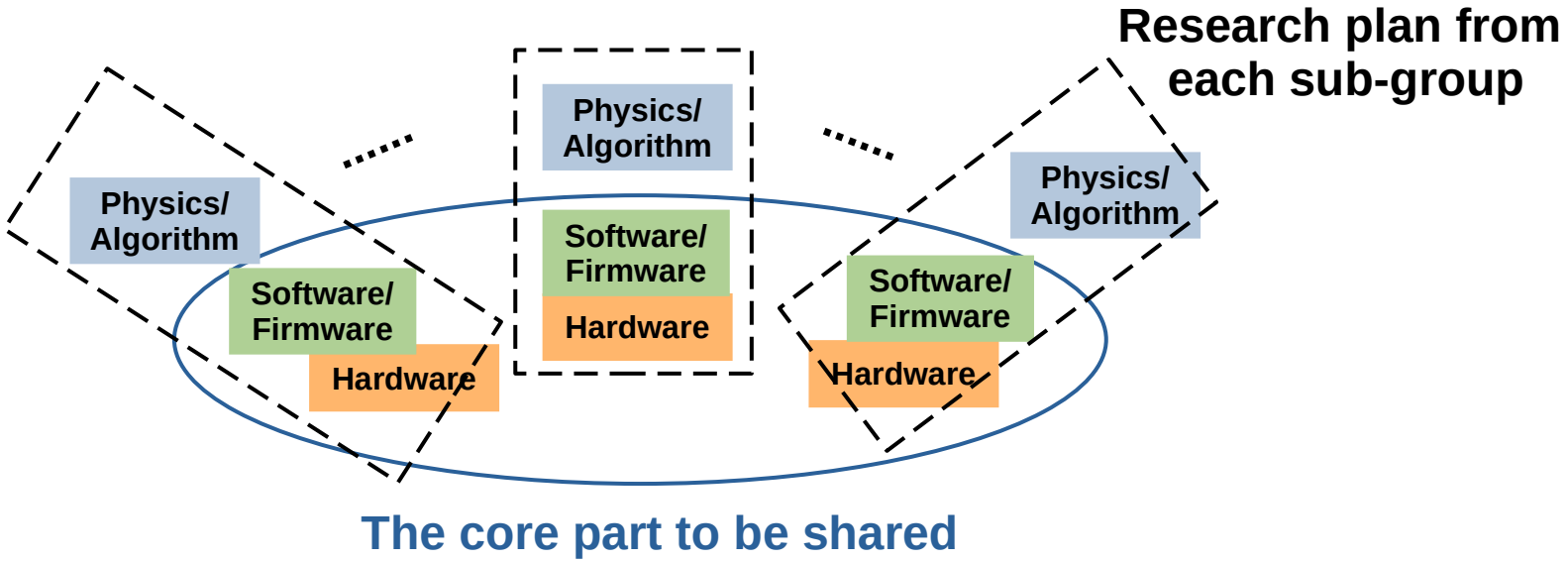


- **High-level**: Software-based algorithm development with computing farm. In addition to CPU/GPU, FPGA acceleration is a new application.

Keywords: Hardware acceleration platforms with CPU/GPU/FPGA, Alveo, Versal acceleration card, Versal DPU.

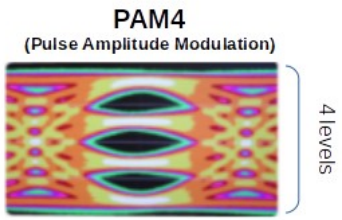
Collaboration within 7.5a

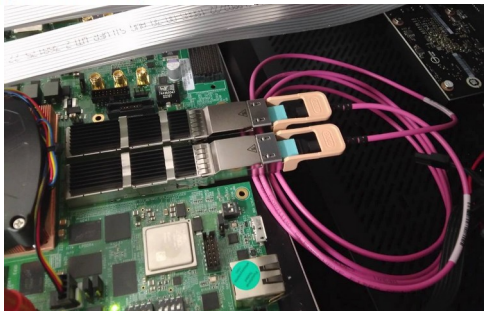
- How do we work together?
- The physics/algorithm part is mostly dedicated to experiment purpose, so the source codes might not be suitable to be shared.
- The **framework of software/firmware + hardware** is expected part to share.
  - The major core technique for TDAQ experts.
  - The unique core technique from each sub-group.
  - A git repository has been prepared for maintenance purpose.
    The contribution from each sub-group is under discussion within 7.5a.



Our Veral project @ DRD7.5a

- So here are the works to be shared by our Versal project:





Summary

- CEF organized a research project "Versal project" for the common R&D of future universal FPGA device mainly based on the study on Xilinx Versal ACAP.
- Fundamental functionalities with evaluation kits:
  - PAM4, PCIe, AI engine, and DPU.
- Algorithm implementation and methodologies
  - General study on the techniques: HLS, ML, AI engine, and DPU.
  - Persist the technical knowledge as a database, and hold hand-on lectures for experience sharing.
- Plan:
  - Implementing various kinds of existing trigger algorithms in Belle II and ATLAS with Versal and different skills.
  - R&D on the new trigger device UT5.