环形正负电子对撞机
Circular Electron Positron Collider

CEPC Electronics System for Ref-TDR Overview, Status & Plan

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On behalf of the Elec-TDAQ system of the CEPC Ref-TDR

IHEP, CAS

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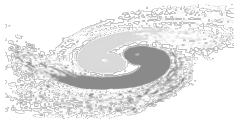
Outline

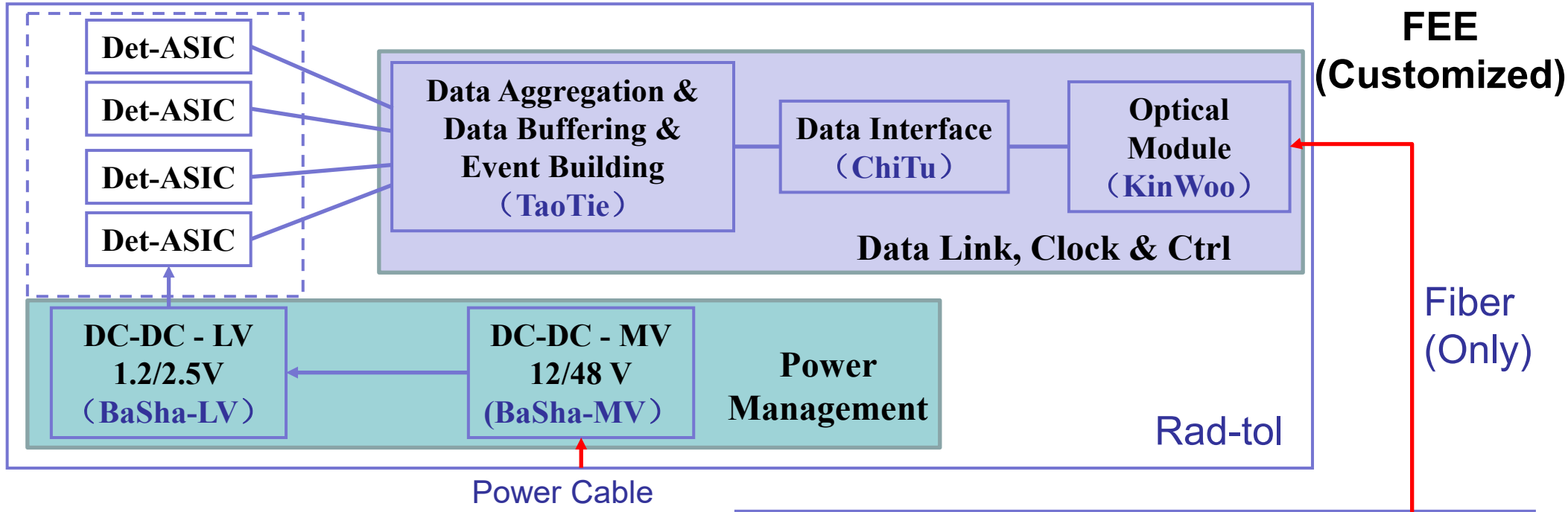
- Global Framework of the Elec-TDAQ system
- Main challenges & tasks of the FEE of Sub-Det
- Key blocks & plan of the common electronics
- Summary

Requirement from Sub Detectors (@Higgs)

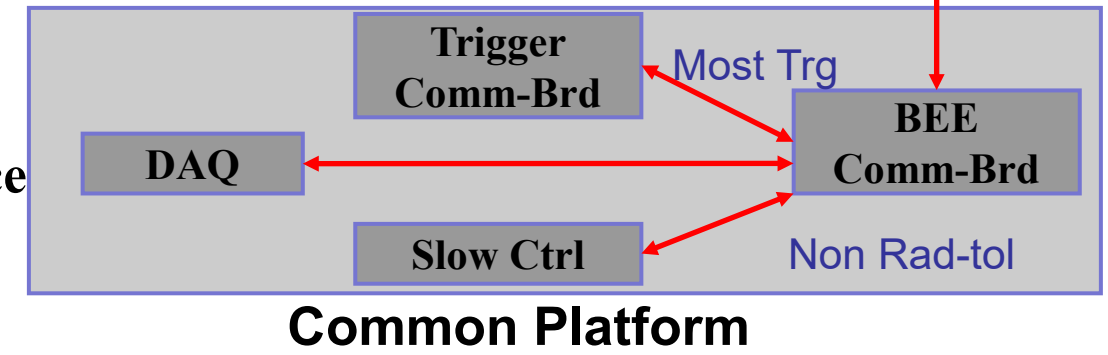


	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Ref. Signal processing	XY addr + BX ID	XY addr + timing	Hit + TOT + timing	ADC+TDC/TOT+TOA		ADC + BX ID	TOT + TOA/ ADC + TDC				
Data Width /hit	32bit	42bit	32bit	40~48bit		48bit	48bit				
Max Data rate / chip	2Gbps/chip@Triggerless@Low LumiZ Innermost	Avg. 3.53Mbps/chip Max. 68.9Mbps/chip	Avg. 21.5Mbps/chip Max. 100.8MHz/chip	Avg：2.9Mbps/chip Max：3.85Mbps/chip	Avg：38.8Mbps/chip Max：452.7Mbps/chip	~70Mbps/module Inmost	Avg. 0.96Gbps/module Max:9.6Gbps/module		Max. 144Mbps/module-layer	Max. 350Mbps/module-layer	Avg： 15.36 Mbps/chip Max： 153.6 Mbps/chip
Data aggregation	10~20:1, @2Gbps	14:1@O(100Mbps)	22:1 @O(100Mbps)	i. 22:1 @O(5Mbps) ii. 7:1 @O(100Mbps)	i. 22:1 @O(50Mbps) ii. 10:1 @O(500Mbps)	1. 279:1 FEE-0 2. 4:1 Module	i. 4~5:1 side ii. 7*4 / 14*4 back brd @ O(100Mbps)		< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)	< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)	<=24:1 @ O (400 Mbps)
Detector Channel/module	1882 chips @Stch &Ladder 2204 modules	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	0.52M chn ~32500 chips 260 modules	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	43.2k ch 72 Aggregation board
Avg Data Vol before trigger	474.2Gbps	101.7Gbps	298.8Gbps	249.1Gbps	27.9Gbps	34.4Gbps	460Gbps	250Gbps	811.2Gbps	537.6Gbps	24.1 Gbps

Global framework of the CEPC Elec system



- Common subsystems (data buffering, aggregation, transmission; powering)
- Det. specific ASICs waiting for detector final choice
- A common BEE hardware, configurable for individual subsystems.
- TDAQ interface is (probably) only on BEE



Outline

- **Global Framework of the Elec-TDAQ system**
- **Main challenges & tasks of the FEE of Sub-Det**
  - New technology: Wafer-scale chip design with stitching
  - High performance for Q & T
  - Ultra low power & cooling
  - Limited space vs advanced PCB & packaging
- **Key blocks & plan of the common electronics**
- **Summary**

Detector Key Specifications

Sub-system	Key technology	Key Specifications
Vertex	6-layer CMOS SPD	$\sigma_{r\phi}$ ~ 3 μm, X/X_0 < 0.15% per layer
Tracking	CMOS SPD ITK, AC-LGAD SSD OTK, TPC + Vertex detector	$\sigma\left(\frac{1}{P_T}\right) \sim 2\times10^{-5} \oplus \frac{1\times10^{-3}}{P\times sin^{3/2}\theta}(GeV^{-1})$
Particle ID	dN/dx measurements by TPC Time of flight by AC-LGAD SSD	Relative uncertainty ~ 3% σ(t) ~ 30 ps
EM calorimeter	High granularity crystal bar PFA calorimeter	EM resolution ~ $3\%/\sqrt{E(GeV)}$ Granularity ~ 1×1×2 cm^3
Hadron calorimeter	Scintillation glass PFA hadron calorimeter	Support PFA jet reconstruction Single hadron $\sigma_E^{had} \sim 40\%/\sqrt{E(GeV)}$ Jet $\sigma_E^{jet} \sim 30\%/\sqrt{E(GeV)}$

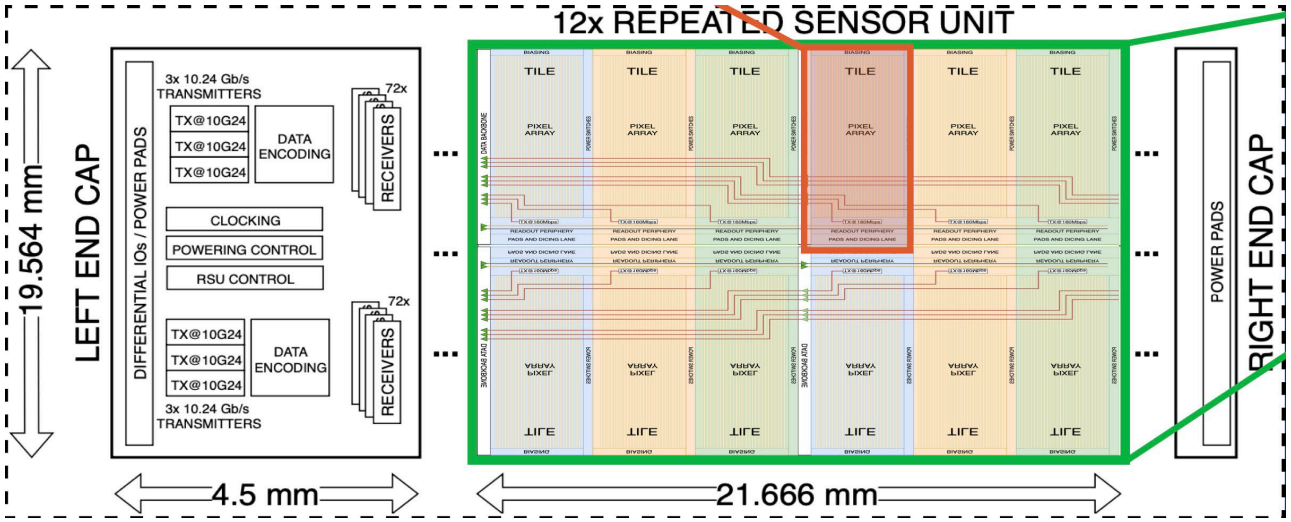
- Design of the CEPC detector evolves with R&D progressing and better understanding of the physics reach.
- The key specifications continue to be optimized.

from Wang JC

Vertex detector schemes for FEE

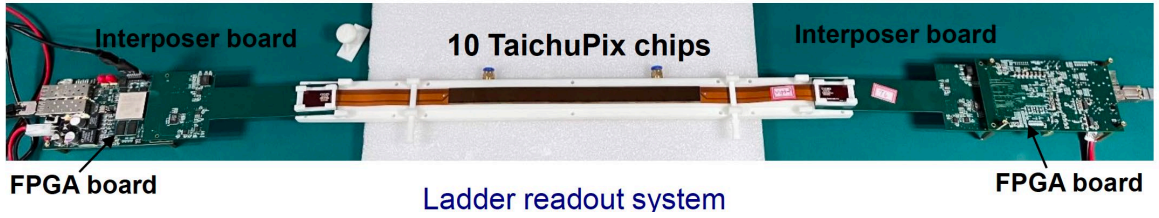
- **Baseline: stitching and RDL metal layer on wafer to replace PCB**
- **Alternative: flexible PCB**
  - **Signal, clock, control, power, ground will be handled by control board through flexible PCB**

baseline: ALICE ITS3 like stitching and RDL layer on bent MAPS [1]

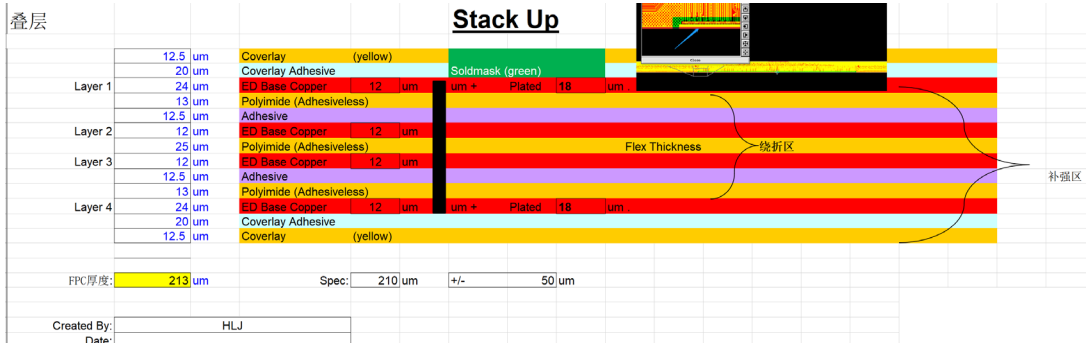


[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

Alternative: flexible PCB

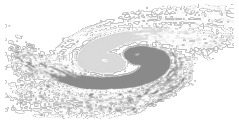


Ladder readout system



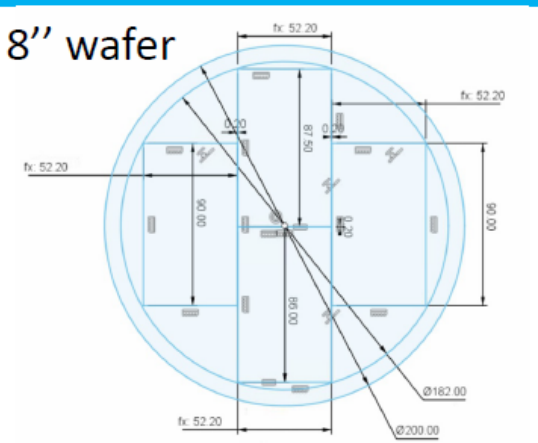
from Liang ZJ

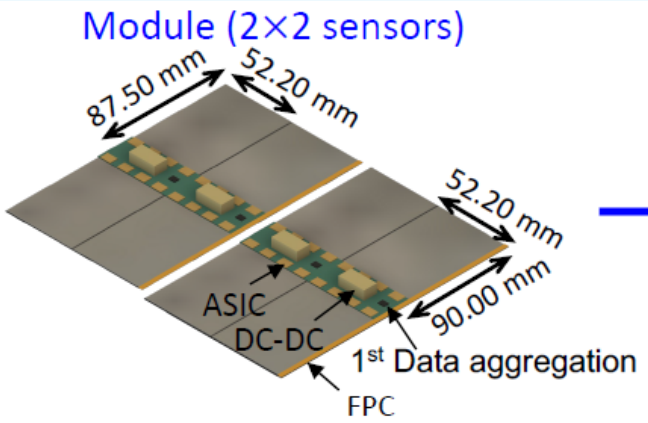
New technology: wafer-scale chip design with stitching

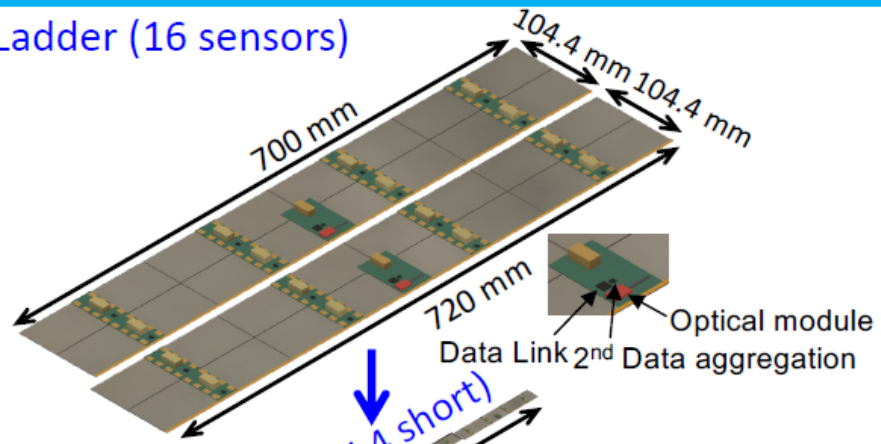


- **Stitching technology**
  - Reliability strategy due to the potential risk introduced by bending & thinning
    - Redundancy & reliability switches may needed from the top level design
    - Conservative design rule needed, routing resources limited
  - Chip size from 2.5cm → 25cm
    - Long transmission length for both signals and power, parasitics dramatically impact
    - Timing sequence for ultra large chip size
- **High rate vs background**
  - BX Freq @40MHz while power limits to 40mW/cm^2
    - Pixel frontend requires more power to match the BX ID
  - FEE-Triggerless readout vs high background
    - 1~2Gbps raw data rate for a RSU area @ Low LumiZ
- **New process from industrial**
  - RDL to help the long distance transmission & powering

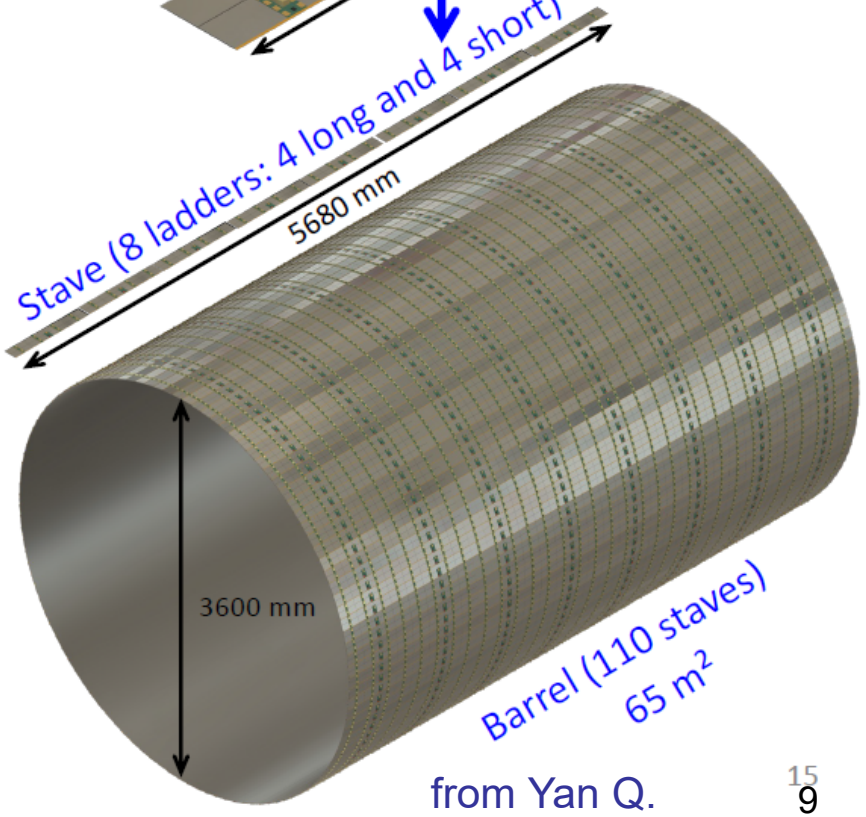
CEPC OTK Barrel Design (AC-LGAD Strips)







- CEPC outer silicon tracker (OTK) utilizes AC-LGAD (Low Gain Avalanche Detector) developed by IHEP+IME:
  - Sensor size: 8.75 cm × 5.22 cm
    9.00 cm × 5.22 cm
  - Strip number per sensor: 512
  - Strip pitch size: 100 μm
  - Spatial resolution: 10 μm
  - Time resolution: 50 ps
  - Power consumption: ~300 mW/cm^2



Maximum usage of silicon wafers for OTK barrel: a total 3,520 wafers, with 15% higher efficiency compared to a conventional single-piece sensor cut from a wafer.

from Yan Q.

Crystal ECAL: specifications

Key Parameters	Value	Remarks
MIP light yield	~200 p.e./MIP	Ensure EM resolution $\sim 3\%/\sqrt{E}$
Energy threshold	0.1 MIP	Balance between S/N and dynamic range
Crystal non-uniformity	< 1%	Along the crystal length and between crystals
Dynamic range	0.1~3000 MIPs / channel	Maximum energy deposition with 360 GeV Bhabha
Timing resolution	~500 ps @ 1 MIP	Bunch Crossing ID; clustering and hadron performance

Detector requirements

- Moderate MIP light yield
- Good uniformity
- Optimal time resolution
- Large dynamic range
- Moderate S/N ratio

Hardware activities: addressing crucial issues

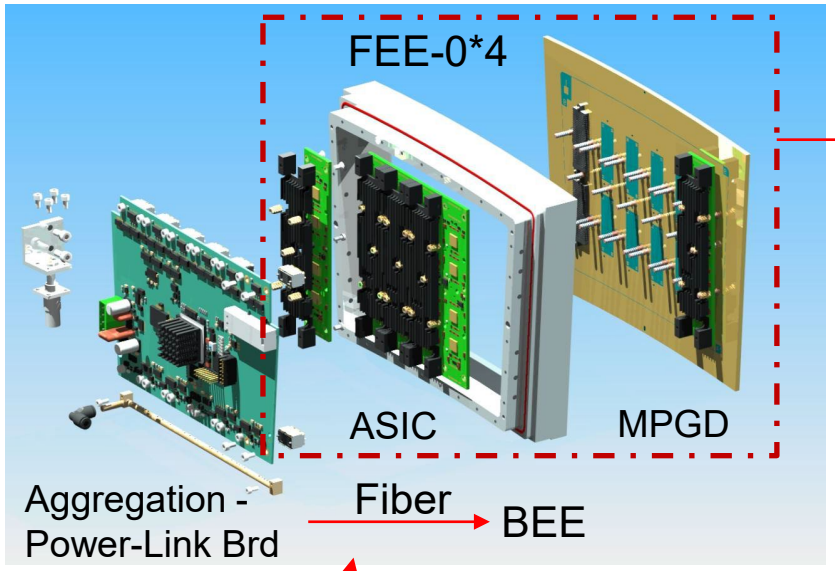
- SiPM response linearity
- Uniformity of long crystal bar
- Time resolution: different crystal dimensions
- Dynamic range of electronics
- Energy response of crystal module

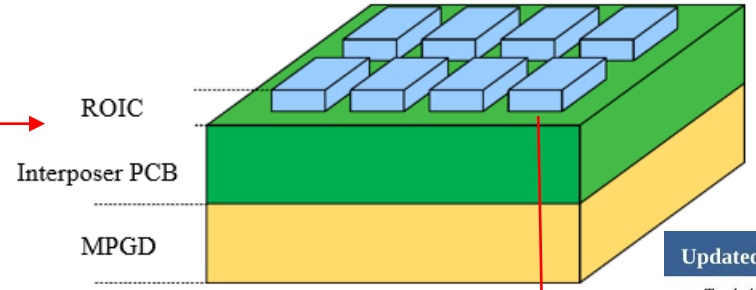
from Liu Y.

Challenges for high performance Q & T vs ultra low power

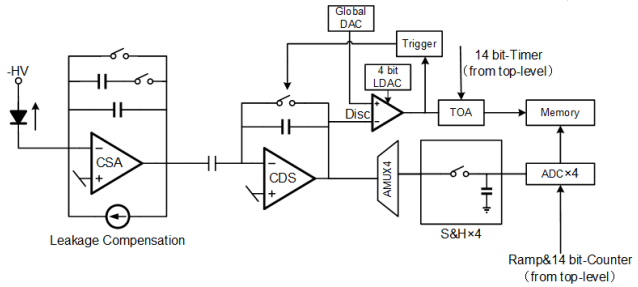
- **OTK: 300mW/cm2 vs σ_t~ 50ps**
  - Detector Cd: 10pF @CEPC AC-LGAD vs ATLAS HGTD 4pF, while timing is aiming the same
    - Power $\propto$ Cd^2, estimated 15mW/chn @ σ_t~30ps
    - Optimization of the detector expected, while a smart design of ASIC with low power is also critical
- **TPC：280μW/chn vs 500μm Pixel**
  - High precision Q & T measurement in very limited power
- **SiPM ASIC for ECAL, HCAL & Muon, 15mW/chn**
  - 0.1~3000 MIPs/chn, requires 2~3 gain channels per input
  - 0.5ns time resolution at the same time
  - 15mW/chn → 120kW of CAL in total, also expects a low power solution
- **Comment & Solution**
  - Co-optimization with ASIC & Detector: Cd matters a lot
  - Can we be benefit from advanced ASIC technology node? Speed maybe yes, others maybe no
  - Can we find a smarter FEE design scheme?

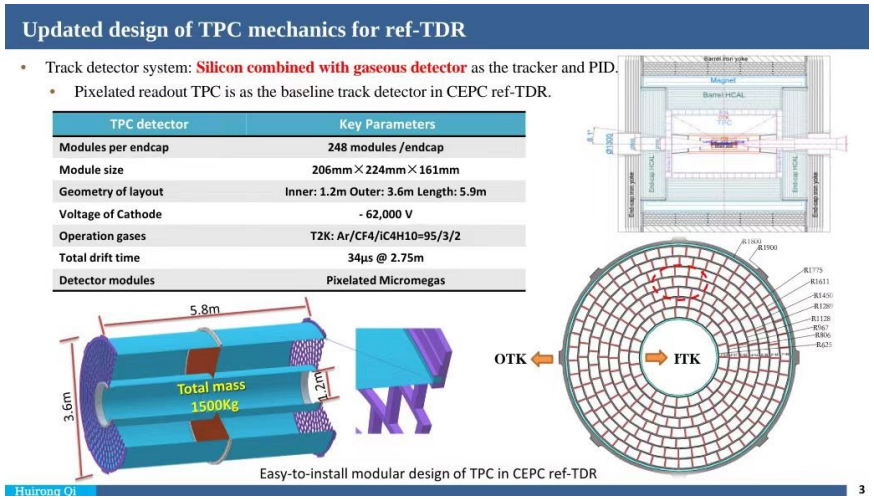
Preliminary readout scheme of Pixel TPC





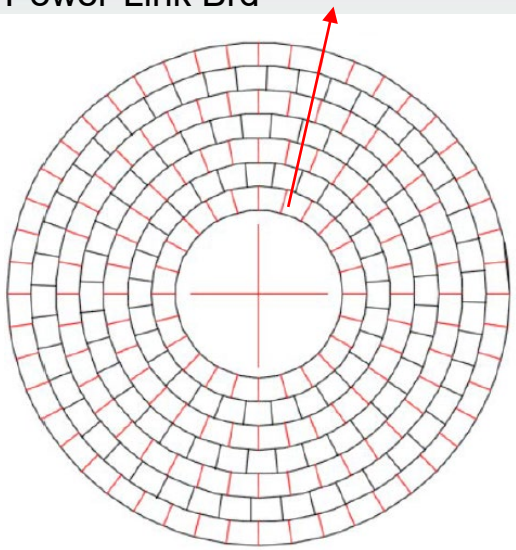
An integrated board with ASIC & MPGD, N(now 4) for a module
0.5mm*0.5mm / pixel





128 chn ASIC, Q+T measurement
142.8k pixel/module → 1115 chip/module→ 279 chip/FEE-0

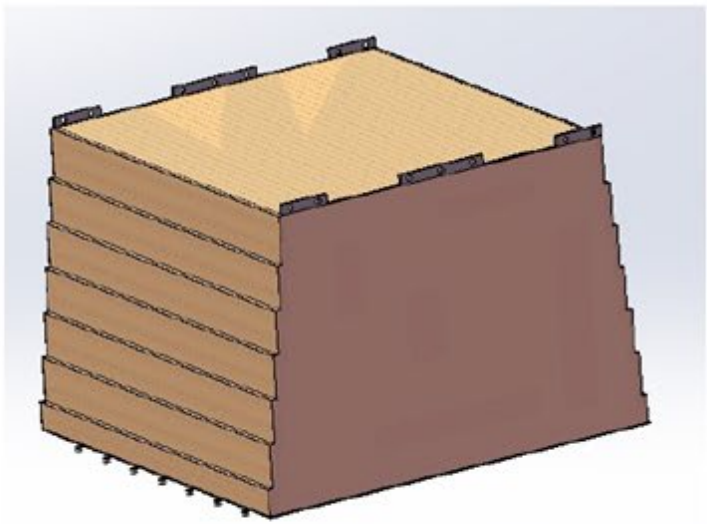
From Qi HR & Deng Z.

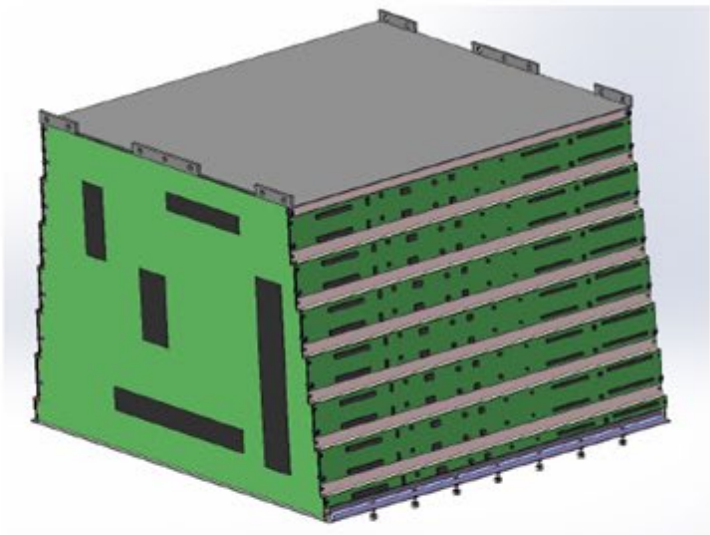


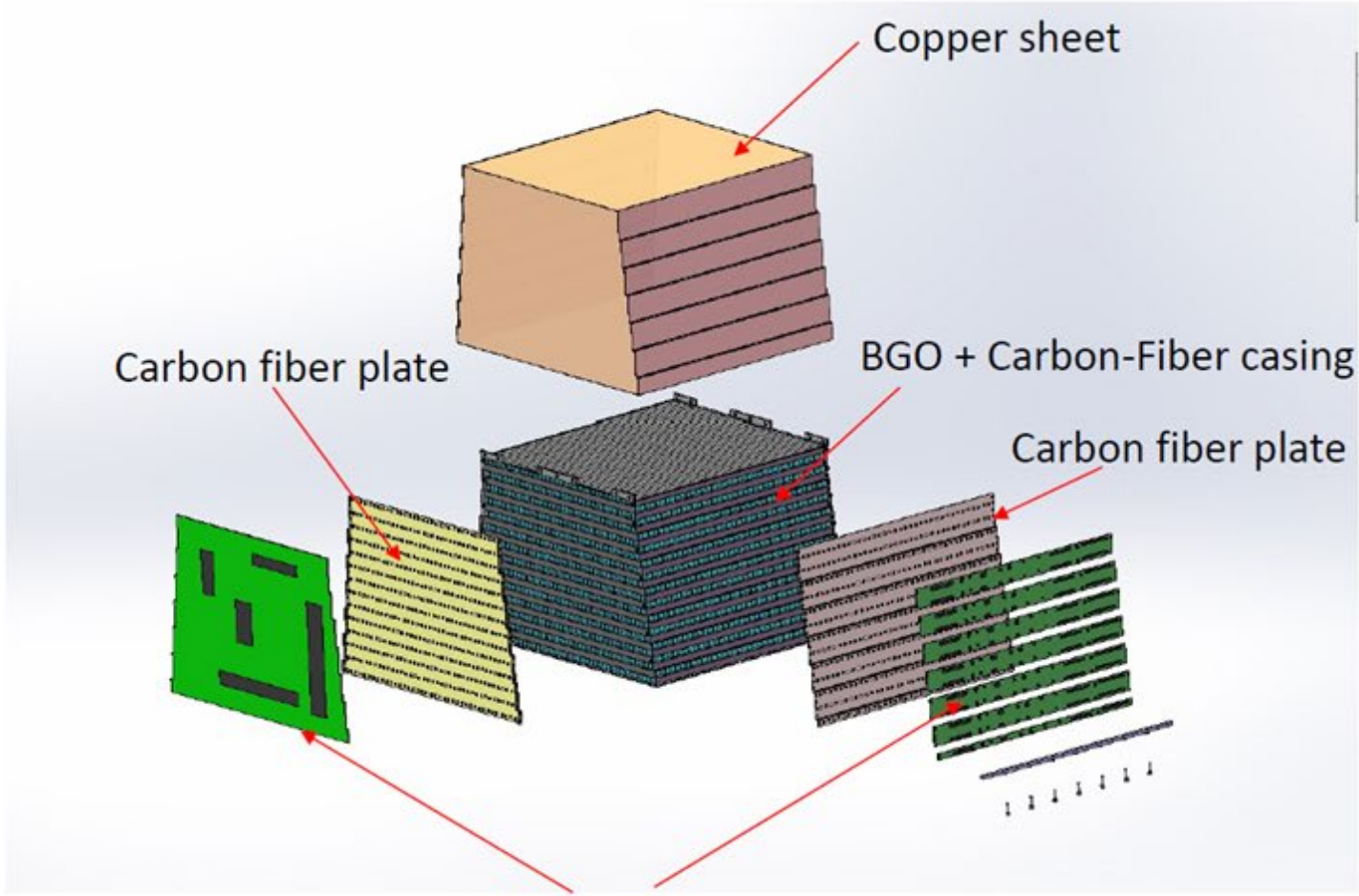
~248 Module/Endplate

Power:
Limit: <10 kW/endplate ~ 39.7 W/module ~10 W/FEE-0
35mW/ASIC ~ **280μW/chn**
Data rate:
80 particles/BX, 12,000 hit/particle, 32(48)b/hit, @ 40M BX Z pole
1 Module: ~100 Mbps(@ innermost)

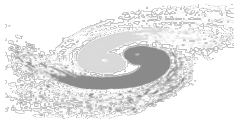
Barrel ECAL: module integration







Limited space vs advanced PCB & packaging



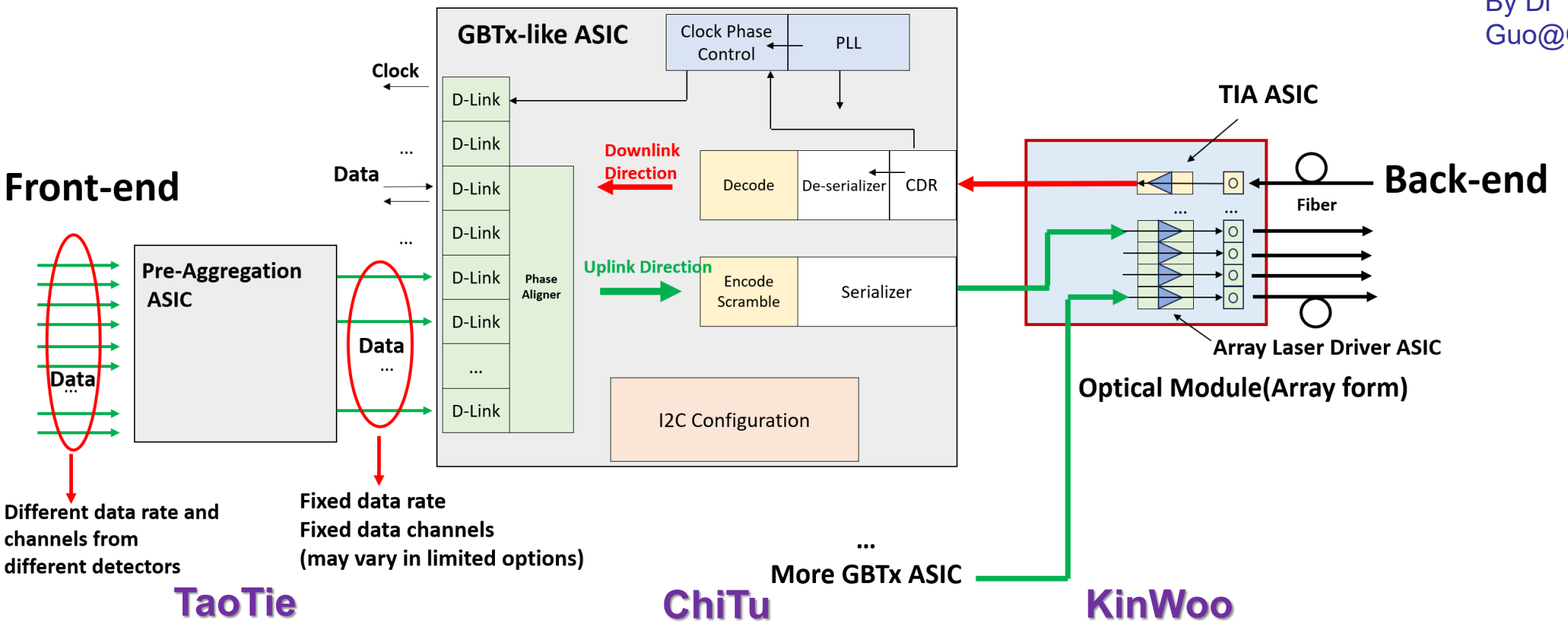
- **ECAL module**
  - A 1cm high & 40cm long narrow PCB, with close touch to SiPM, and density ASICs & routing only on one side
- **HCAL module**
  - A thin (1.2mm) but wide (40cm×40cm) PCB is allowed, risk of wrapping
  - While no large component is allowed, challenges for the local powering
- **TPC module**
  - Multiple layers with high density ASICs & sockets for the pixel TPC
  - Cooling pipe embedded closely with PCB & module
- **VTX Flex Cable**
  - Low material PCB based on Al is expected, while currently no vendor is available
  - A dedicated development may be needed
- **Comment**
  - Co-R&D and collaboration with PCB vendors become critical

Outline

- **Global Framework of the Elec-TDAQ system**
- **Main challenges & tasks of the FEE of Sub-Det**
- **Key blocks & plan of the common electronics**
  - Common data link
  - Common powering
  - Common BEE
  - Wireless communication based scheme
- **Summary**

Structure of the Data Transmission

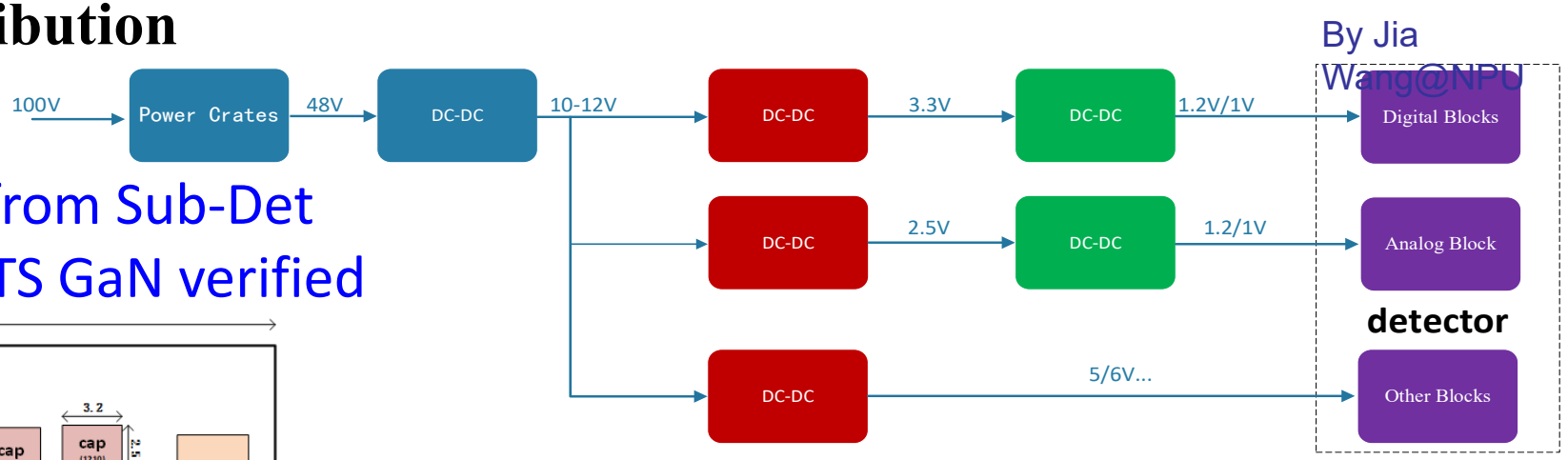
By Di Guo@CCNU



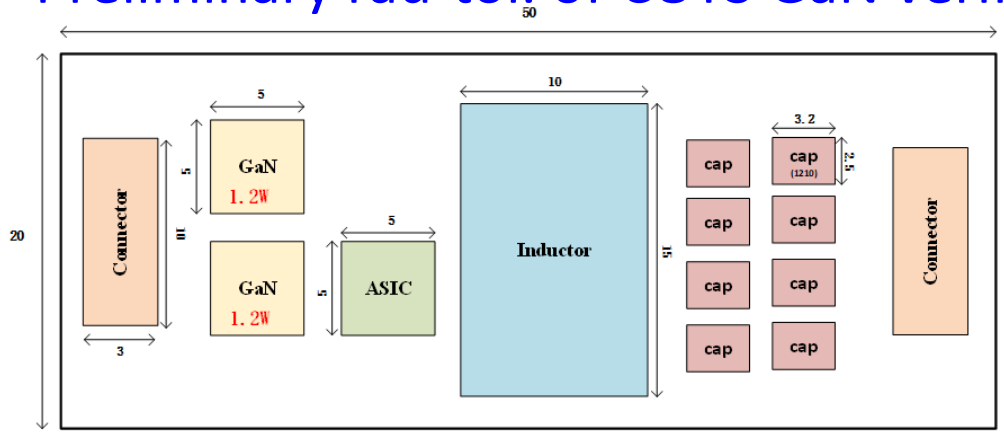
- **Pre-Aggregation ASIC (TaoTie): Intend to fit with different front-end detector (different data rates/channels)**
- **GBTx-like ASIC (ChiTu): Bidirectional serdes ASIC including ser/des, PLL, CDR, code/decode …**
- **Array Laser Driver ASIC + TIA ASIC + Customized Optical module (KinWoo)**

Power distribution & DC-DC module

- **Structure of power distribution systems**



- Design spec summarized from Sub-Det
- Preliminary rad-tol. of COTS GaN verified



	Nominal	Range
Input V	48V	36V-48V
Output V	1.2V	1.2V、2.5V
Output Current	10A	
Output ripple	10mVpp	
Efficiency	85%	80%-85%-80%（light-nom -heavy）
Dimension	50mmX20mmX6.7mm	Including cooling & shielding
TID	5 Mrad（Si）	
Magnet	3T	

- Proposed design of BUCK DC-DC converter

BaSha Series

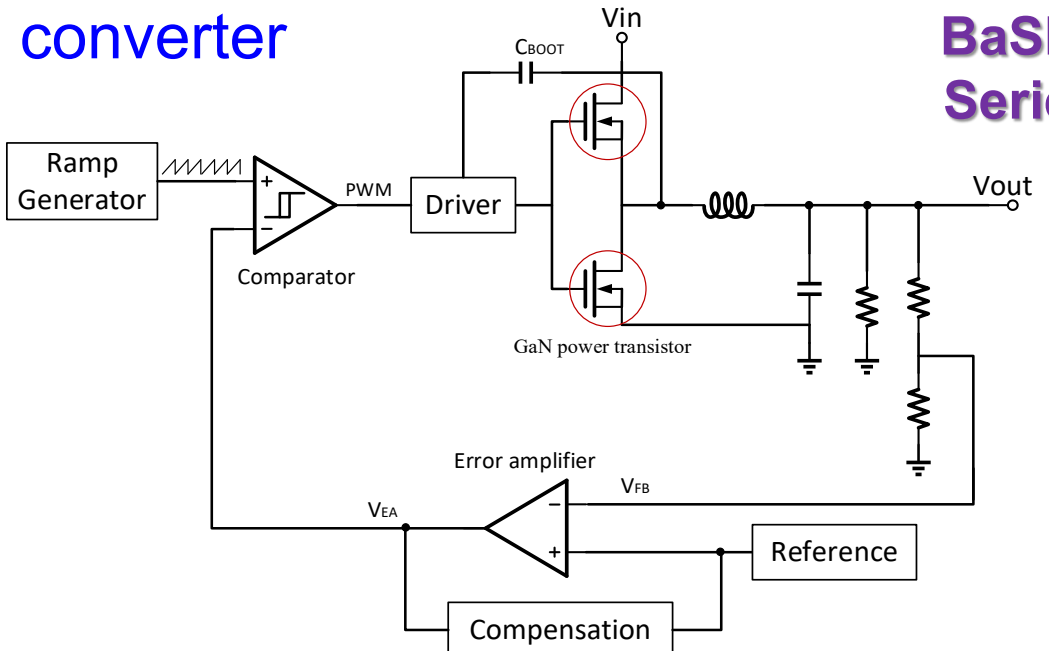
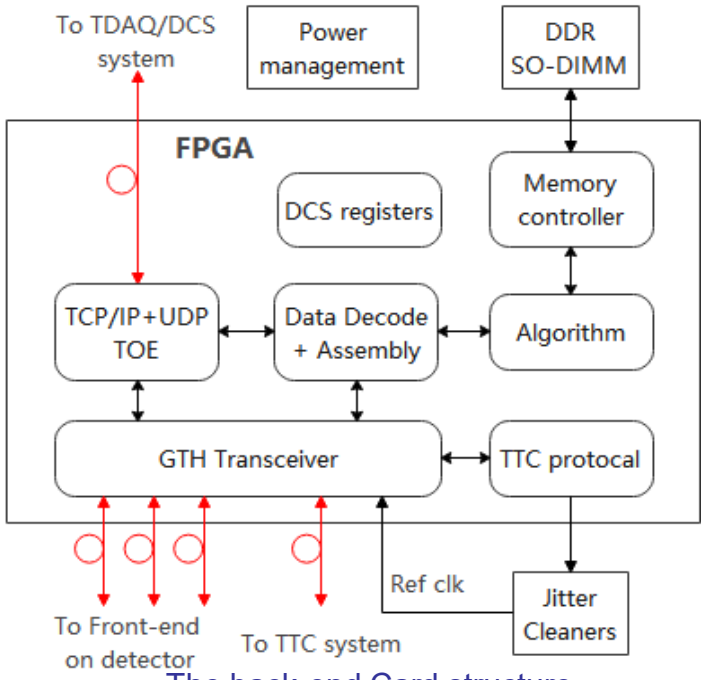
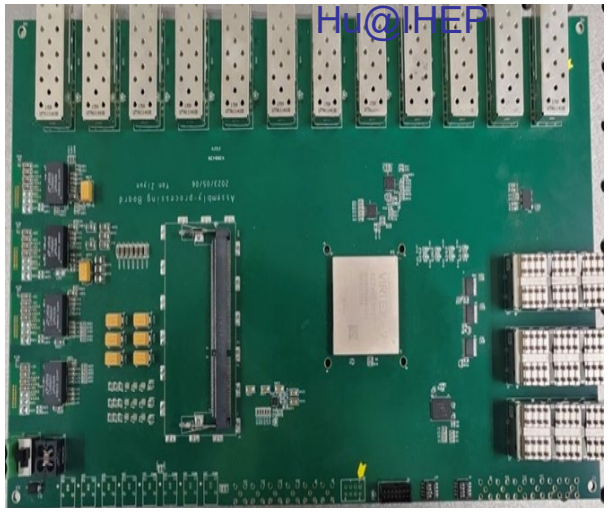


Diagram & prototype of common BEE



The back-end Card structure

By Jun Hu@IHEP



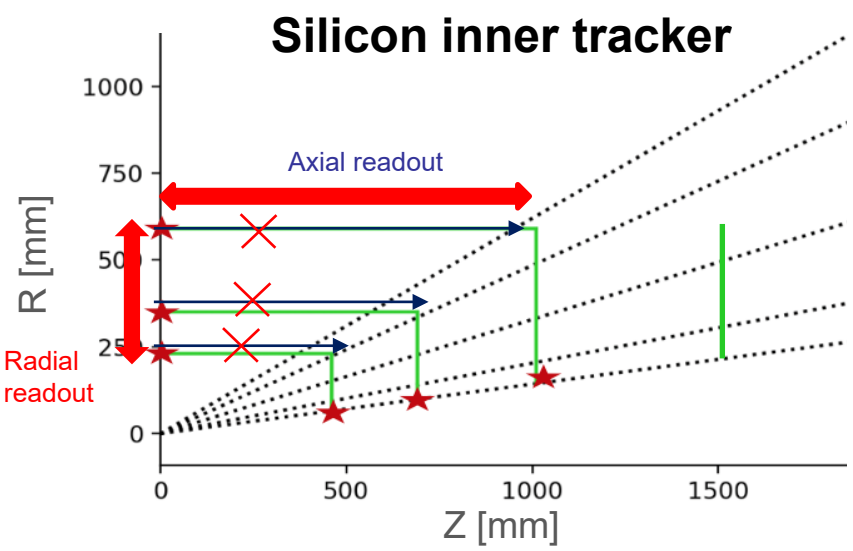
Data aggregation and processing board Prototype for Vertex detector

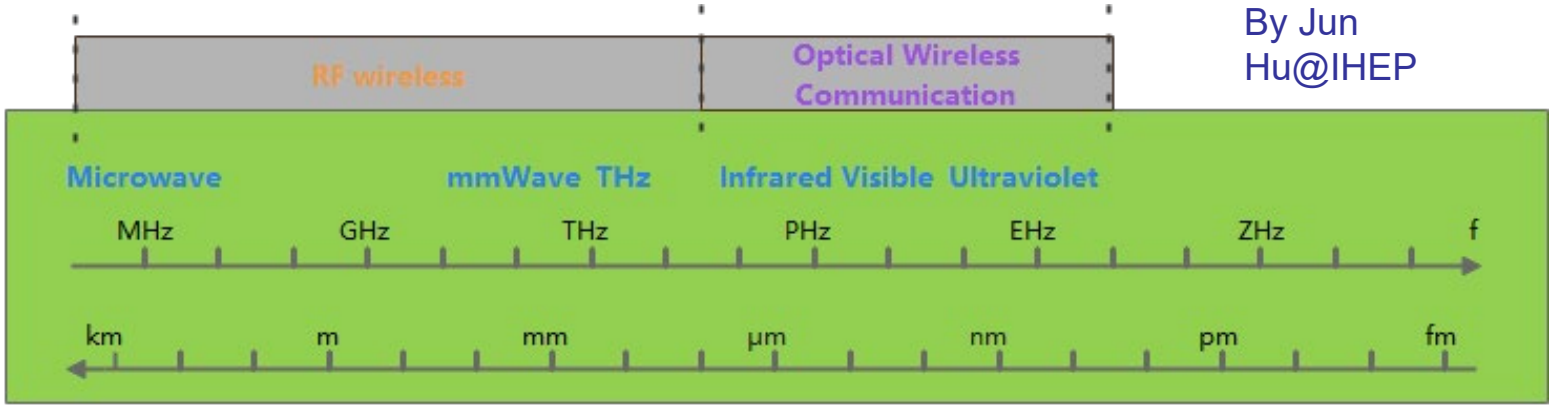
	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory (Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3 Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	

- Routing data between optical link of front-end and the highspeed network of DAQ system.
- Connect to TTC and obtain synchronized clock, global control, and fanout high performance clock for front-end.
- Real-time data processing, such as trigger algorithm and data assembly.
- On-board large data storage for buffering.
- Preference for Xilinx Kintex UltraScale series due to its cost-effectiveness and availability.

- A cost-driven device selection: FPGA XC7VX690T
- Interface：SFP+ 10Gbps X12 + QSFP 40Gbps X3
- Implement real time FPGA based machine learning for clustering, hit point searching, and tracking algorithms

Backup scheme based on wireless communication





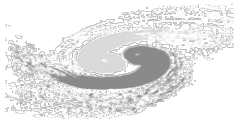
By Jun Hu@IHEP

- Radial readout with mm-wave
  - 12- 24 cm transmission distance
  - Data rate : < 30Mbps
- Axial readout to endcap
  - Only at the outermost layer or dedicated aggregation layer.

- WiFi (2.4GHz, 5GHz)
  - large antenna volume, high power consumption, narrow frequency band, and high interference
- Millimeter Wave (24GHz，45GHz，60GHz，77GHz)
- Optical wireless communication (OWC) / Free Space Optical (FSO)

- Wireless communication based readout scheme was proposed to mitigate the cabling problem, as a backup scheme
- Three major solutions were investigated through R&D, two were selected with corresponding schemes

Summary



- **Global framework of the electronics system defined for Ref-TDR**
- **A full ASIC FEE + a common platform BEE proposed for each sub-det, however main challenges should be solved from many aspects**
- **Recent & long plan**
  - **Prototypes of common platform and common blocks will be demonstrated in ~ 3y**
  - **Stitching VTX, high timing precision OTK ASIC & common SiPM ASIC for ECAL & HCAL & Muon are the major R&D tasks for FEE**
    - **Also expected to be demonstrated in ~3y**
- **Collaborations, from China & all over the world, are warmly welcome, for both FEE & common projects**

Backup

Naming of the common ASICs

ChiTu & Guan Yu

KinWoo in the sun

TaoTie

BaSha carrying a monument

- **GBTx-like: ChiTu (赤兔），the most famous horse in Chinese tales, ridden by the Chinese God of War Guan Yu. It is in charge of transportation with ultra fast speed, just as GBTx-like chip is doing.**
- **VTRx: KinWoo (金乌），the bird who lives in the sun in Chinese tales, an avatar of the sun and in charge of the light, just as the VTRx chip does, to convert electronic signal to/from optical.**
- **Data aggregation: TaoTie (饕餮），a mythical animal in Chinese tales, who can swallow anything, just as the chip does, to collect all the input data streams.**
- **DC-DC module: BaSha (霸下），one of the nine sons of the Chinese Loong, who is famous for its strongness and always to bear a monument. Just like the powering system which is the basement and support of all electronics.**

Choice on global framework

- **We choose FEE-triggerless readout (Backend Trigger) as our baseline global framework, while keep conventional trigger readout as the backup, for the Elec-TDAQ system:**

1. **Keep the max possibility for new physics and future upgrade**
   - readout all the information w/o pre-assumed trigger condition.
2. **Speed-up the FEE-ASIC iteration & finalization process**
   - w/o the need to consider the undefined trigger algorithm, esp. regarding the potential tight schedule.
3. **Make it possible for a common platform design for all Sub-Det**
   - Common BEE Brd, common Trg Brd, common data interface…
   - Scalable based on the detector volume
4. **Sufficient headroom for FEE data transmission based on current MDI background rate**
   - 10Gbps per link on FEE (max by ×4 links）