A timing circuit prototype design for sub-10ps time measurement applications

Chuanye Wang[1,4], Xiaoting Li[1,2,3], Wei Zhang[5], Xiongbo Yan[1,2,3]

Binwei Deng[6], Di Guo[7], Le Xiao[7], Jingbo Ye[1,2,3] , Lei Zhang[4]

[1]Institute of High Energy Physics Chinese Academy of Sciences, [2]State Key Laboratory of Particle Detection and Electronics, [3]School of Physical Sciences, University of Chinese Academy of Sciences,

[4]NanJing University, [5]Wuhan Textile University, [6]Hubei Polytechnic university, [7]Central China Normal University

Outline

- Introduction
- Circuit design
- Simulation result
- Conclusion

Introduction

◆ Applications

- HEP: Time Of Flight (TOF) measurements in timing detectors
- TOF-PET (positron-emission tomography)

◆ Current high-precision TDC ASICs

- ALTIROC
  - *Vernier delay line, LSB = 20 ps*
- ETROC
  - *Gated ring-oscillated (GRO) delay line, LSB = 19 ps*
- picoTDC
  - *Differential delay line with a 2nd-stage interpolation, LSB = 3 ps*

◆ Challenges

- Bin-size uniformity
- Multi-channel integration VS power consumption
- Readout bandwidth
- Potential bubble codes

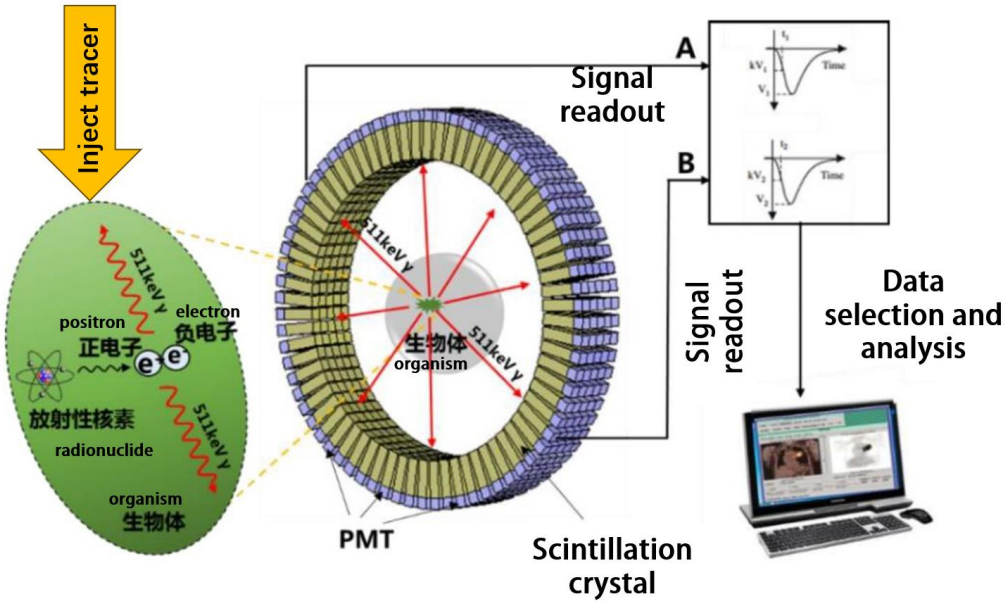


Fig 1. Basic structure of a TOF-PET detector system

Introduction

◆ Architecture

- ➢ Ring-oscillator based timing block
  - *RO Delay line (include passive interpolation)*
  - *Low-jitter phase-locked loop (PLL, 2.56/1.28/0.64 GHz)*
  - *Delay locked loop (DLL)*
- ➢ Quantization and readout
  - *DFFs*
  - *Synchronous coarse counter (7 bits)*
  - *Encoder*
  - *Serializer (1.28 Gbps)*

◆ Submitted in July 2024.

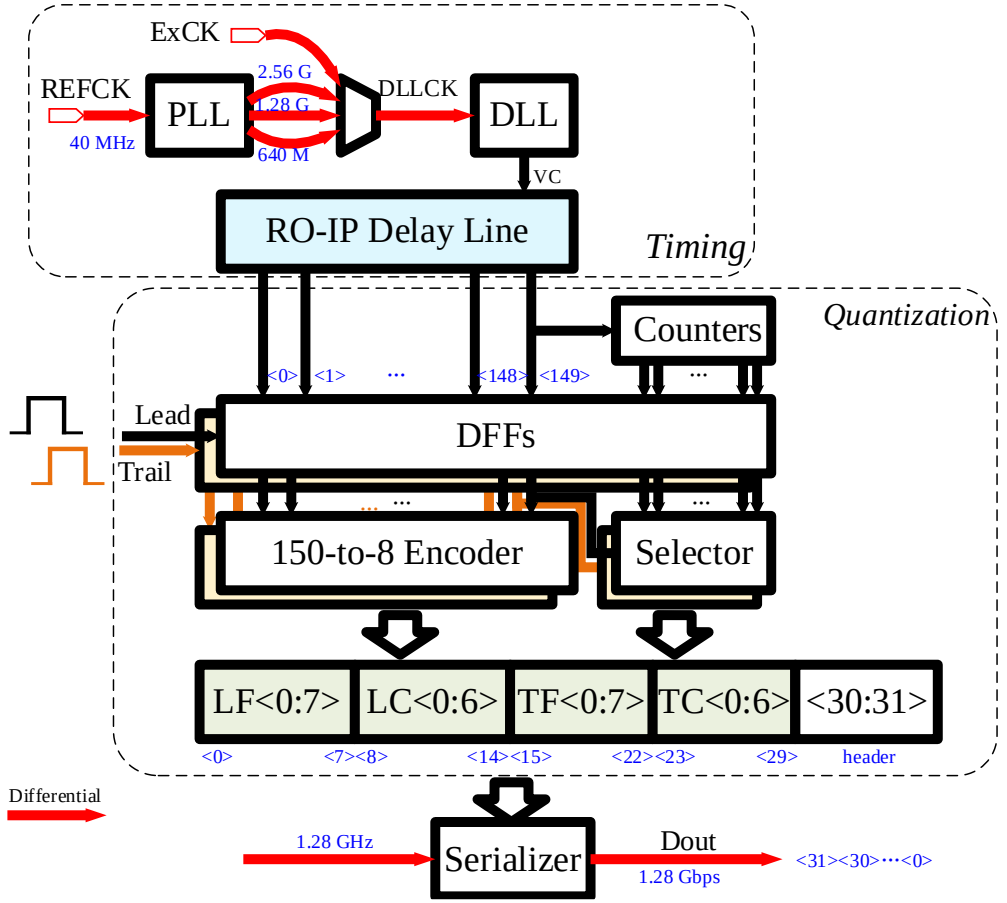


Fig 2. The overall block diagram

Circuit Design

DLL Design

- Based on a voltage-controlled delay line (VCDL)
  - *15 differential delay cells*
  - *2 dummy cells*
  - *Time intervals: 26 ps @ 2.56 GHz*
- Initial control-voltage settings (4 bit DAC)
- Provide a DVC signal to control the RO-IP delay line

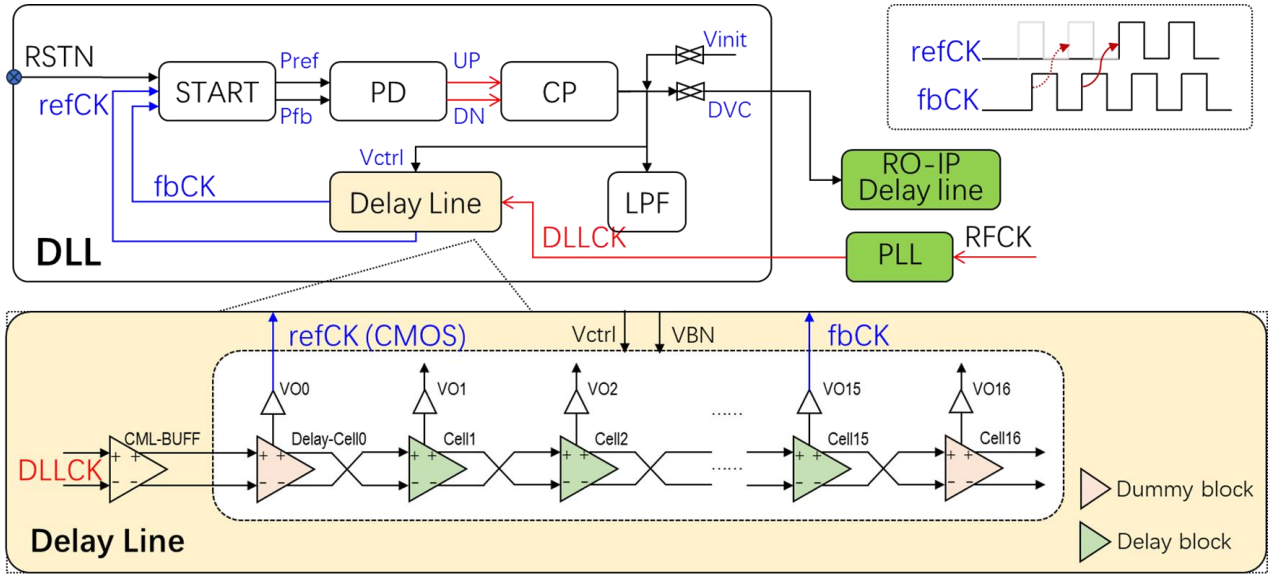


Fig 3. The block diagram of the DLL circuit

Circuit Design

RO-IP DL design

- 15 differential delay cells
  - *Same delay cells and same unit delays (26 ps)*
  - *Cross connections*
  - *Oscillating frequency ≈ ½ DLL clock frequency*
- 5-stage passive interpolation
  - *Resistor chain and buffers*
  - *LSB = 26 ÷5 = 5.2 ps.*
- Generate 150 fine-time phases

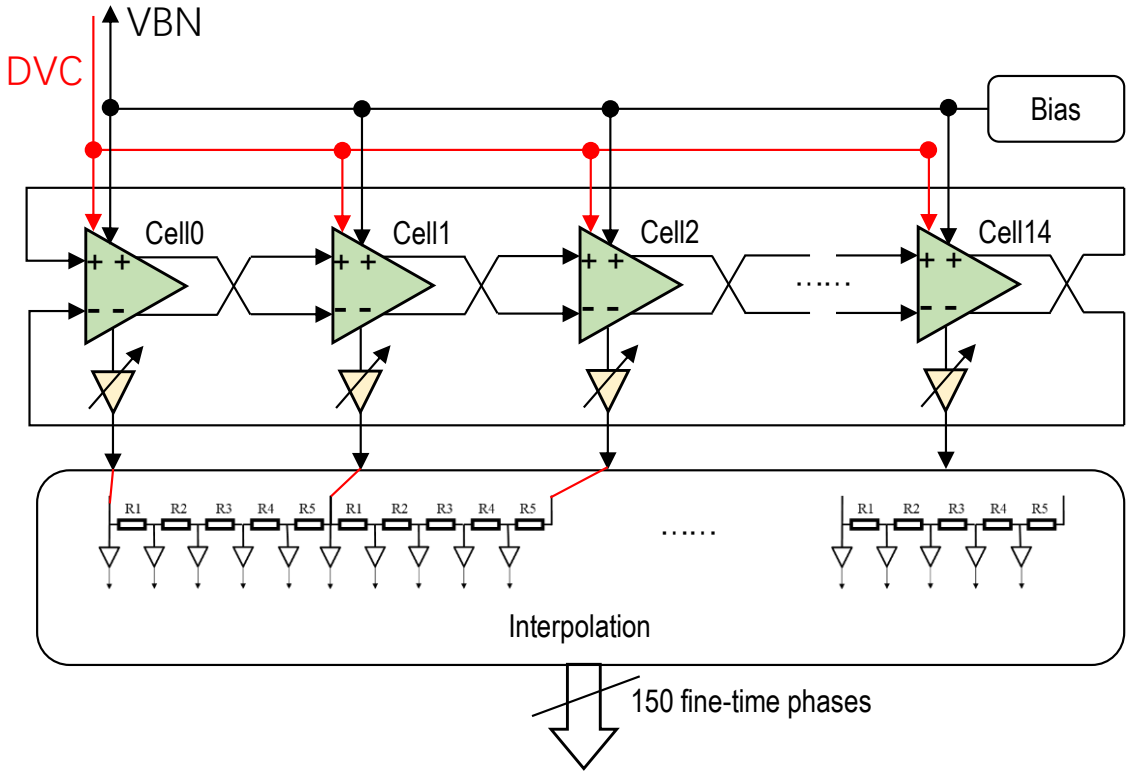
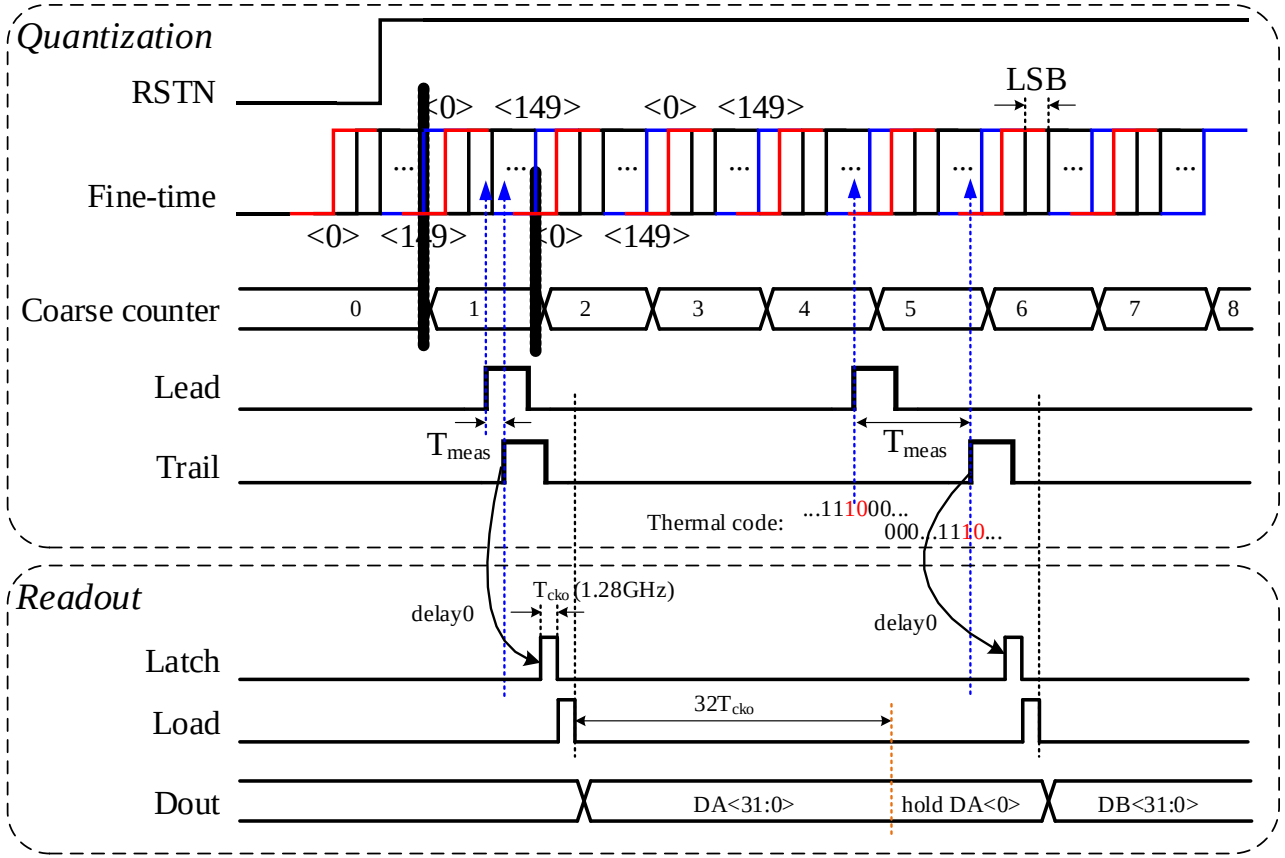


Fig 4. The architecture of the RO-IP delay line

Circuit Design

Quantization and readout

- Two groups of d-flip-flop (DFF) registers
  - *Connected to 150 fine-time phases and coarse counters.*
  - *Event trigger mode: Lead and Trail.*
- The difference in delay between rising edges of Lead and Trail represents the event pulse width.
- By tuning the delay with a step smaller than a bin-size, we can obtain an input-output transfer function.
- Calibrations can be made by setting the Lead or Trail to a fixed cycle.



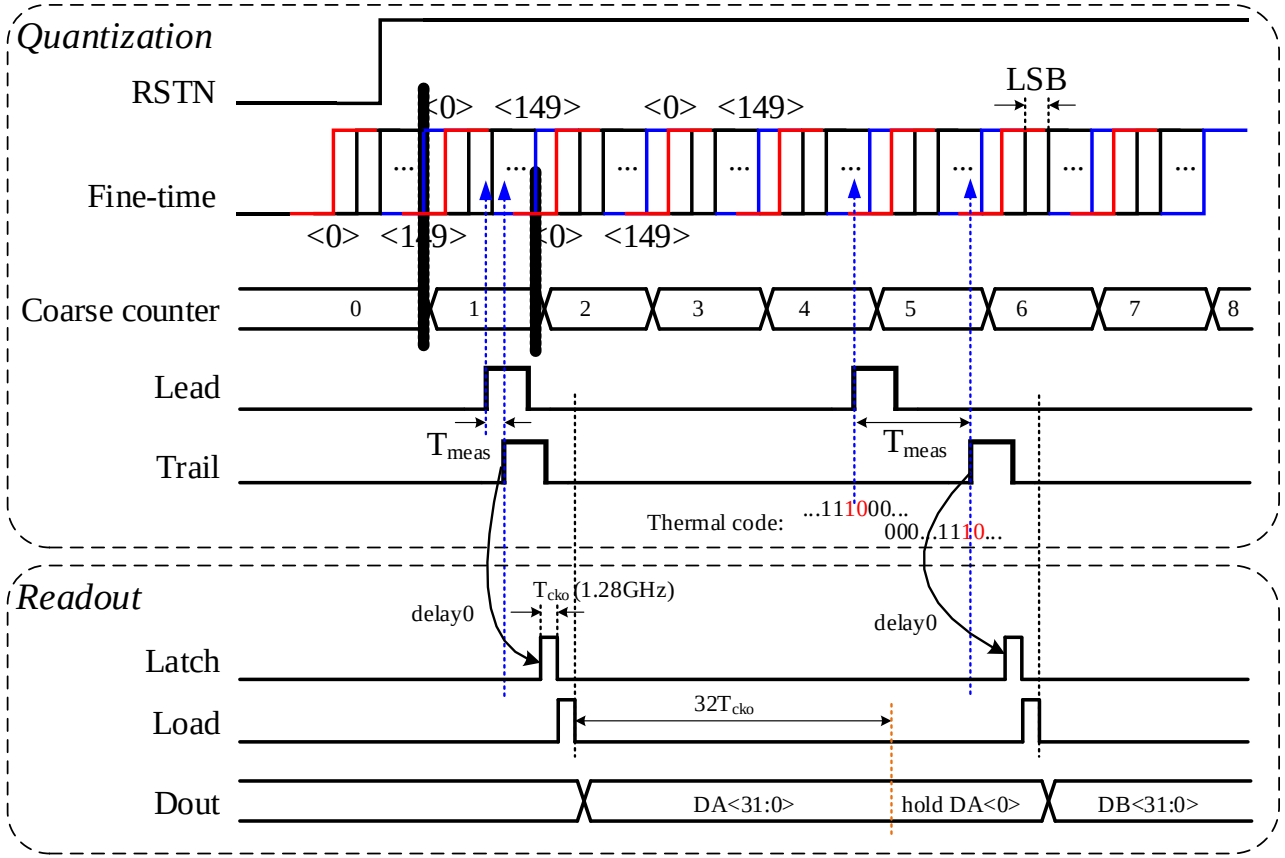
$$T_{meas} = Counter\langle Trail\text{-}Lead\rangle \times T_{RO} + Fine\langle Trail\text{-}Lead\rangle \times LSB$$

Fig 5. The overall timing of the quantization and readout

Circuit Design

Quantization and readout

- Two 7-bit synchronous counters (1.28 GHz)
  - *Metastability issue caused by asynchronous event signals*
  - *A nominal range of 100 ns.*
- Parallel data is serialized and output at 1.28 Gbps.
  - *Latch pulses capture the quantized codes into the input registers of the serializer.*
  - *Load pulses sequentially load the codes onto the output data line.*
- Serializer can be verified using an integrated pseudo-random binary sequence (PRBS7) generator.



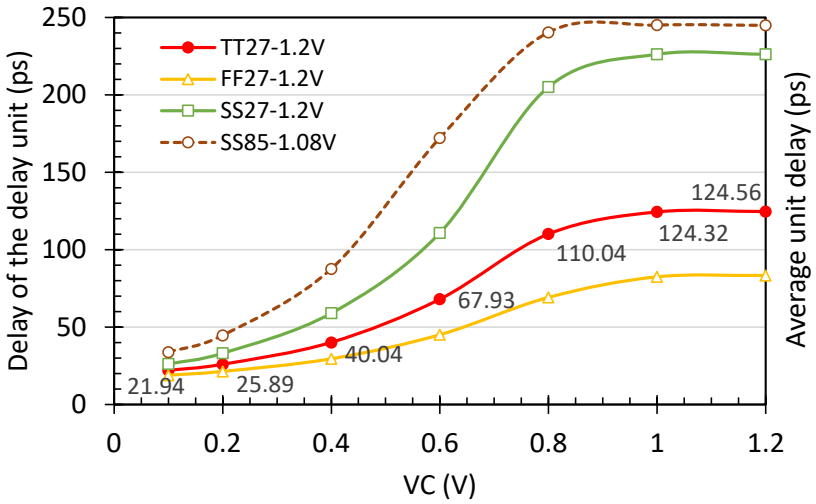
$$T_{meas} = Counter\langle Trail\text{-}Lead\rangle \times T_{RO} + Fine\langle Trail\text{-}Lead\rangle \times LSB$$

Fig 5. The overall timing of the quantization and readout

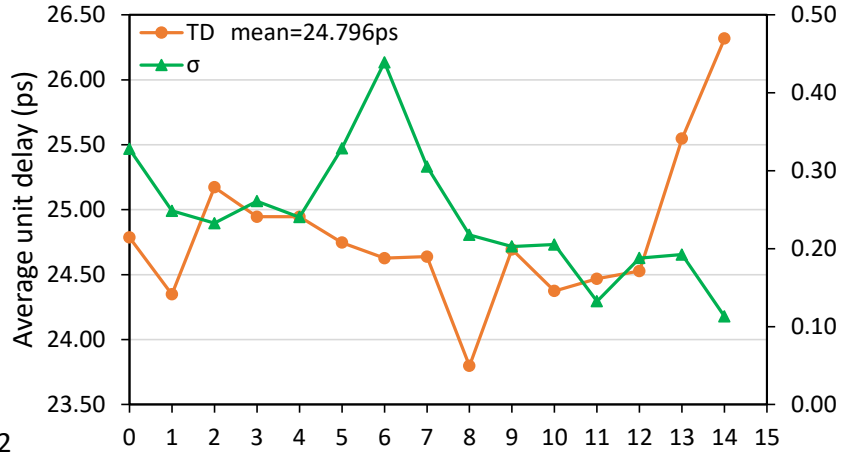
Simulation Result

Performance of the DLL

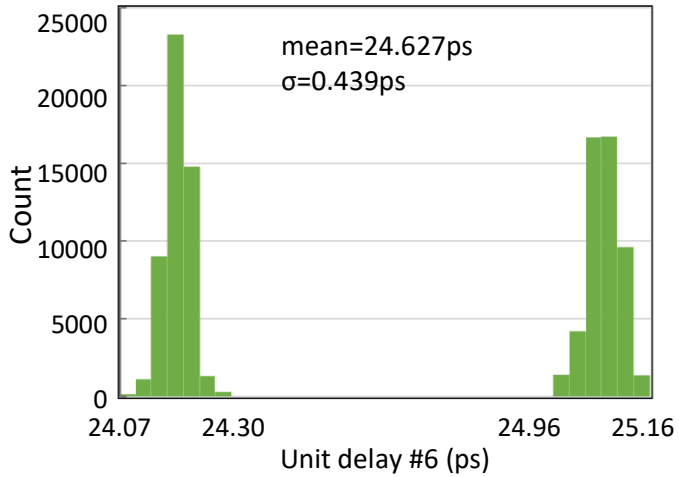
- The delay of each VCDL unit ranges from 21.94 to 124.56 ps under typical conditions (Fig 6a).
- Fig 6b shows the delays of 15 units in the DLL; Fig 6c presents the distribution of the 6th delay.
- The simulated total current is about 25 mA.



(a) Unit delay post-simulations of the basic delay cell



(b) 15 unit delays of the DLL



(c) 6th unit delay of the DLL

Fig 6. Performance of the delay cell and the DLL delay cells

Simulation Result

Performance of the RO-IP DL

- Fig 7 presents simulation results for the 150 bin-sizes with and without control of the DLL.
- The average bin-size is about 4.99 ps under typical conditions (maximum 6.02 ps; minimum 2.61 ps).
- The simulated current is 22 mA.

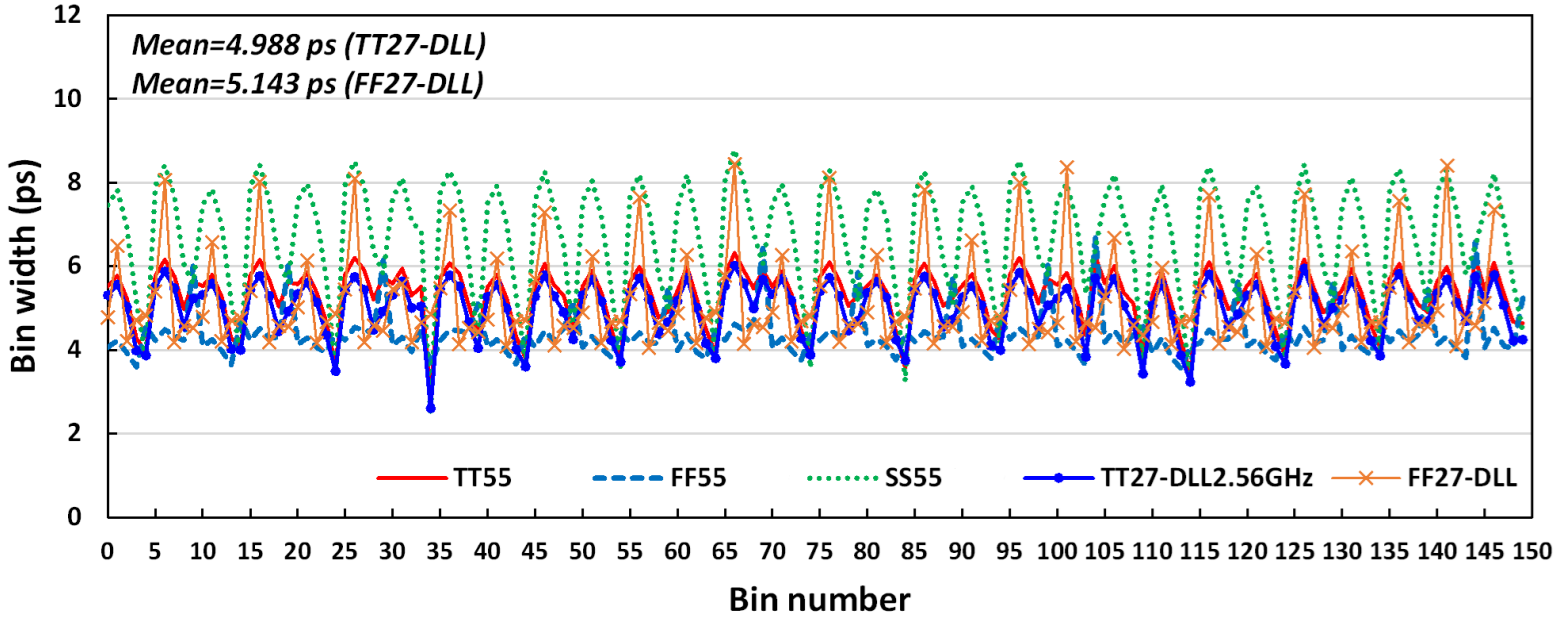


Fig 7. 150 bin-sizes of the RO-IP DL w/ and w/o the DLL

Simulation Result

Transfer function

- The simulated transfer function curve indicates that the timing circuit achieved the expected functionality, with an average bin-size of about 5.2 ps.
- Bubble and inconsistency issues.

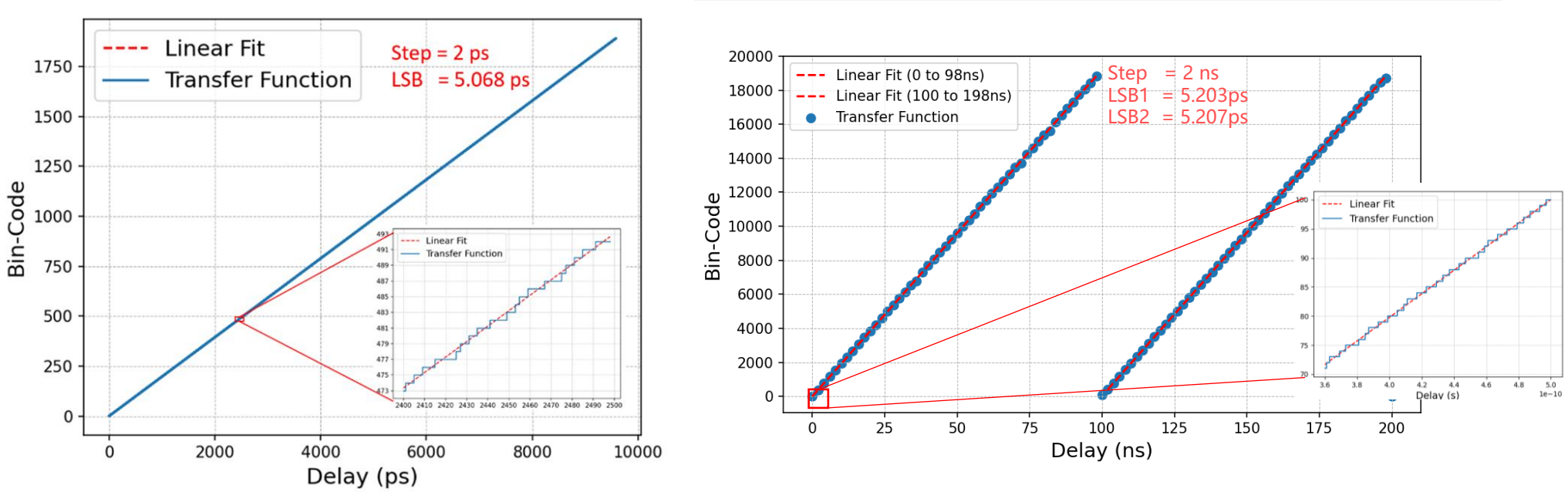


Fig 8. Transfer function curves: (left) pre-simulations and (right) post-simulations

Conclusion

- We designed a timing circuit for time measurement applications in high-energy physics experiments. It can achieve a nominal bin-size of 5.2 ps.
- The proposed RO-IP delay line architecture mitigates conflicts arising from DLL duty cycle distortion, the ring oscillator and the passive interpolator, and balances driving capability with power consumption.
- However, the current quantization circuit is very basic, and issues like bubble and inconsistency has not yet been addressed.
- To evaluate the performance of the 150 fine-time phases, we can derive an average transfer function curve by conducting repeated measurements and excluding any anomalous bubble data.
- Preparation for the test board and platform are underway. Chips are expected to be received and tested in November.

Thank you!