环形正负电子对撞机
Circular Electron Positron Collider

CENTRAL CHINA NORMAL UNIVERSITY

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A 14bit 100 MS/s Two-Step Split SAR ADC using low-power RA and in-stage redundancy technology

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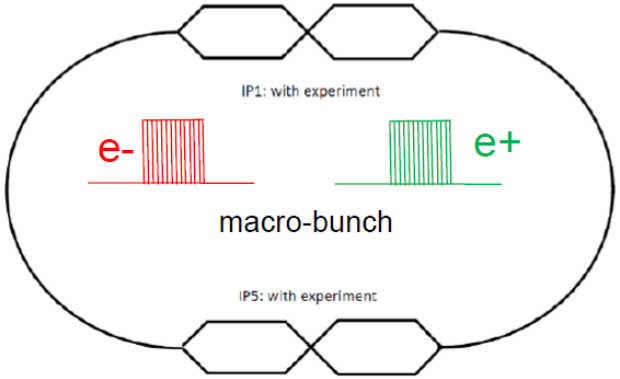
Outline

- ✓ Introduction
- ✓ 14bit 100 MS/s Two-Step Split SAR ADC
  - SAR ADC design
  - Residual amplifier design
  - Overall analysis
- ✓ Summary and Outlook

Introduction: CEPC and its beam timing

Circular e^+e^- Higgs (Z) factory **Fast readout speed**

E_{cm}≈240GeV, luminosity ~2×10^{34} $cm^{-2}s^{-1}$, can also run at the Z-pole

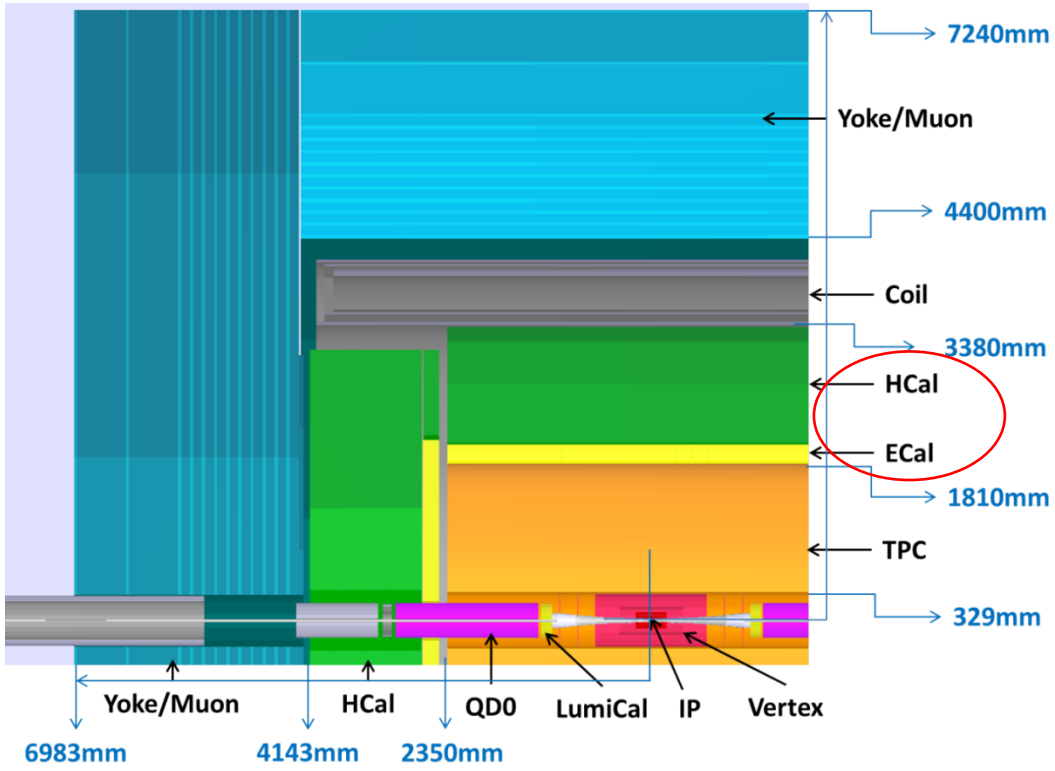


Partial Double-ring Scheme

- Crab-waist collision to reduce beam and AC power
- Avoiding pretzel scheme to increase the flexibility and luminosity
- 196ns bunch spacing
- 48 bunches / train
- Duty cycle: 9.4μs/181μs

Reference: CEPC/SppC with ILC (FCC), J. Gao, LCWS 2015, Nov. 2-6, 2015, Whistler, Canada

Introduction

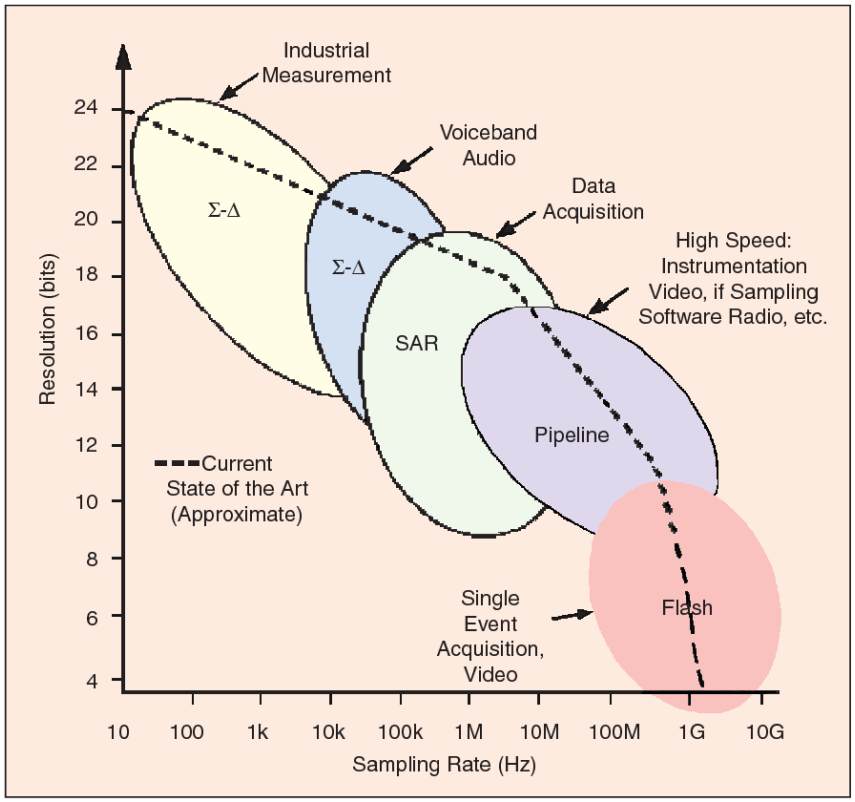


- Accurate measurement of particle energy requires a Calorimeter system to accurately measure the energy of the jet formed along various directions after particle collision.
- Approximately 72% of jet energy is measured by electromagnetic calorimeter (ECAL) and hadron calorimeter (HCAL).

The Calorimeter requirements:

- The high collision energy – high radiation tolerance
- High brightness – high energy resolution
- High speed analog-to-digital converter with high radiation tolerance

ADC architectures



ADC architecture, applications, resolution, and sampling rate

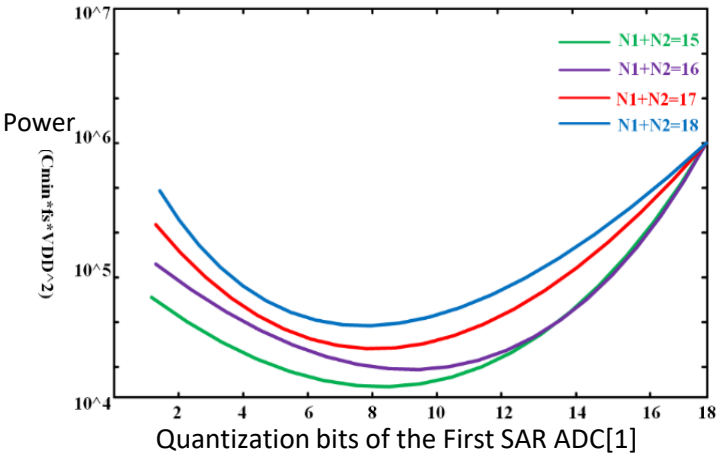
- Sigma-Delta ADC: High precision, low power consumption, but slow speed
- SAR ADC: Low power consumption, slow speed
- Pipeline ADC: High speed, high precision, large power consumption and area
- Flash ADC: high sampling rate, low resolution

- Pipelined SAR ADC: Combining the advantages of pipeline ADC and successive approximation ADC, it achieves high speed and accuracy while maintaining low power consumption and small area.

ADC architectures analysis

Analyzing the selection of quantization bits for each SAR ADC from the perspectives of linearity and power consumption.

Two step SAR ADC



The relationship between power consumption and first level quantization bits of Pipelined SAR ADC

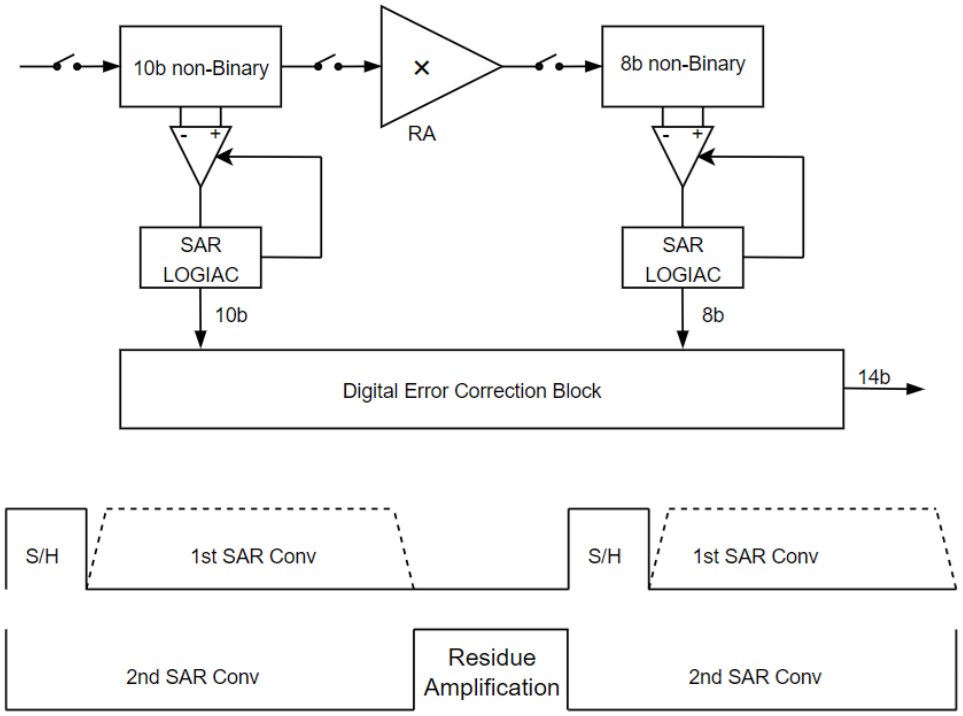
The higher the resolution of the first SAR ADC

- The lower requirement for capacitor matching and the smaller the nonlinearity caused.
- The higher the inter stage gain.-> use redundancy
- The nonlinearity of the second SAR ADC will be attenuated more.

- **Choose the first stage SAR ADC with an accuracy of 9 bits and the second stage SAR ADC with an accuracy of 7 bits.**

[1]Chen K, Duong Q, Alvandpour A. Power analysis for two-stage high resolution pipeline SAR ADC[Z].

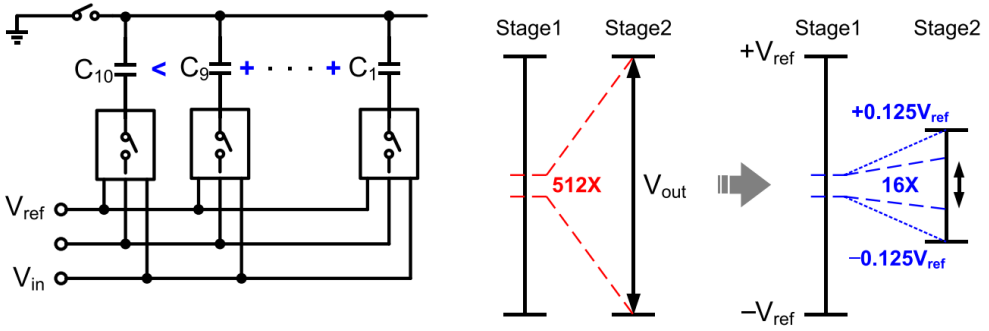
ADC diagram design



Block diagram of the ADC and its timing diagram

- 9 bits SAR ADC： Quantify the input signal with 10 bits, including 1-bit internal redundancy.
- RA： Amplify the residual error of the first level quantization.
- 7 bits SAR ADC： Quantify residual signal, including 1-bit internal redundancy.
- Digital Error Correction Block： Delay align the output digital code and perform redundancy calibration.
- Asynchronous switching logic. -> save power consumption.

ADC diagram design



$$\frac{k_B T}{C} \le \frac{\Delta^2}{12} \longrightarrow C \ge 12 k_B T \left(\frac{2^B - 1}{V_{FS}}\right)^2 \longrightarrow C \ge 12 k_B T \times \frac{2^{2B}}{{V_{FS}}^2}$$

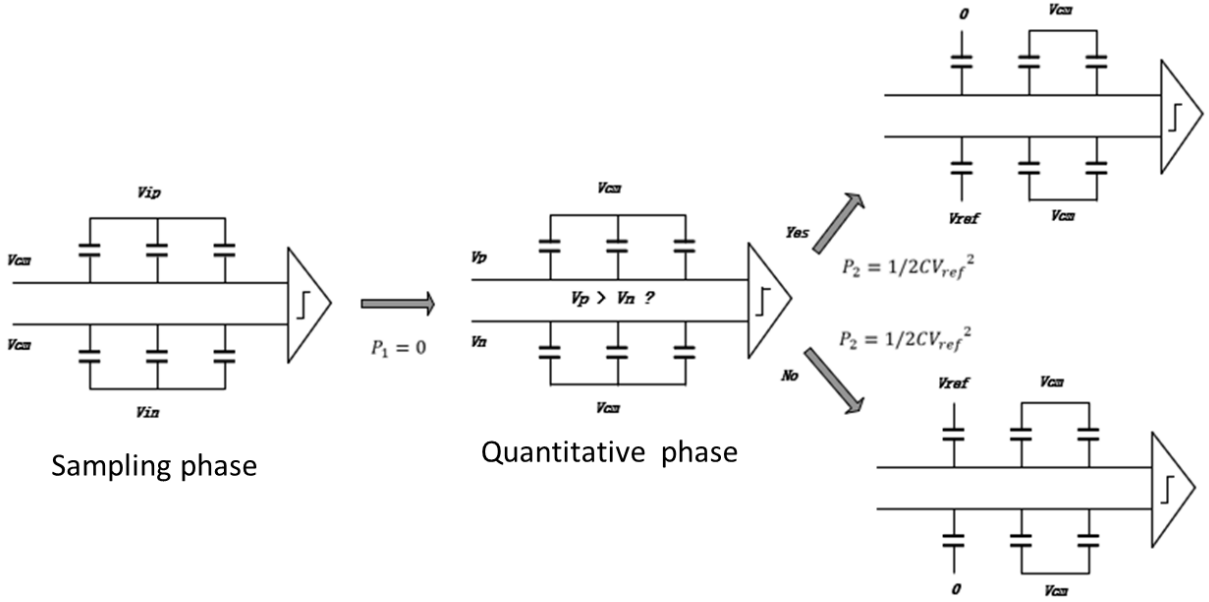
C1 total≥280 fF

- First stage SAR ADC Ctotal is 511 fF, Vref1 is 1.2V.
- Second stage SAR ADC Ctotal is 63 fF, Vref2 is 150mV.
- Due to inter-stage 2-bit redundancy and the Vref2 is smaller，
  The gain of RA is reduced from 512 to 512/4/8=16.

◆ 10 bit non binary weight, with 1 bit internal redundancy

C	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	Total
weight	230	130	68	36	20	12	8	4	2	1	511

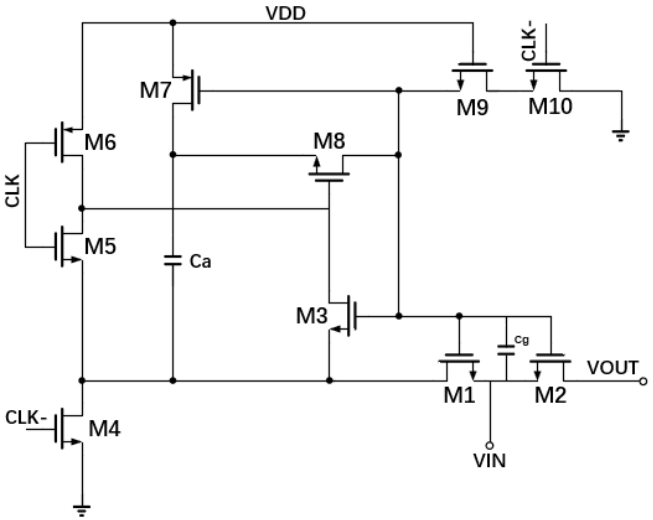
SAR ADC Switching strategy



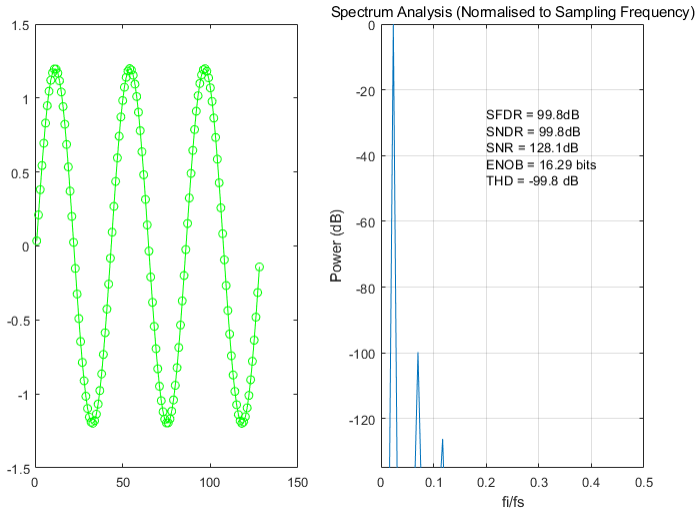
- Sampling of the lower plate of capacitors.
- Vcm-based switching strategy.

  the power consumption is reduced by 87.9%.
- No shift of the common voltage during successive approximation.

bootstrapped switch



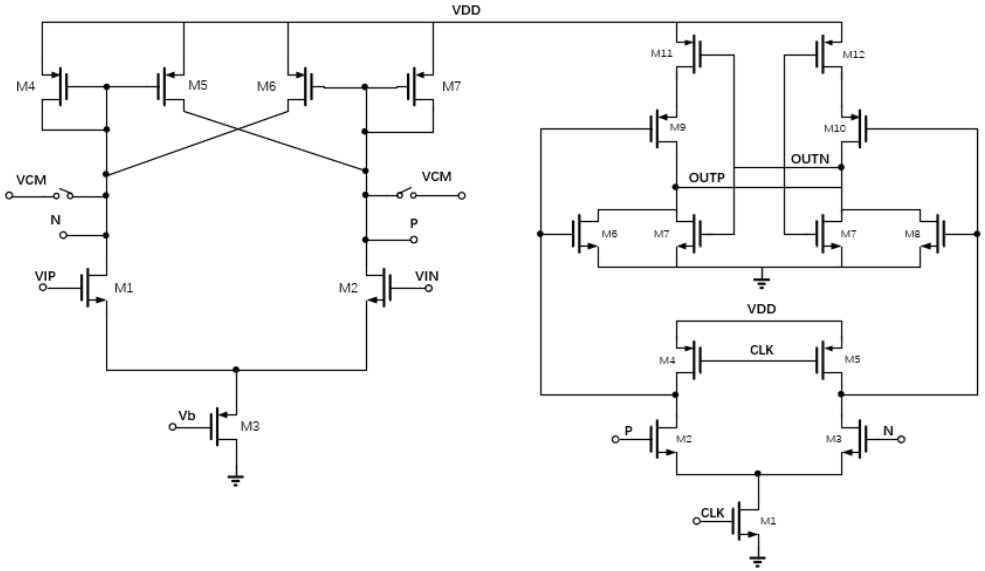
bootstrapped switch scheme



FFT analysis

- maintain the turn-on resistance and reducing nonlinearity.
- At an input signal frequency of 3M, its SFDR is 99.8dB, SNDR is 99.8dB, SNR is 128.1dB, and ENOB is 16.29bit, all of which are higher than the overall design specifications of the ADC.

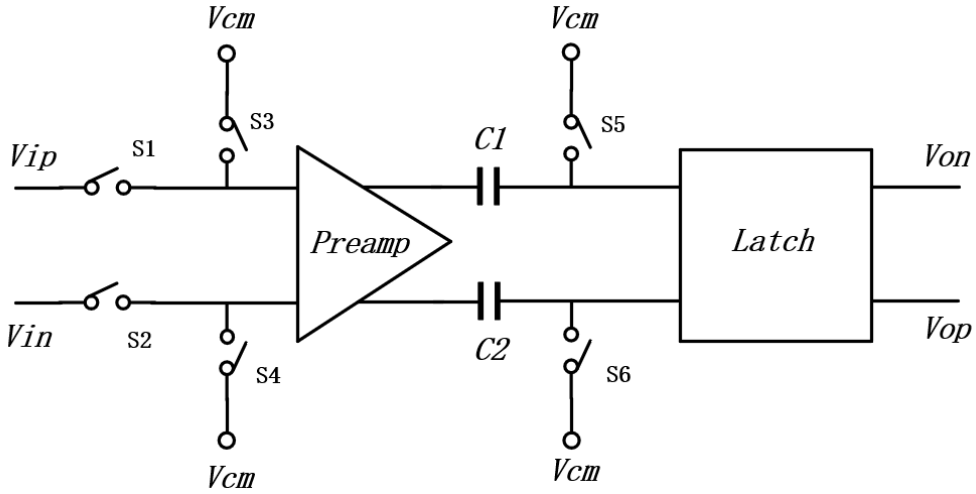
Dynamic comparator design

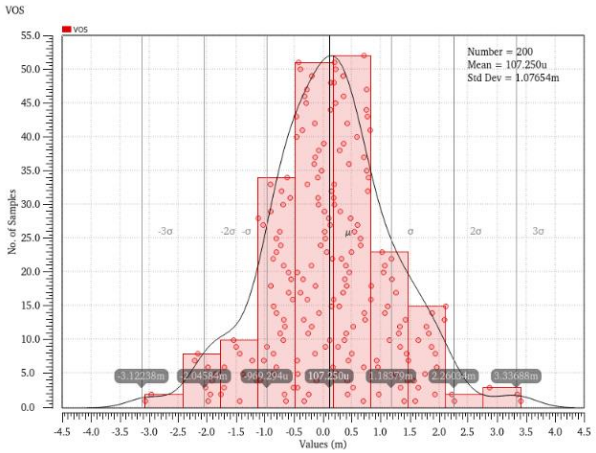


Block diagram of comparator

- By using a preamplifier and latch structure, the impact of kickback noise on the front-end can be suppressed.
- Add a reset signal to the output of the preamplifier to improve fault tolerance.
- Positive feedback structure, high resolution, fast speed, and low power consumption.

Dynamic comparator design

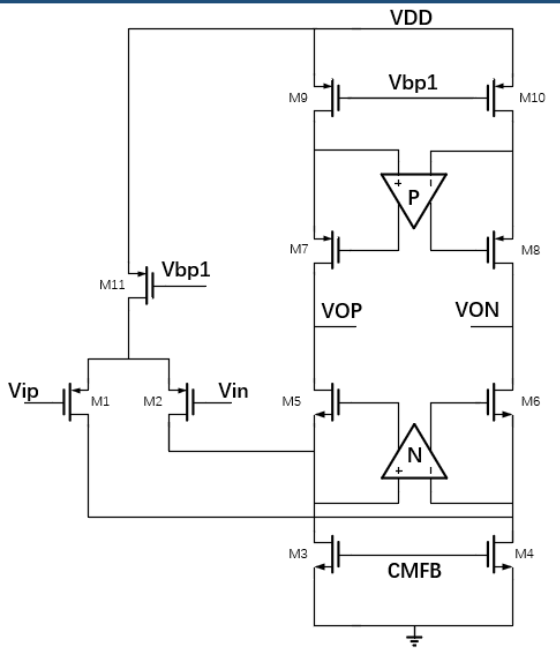




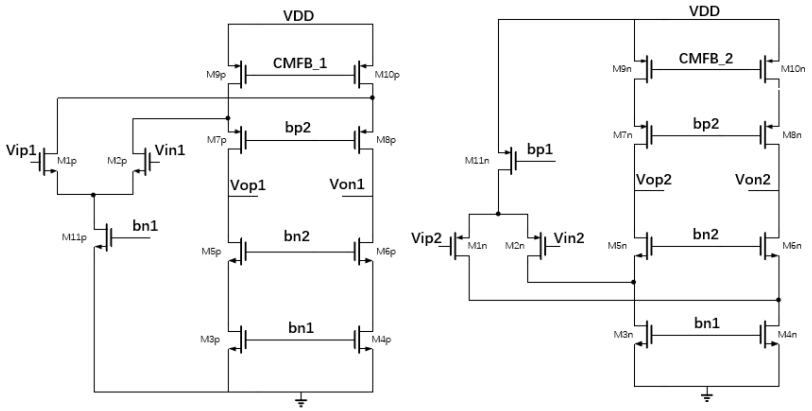
Misalignment self calibration circuit

- Using OOS(Output Offset Storage), the de misalignment technique is divided into a calibration stage and a comparison stage.
- The Monte Carlo simulation results in the left figure show that the equivalent input offset voltage 3 σ is about 3.2mV, which meets the design specifications.

RA design



Gain enhanced operational amplifier

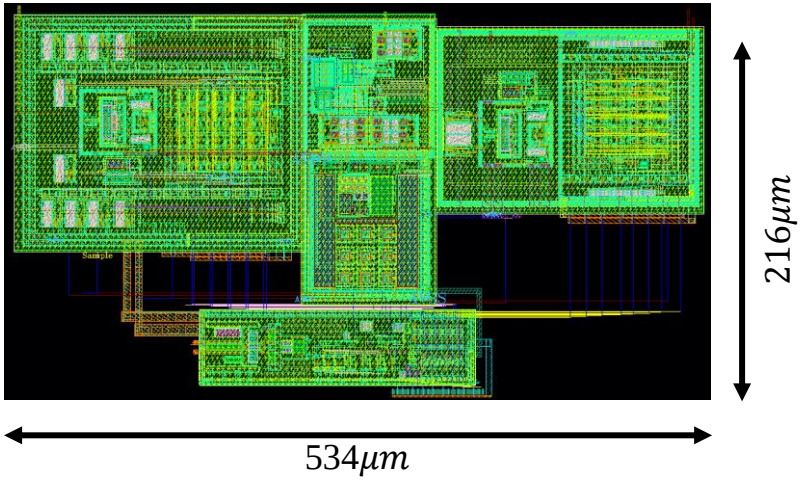


Auxiliary operational amplifiers

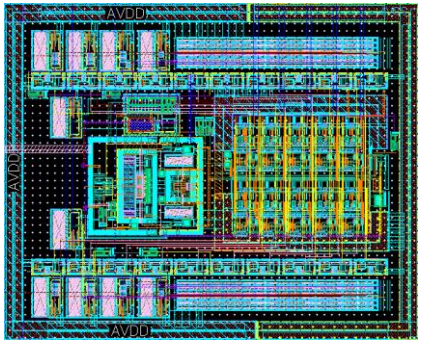
corner	Ao (dB)	GBW (Hz)	PM(°)	POWER (mW)
ss@-40°	62	4.5G	62	3.8
tt@27°	66	5.1G	63	4.5
ff@85°	61	4.6G	77	6.2

- The main operational amplifier adopts a folded cascode structure.
- The auxiliary operational amplifier adopts a folded cascode structure similar to the main operational amplifier.
- Switching capacitor common mode feedback to maintain circuit common mode operating point .

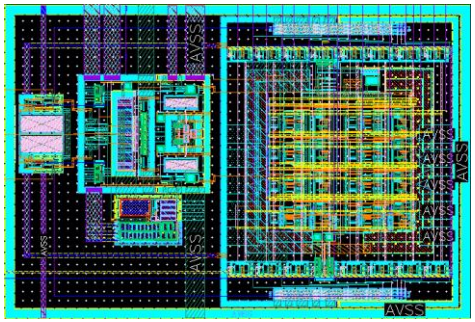
Layout design



Core Circuit Layout



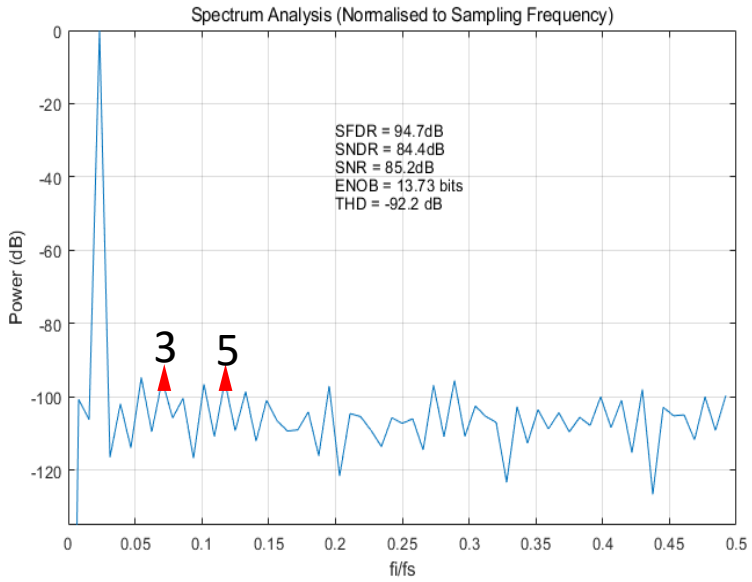
First SAR ADC Layout



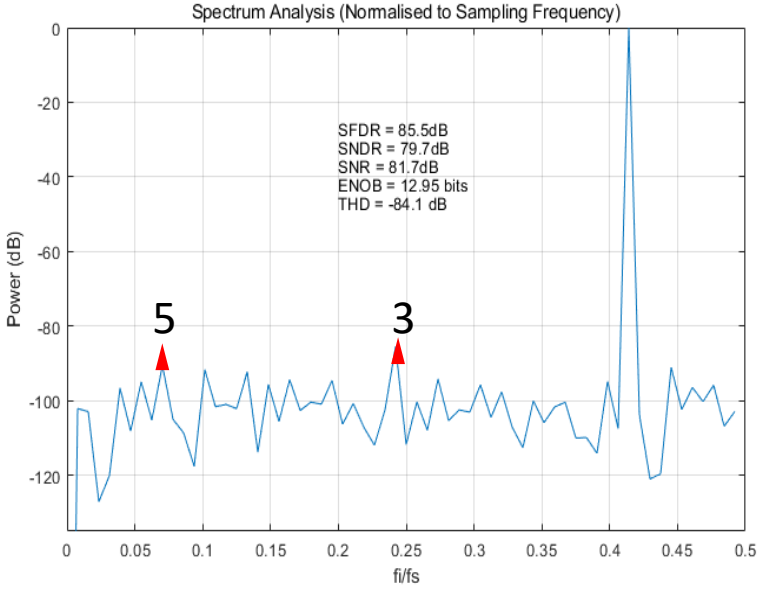
Second SAR ADC Layout

- Separate analog and digital power supplies.
- The capacitor array adopts the same height of the MOM cap and add dummy cap around.
- The SAR logic connection is the shortest to decrease signal delay.
- The core circuit area is 534 $\mu m*$ 216 μm.

Simulation results



FFT analysis results(fin=3M and fs=100M)



FFT analysis results(fin=40M and fs=100M)

- In a typical process corner tt@27℃ and an input signal frequency of 3M, the SNR is 85.2dB, SFDR is 94.7dB, and ENOB is 13.73 bit.
- In a typical process corner tt@27℃ and an input signal frequency of 40M, the SNR is 81.7dB, SFDR is 85.5dB, and ENOB is 12.95bit.

Summary and outlook

➢ Summary

Supply	1.2V	SNR	76.0dB
Resolution Ratio	14 bit	SFDR	85.0dB
Input Range	0 ~ 2.4V	SNDR	75.4dB
Sampling Ratio	100Msps	ENOB	12.95 bit@40M
Power	11.8mW	Area	650×380μm²

Performance Summary of the Pipelined SAR ADC

➢ Outlook

- Adding on-chip calibration technology to the capacitor array can further reduce the capacitance and to save power.
- Radiation resistance considerations.
- On-chip high speed clock circuit and bias block.
- Multichannel design.

Thank you for your attention!