Design of High-Speed and Large Input Dynamic Range SiPM Readout Chip

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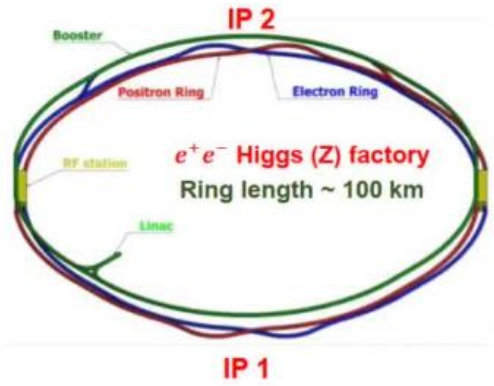
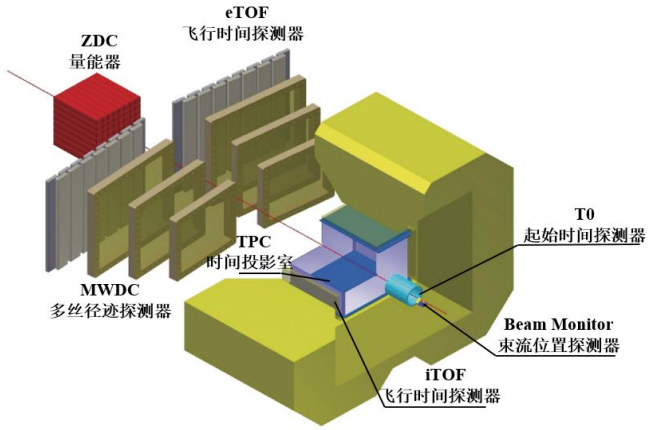
01 Research Background

- Many high-energy physics experimental installations have been built in China, such as CEPC and HIRFL. These physics experimental devices will provide an experimental basis for exploring the microscopic world.
- CEPC is aimed at exploring the Higgs particle, and HIRFL is used to carry out research in heavy ion physics and its interdisciplinary aspects.
- We have done some research on fast, large dynamic range readout circuits that process signals covering a dynamic range of 160 fC-160 pC with a signal pulse width of 10 ns.

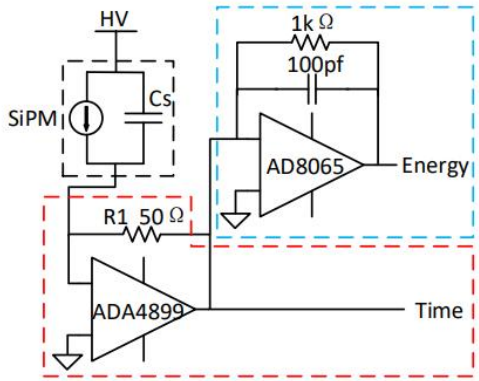


CEPC

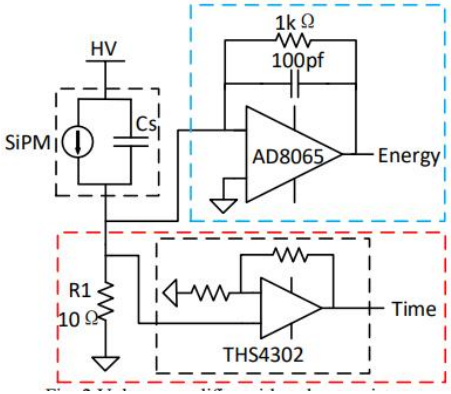


CSR External Target Experiment

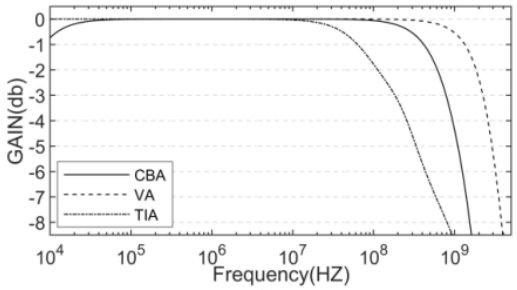
01 Research Background



Trans-impedance amplifier



Voltage Amplifier



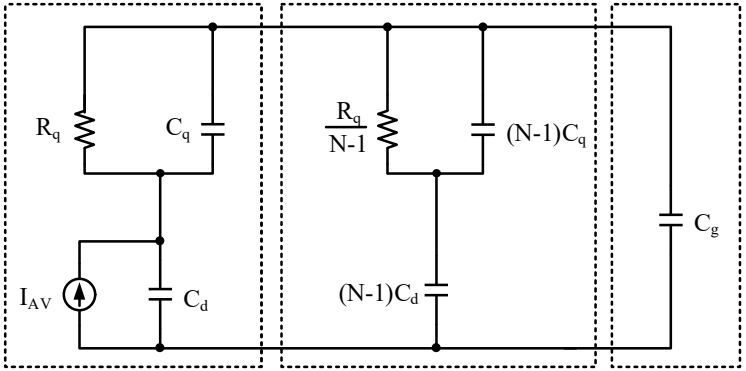
Bandwidth comparison between TIA and VA

（doi:10.1109/ISCAS.2019.8702411 ）

Comparison of three common preamplifiers

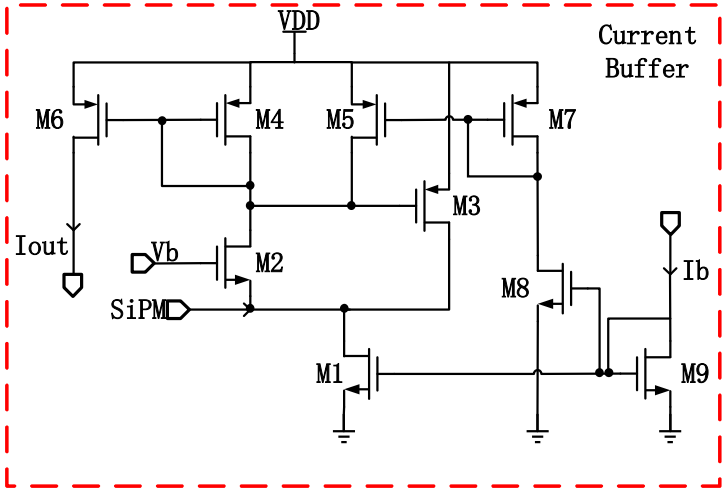
	advantage	disadvantage
CSA	High sensitivity, high gain, high linearity	Slower response and lower input impedance
VA	High input impedance, wide measurement dynamic range, high linearity	more susceptible to noise
TIA	Fast response time and large dynamic range	Low input impedance, complex design

02 Current Buffer Design



SiPM Equivalent Circuit Diagram

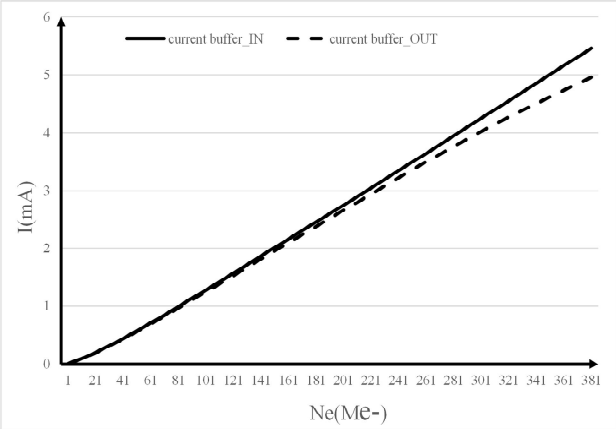
- Quenching resistance Rq, capacitance Cq formed with the substrate, junction capacitance Cd of the photodiode
- The capacitance to ground, Cg, is close to 50 pF(https://indico.ihep.ac.cn/event/14082/contributions/28390/attachments/13841/15759/SIPM.pdf), which affects the bandwidth of the amplifier circuit



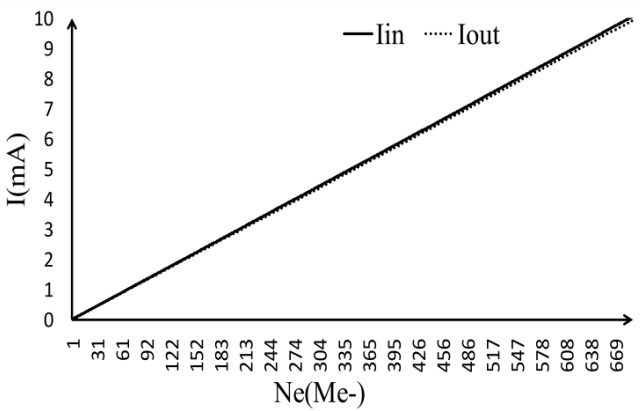
Schmetic of the Current Buffer.

- Common gate input, low circuit input impedance.
- M1, M2, and M3 form a negative feedback loop to improve the circuit's frequency response characteristics.

02 Current Buffer Design



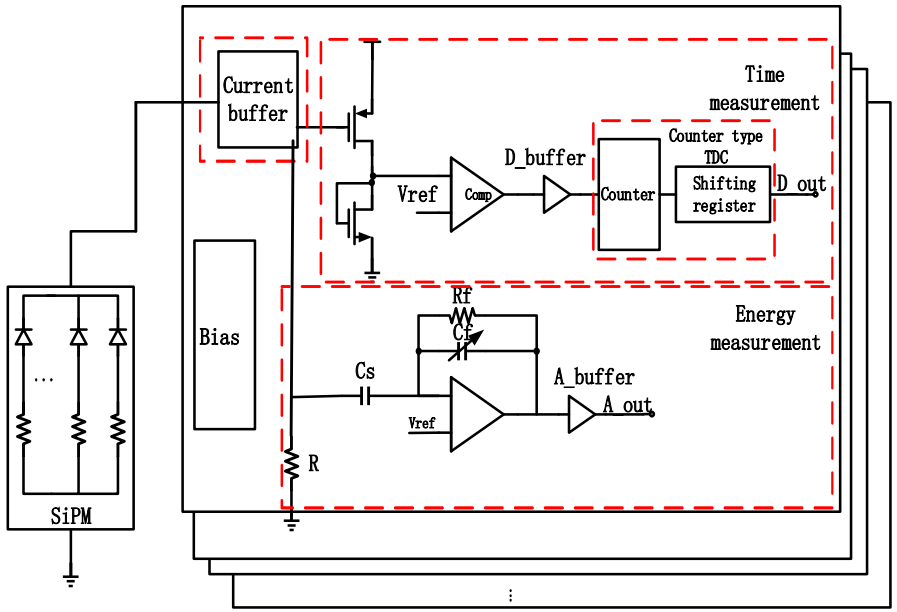
Results of the initial version of CB



Improved CB results

- The figure on the left shows the input-output curve of the initial version of the CB of the design, in which the Current Buffer can follow only 160 fC-48 pC with a power consumption of 100 µA.
- The circuit was then improved with a low-voltage cascode current mirror technique, resulting in a dynamic range of 160 fC-160 pC with a power consumption of 480 µA. The nonlinear error introduced by the improved CB is small, below 0.5%.

03 Front-end circuit design

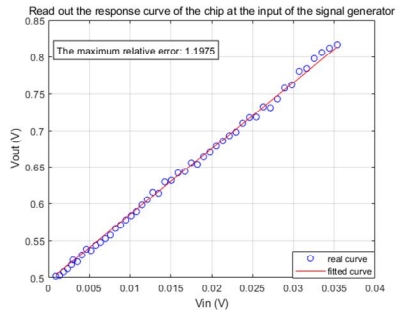


Schmetic of the SiCC1.

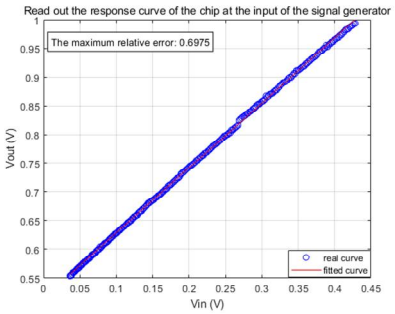
- SiCC1 is an initial attempt at a high-speed, large dynamic range readout circuit with 8 channels.
- use a traditional readout scheme, with external gain control to cover a dynamic range of 300 times.
- The time path generates a start signal through threshold comparison.

The chip is set with three gain gears: 20, 2, 1/2. The power consumption is 4.54 mW/channel, with the area of 1865 μm x 1970 μm and the input dynamic range of 10 μA to 3 mA.

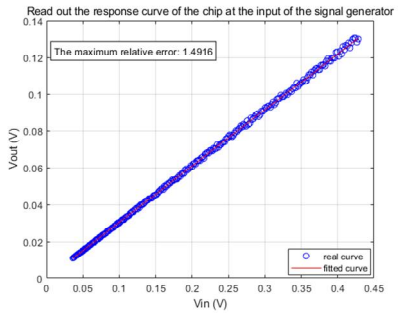
03 Test of the SiCC1 analog channel



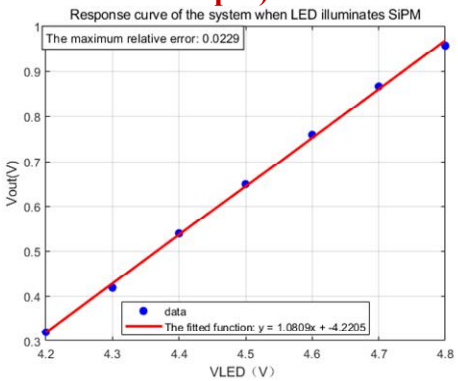
Linearity of K1 gear(Signal generator input).



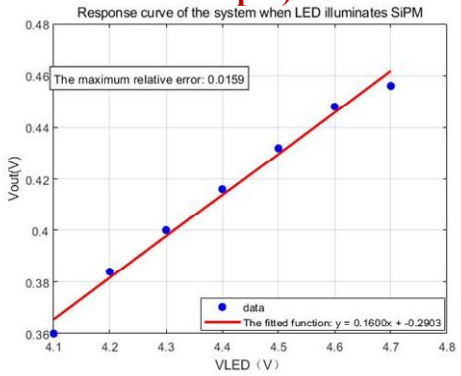
Linearity of K2 gear(Signal generator input).



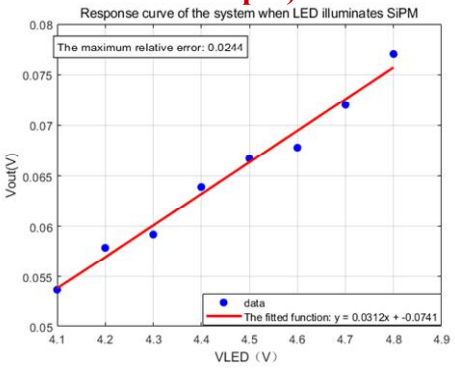
Linearity of K3 gear(Signal generator input).



Linearity of K1 gear(LED Driver SiPM Input).



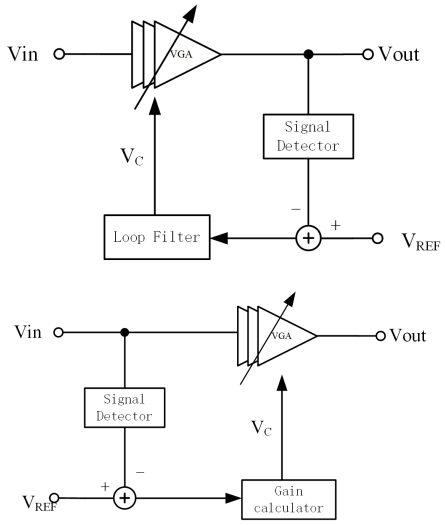
Linearity of K1 gear(LED Driver SiPM Input).



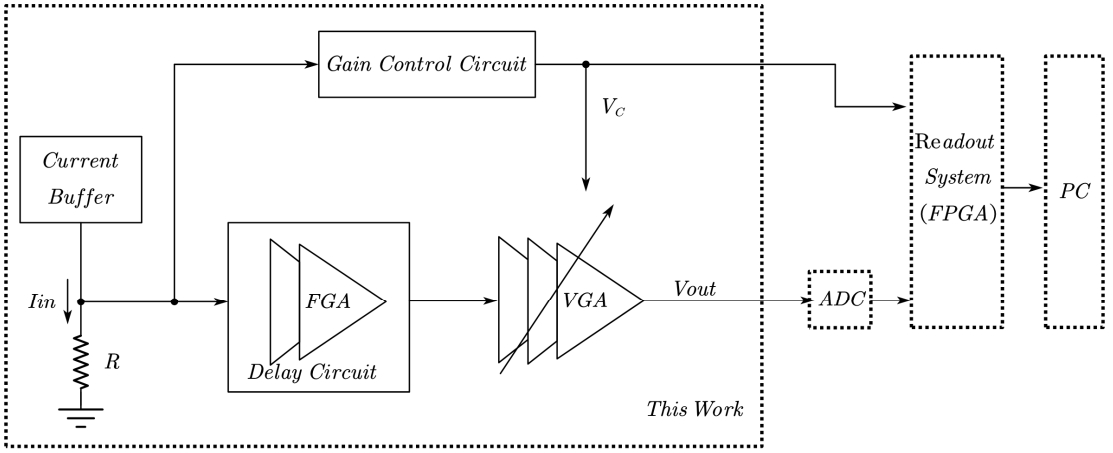
Linearity of K1 gear(LED Driver SiPM Input).

- The signal generator's input nonlinear error is below 1.5%, while the LED driver for SiPM input has a nonlinear error below 2.5%.

03 AGC Amplifier Circuit Design



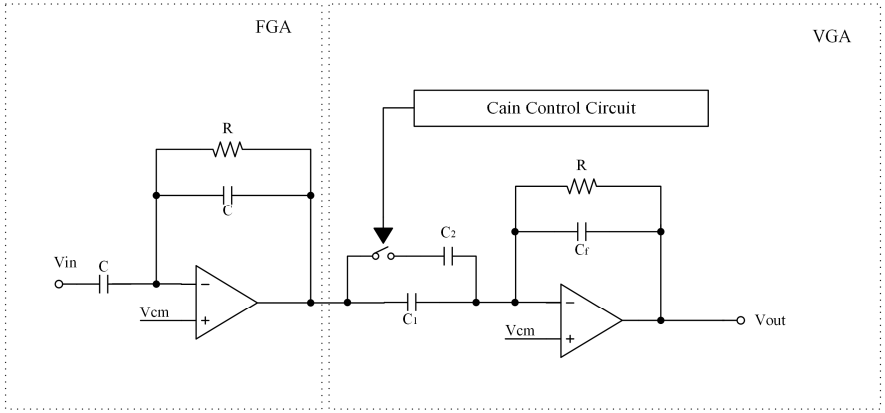
Automatic gain control mode.



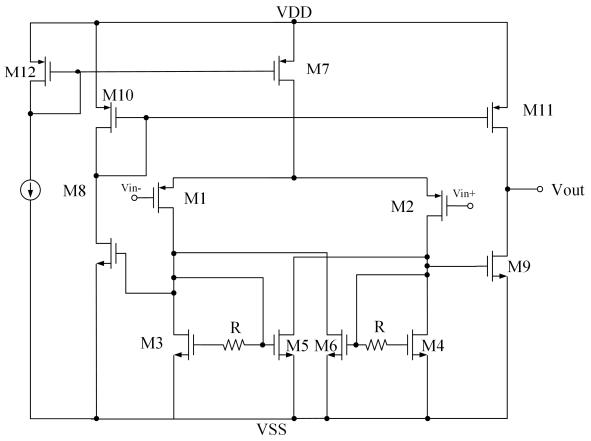
Proposed AGC circuit diagram.

- The SiCC1 chip requires external adjustment before testing, To improve this issue, an automatic gain control circuit has been applied to the SiPM readout circuit.
- Automatic gain control is divided into feedforward and feedback types. To ensure response speed, a feedforward automatic gain control circuit was ultimately adopted.
- The automatic gain control chip includes a current buffer, gain selection control stage, fixed delay stage, and controllable delay stage, with measurements taken by an external ADC and data processed by an external FPGA.

03 Core Circuit Design of the AGC



schematic of the VGA and FGA .



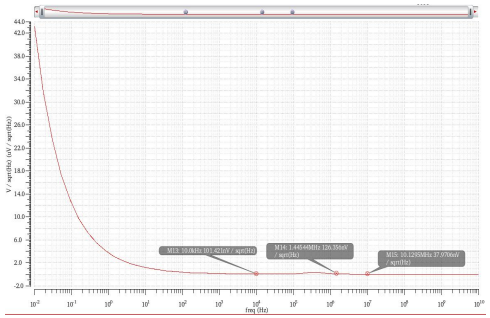
Schematic of the hysteresis comparator.

- The core modules of the circuit are the FGA (Fixed Gain Amplifier) and VGA (Variable Gain Amplifier). The diagram shows a schematic representation. The delay stage is implemented by cascading fixed gain amplifier stages, while the variable gain stage provides 1/2x and 10x amplification, achieved through cascading two stages with 2x and 5x gain.
- Another core module of the circuit is the hysteresis comparator. To prevent false triggering due to noise during gain control switching, the comparator is configured as a hysteresis comparator, with a hysteresis window set to 20 mV.

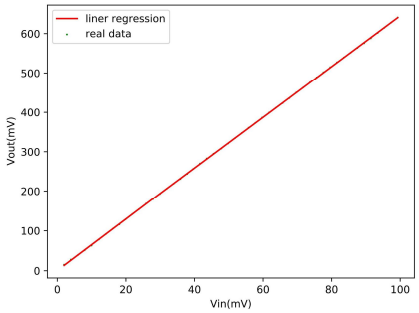
03 Simultion Results of the AGC

- The curve for the high gain setting is shown in the figure on the right, with a maximum nonlinear error of 1.29%. The maximum nonlinear error in the low gain setting is 0.27%.

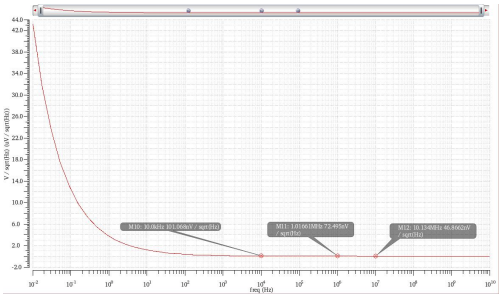
- The integral of the output noise of the high gain gear within 10kHz~300MHz is 1.416 mV.



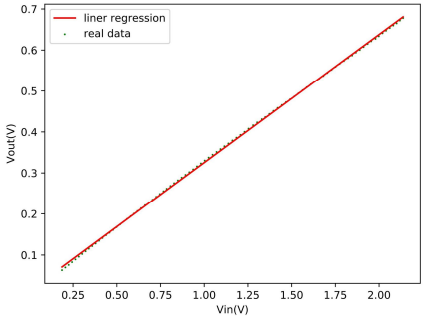
High gain gear noise simulation.



High gain gear Linearity simulation

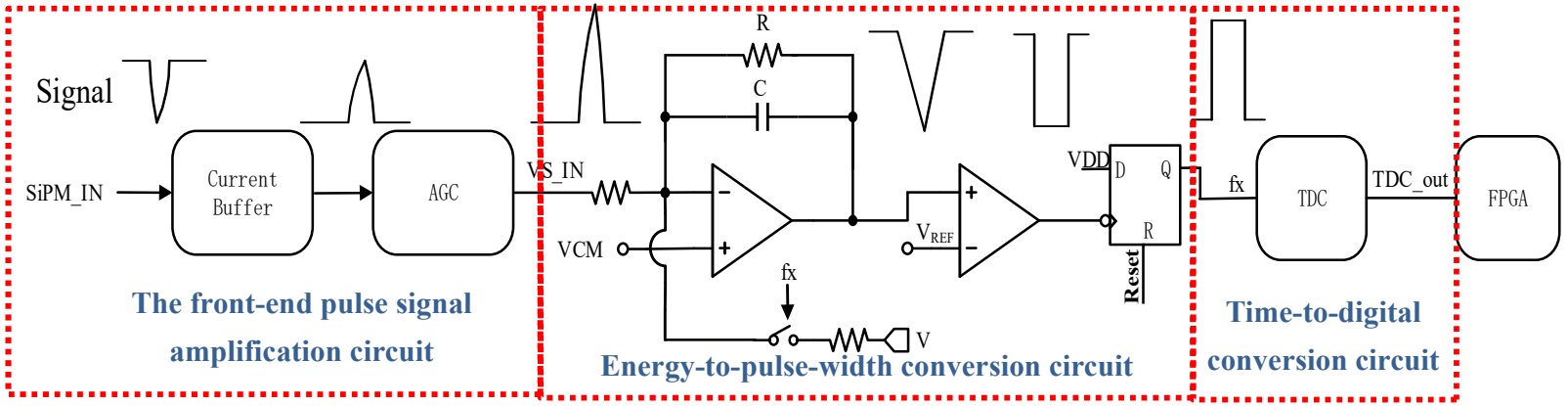


Low gain gear noise simulation.



Low gain gear Linearity simulation.

03 SiCC3 Design

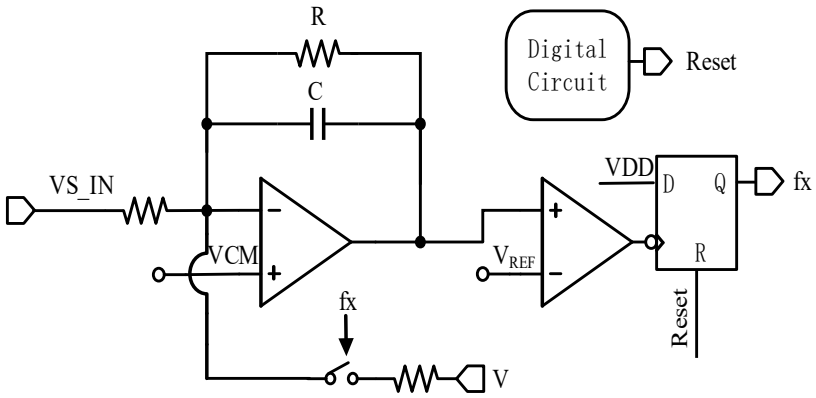


SiCC3 Circuit.

The advantages of the SiCC3 as follows:

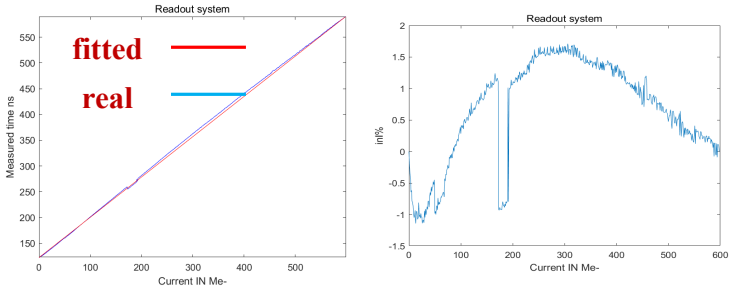
- To further optimize the circuit, the SiCC3 circuit has been proposed.
- In the signal preprocessing circuit, a single-channel 60 dB dynamic range input signal is processed through an automatic gain amplifier (AGC).
- The paper achieves linear conversion of energy to pulse width by designing a first-order Delta-Sigma Modulator (DSM) circuit similar to the Time-Over-Threshold (TOT) technique.
- At the back end of the circuit, a Time-to-Digital Converter (TDC) is used for energy measurement, which saves power compared to using a high-speed ADC.

03 Core Circuit of the SiCC3

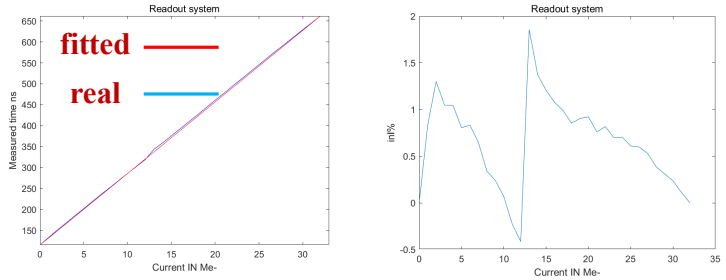


The energy-to-pulse-width conversion circuit diagram.

- The output is set to a pulse signal.
- The circuit generates pulse width using a charge integration method, where the output is linearly related to the input signal's energy.
- Maximum non-linear error less than 1.8%

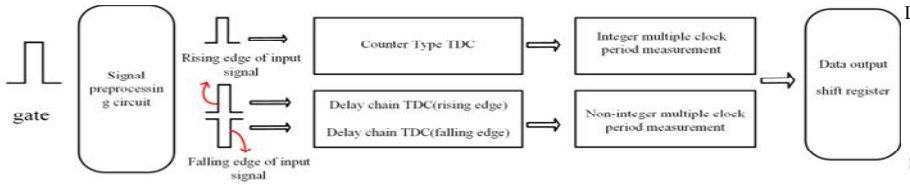


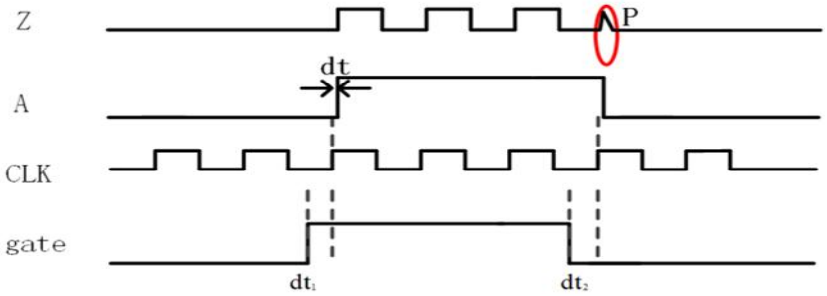
Post-simulation results of the low-gain gear



Post-simulation results of the high-gain gear

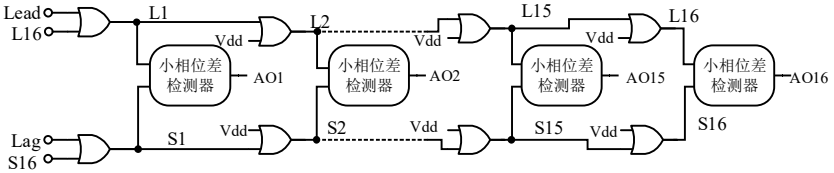
04 TDC Design



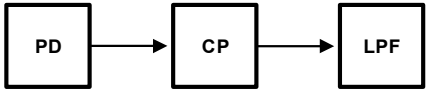


Schmetic of the TDC.

- use two-step method, with coarse measurement obtained from a counter and fine measurement obtained from the delay chain.
- measurement time = N*Tclk+dt1-dt2



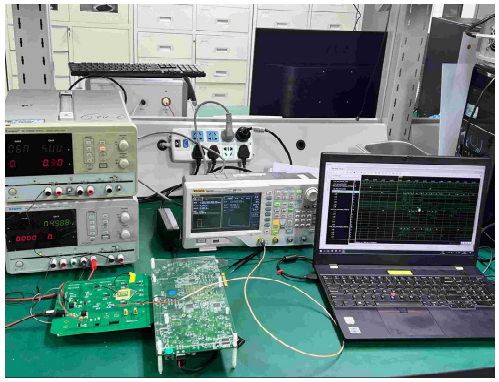
Cycle TDC circuit diagram.



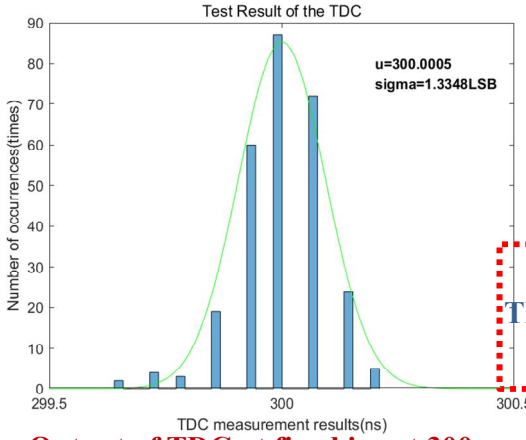
DLL circuit diagram.

- TDC is implemented using a circular cursor structure, with a dynamic range of 800 ns and the LSB is 20 ps.
- The DLL provides control voltages for the delay units of the TDC, consisting of a phase detector, charge pump, and low-pass filter.

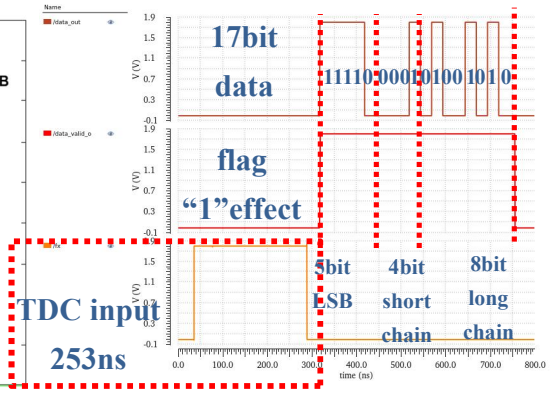
04 Test of the TDC



TDC Test System.

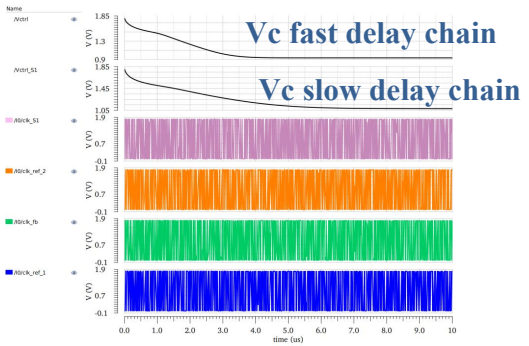


Output of TDC at fixed input 300ns.



TDC post-simulation result

- The test system consists of a FPGA signal generator and a PC for processing FPGA data.
- The average value of the TDC output is close to 300 ns, with a single sigma error of 1.33 LSB.
- The Ring Cursor TDC has now been flowed back and is writing firmware waiting to be tested, and the post-simulation results show that the TDC can achieve 20ps accuracy.



DLL post-simulation result

05 Outlook

➢ Outlook

1. We tried three different front-end structures for processing SiPM signals. The SiPM readout circuit can cover a dynamic range of 160 fC to 160 pC within 3% linearity error, with a signal processing time of less than 1 μs and the LSB of the TDC is 20 ps.

2. The SiCC3 and AGC circuits are currently only simulationed. The chips have been fabricated and are under testing to verify their performance. The design can be improved and applied to calorimeter.

3. In the future, the ADC will be integrated into the SiPM readout circuit to form a complete front-end readout chip.


THANKS