A common project for detector data links

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1、The Concept of the Data Link Project

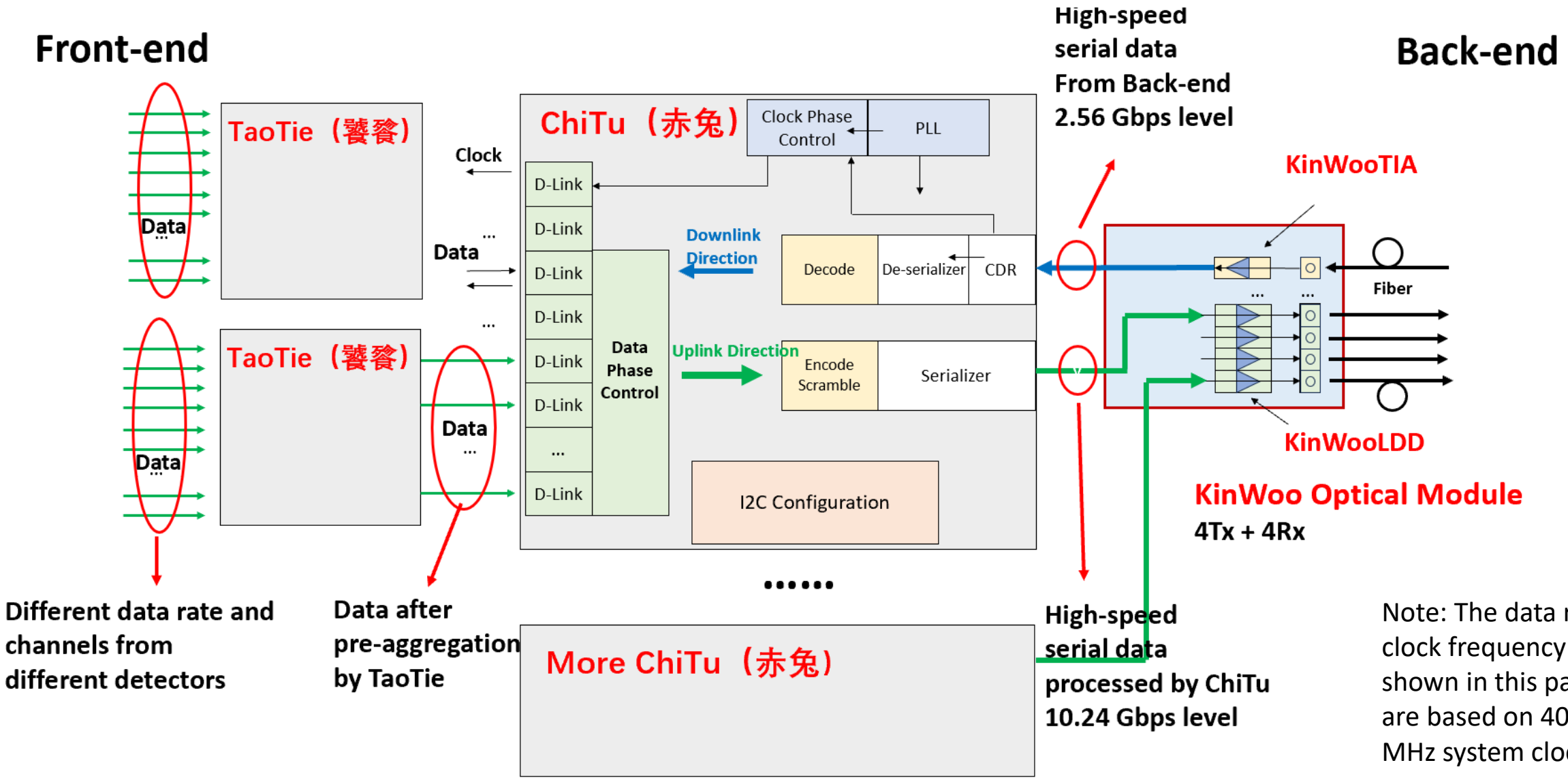
2、ASICs and Module Development in the Project

3、Summary and the Future Plan

The Concept of the Data Link Project

- **What are the requirements of the detector front-end for communication with the back-end?**
  - Massive data uplink transmission requirements (High data throughput) 10 Gbps/ch +
    → Various detectors have various channel numbers and various data rates
  - Front-end electronics need clock
    → maybe different frequency or different phases are needed
  - Front-end electronics need trig signals, control signals from Back-end
    →Relative low data throughput (Downlink)
    →Massive front-end units need to be configured (I2C, …)
  - Front-end units need to transmit current, temperature, status… monitoring information to the Back-end
  - All these transmissions need to be robust and radiation-tolerant.
- **The concept of the Data Link Project**
  - Aims to build a universal, bi-directional, high-speed data link system between the front-end and the back-end for various detectors requirements in CEPC.

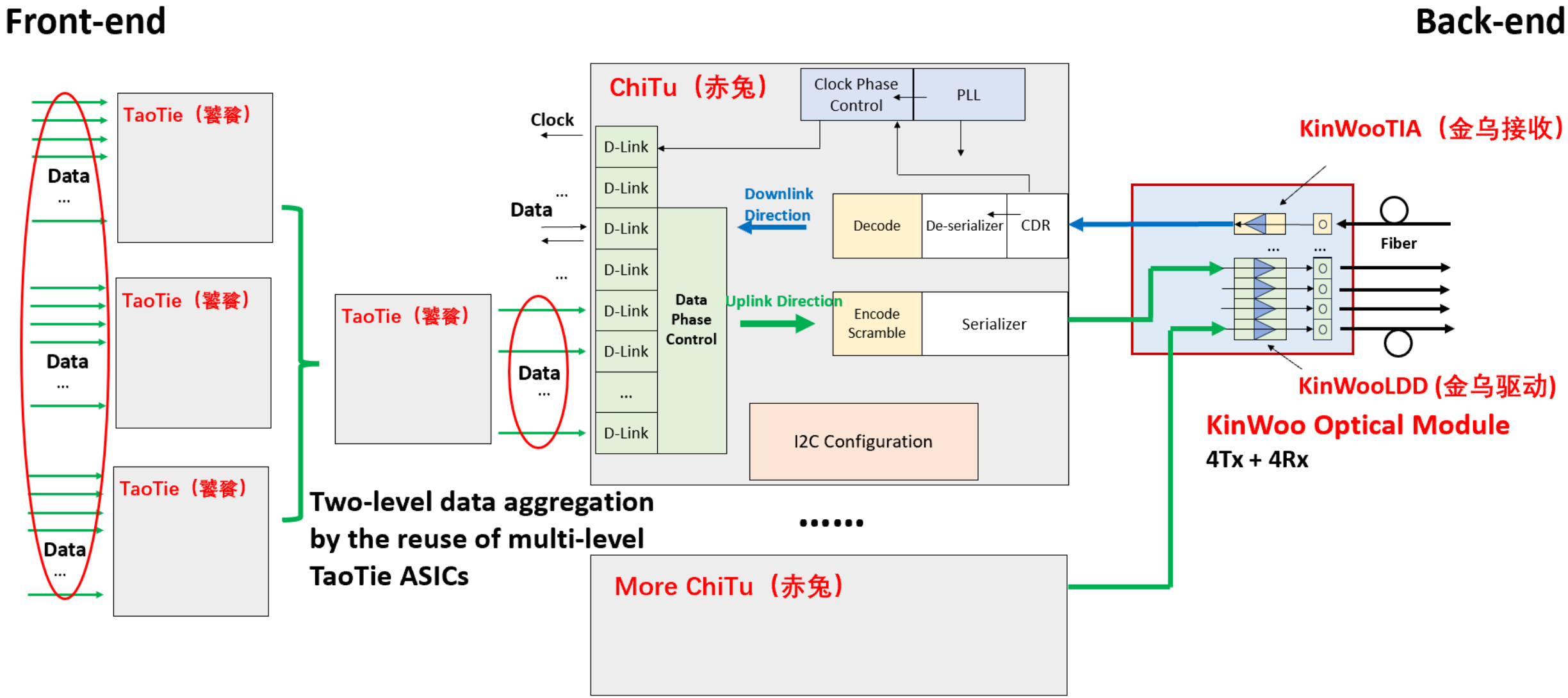
Structure of the Data Link System



Note: The data rate, clock frequency shown in this page are based on 40 MHz system clock.

The System Block Diagram of this Data Link Common Project

Structure of the Data Link System



The System Block Diagram of this Data Link Common Project

1、The Concept of the Data Link Common Project

2、ASICs and Module Development in the Project

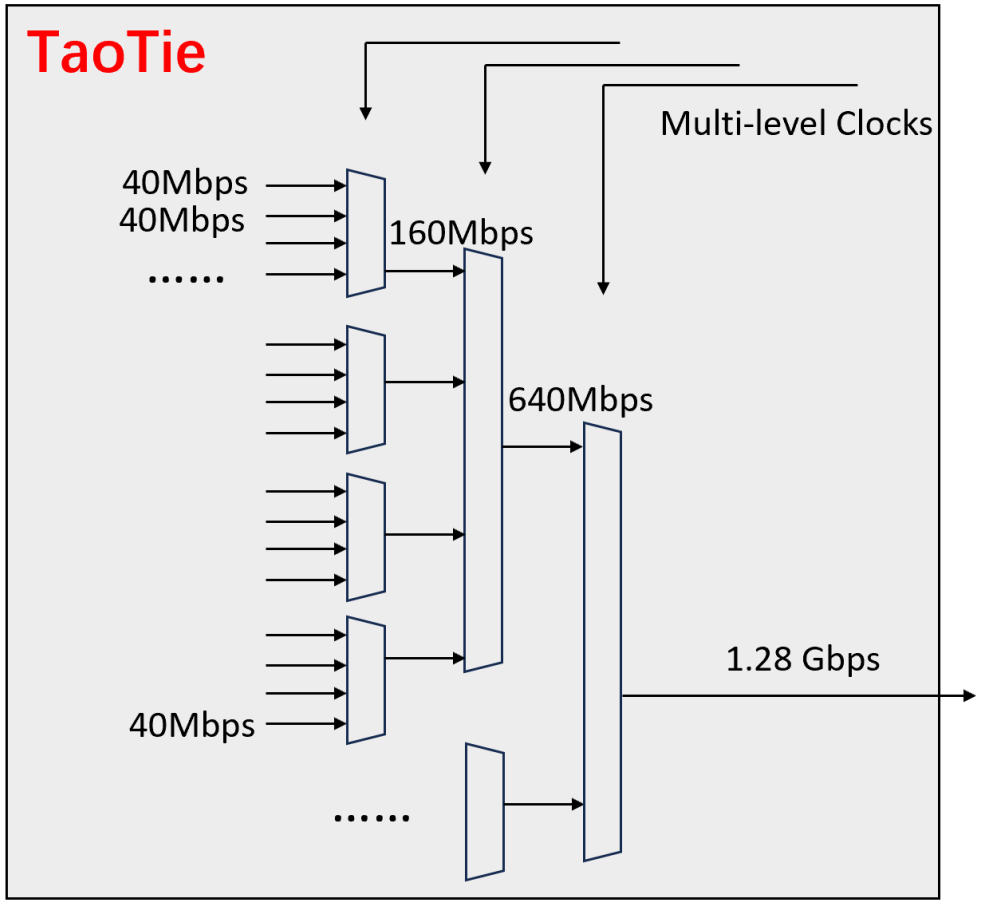
3、Summary and the Future Plan

ASICs and Module Development in the Project

- ASICs
  - **TaoTie** : Data Pre-aggregation ASIC
  - **ChiTu** : Bi-directional Data Interface ASIC
    Uplink: 10 Gbps/ch Downlink: 2.5 Gbps/ch
  - **KinwooLDD** : High-speed Laser Array Driver ASIC
    ~10 Gbps/ch
  - **KinwooTIA** : High-speed Transimpedance Amplifer Receiver ASIC
    ~2.56 Gbps/ch
- Kinwoo Optical Module
  - Array optical module (eg. 4Tx + 1Rx channel configurable)

TaoTie: Data Pre-aggregation ASIC

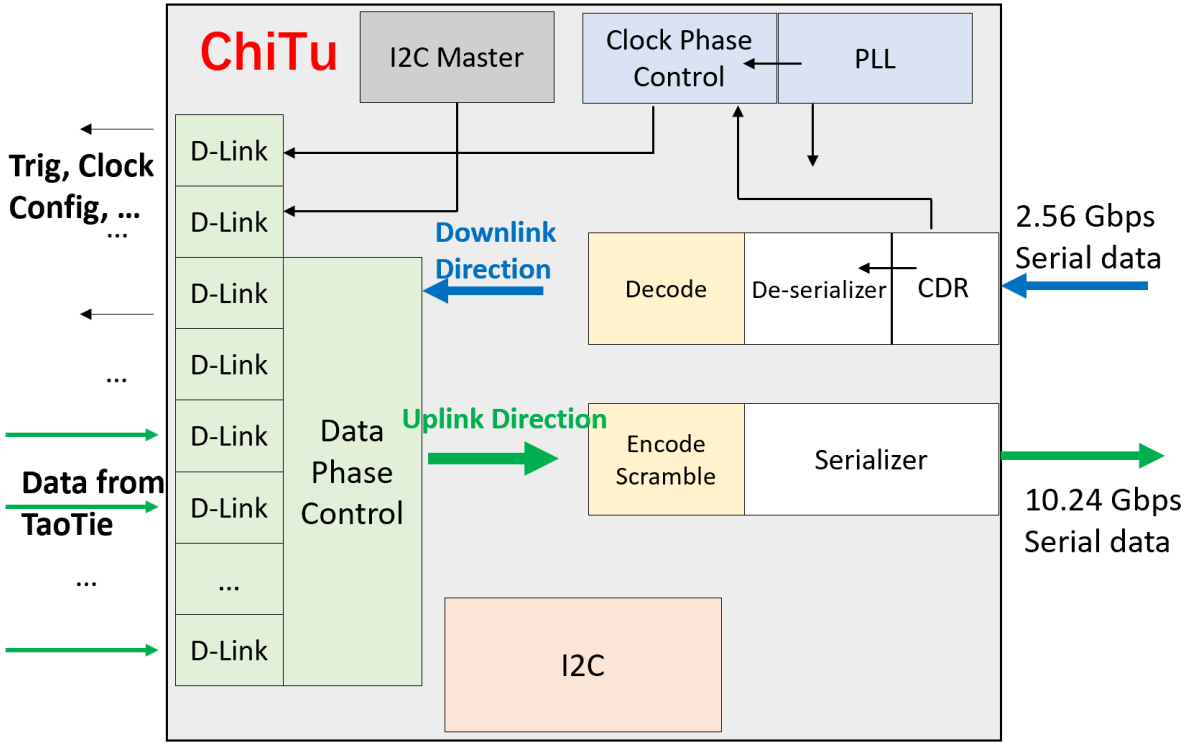
- Structure of TaoTie ASIC
  - Multi-level configurable Mux
  - Front-end parallel data rate will be fixed to 2 or 3 cases for all front-end detectors
    - E.g. Fixed to 40 Mbps/ch or 160 Mbps/ch if system clock is 40 MHz
  - Some font-end detectors that already have Gigabit-level data rate will bypass the TaoTie, and go directly into ChiTu.
    - The data rate will also be fixed, e.g. 1.28 Gbps/ch
  - So that after TaoTie (or bypass TaoTie), data rate will be unified to 1.28 Gbps/ch, which can release the design complexity in following ChiTu ASIC.
- Considerations under discussion
  - Buffer or not, when dealing with different data rate inputs, or when we have unconnected channel.



One specific working structure of TaoTie

ChiTu: Bi-directional Data Interface ASIC

- Structure of ChiTu ASIC
  - Uplink Direction:
    - Up to 1.28 Gbps/ch Data Rx (Inside D-Link)
    - Multi-channel Data Phase Control
    - Data Scrambler, Encoder, Frame Builder
    - 10.24 Gbps Serializer + High-speed Tx (Pre-emphasis)
  - Downlink Direction:
    - 2.56 Gbps Clock Data Recovery (CDR)
    - 2.56 Gbps Deserializer
    - Data Decoder
    - Data Tx (Inside D-Link)
  - Other sub-modules:
    - 5.12 GHz Phase Lock Loop (PLL)
    - Clock Phase Control
    - I2C Master and related configuration submodules
    - …

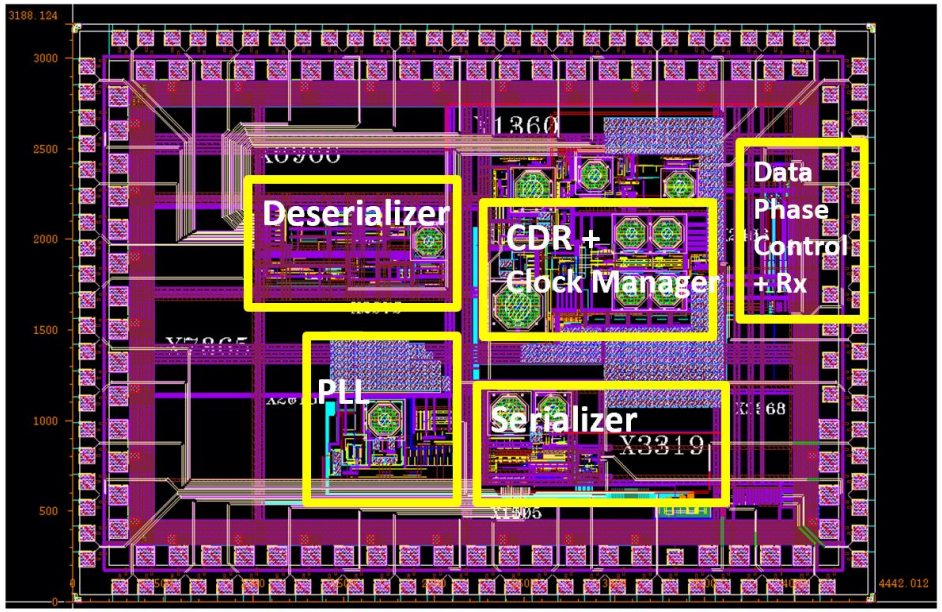


Structure of ChiTu ASIC

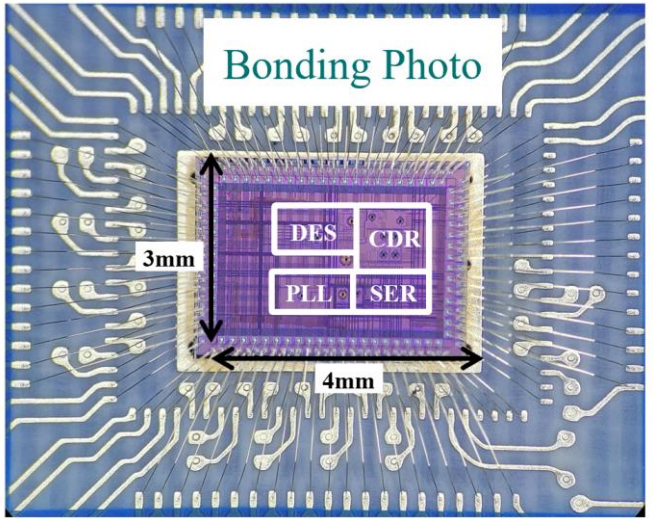
Development of ChiTu ASIC

- Sub-module Designs of ChiTu ASIC
  - Based on a domestic commercial 55 nm CMOS Technology
  - Die size: 3 mm x 4 mm
  - 166 pins

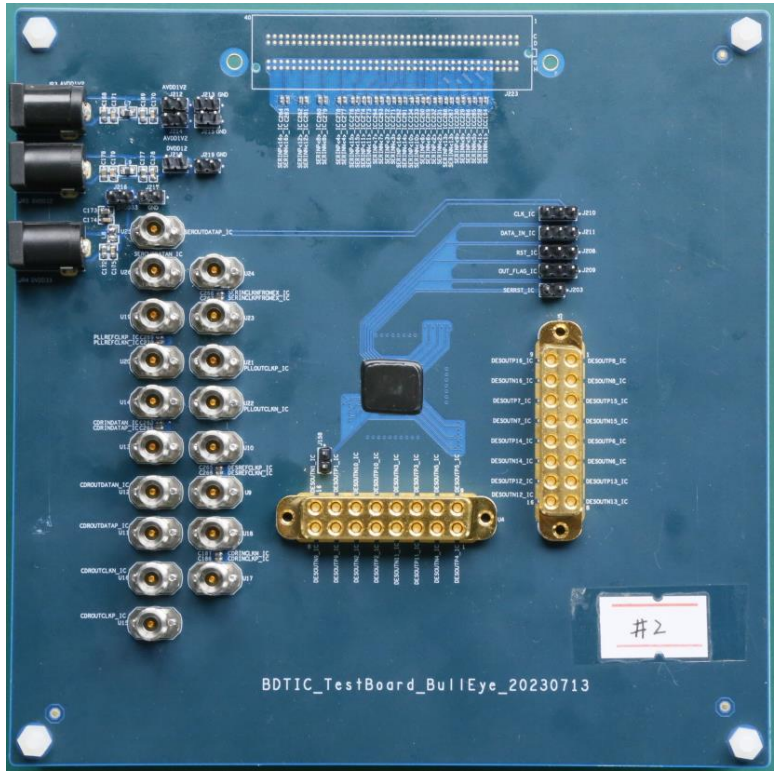
- Including the following sub-modules:
  - 10.24 Gbps, 16:1 Serializer
  - 2.56 Gbps, 1: 16 Deserializer
  - 5.12 GHz PLL
  - 2.56 GHz CDR (Full rate)
  - Multi-channel Data Phase Control
  - Up to 1.28 Gbps/ch Rail-to-Rail Rx
  - 10.24 Gbps Tx with pre-emphasis



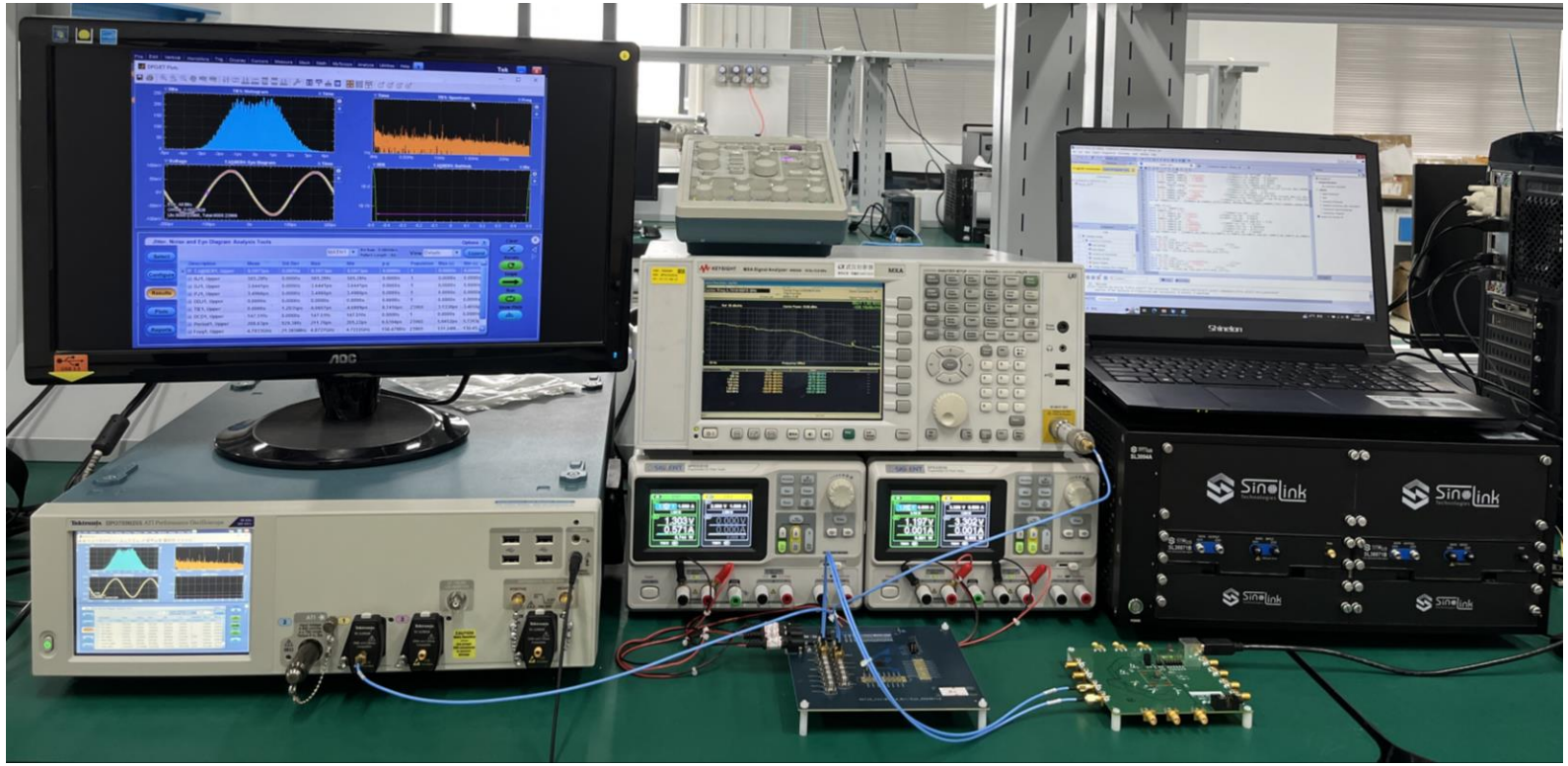
Sub-module Designs of ChiTu



Development of ChiTu ASIC



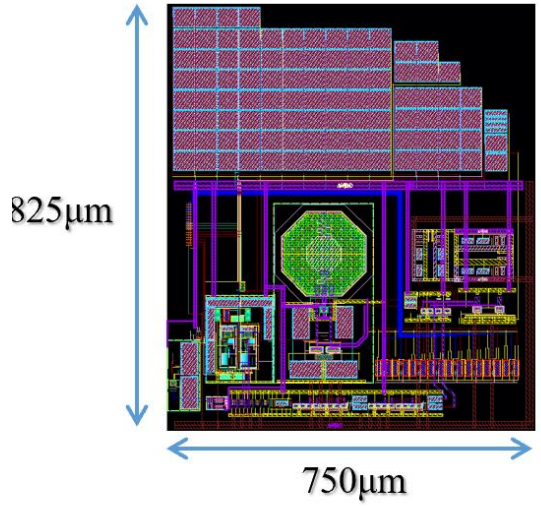
ASIC Testing PCB



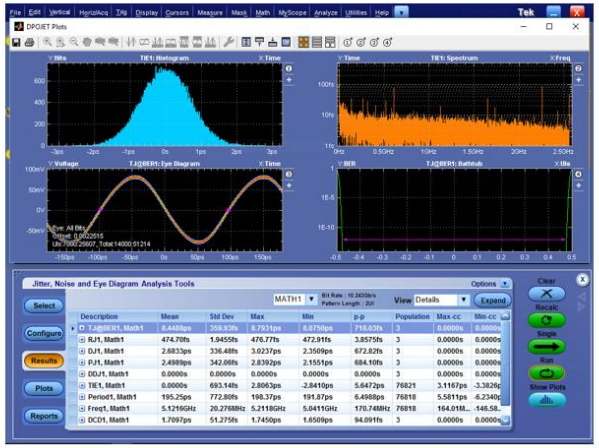
Test setup

- The ASIC uses COB (chip on board) package for the testing.
- PCB uses SMA and high-density high-speed connectors for multi-channel high-speed test.

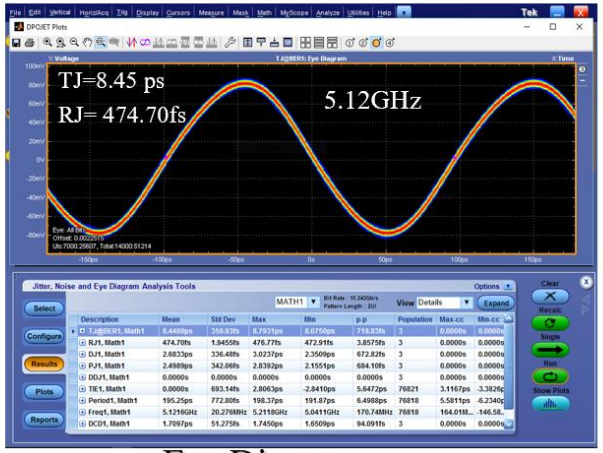
Development of ChiTu ASIC: PLL



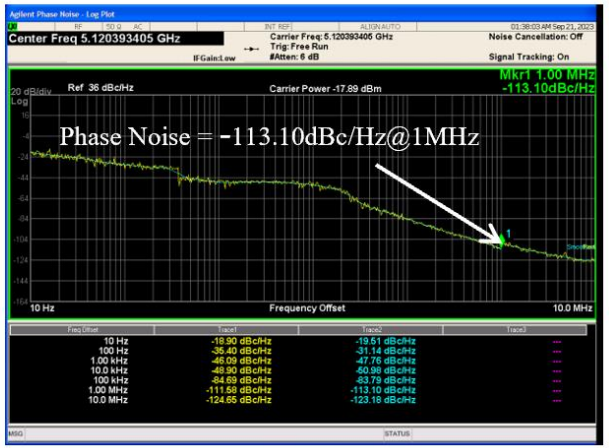
- 5.12 GHz PLL
  - Tested and verified √



Jitter analysis



Eye Diagram



Phase Noise Curve

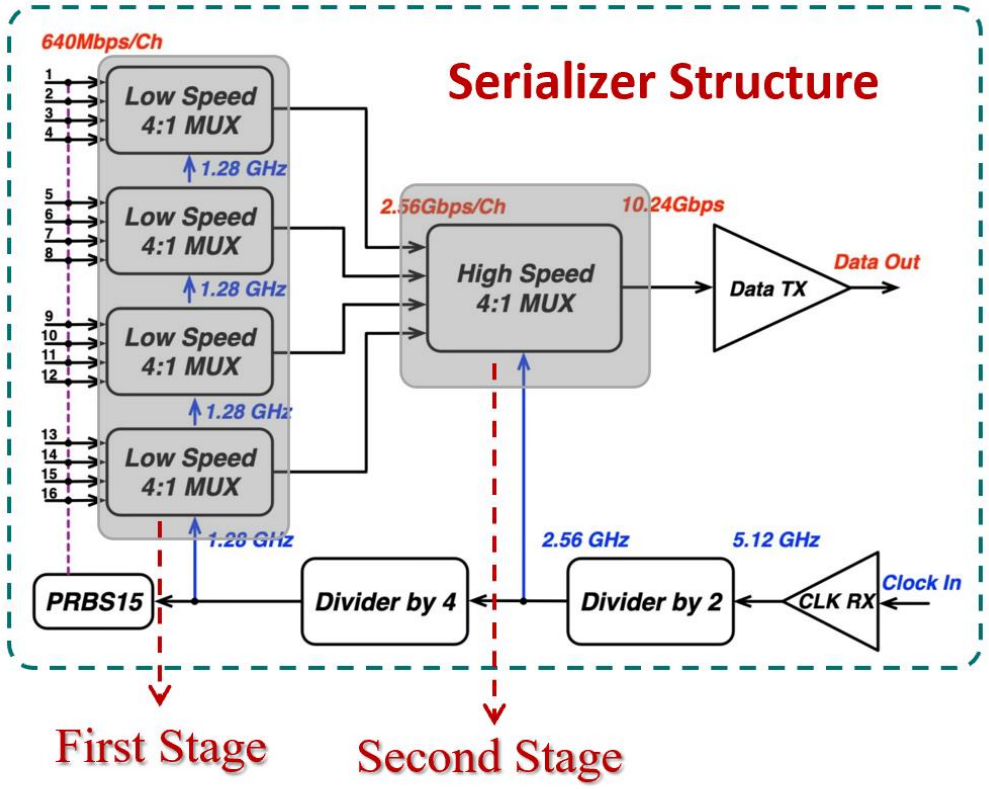
✓ Frequency： 5.12 GHz

✓ RMS Jitter： 474.70 fs

✓ Total Jitter： 8.45ps

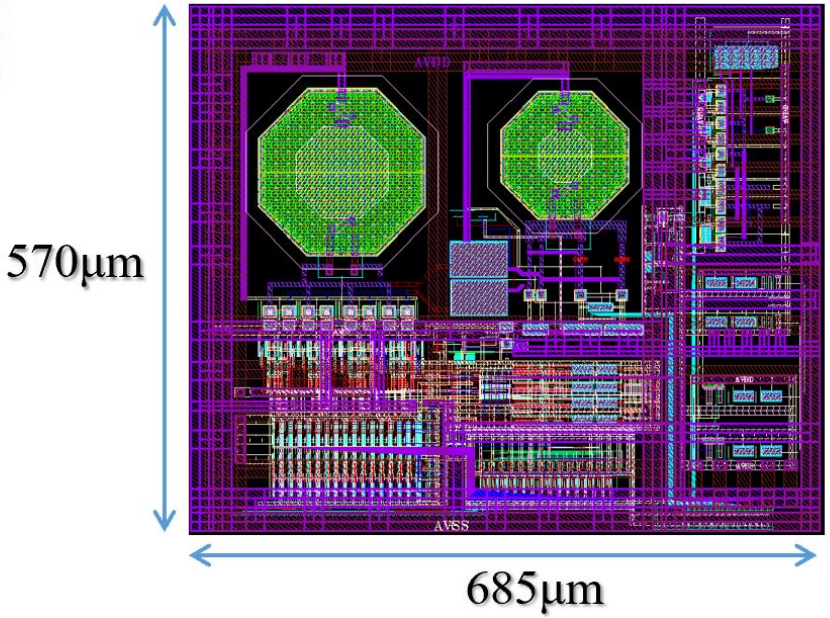
✓ Phase noise： -113dB@1MHz

Development of ChiTu ASIC: Serializer

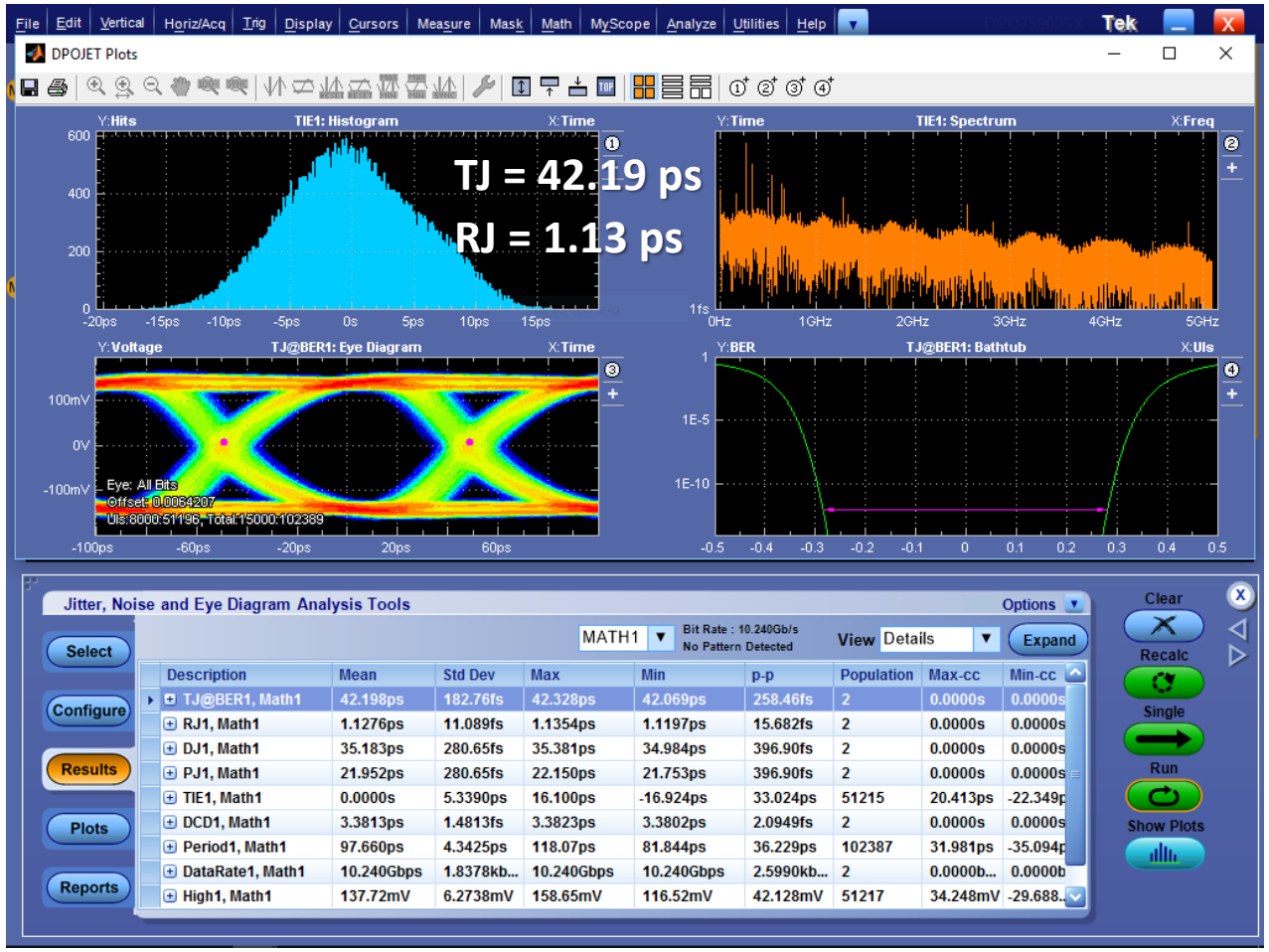


- Input Data： 640 Mbps/Ch × 16
- Input Clock： 5.12 GHz
- Output Data： 10.24 Gbps
- Serializer core size: 685μm × 570μm

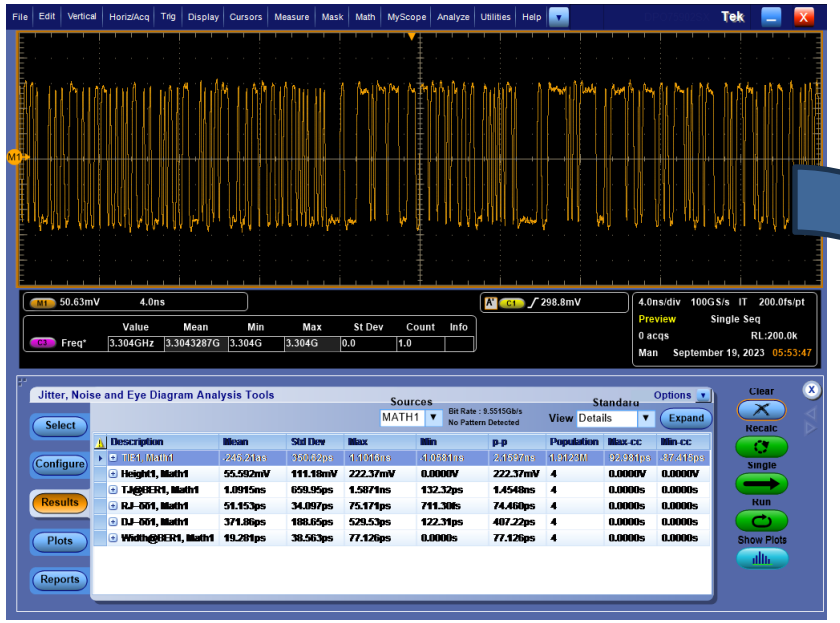
- First Stage: 16→4
- Second Stage: 4→1
- PRBS15: Internal Self-test data source



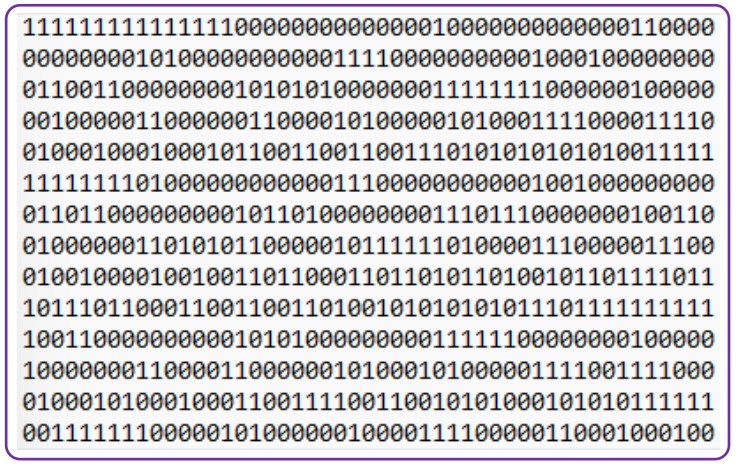
Development of ChiTu ASIC: Serializer



10.24 Gbps eye diagram of the Serializer output



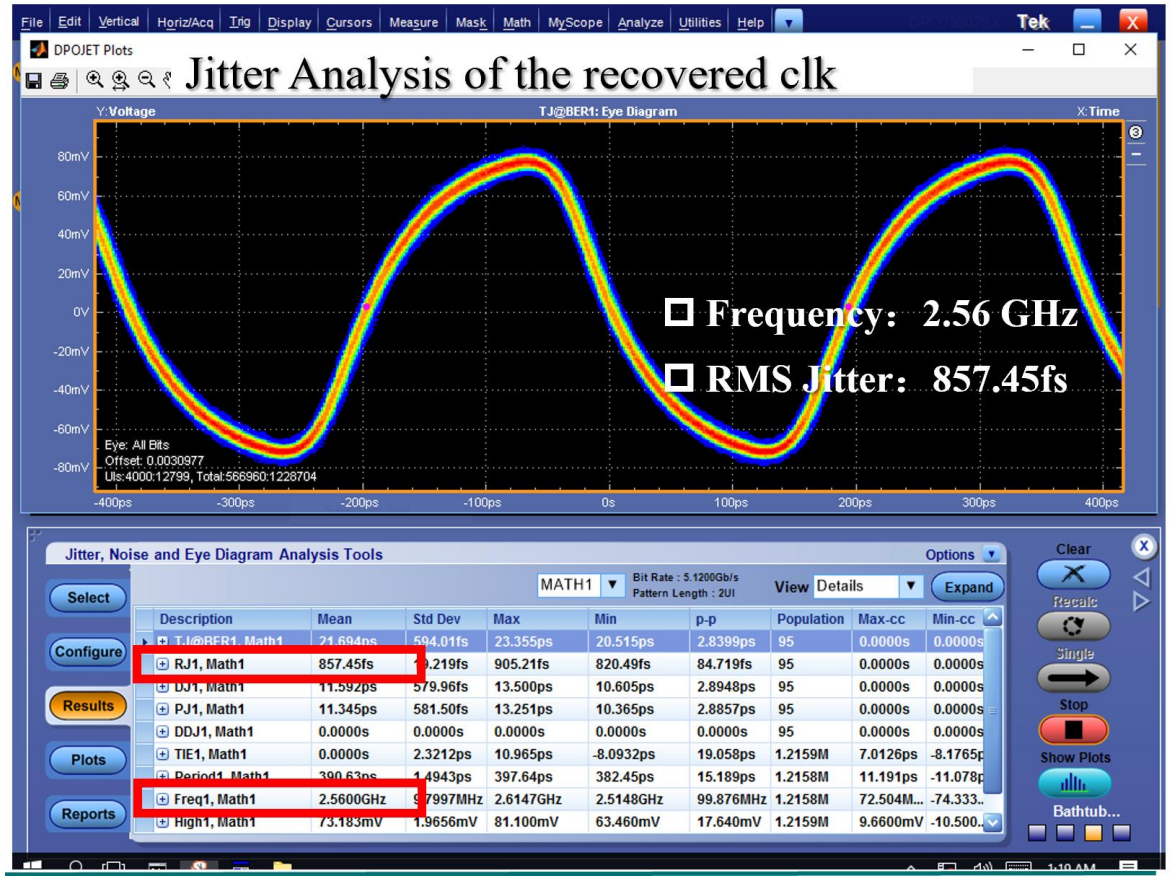
Use real-time scope to capture the output serial data



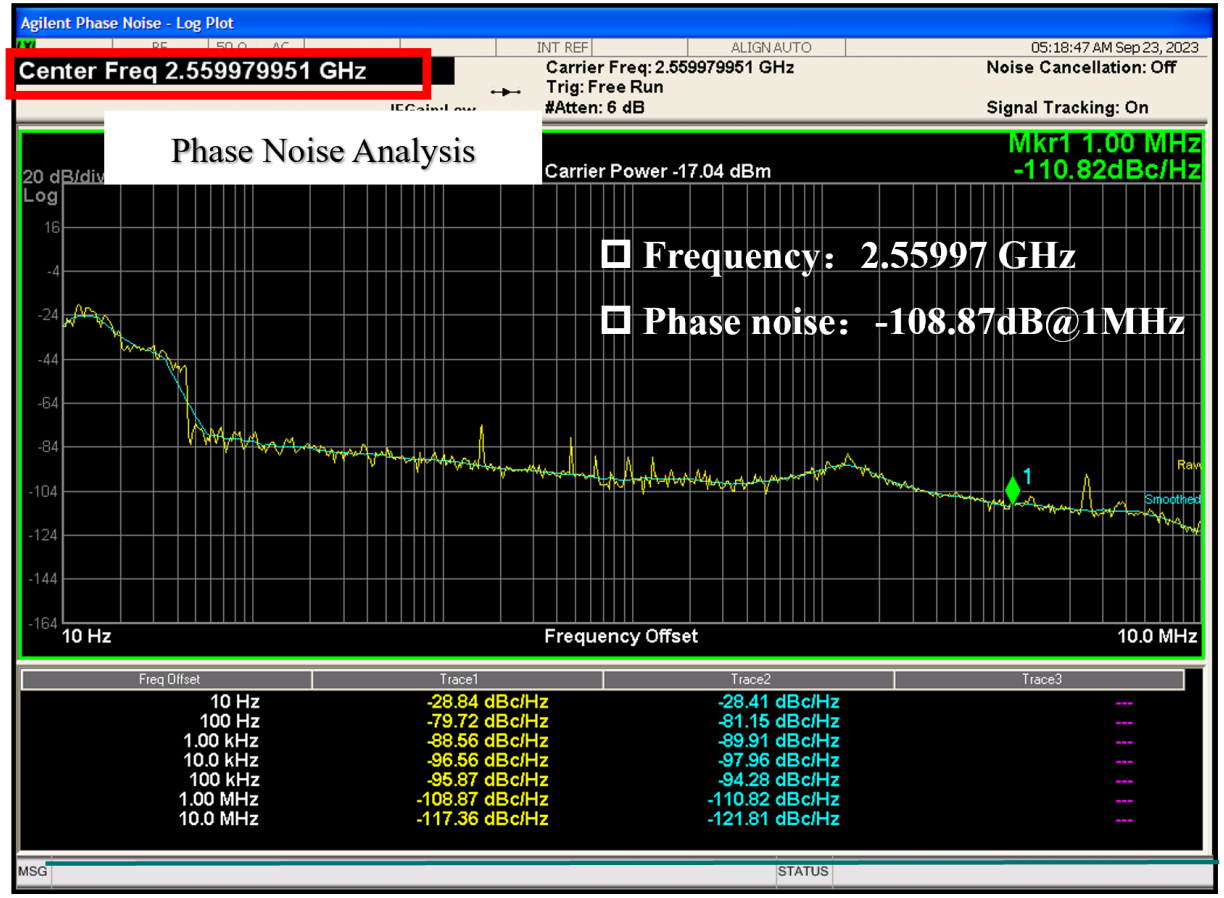
Captured data complies with the expected PRBS15 sequence

- 10.24 Gbps Serializer
  - Tested and verified √

Development of ChiTu ASIC: CDR



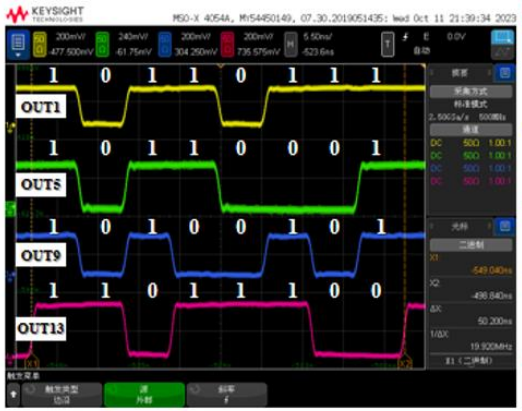
2.56 GHz CDR output (RMS Jitter = 857.45 fs)



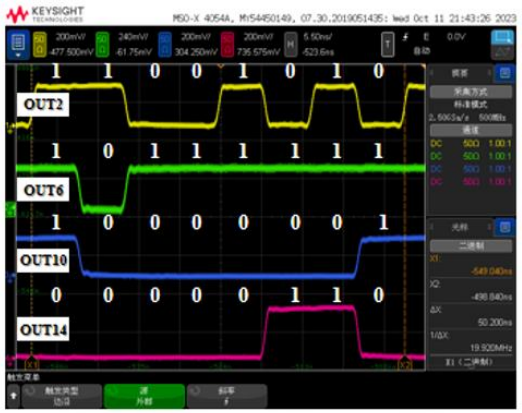
2.56 GHz CDR output phase noise test

- 2.56 GHz CDR
  - Tested and verified √

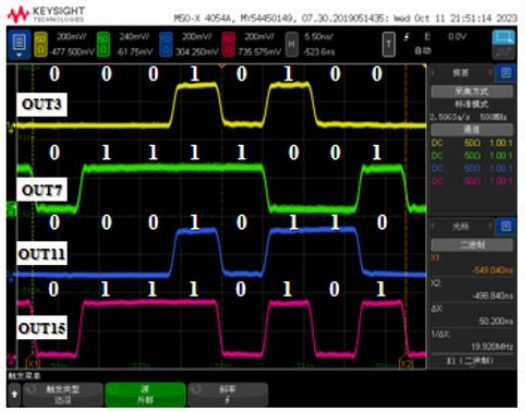
Development of ChiTu ASIC: Deserializer



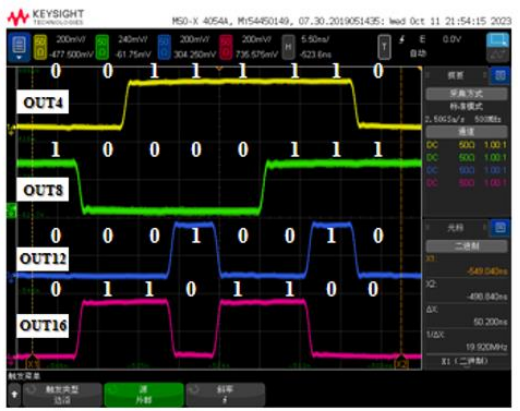
OUT1-OUT5-OUT9-OUT13



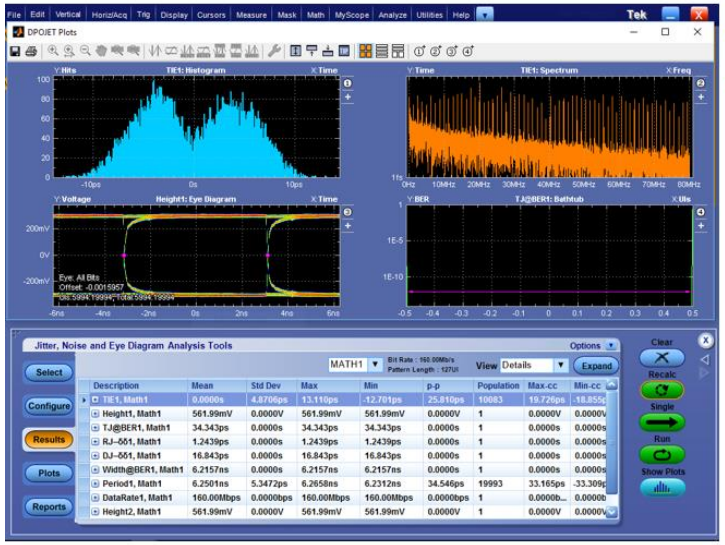
OUT2-OUT6-OUT10-OUT14

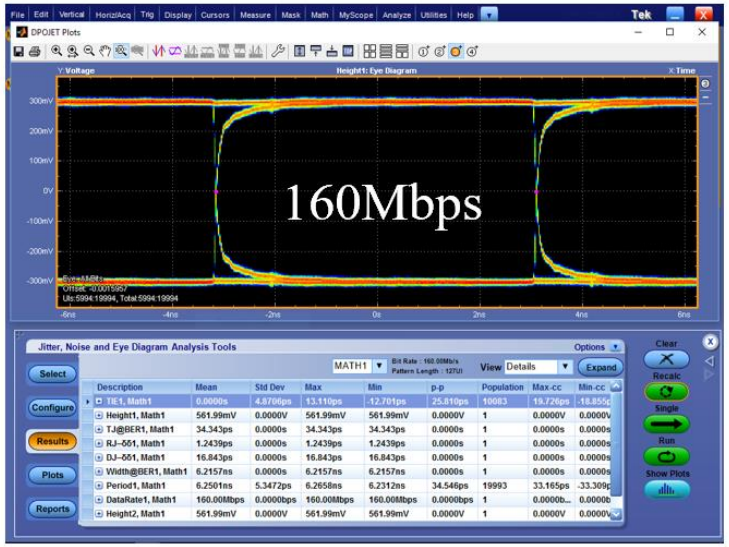


OUT3-OUT7-OUT11-OUT15



OUT4-OUT6-OUT12-OUT16





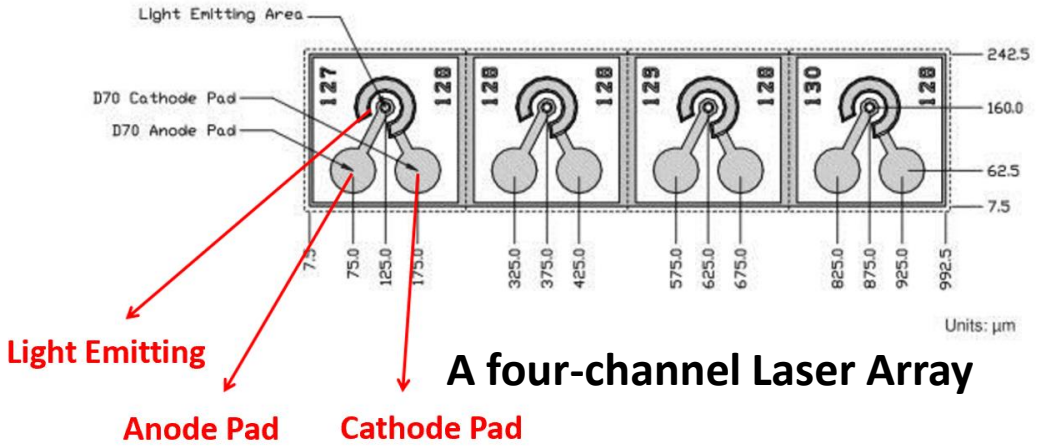
1	OUT1	10110111	9	OUT3	00010100
2	OUT5	10110001	10	OUT7	01111001
3	OUT9	10100101	11	OUT11	00010110
4	OUT13	11011100	12	OUT15	01110101
5	OUT2	11001010	13	OUT4	00111110
6	OUT6	10111111	14	OUT8	10000111
7	OUT10	10000001	15	OUT12	00010010
8	OUT14	00000110	16	OUT16	01101100

- 2.56 Gbps Deserializer
  - Tested and verified √ (use CDR recovered clock)

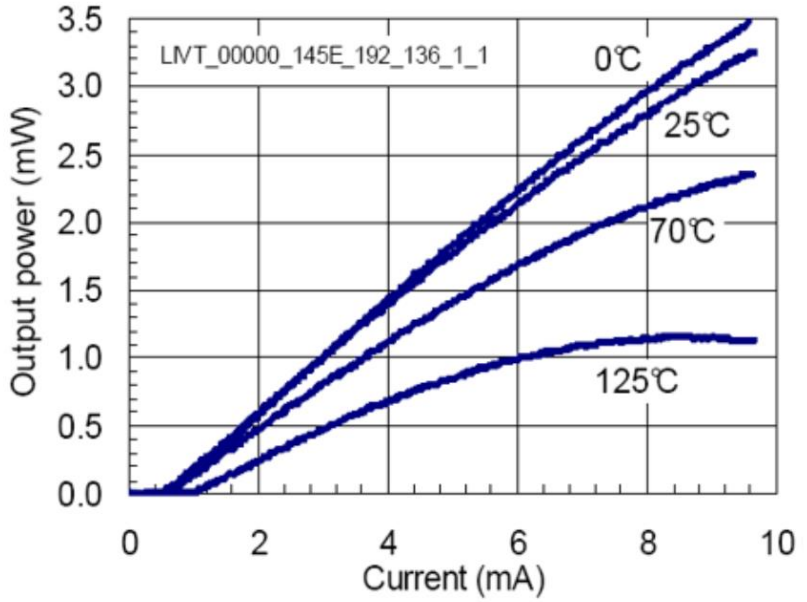
KinwooLDD: Laser Driver ASIC

- KinwooLDD: Laser Driver ASIC

  - Laser chip function
    - Laser works in the linear area of the “Light power-Current” curve
  - KinwooLDD Laser Driver ASIC principle:
    - To amplify the high-speed serial data (typically CML)
    - To convert into high-speed modulated current to driver laser
    - Laser is similar to a 50 ohm AC load in the electrical model.

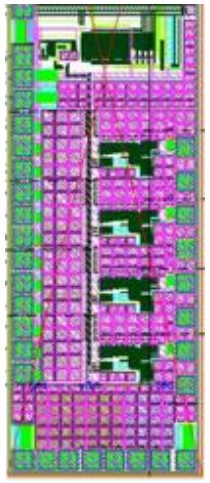


A four-channel Laser Array

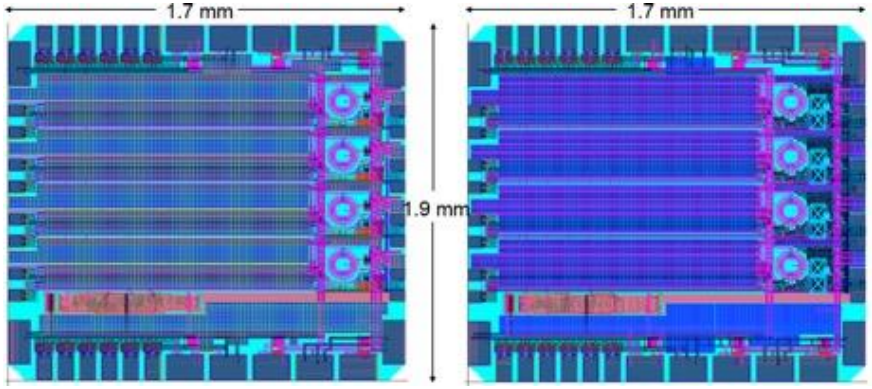


The “Light Power – Current” curve of a typical 850 nm laser

Development of KinwooLDD ASIC and Kinwoo Optical Module

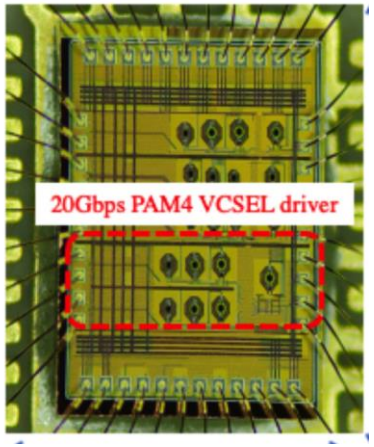


4 x 5Gbps/ch
Laser driver 180nm

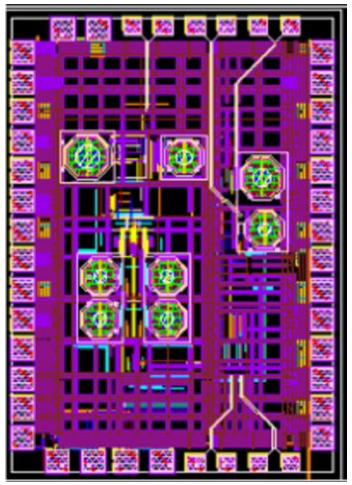


4 x 10Gbps/ch
Laser driver 65nm

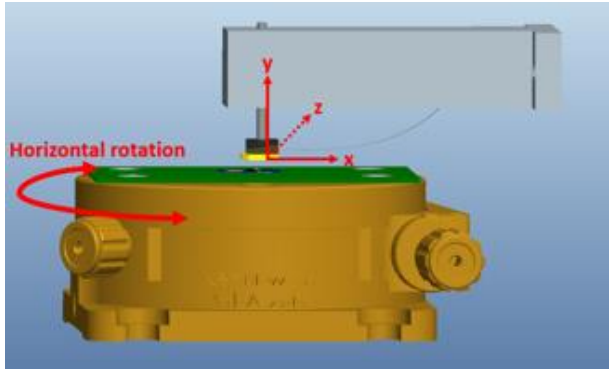
4 x 10Gbps/ch
Laser driver 65nm

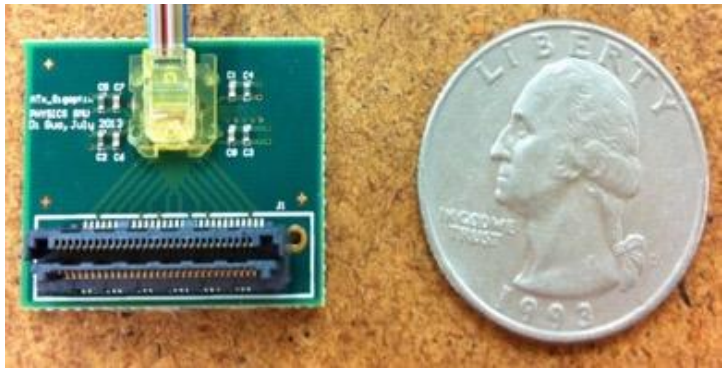


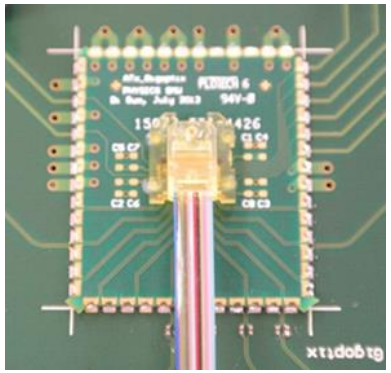
20 Gbps PAM4
Laser driver 55nm

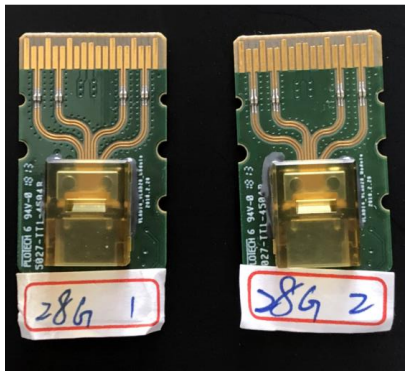


20 Gbps PAM4
Receiver with CDR



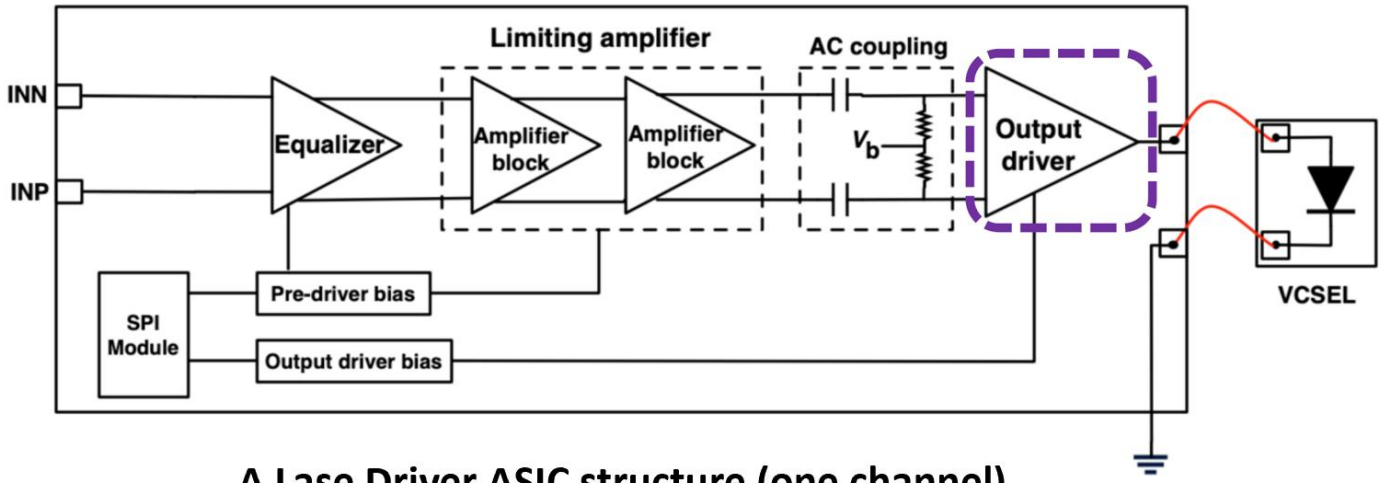






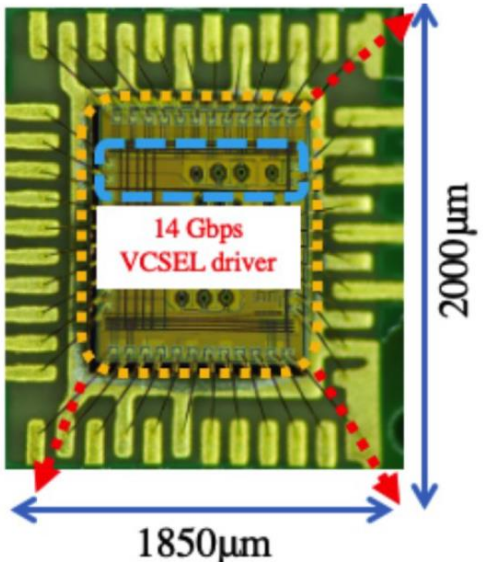
Continuous ustomized array optical module design

Development of KinwooLDD ASIC and Kinwoo Optical Module

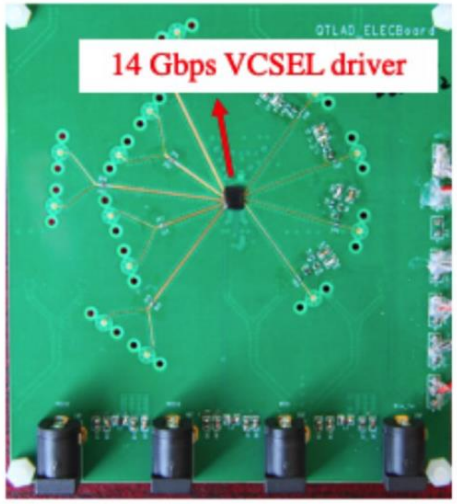


A Lase Driver ASIC structure (one channel)

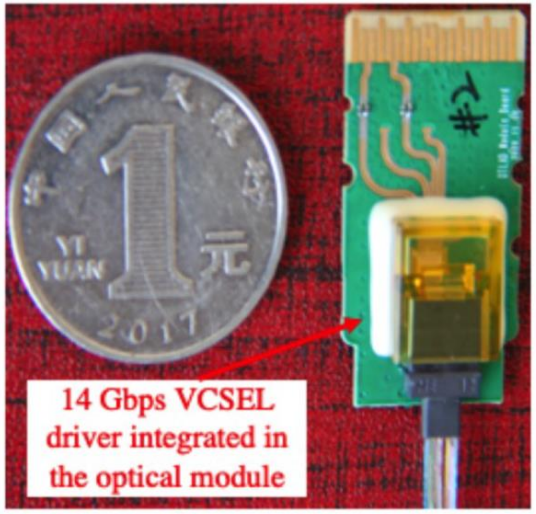
- The recent 14 Gbps/ch laser driver ASIC integrated in the customized array optical module.
  - Based on domestic commercial 55nm CMOS technology

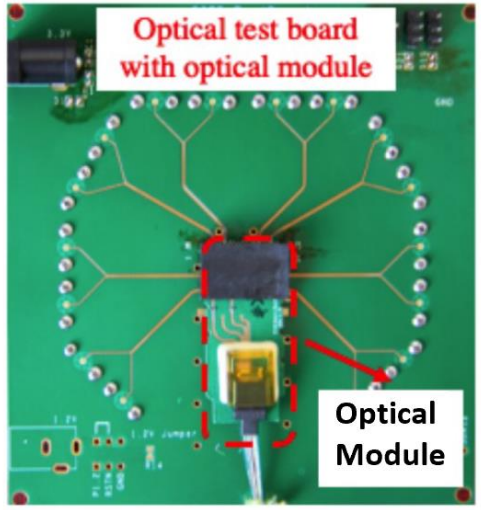


Laser Driver ASIC



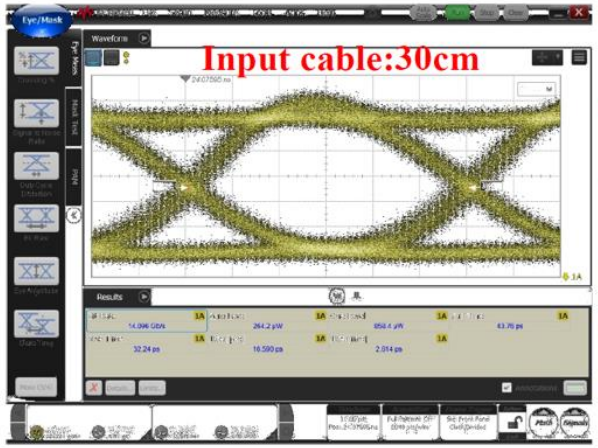
ASIC Electrical Test





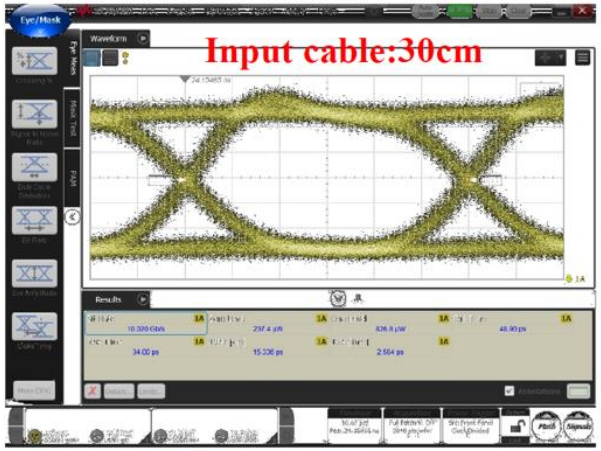
ASIC Integrated in the optical module

Development of KinwooLDD ASIC and Kinwoo Optical Module



14 Gbps optical eye

Bit Rate	14Gbps	RMSJ	2.6ps
Rise Time	32.2ps	PPJ	16.6ps
Fall Time	43.8ps	Amp	594.2μW



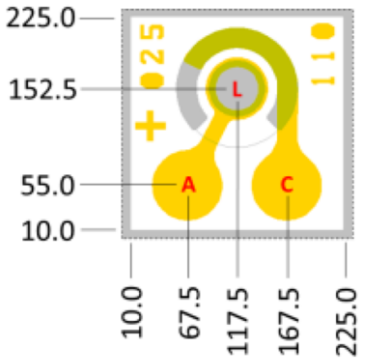
10 Gbps optical eye

Bit Rate	10Gbps	RMSJ	2.6ps
Rise Time	34.0ps	PPJ	15.3ps
Fall Time	48.9ps	Amp	589.4μW

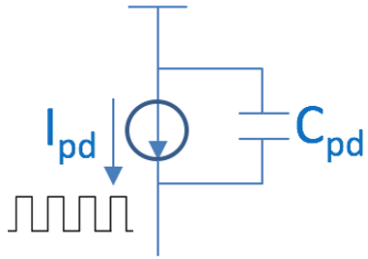
- **Clear and wide-open 10 Gbps optical eye has been captured in the test.**

KinwooTIA: TIA Receiver ASIC

- KinwooTIA: Transimpedance Amplifier Receiver ASIC
  - work with Pin-Diode as part of the “light-to-electrical” for the downlink data transmission.



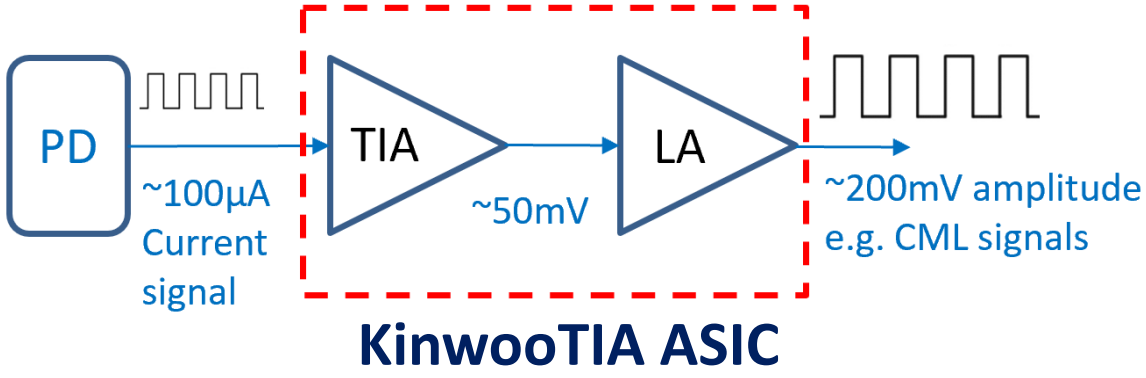
Pin Diode (PD)



PD electrical model

Light Input
Current out

- KinwooTIA ASIC principle:
  - To amplify the high-speed modulated small current signal from PD to voltage signal (TIA core)
  - Then further amplify (LA in the picture) the voltage signal into the regular high-speed signal form, e.g. CML signals



1、The Concept of the Data Link Common Project

2、ASICs and Module Development in the Project

3、Summary and the Future Plan

ASICs and Module Development in the Project

- Four ASICs
  - **TaoTie** : Data Pre-aggregation ASIC
  - **ChiTu** : Bi-directional Data Interface ASIC
  - **KinwooLDD** : High-speed VCSEL Array Driver ASIC
  - **KinwooTIA** : High-speed Transimpedance Amplifer Receiver ASIC
- Kinwoo Optical Module
  - Array optical module
- Developments of ASICs and module are ongoing.

Current Research Group Members

- Detector Data Links Research Group Members :
  - Di Guo (CCNU) : part of ChiTu, KinwooLDD, KinwooTIA
  - Xiaoting Li (IHEP) : High-speed clock related design (PLL, CDR, …)
  - Jinhong Wang (USTC) : High-speed Serdes related design
  - Xiaomin Wei (NPU) : Digital ASIC Design
  - Le Xiao (CCNU) : Digital ASIC Design
  - Lei Zhang (NJU) : System Test , Module Test
  - Suen Hou (SINICA) : Kingwoo Optical Module Assembly
  - Wei Zhang (WTU) : Analog ASIC, FPGA firmware, test
  - Binwei Deng (HBPU) : FPGA firmware, test
  - Phd students

- Need more experts to join the group!

Future Plan

时间	ChiTu ASIC	Kinwoo LDD	Kinwoo TIA	Kinwoo Optical Module
2025.4	Digital Part (Encode/Decode, …) PLL/CDR Update Serializer Update Deserializer Update Data Phase Control Update Data Phase Control Integration Clock Phase Control I2C	KinwooLDD_v1 based on the current design	KinwooTIA_v1	Kinwoo TRx_v1 (Integration with KinwooLDD_v1 and KinwooTIA_v1)
2025.10	ChiTu_v1 Consider BGA Package	KinwooLDD_v2	KinwooTIA_v2	Kinwoo TRx_v2
2026	Design iteration Demo test with other systems	Demo test with other systems	Demo test with other systems	Demo test with other systems

Thanks !

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