The 2024 International Workshop on the
High Energy Circular Electron Positron Collider

Researches on CMOS pixel sensors with on-chip artificial neural networks

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Hangzhou

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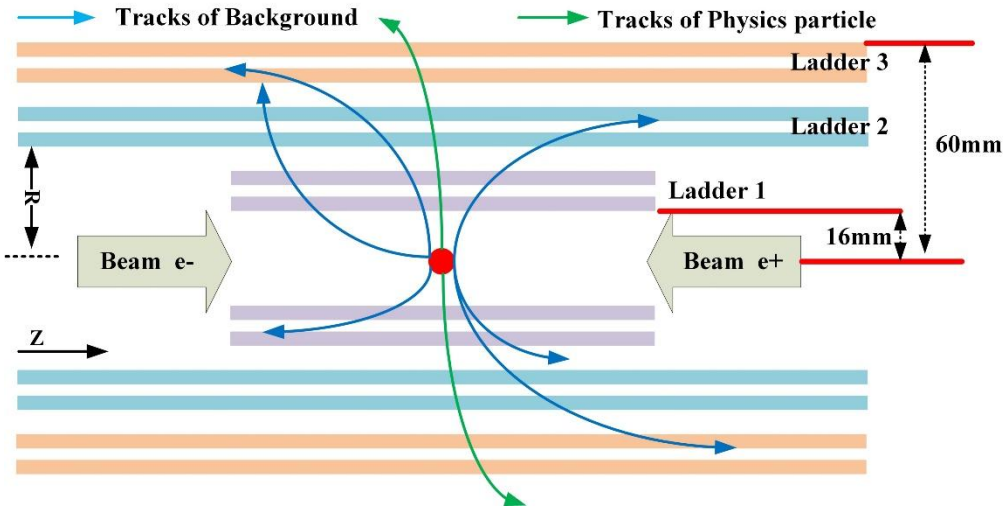
Outlines

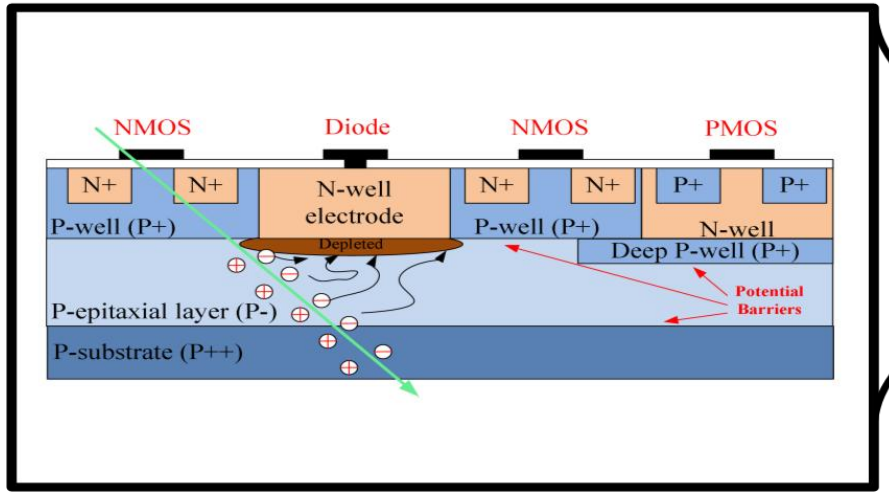
1. WHY ?
2. HOW ?
3. WHAT ?
   - Previous work
   - Now
4. NEXT

1.WHY?



- **Reduce Data Flow**

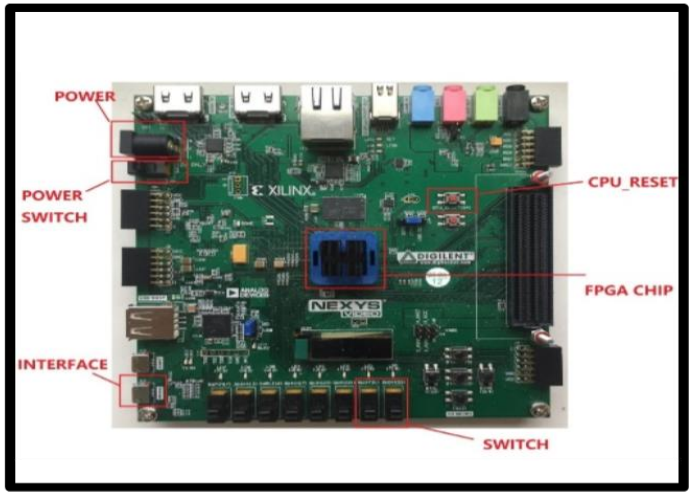
Front-end ASIC (CPS)



Bottleneck

Data Transmission

Back-end FPGA



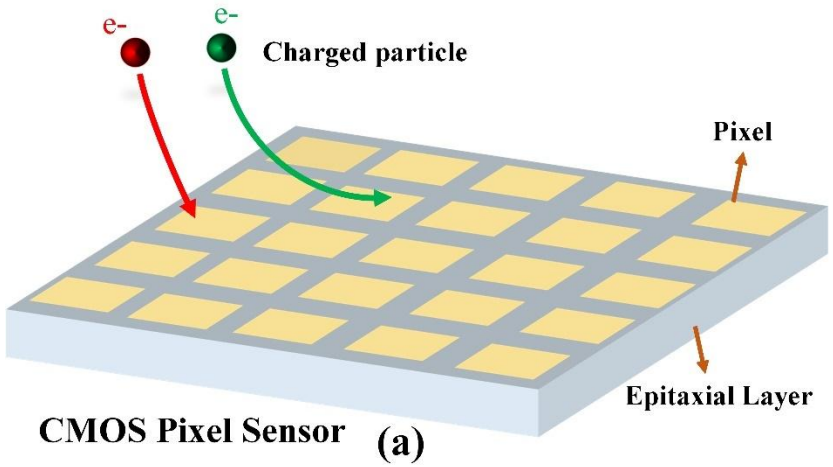
1.WHY?

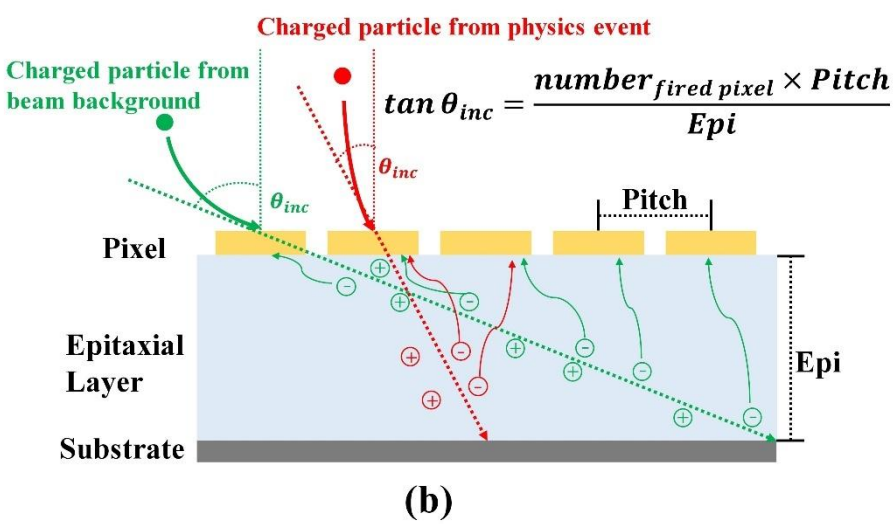
Large amount of hits generated by Beam Background, increasing data flow.

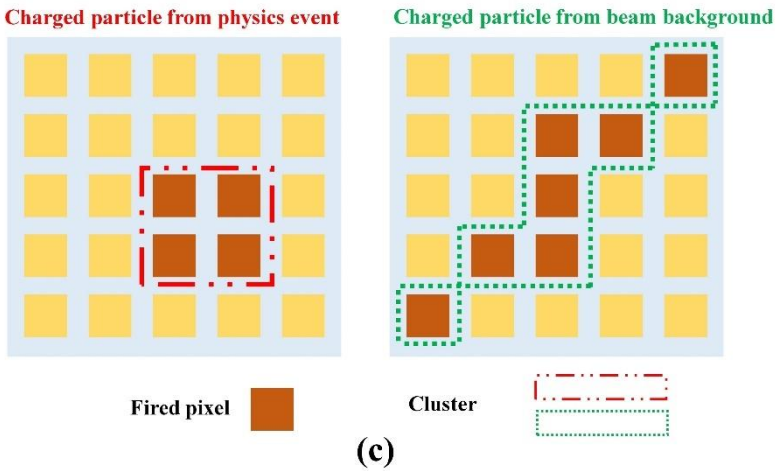
Beam Background with low momentum （10~100MeV）

Large angle of incidence on CMOS Pixel Sensor

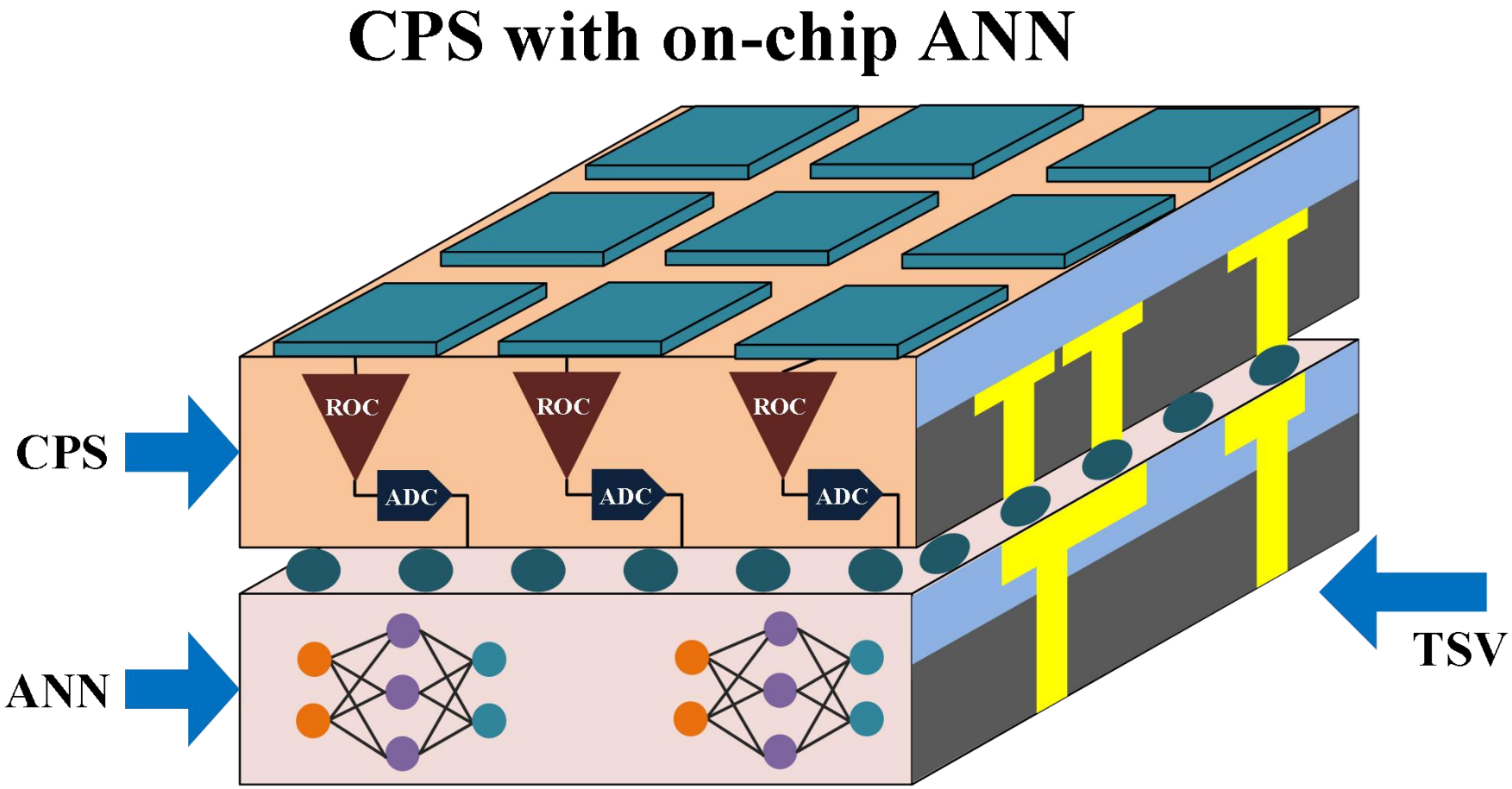
Generate elongated cluster



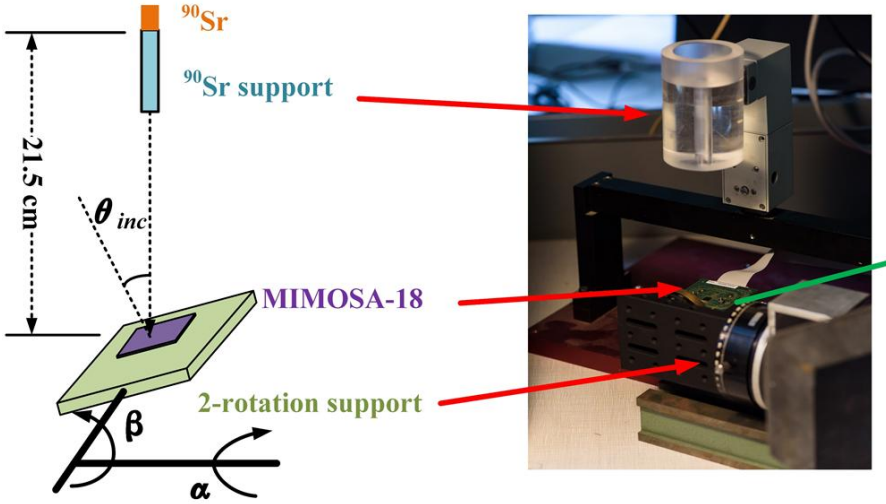


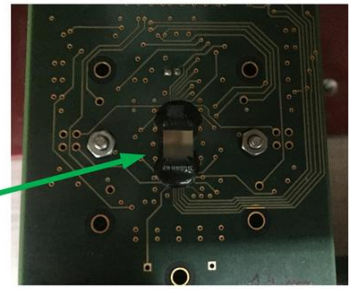


2.HOW?



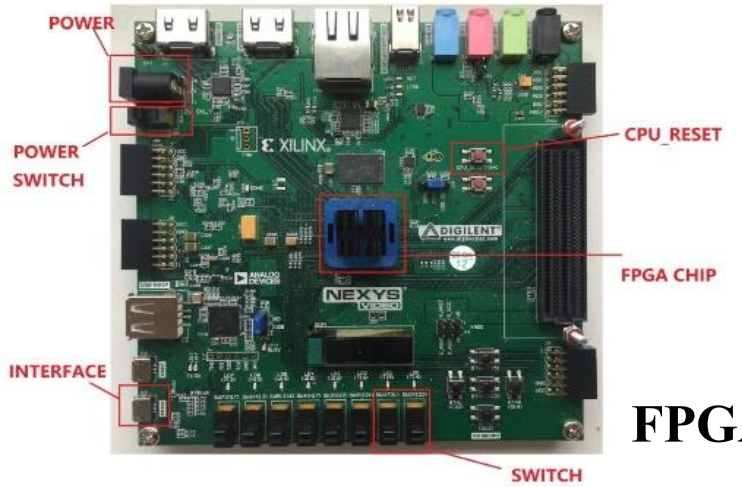
3.1 WHAT-Previous work



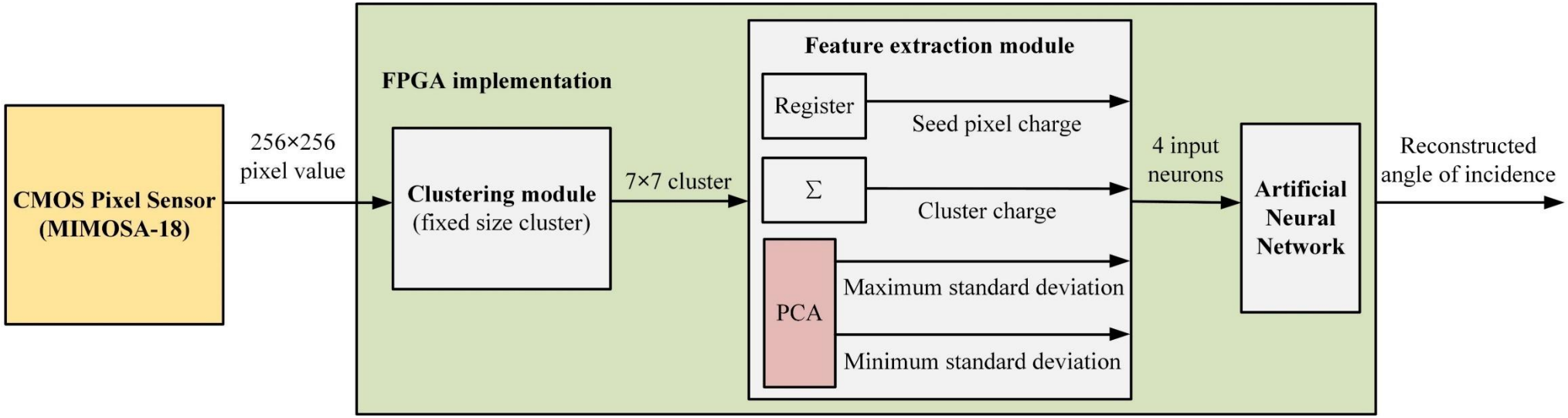


MIMOSA-18

Data acquisition system

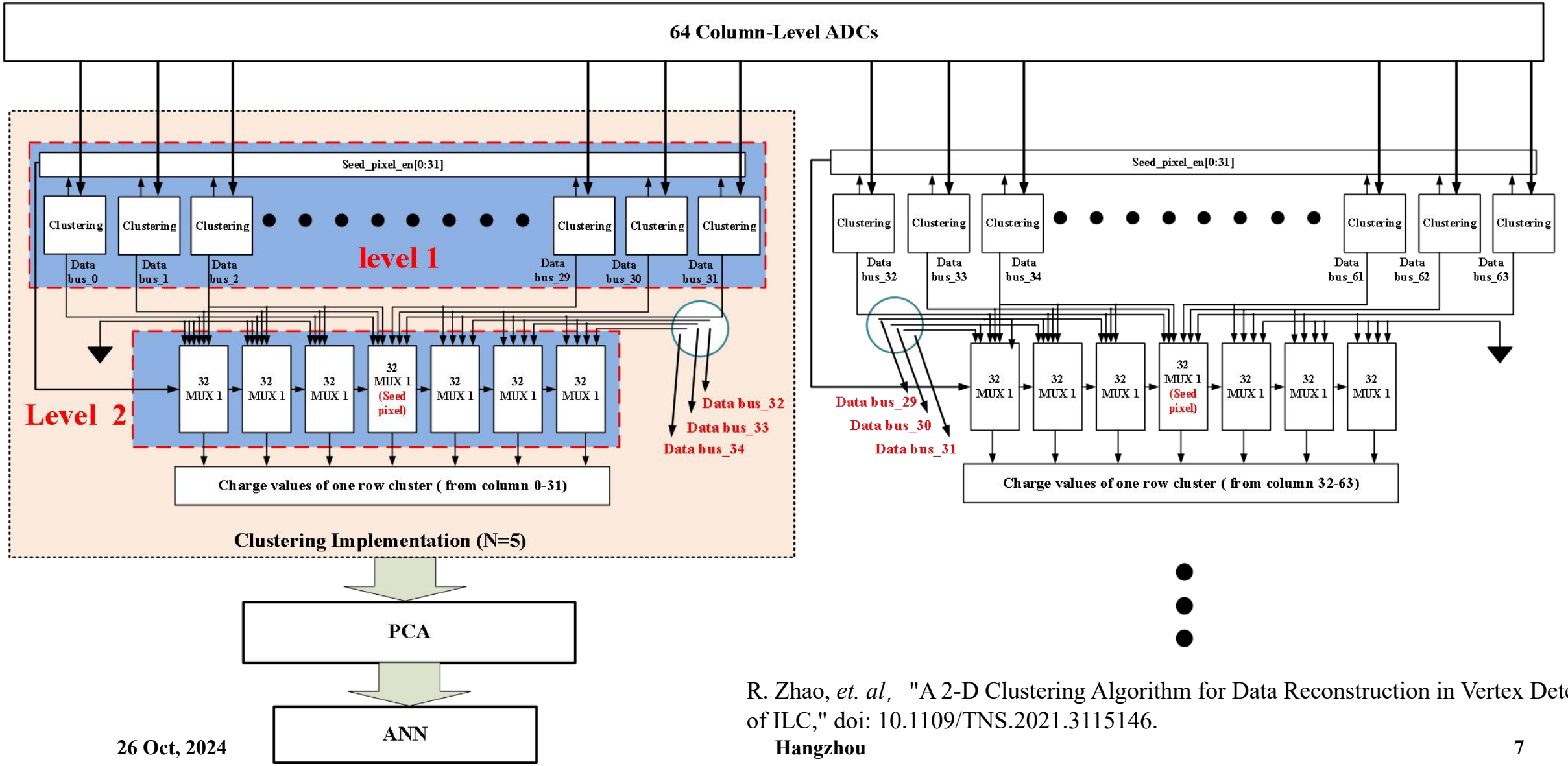


FPGA



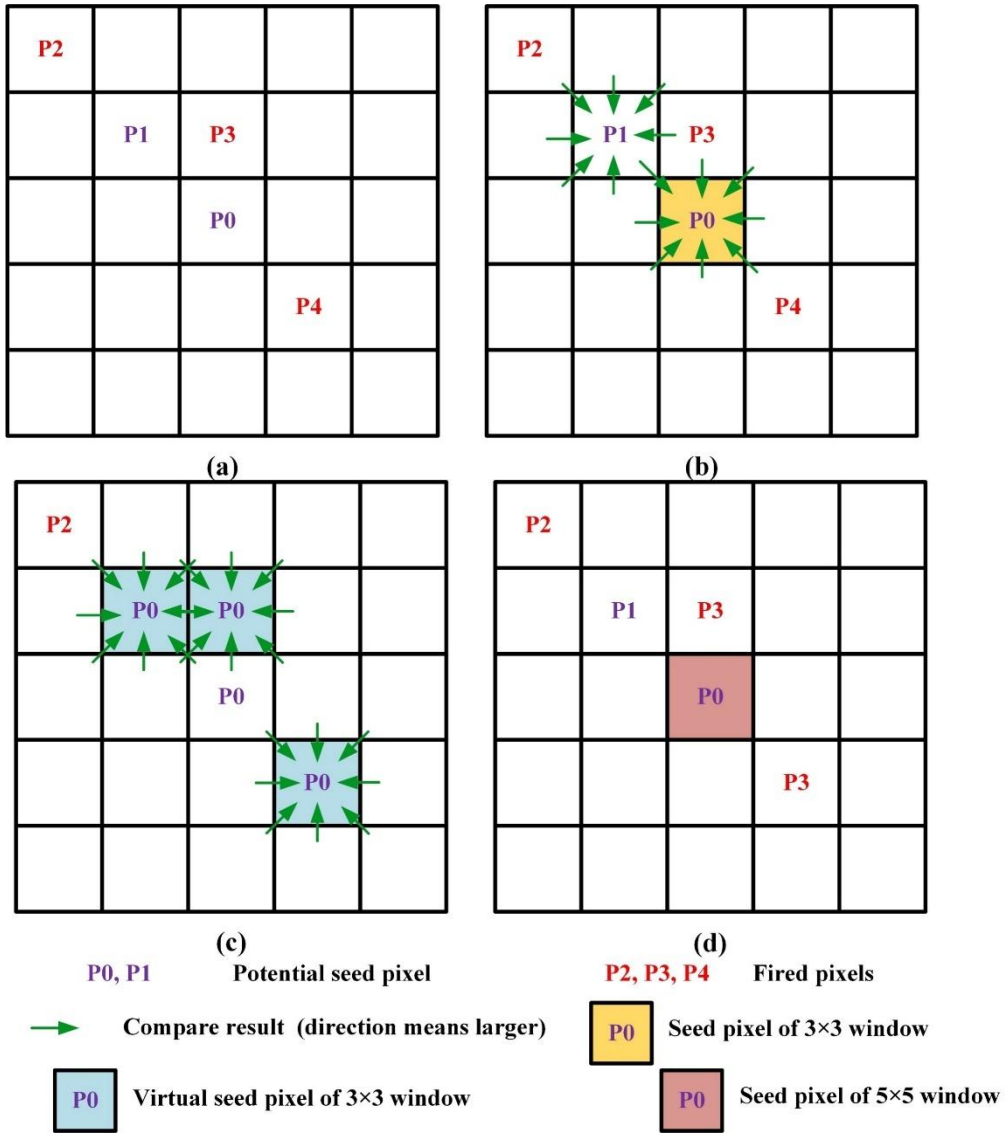
R.ZHAO, *et. al,* "FPGA Implementation of an Artificial Neural Network for Subatomic Physics Experiment Particles Recognition"

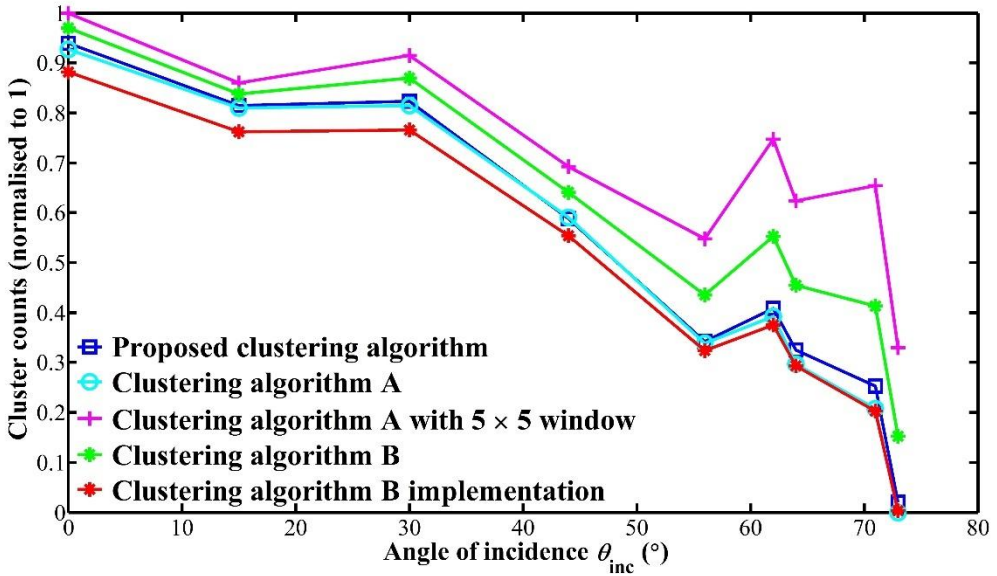
3.1 WHAT-Previous work

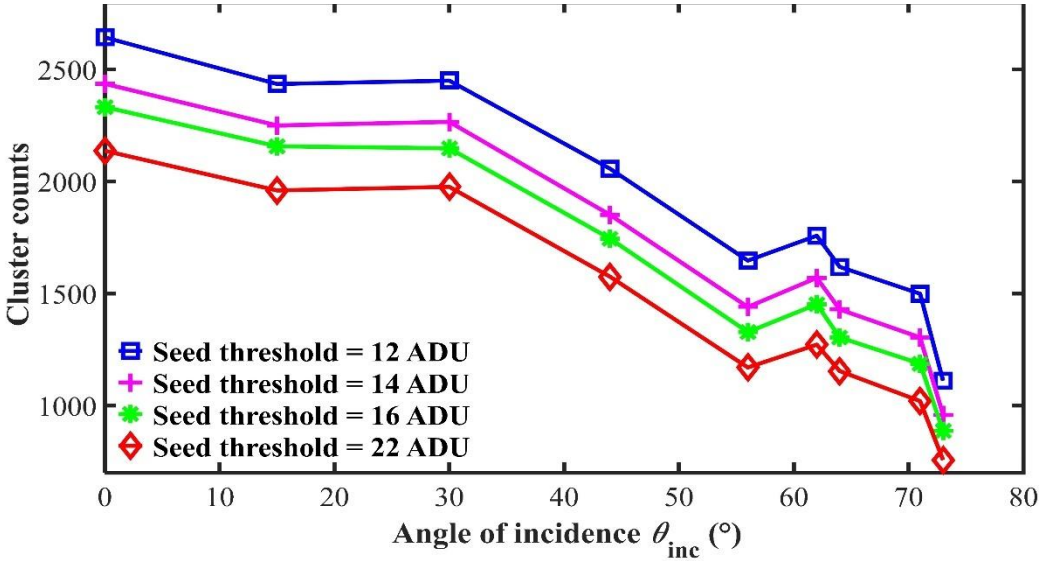


R. Zhao, *et. al*, "A 2-D Clustering Algorithm for Data Reconstruction in Vertex Detector of ILC," doi: 10.1109/TNS.2021.3115146.

3.1 WHAT-Previous work

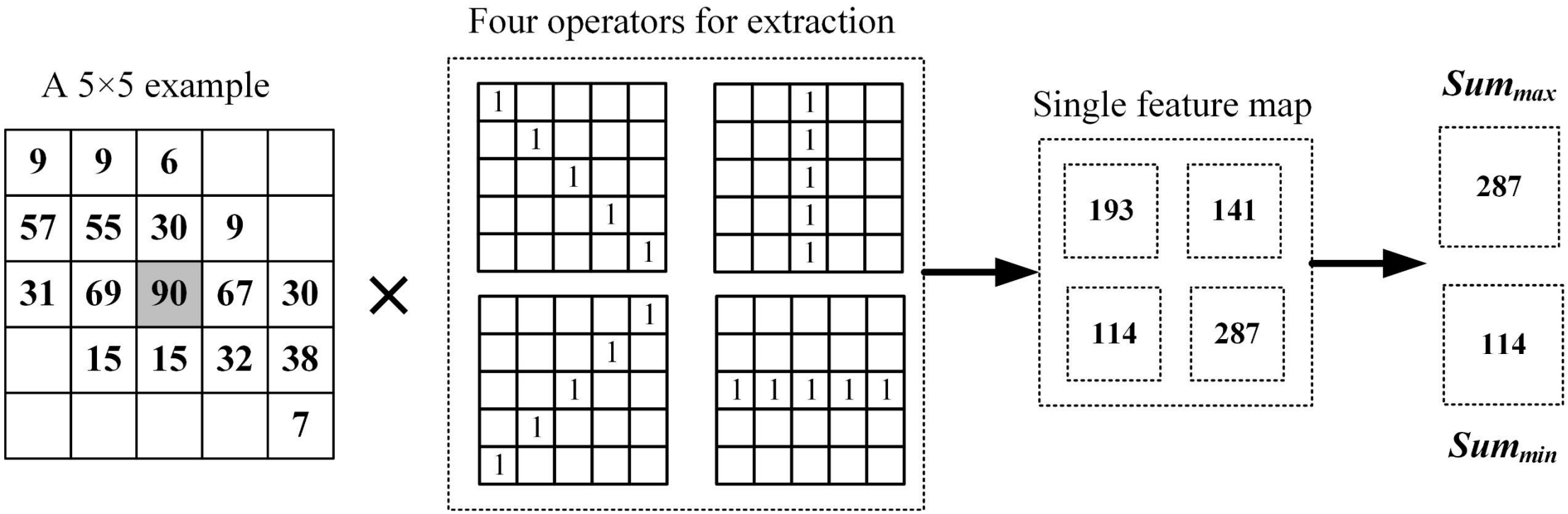






R. Zhao *et al.*, "Pixel-level clustering algorithm for data reconstruction in ILC," doi: 10.1109/TNS.2023.3330537

3.1 WHAT-Previous work



Example of operators for axis feature extraction

$$\left\{\begin{array}{ll} Sum_{\max} = \max(f(i)) & \\ Sum_{\min} = \min(f(i)) & \\ f(i) = \sum_{n=1}^{5} \text{pixel charge}_{i,n}, & i = (1,2,3,4) \end{array}\right\}.$$

R. Zhao, *et. at,* "Performance Analysis of Compact On-Chip Operators for Cluster Feature Extraction,"doi: 10.1109/TNS.2023.3320226.

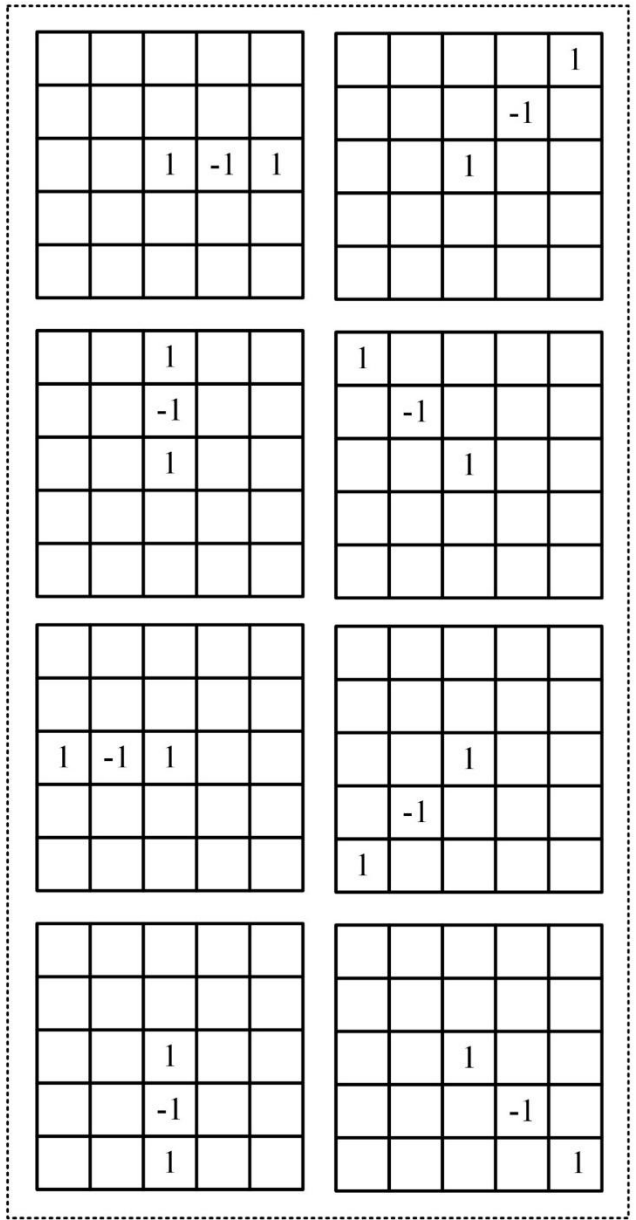
3.1 WHAT-Previous work

A 5×5 example

9	9	6		
57	55	30	9	
31	69	90	67	30
	15	15	32	38
				7

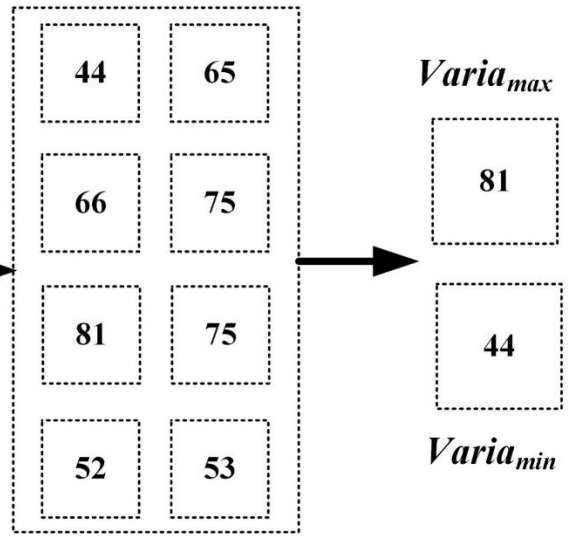
×

Eight operators for extraction



$$\left\{\begin{array}{c} Varia_{max} = max\left(f(k)\right) \\ Varia_{min} = min\left(f(k)\right) \\ f(k) = pixel\ charge_{k,3} - pixel\ charge_{k,2} + pixel\ charge_{k,1} \end{array}\right\}$$

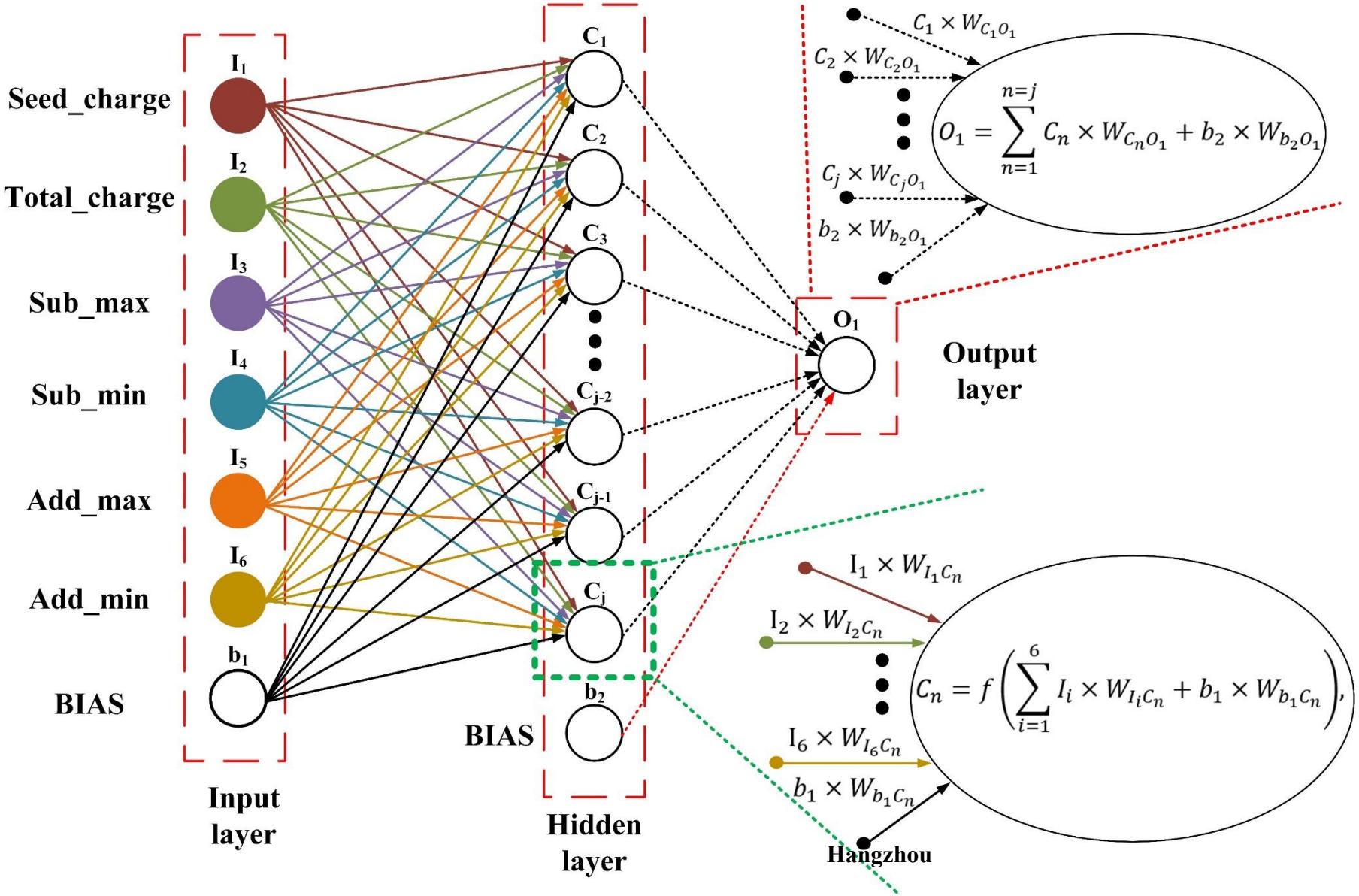
Single feature map



Example of operators for direction feature extraction

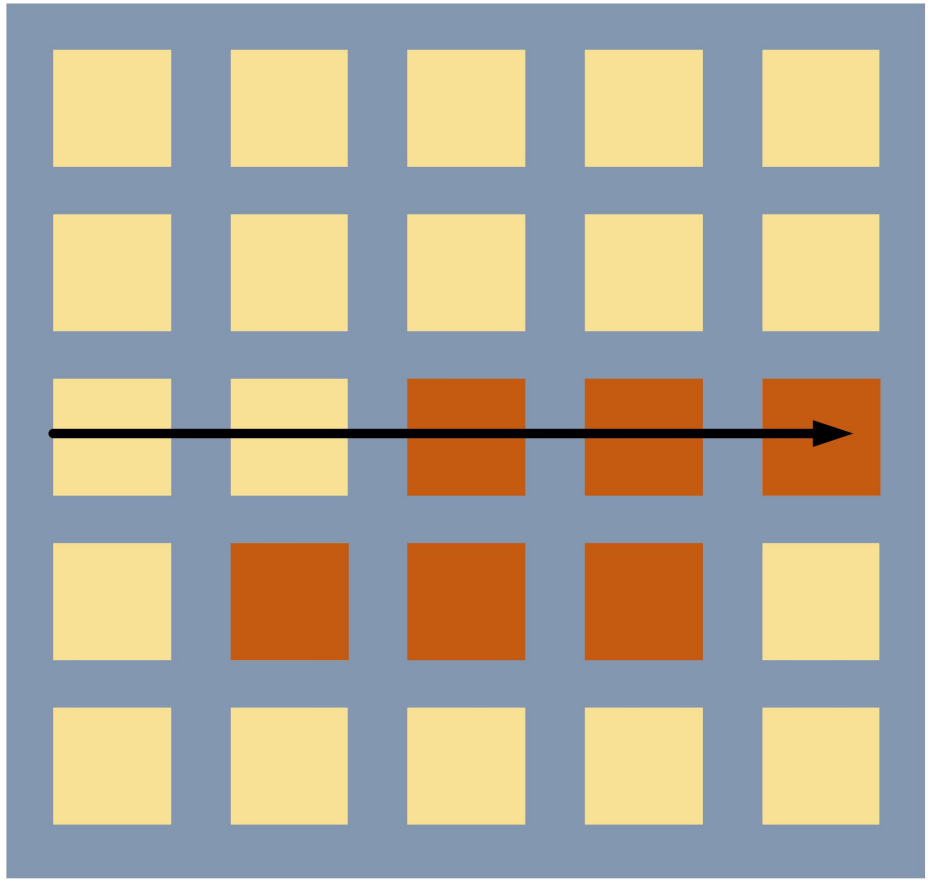
R. Zhao, *et. at,* "Performance Analysis of Compact On-Chip Operators for Cluster Feature Extraction,"doi: 10.1109/TNS.2023.3320226.

3.2 WHAT-Now: ANN model



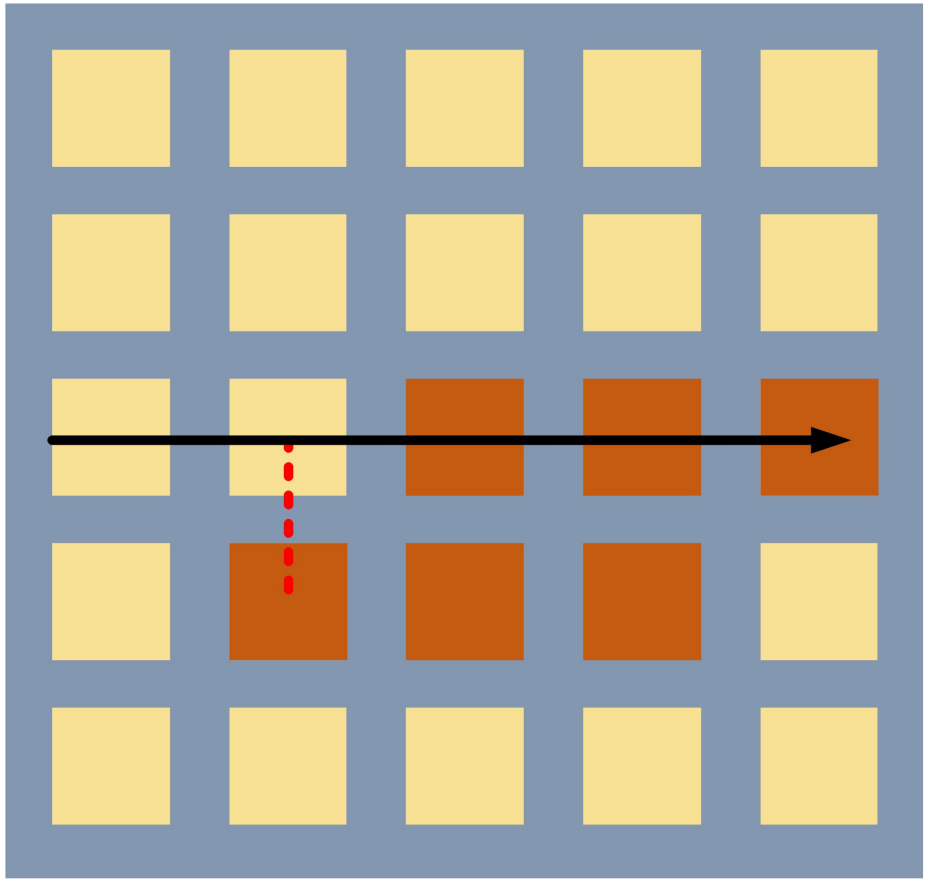
3.2 WHAT-Now: ANN model

Hit count along X axis



Hit count： 3

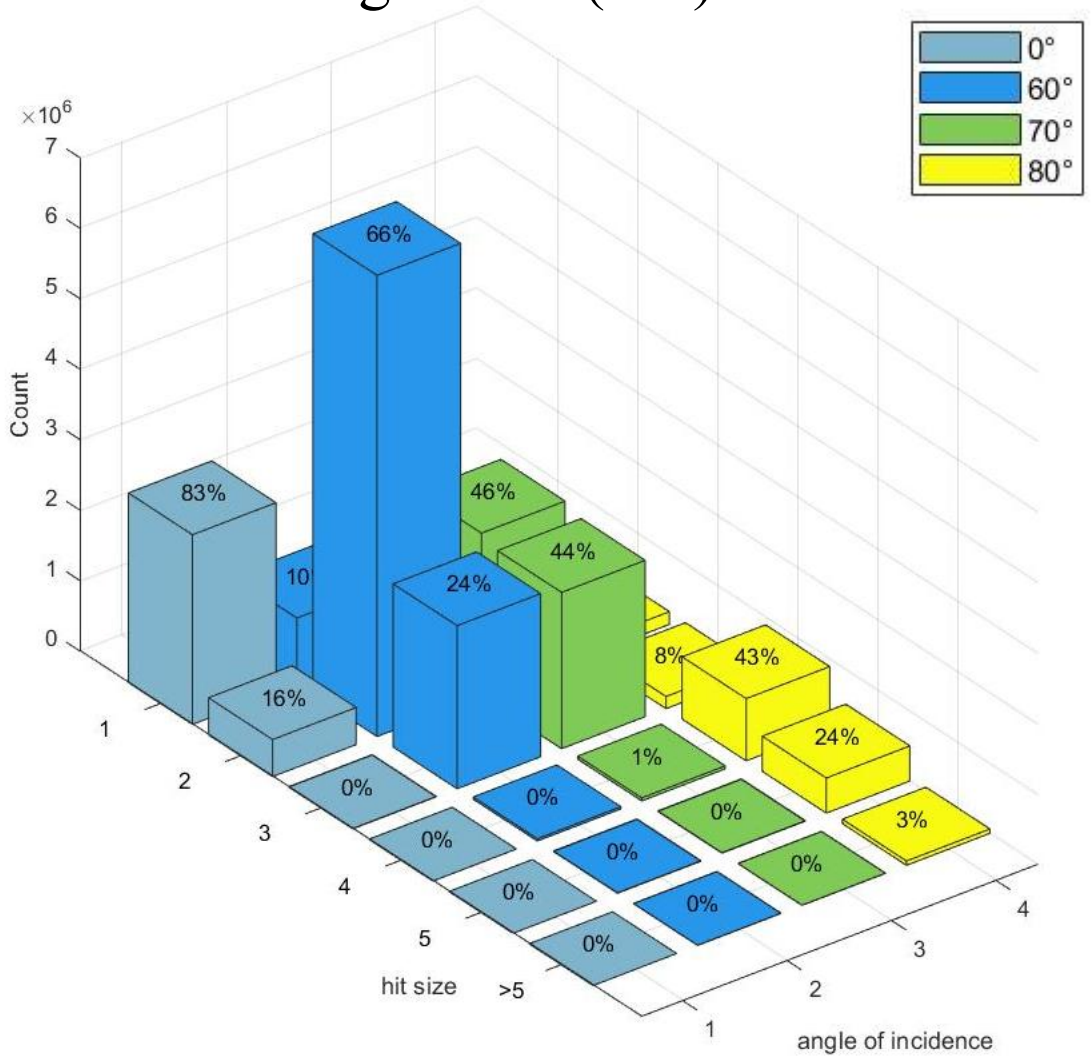
Hit count of cluster projection on axis

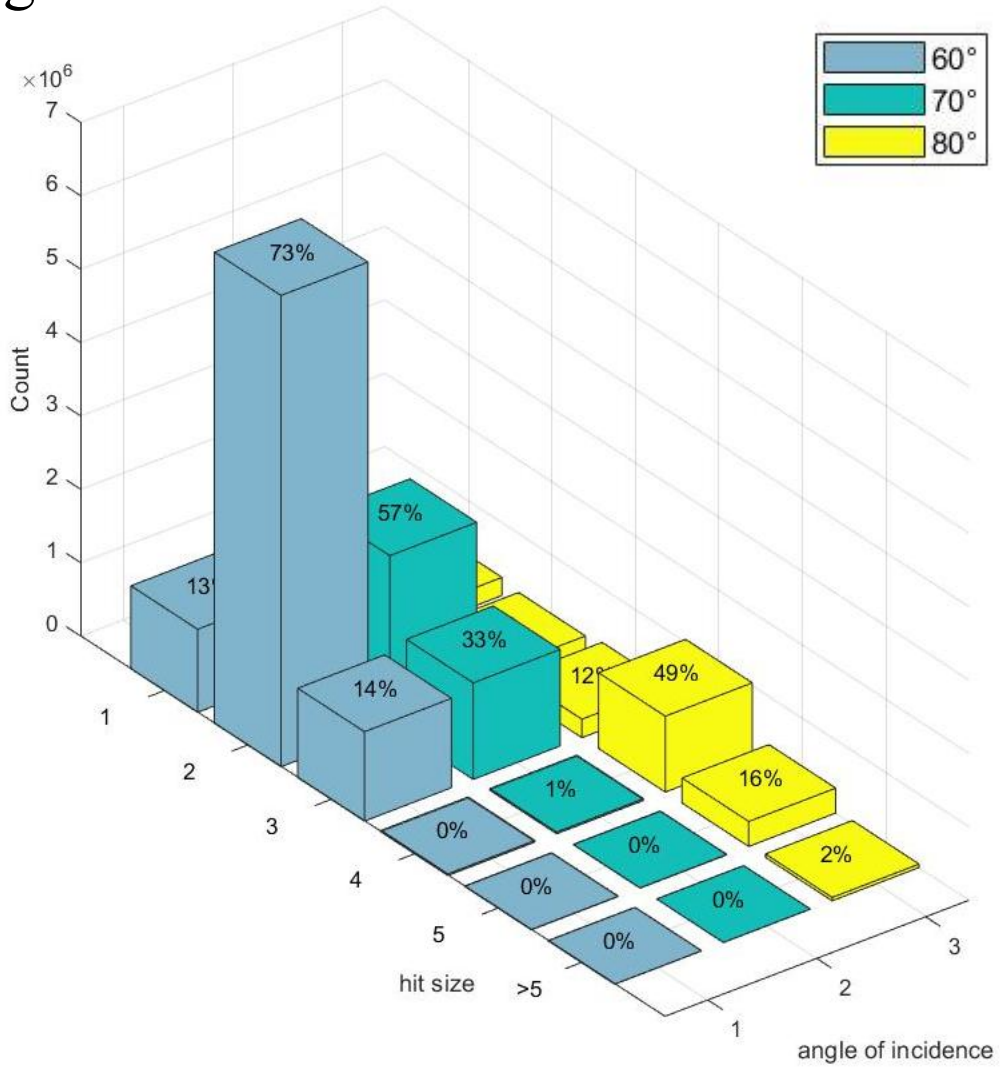


Hit count： 4

3.2 WHAT-Now: Beam Test of Taichu3

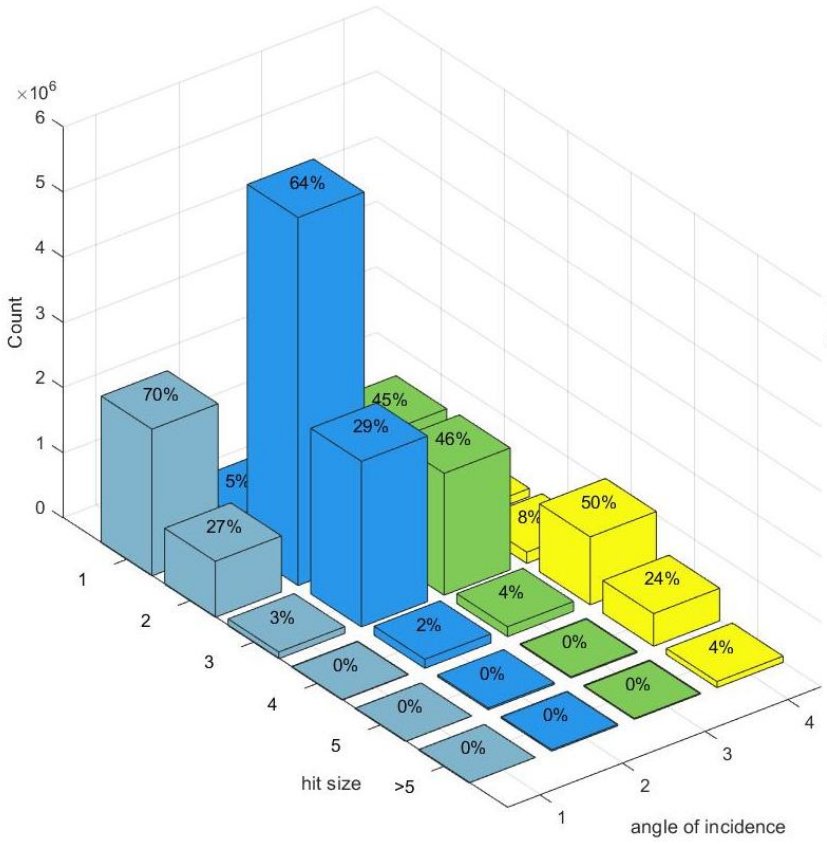
Hit count along Y axis (90°) under different tilt angle



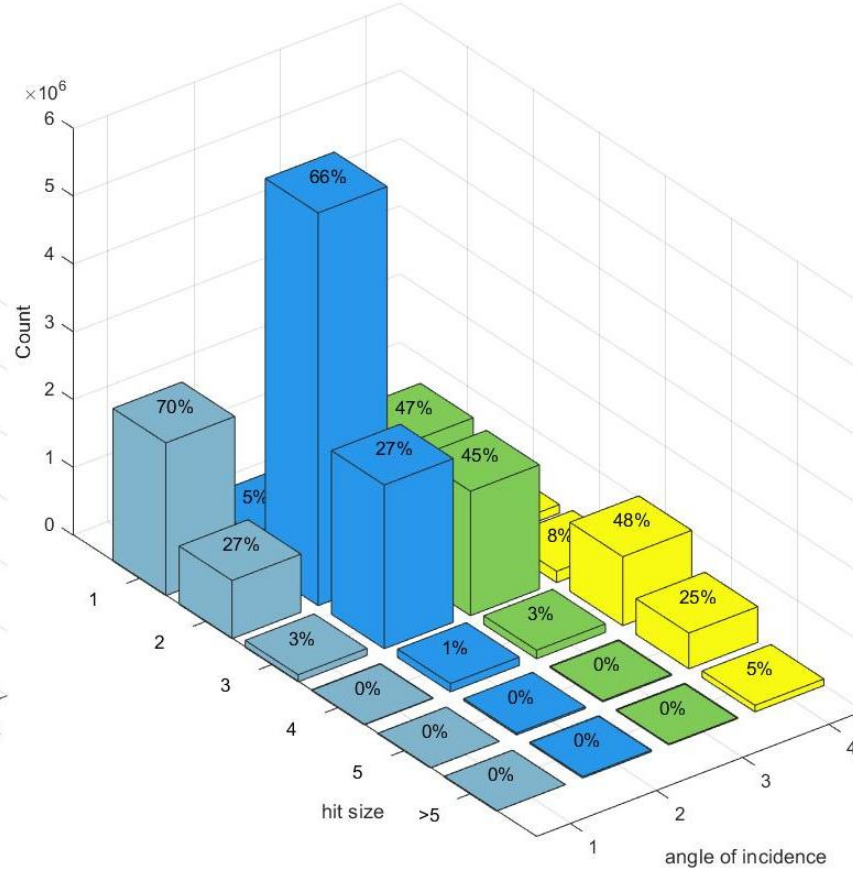


3.2 WHAT-Now: Beam Test of Taichu3

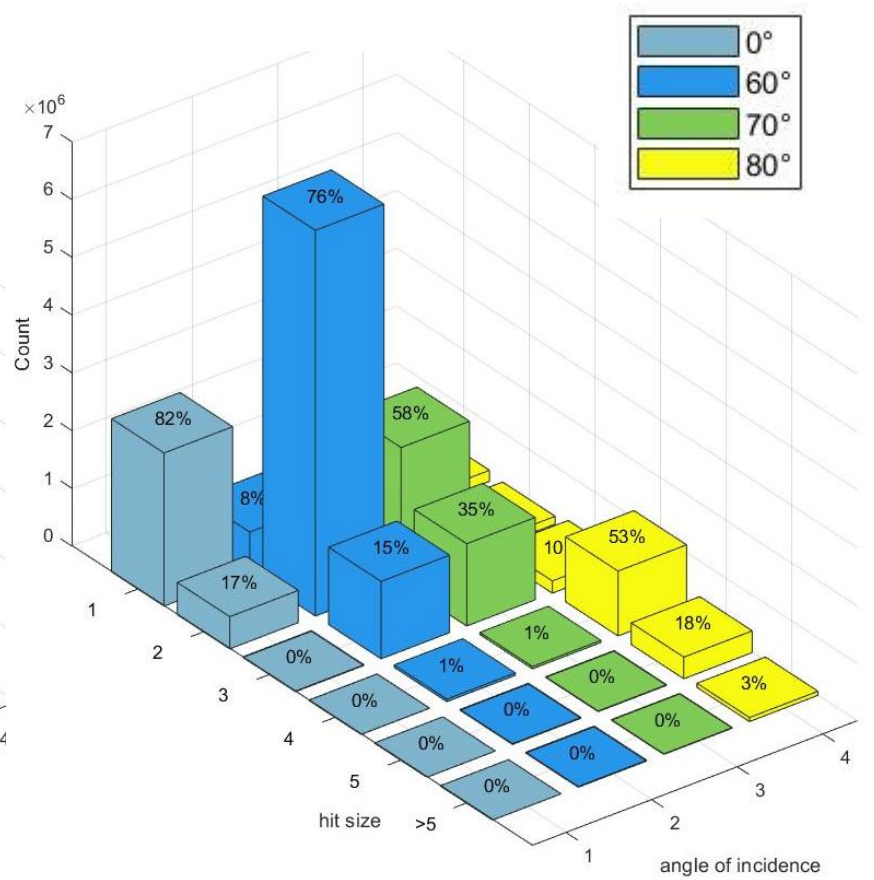
Hit count of cluster projection on axis under different tilt angle



Diagonal A (45°)



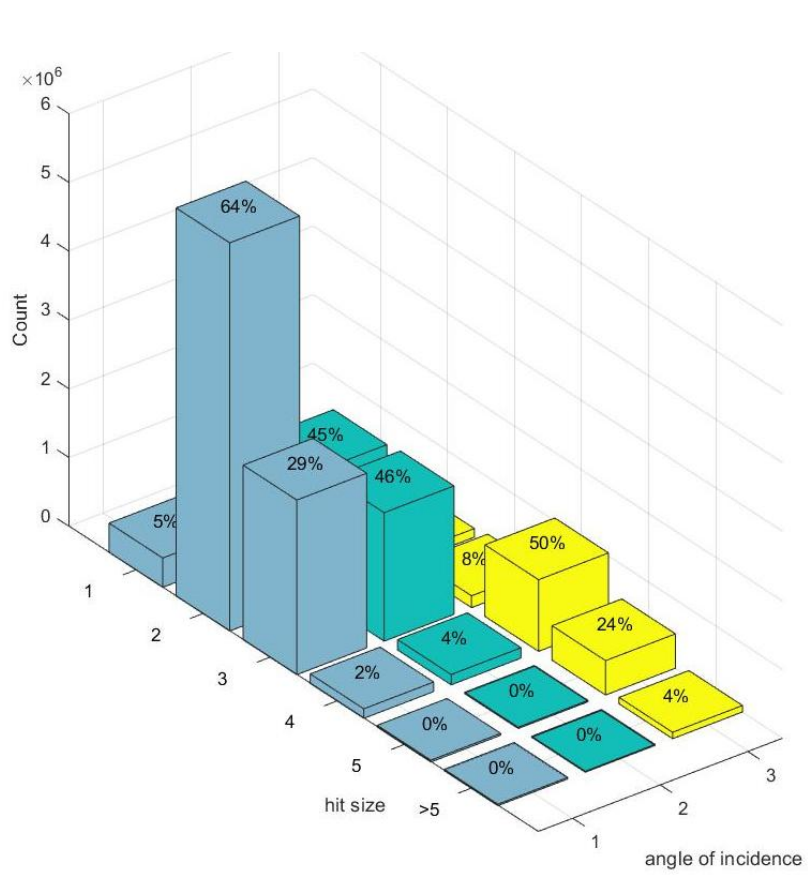
Diagonal A (135°)



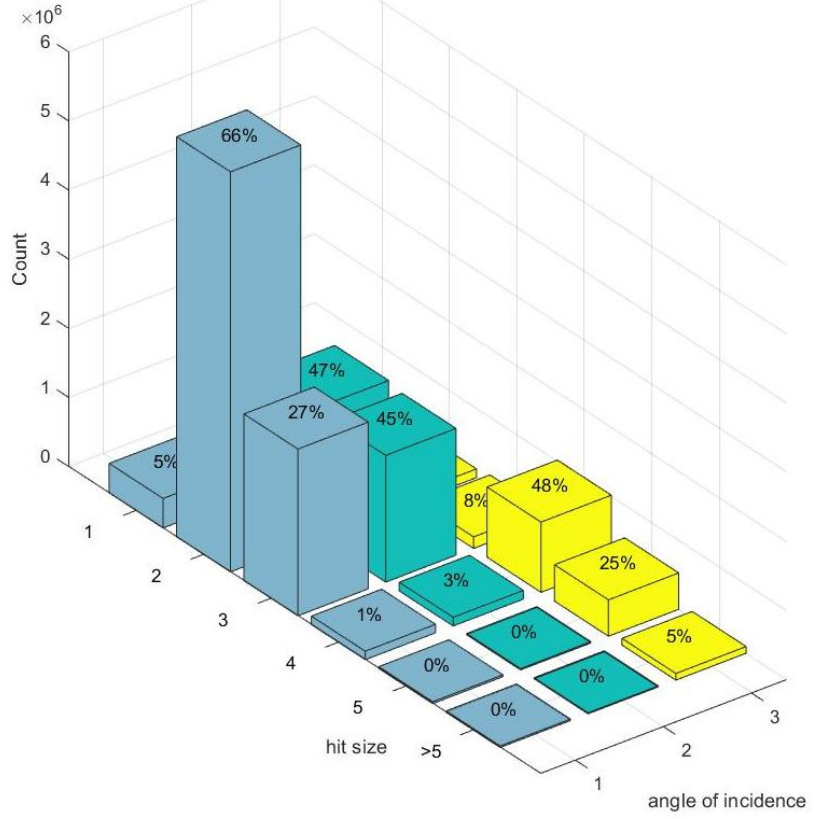
X axis (0°)

3.2 WHAT-Now: Beam Test of Taichu3

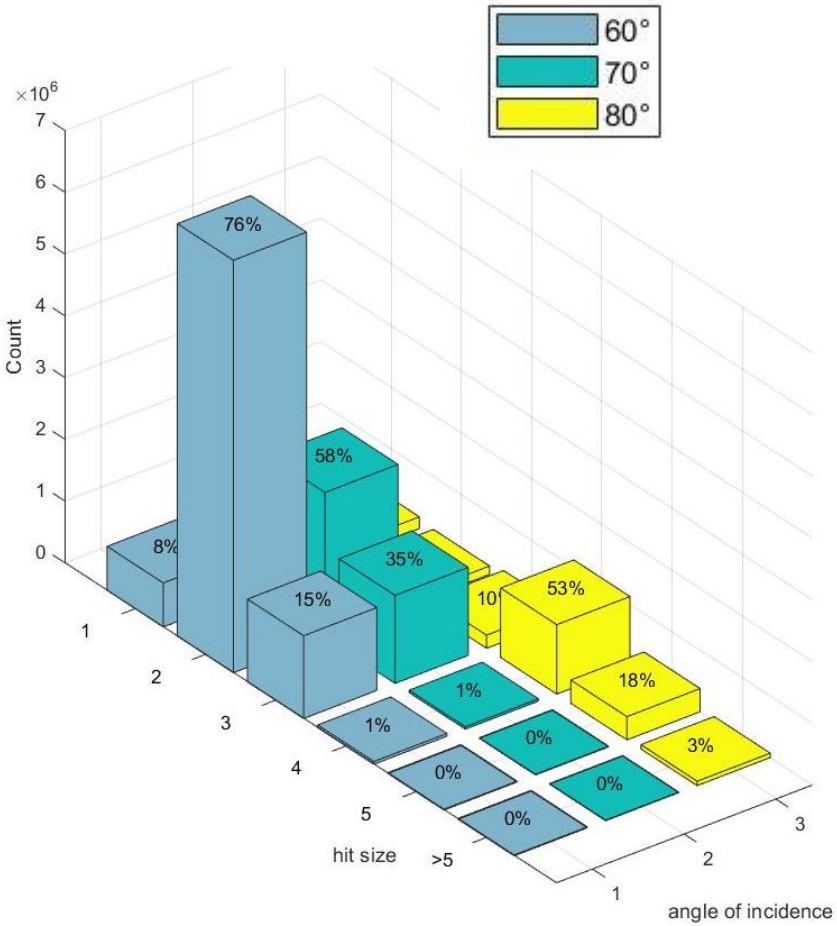
Hit count of cluster projection on axis under different tilt angle



Diagonal A (45°)



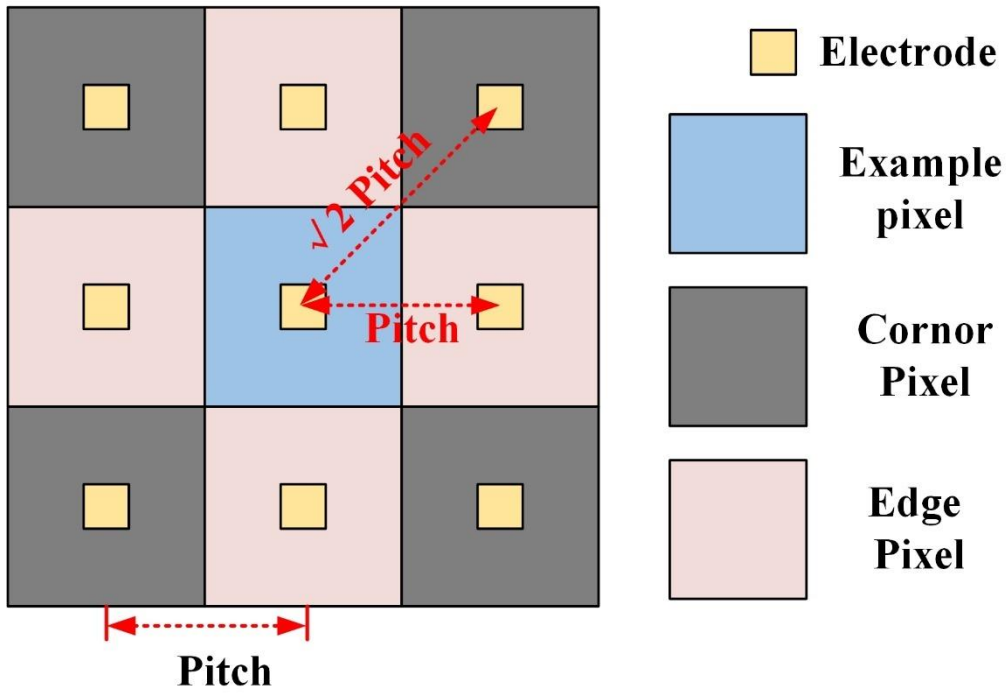
Diagonal B (135°)



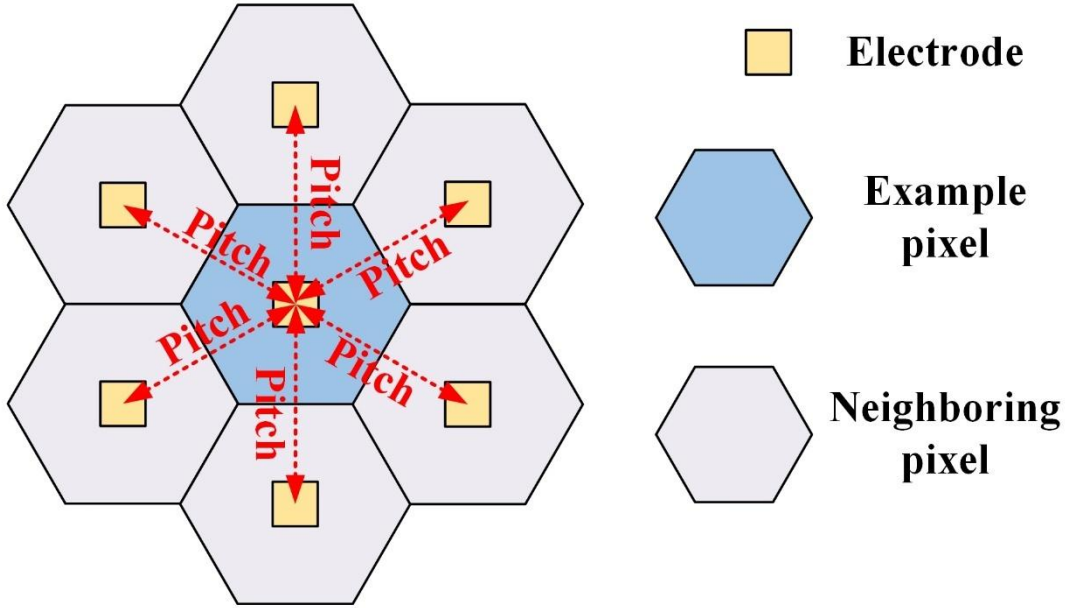
X axis (0°)

3.2 WHAT-Now: Hexagonal Geometry Pixel

Square Pixel Layout



Hexagon Pixel Layout

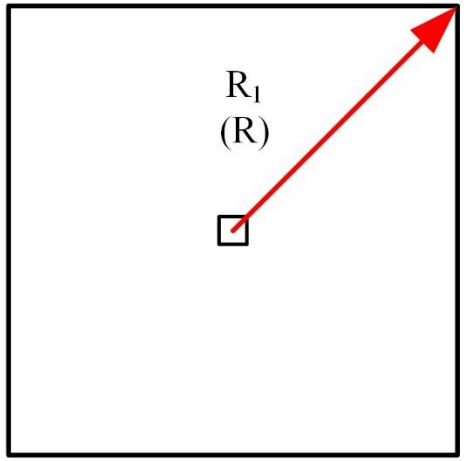


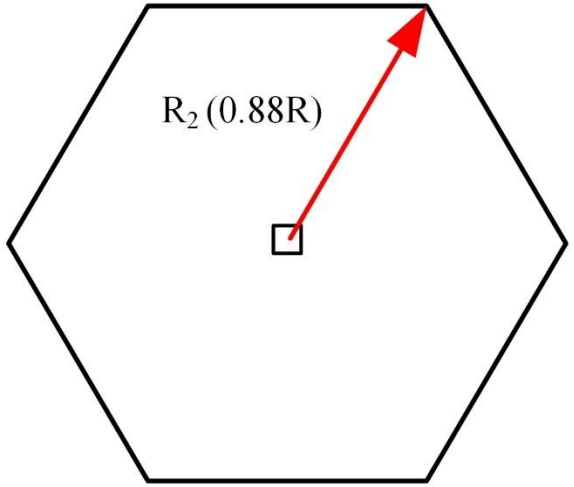
1、Neighbors **2、Same Pitch** **3、Time Resolution**

Ref: Ryuji Moriya, Simulating Hexagonal Pixel Sensor Design in Allpix^2

3.2 WHAT-Now: Hexagonal Geometry Pixel

square and hexagonal geometry for same occupied size





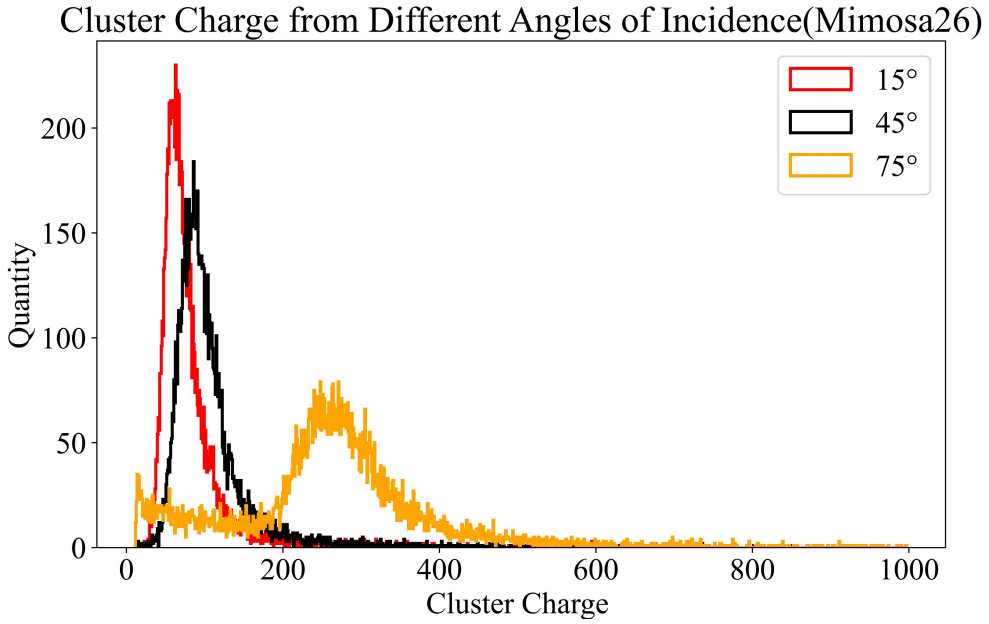
$$S_{square} = \sqrt{2}R_1 \times \sqrt{2}R_1 = 2R_1^2 \qquad S_{hexagon} = R_2 \times \frac{\sqrt{3}}{2}R_2 \times \frac{1}{2} \times 6 = \frac{3\sqrt{3}}{2}R_2^2$$

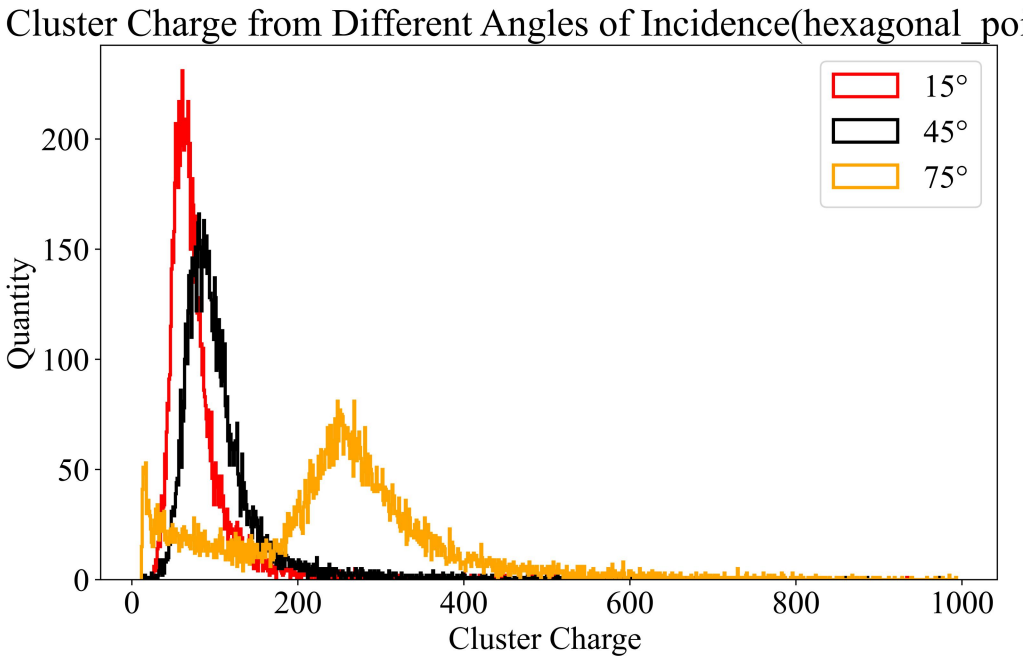
$$S_{square} = S_{hexagon} \Rightarrow R_2 = 0.88R_1$$

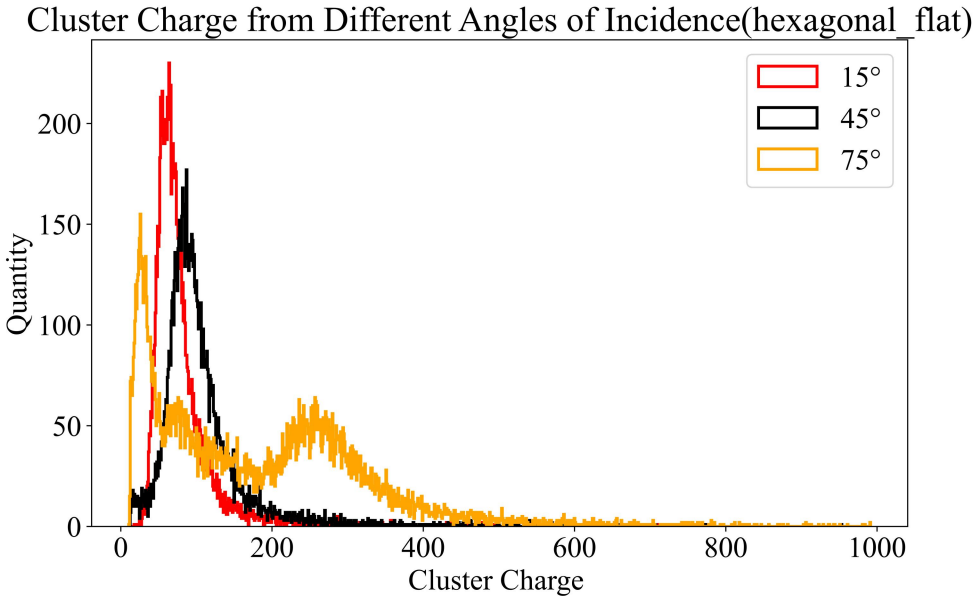
1、Neighbors **2、Same Pitch** **3、Time Resolution**

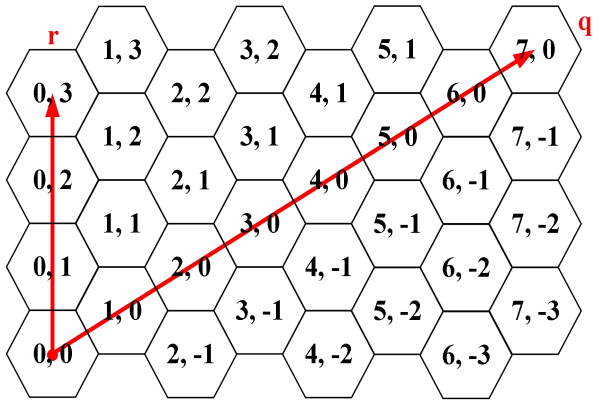
Ref: Ryuji Moriya, Simulating Hexagonal Pixel Sensor Design in Allpix²

3.2 WHAT-Now: Hexagonal Geometry Pixel

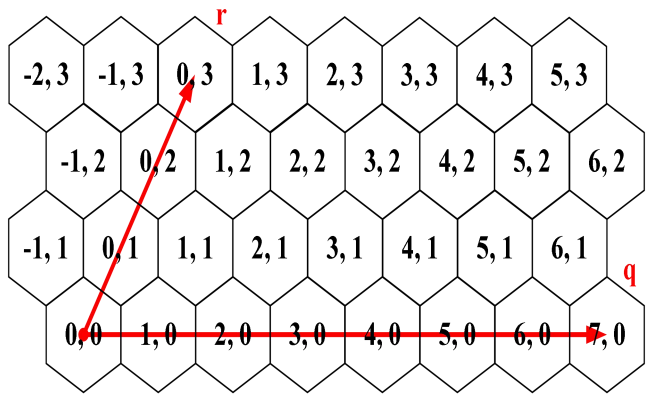






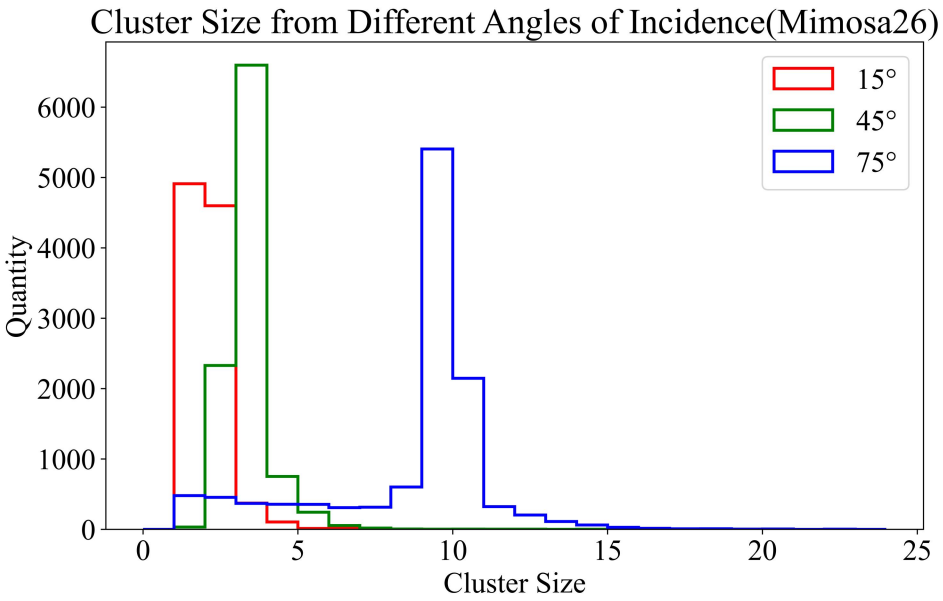


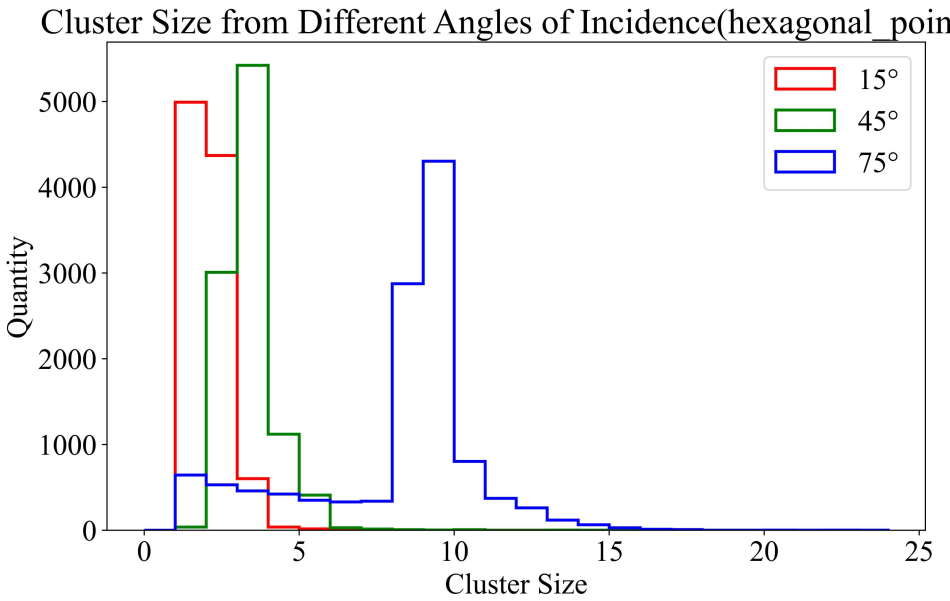
Hexagonal-pointy

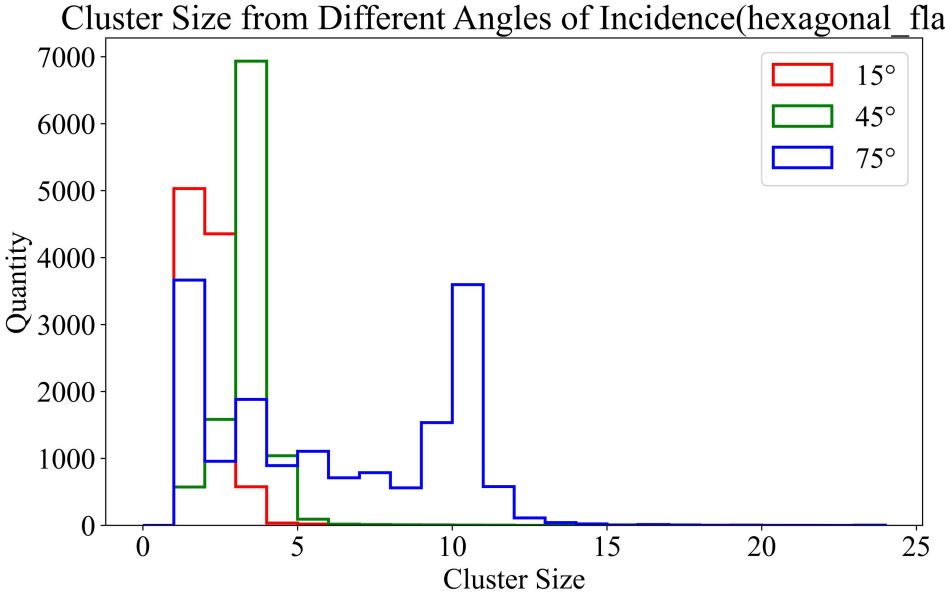


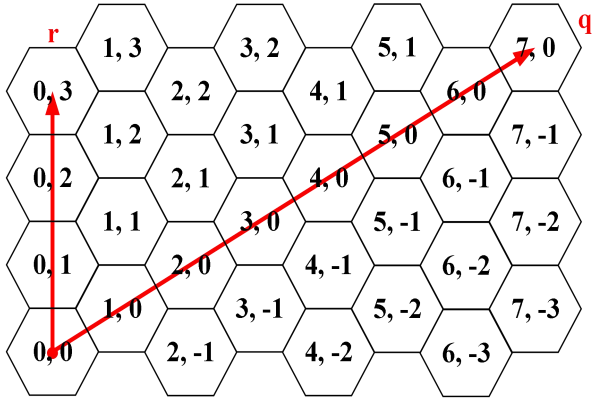
Hexagonal-flat

3.2 WHAT-Now: Hexagonal Geometry Pixel

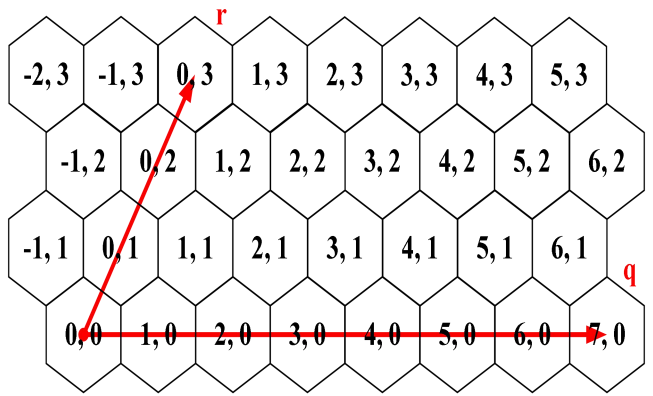








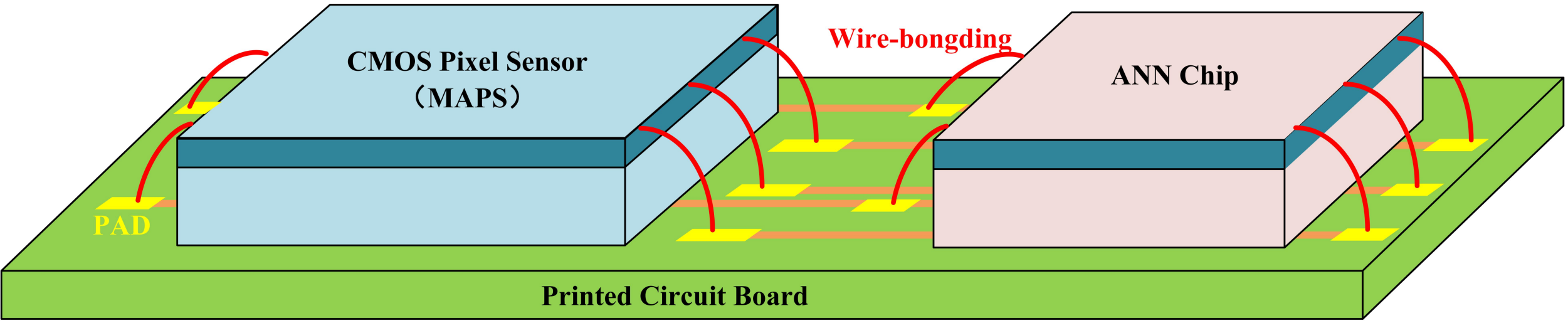
Hexagonal-pointy



Hexagonal-flat

4. NEXT

- **Develop ANN Model and Implementation in FPGA**
- **Develop artificial neural network ASIC for test**



Acknowledge

- Thanks our colleagues from IHEP and IPHC for their support
  - Hancen LU
  - Haoyu SHI
  - Jingbo YE
  - Shuqi LI
  - Yanping HUANG
  - Yang ZHOU
  - Ying ZHANG
  - Zhijun LIANG

Thanks for your attention

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