清華大學工程物理系

Department of Engineering Physics, Tsinghua University

The 2024 international workshop on the high energy Circular Electron Positron Collider

Development of Interposer based pixel TPC Readout

Liu Canwen[*1]、Yang Yanxiao[*1]、Deng Zhi[*1]、Gong Guanghua[*1]、Dong Jianmeng[*1]、
Qi Huirong[*2]，Chang Yue[*2]、She Xin[*2]、Zhang Jinxian[*2]、Wang Jianchun[*2]、Zhang Jian[*2]

1: Tsinghua University
2: Institute of High Energy Physics, Chinese Academy of Sciences

Oct. 23 – 27, 2024 Hangzhou, China

OUTLINES

01 | Introduction

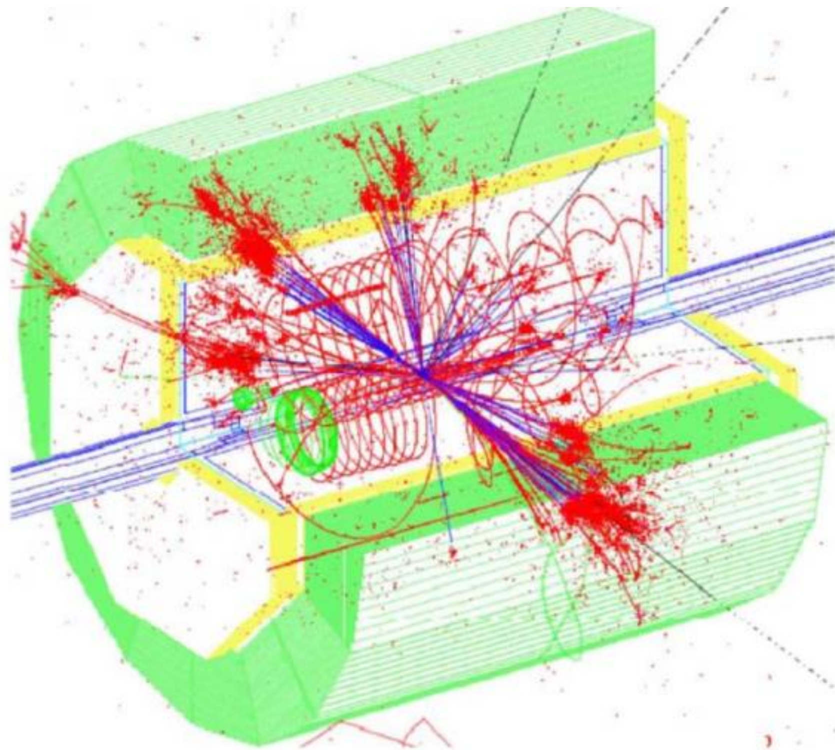
02 | Interposer based pixel TPC

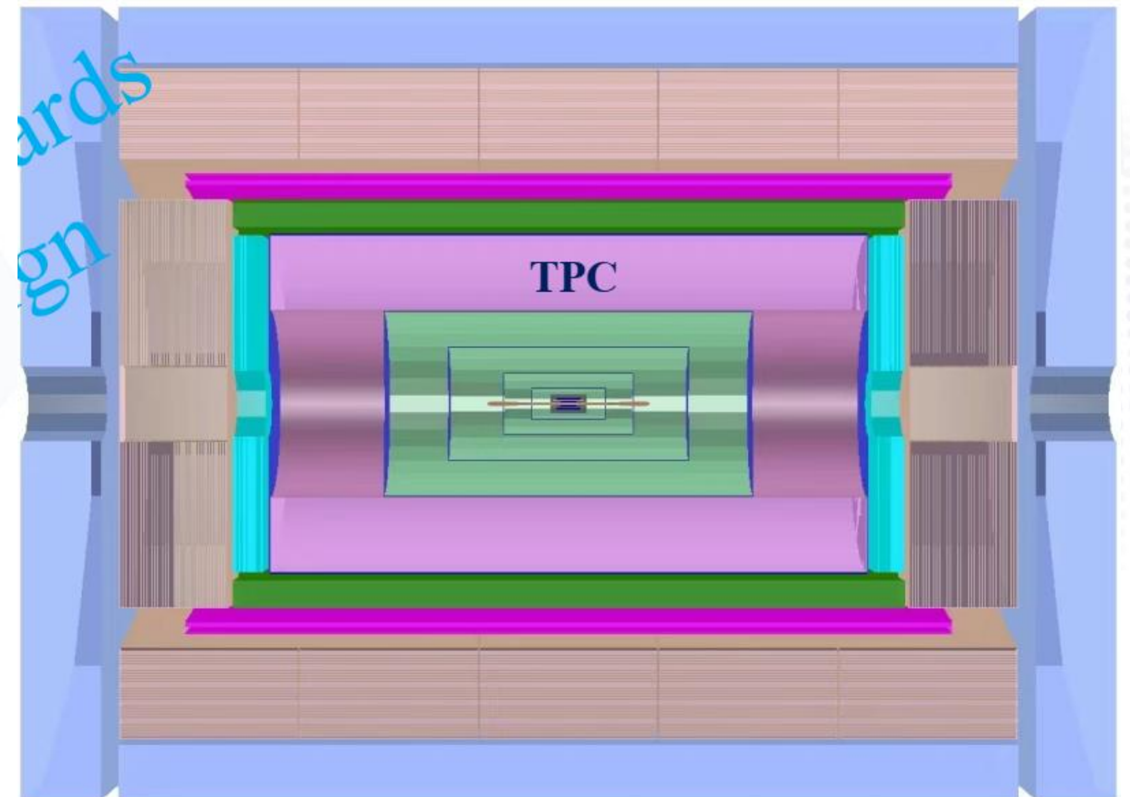
03 | Current progress on the demonstrator

04 | Summary

Time Projection Chamber for CEPC

- TPC is a gas detector and can measure particle track precisely in **three dimensional** with **low mass**
- TPC is as the **baseline** main tracker in CEPC ref-TDR, achieving good **momentum resolution** and **particle identification**



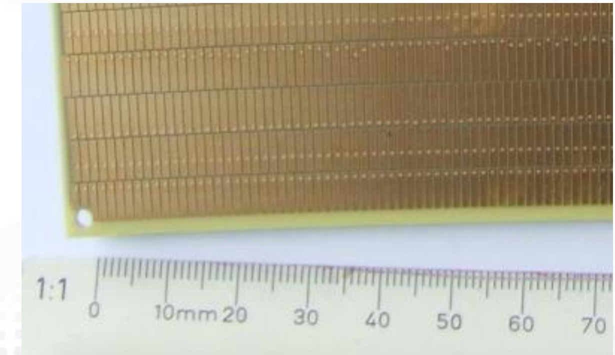


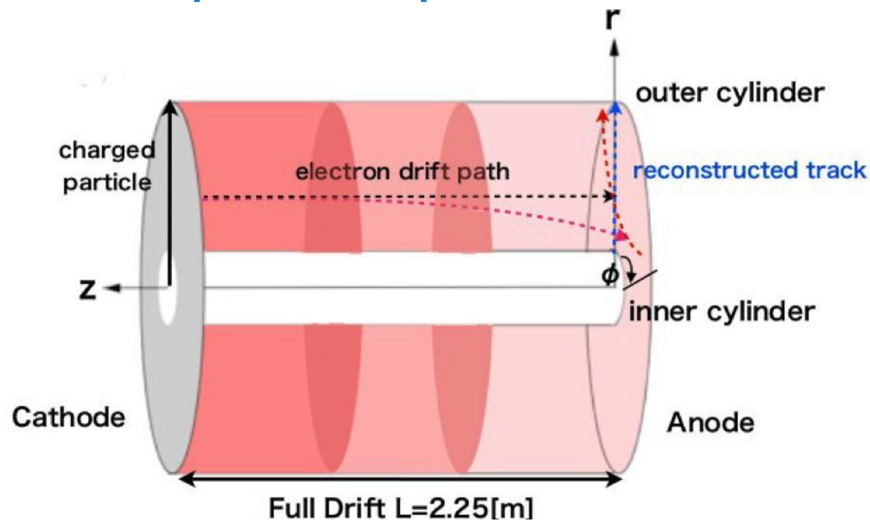
Geometry of the track detector system in CEPC TDR

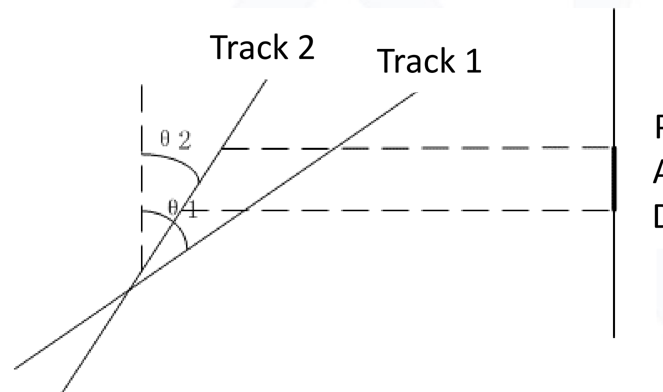
Pad Readout TPC

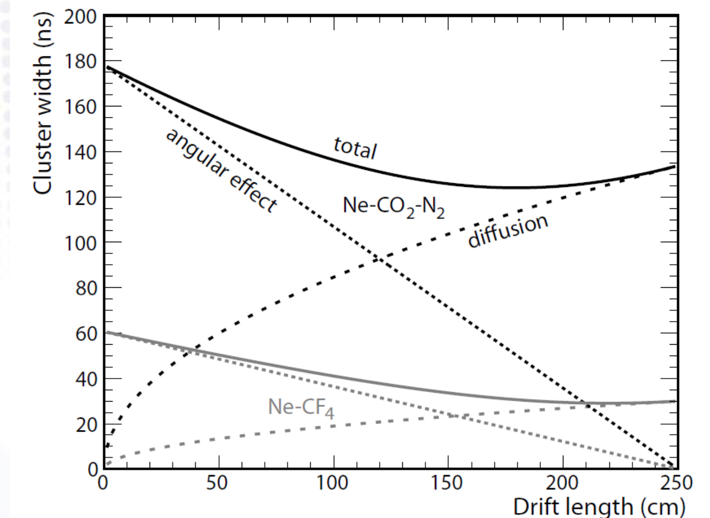
- Signals induced in readout pads **in mm²**:
  - ALICE TPC: 4x7 mm² - 6x15 mm²
  - T2K TPC: 10x11 mm²
  - ILC TPC: 1x6 mm²
- **Ballistic Loss** vs signal pileup
- Acquire amplitude and time information at the same time

Waveform Sampling



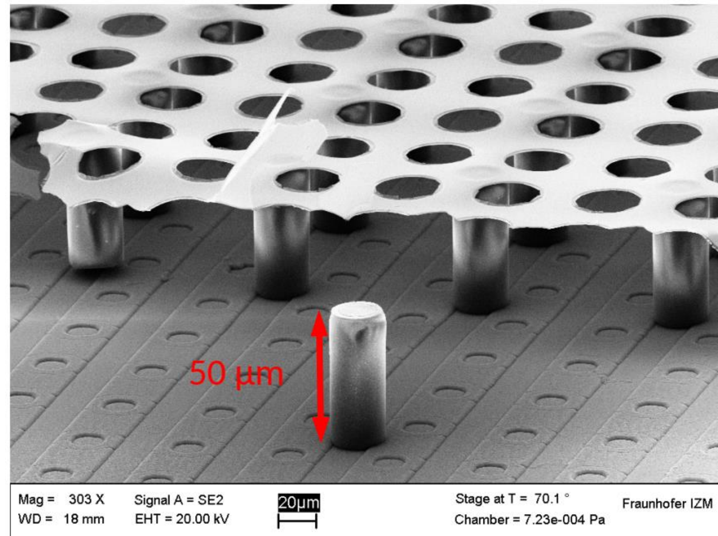


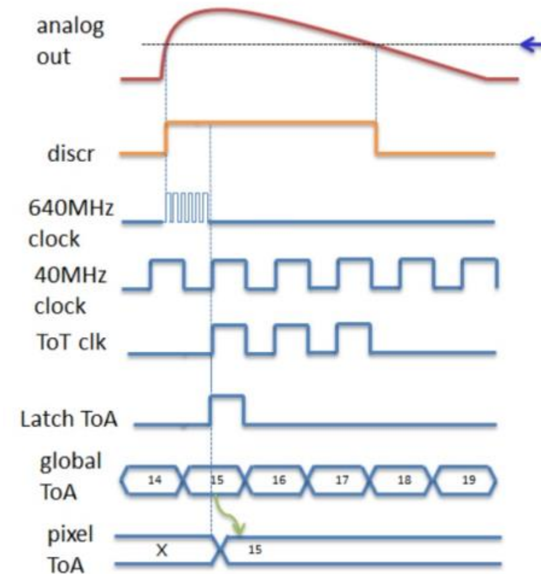


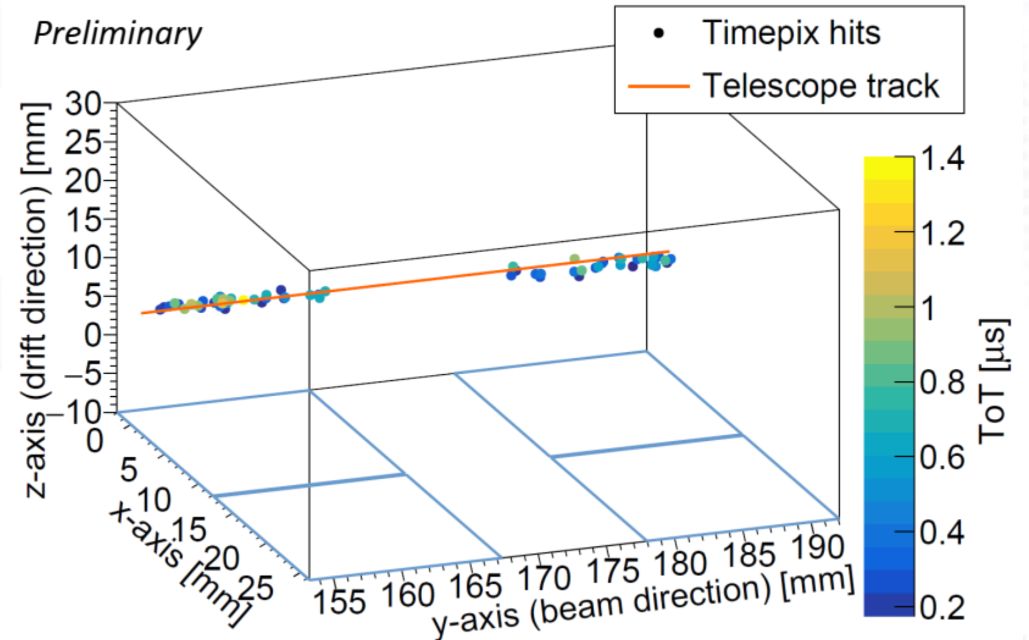


Pixel readout TPC

- Combination of a pixel ASIC with TPC, e.g., **55 um pixels** using TPX3/4
- The signal duration variation reduces as the pixel size
  - no need for waveform, only charge and arrival timing
- PID improvement: dE/dx → **dN/dx**

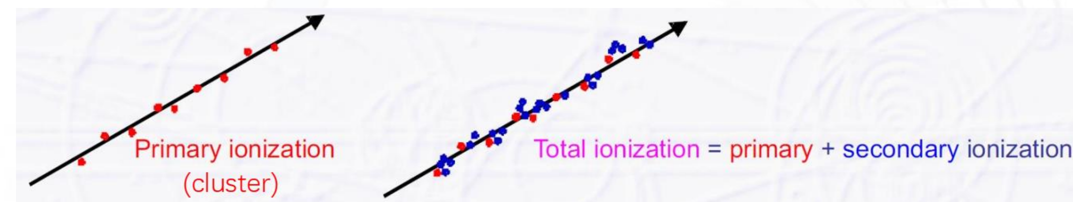


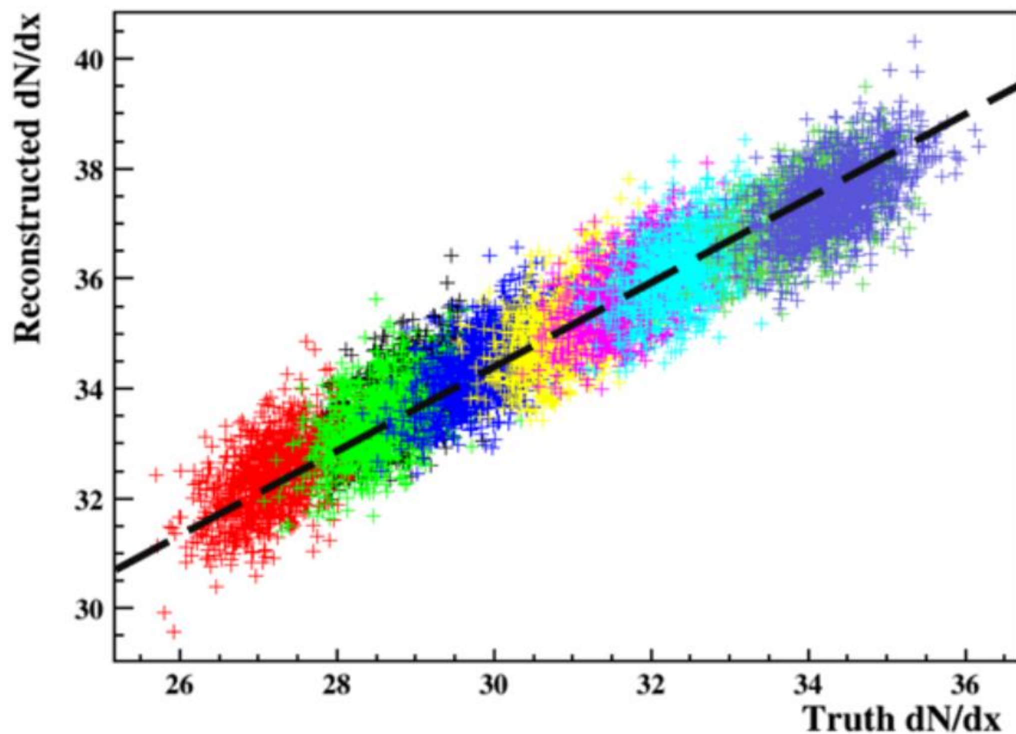


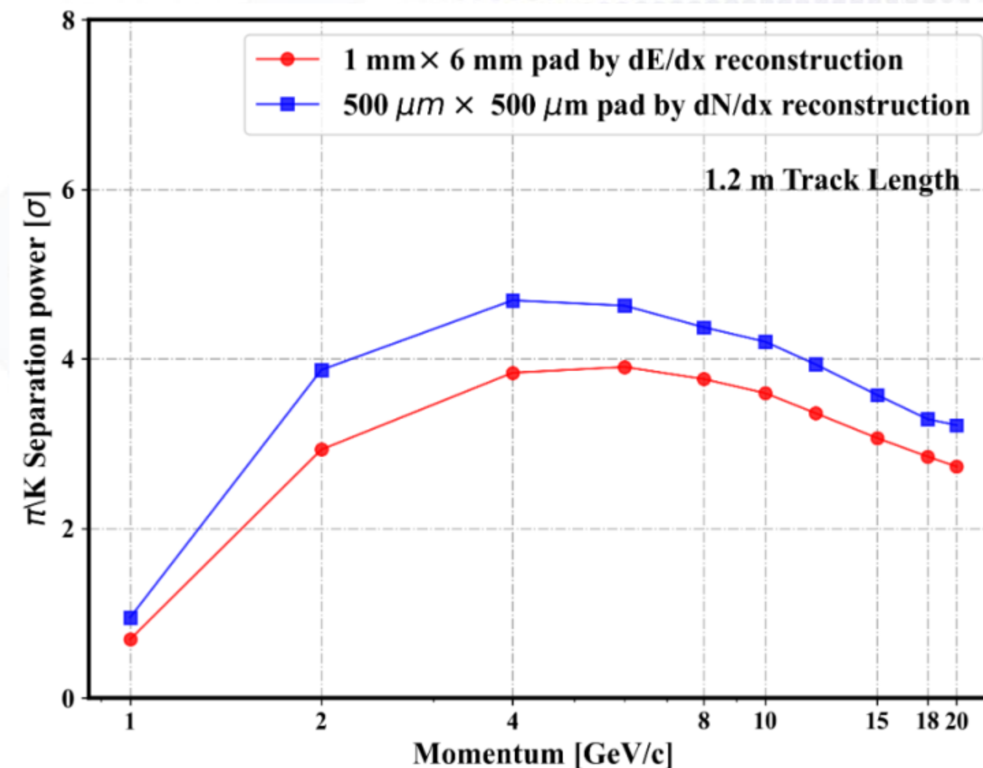


Why pixel TPC for CEPC

- CEPC: **10-year Higgs → 2-year Z pole → 1-year W**
- **High rate** @ Z-pole: small pixel readout
- Better **PID** requirement: ~3% → dN/dx

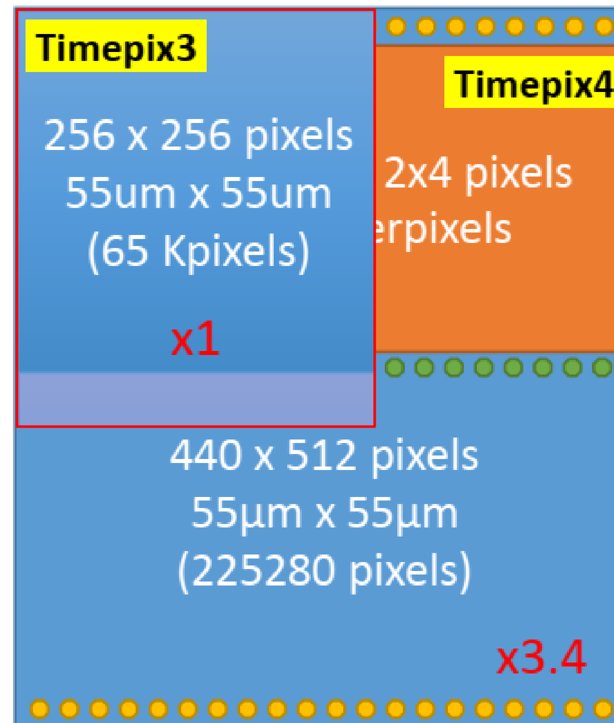


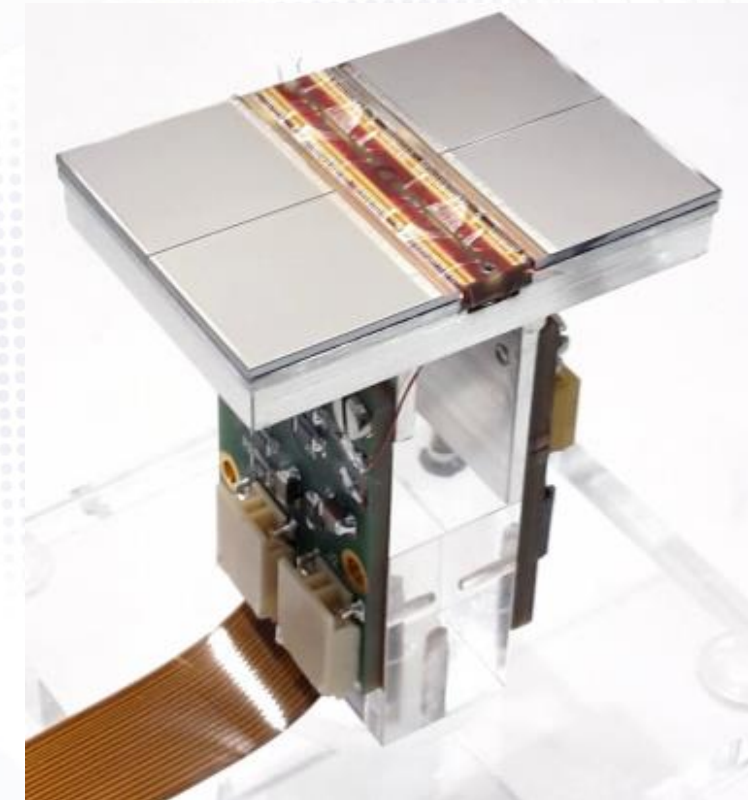




Current Pixel TPC: Gridpix

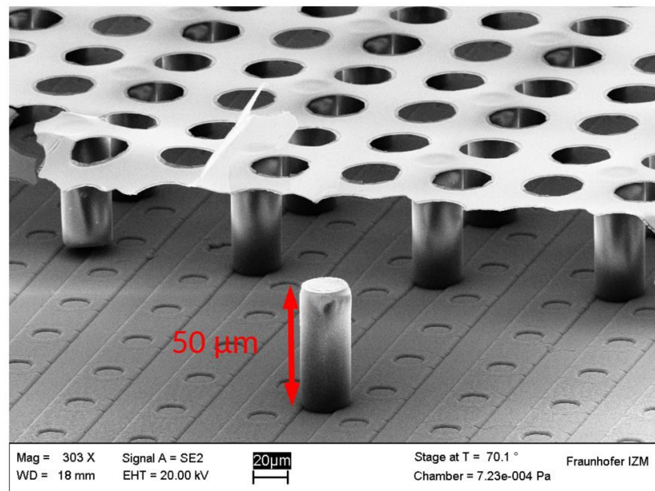
- More than **10 years** development
- Direct readout with a pixel ASIC, e.g., **TPX3**
  - Number of pixels: 256 x 256
  - Pixel pitch: 55 um
  - ENC: ~ 60 e
  - ToT and ToA
  - Power: ~**1W/cm2**
- Next version **TPX4**:
  - 3.4 times larger
  - 4-side buttable with TSV
  - Low power mode



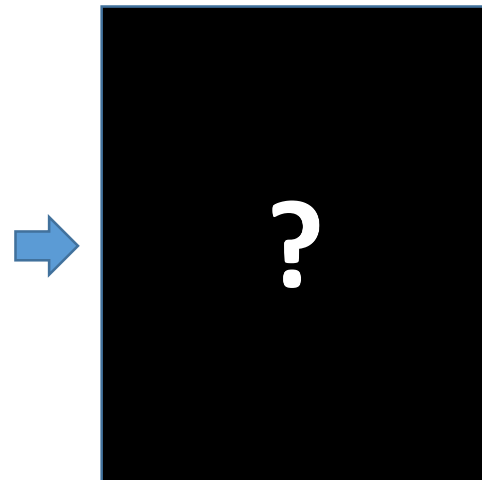


Readout challenging for pixel TPC

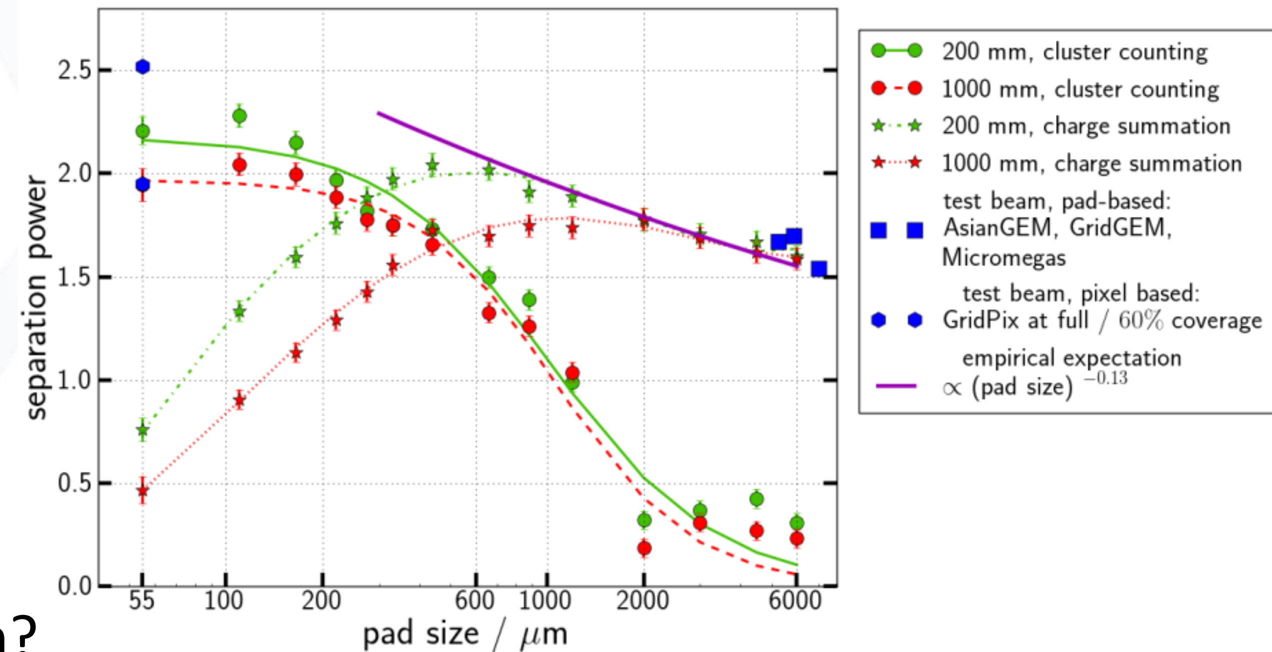
- How to build in large area ~1m^2? Module **scale-up**, **low power consumption**…
- What is the optimum pad/pixel size for CEPC TPC? **200-600um**
- Any other technology for different pixel size with the same chip? **YES**



55um x 55um

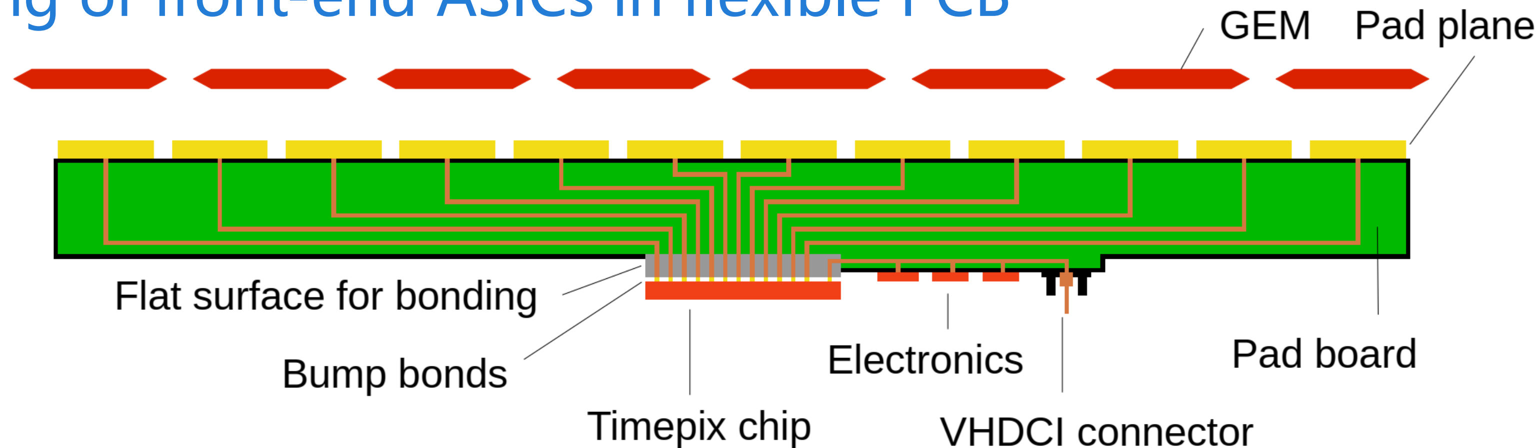


~0.1 mm x ~0.1 mm?



Readout challenging for pixel TPC

- PCB fanout: pad or pixel size limited by its feature size to 700um
- Embedding of front-end ASICs in flexible PCB

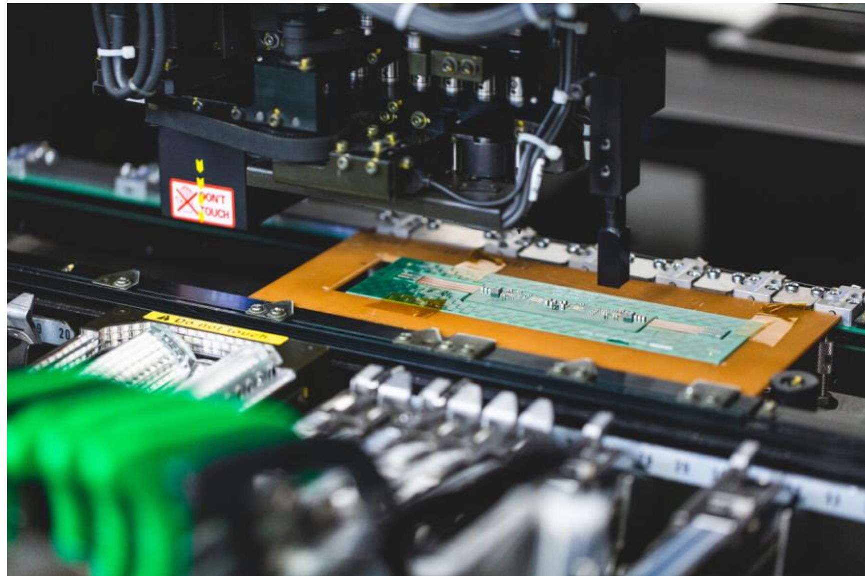


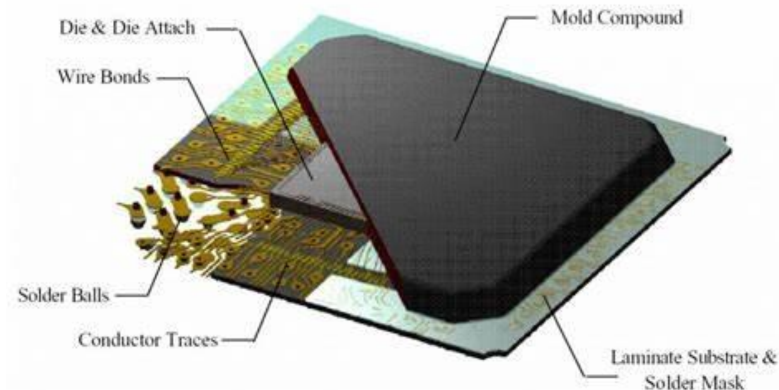
PID with high granularity dE/dx by Ulrich Einhaus, 2020

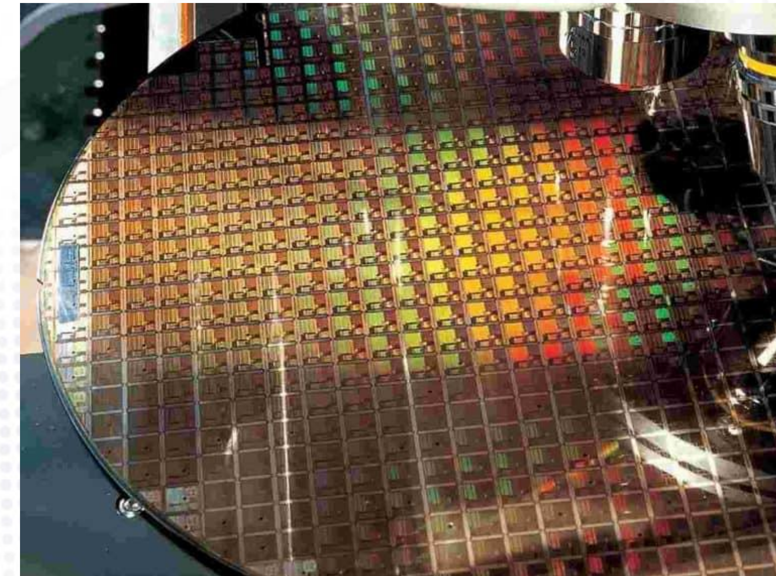
Towards MPGD with embedded pixel ASICs by Lucian Scharenberg, 2024

Readout challenging for pixel TPC

- What we may look for....







High density PCB process
Precision: 100 um
Pads: 10 mm

Chip packaging process
Precision: 1-10 um
Pixels/Pads: 0.1-1 mm

IC process
Precision: 0.1 um
Pixels: ~10 um

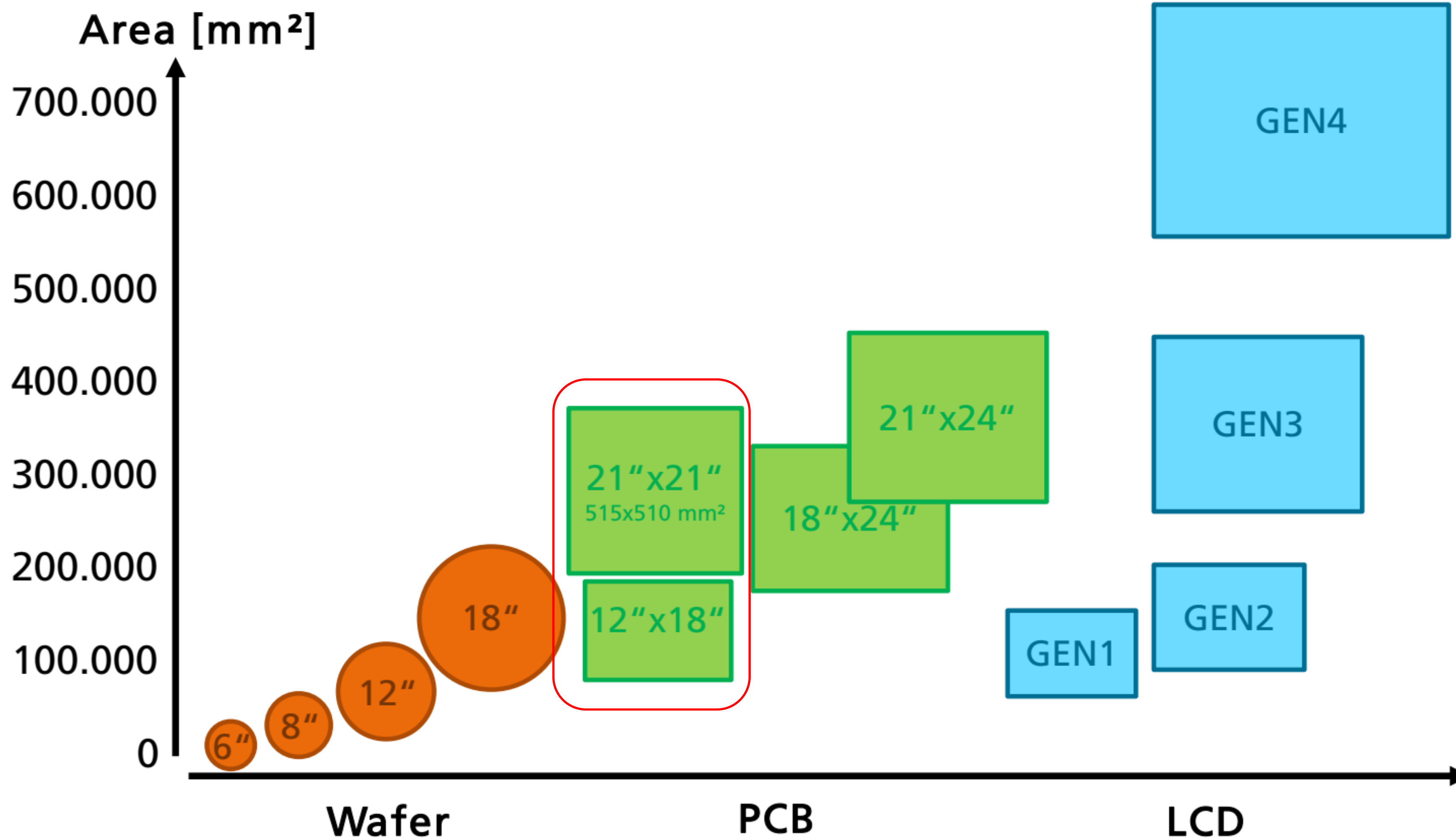
Readout challenging for pixel TPC

清華大学 工程物理系
Department of Engineering Physics, Tsinghua University

➢ Advanced chip packaging technologies

Readout challenging for pixel TPC

➢ Advanced chip packaging technologies

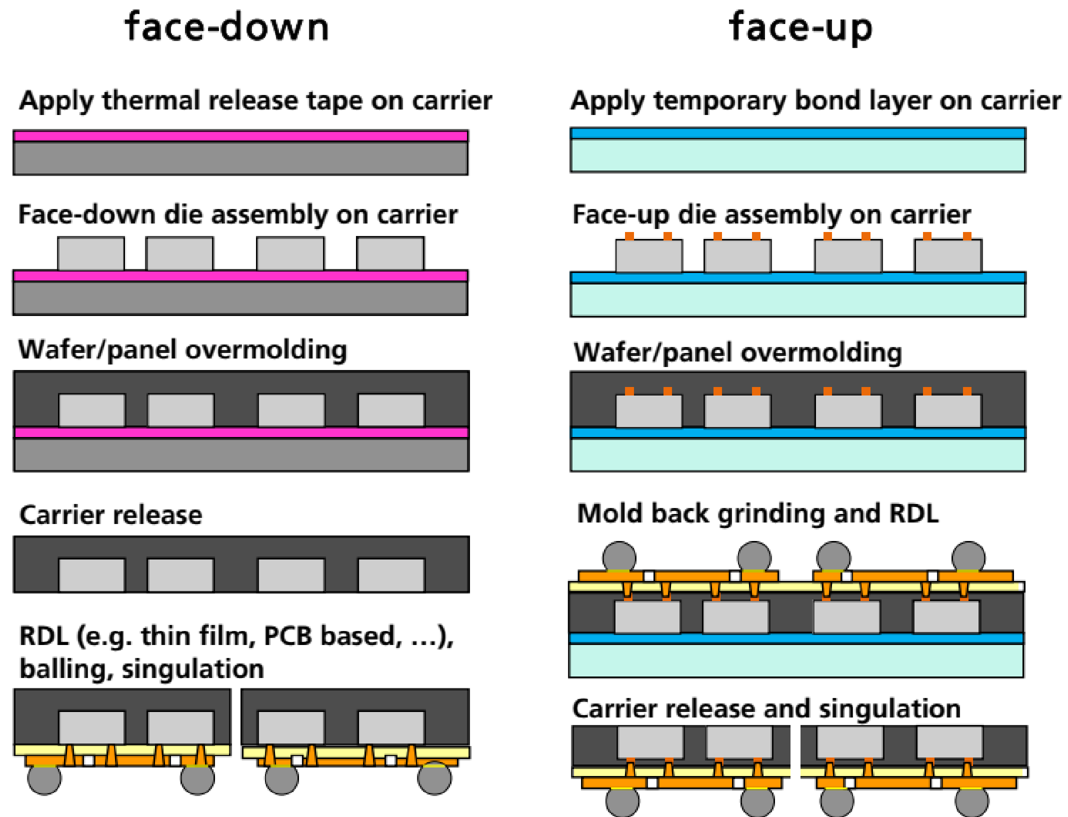


Readout challenging for pixel TPC

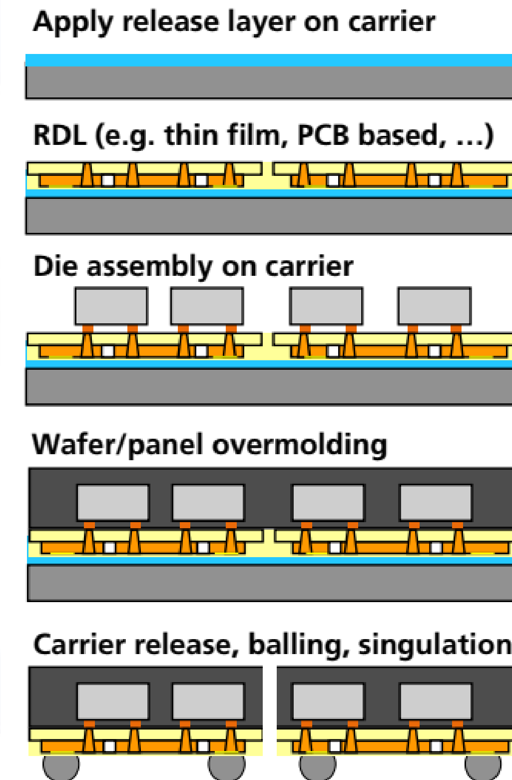
清華大學 工程物理系
Department of Engineering Physics, Tsinghua University

➢ Advanced chip packaging technologies

Chip First



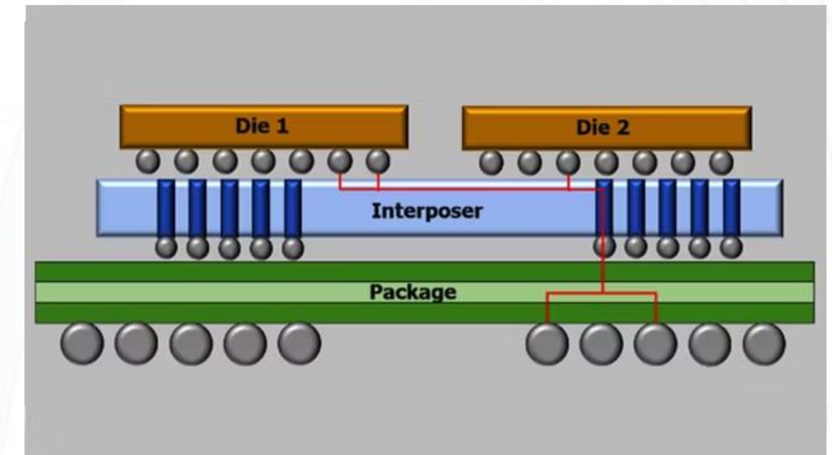
Chip Last

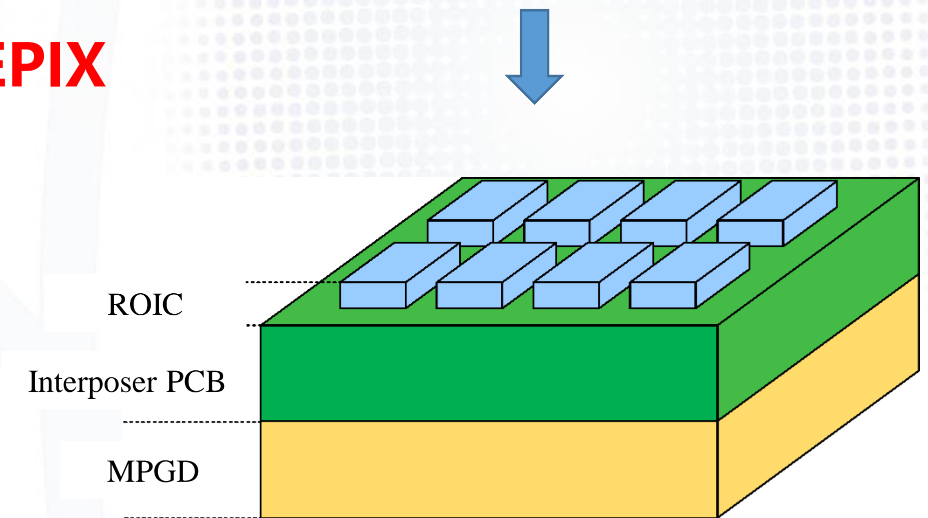


Interposer based pixel TPC

清华大学工程物理系
Department of Engineering Physics, Tsinghua University

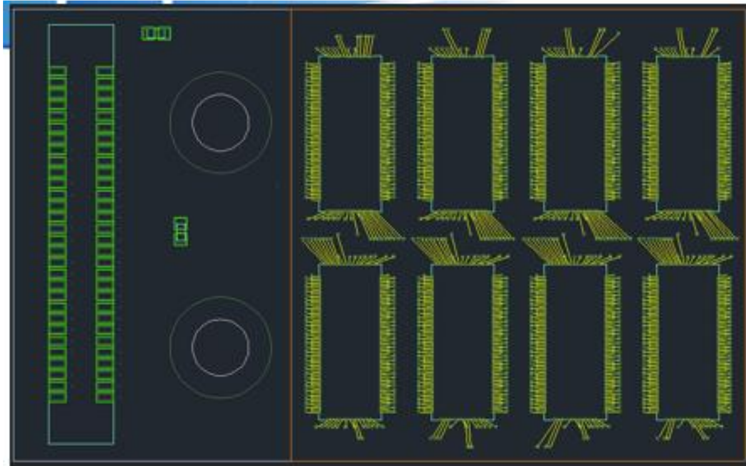
- Pixel readout electronics
  - Multi-ROIC chips + **Interposer** PCB as RDL
  - High metal coverage
  - 3 or 4-side buttable
- Low-power energy/time measurement ASIC： **TEPIX**
  - Low noise: ~100 e noise
  - 5 ns drift time resolution
  - Low power: 100 mW/cm2 (250uW/ch)



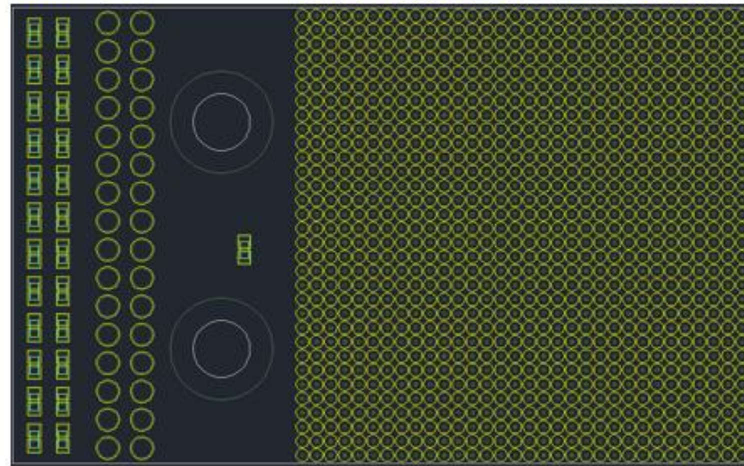


Interposer based pixel TPC

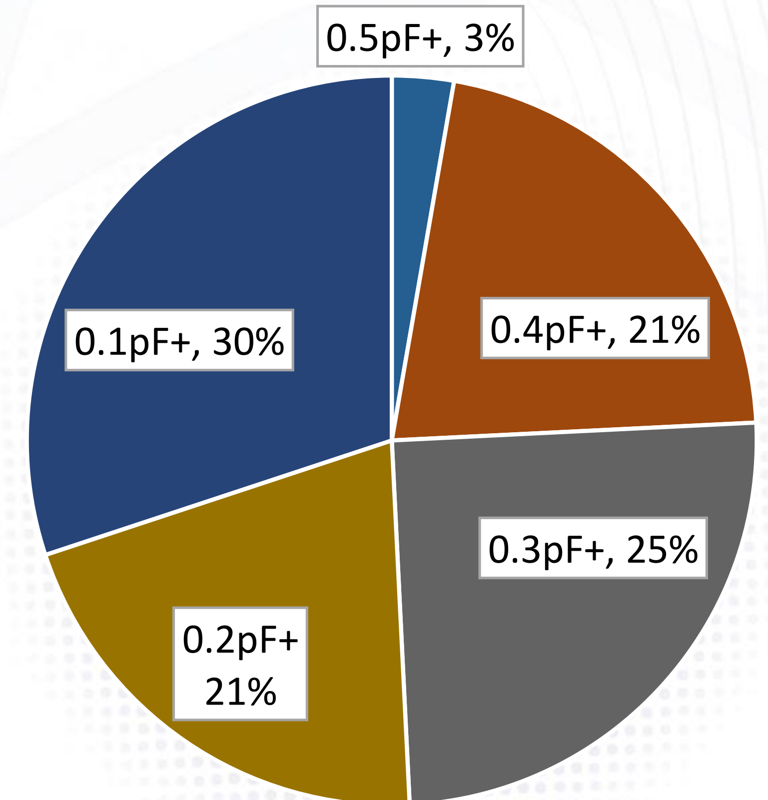
- Interposer design: 3-side buttable
  - **8 TEPIX chips** in one interposer: **32 x 32** pixels
  - L/S: **15 um/15 um**, hole size: **50 um**, 8 layers
  - Parasitic capacitance optimized: **<0.6 pF**



8 TEPIX chips

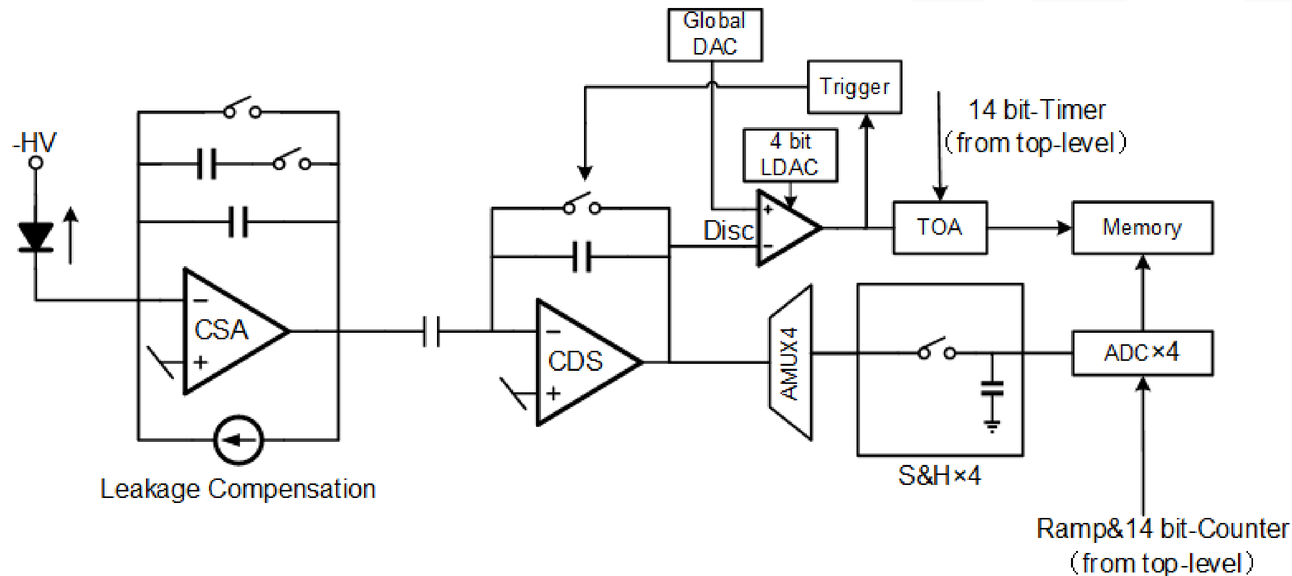


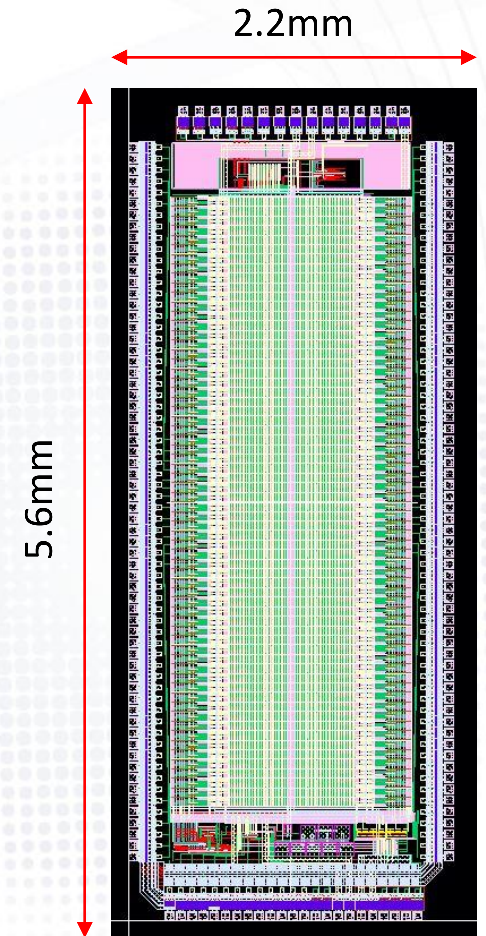
0.5mm x 0.5mm pixels



Readout ASIC: TEPIX

- Block diagram
  - Charge Sensitive Preamplifier(CSA)
  - CDS amplifier provides additional gain and noise shaping
  - Wilkinson type ADC each pixel
  - Timing discriminator with Time of Arrival information





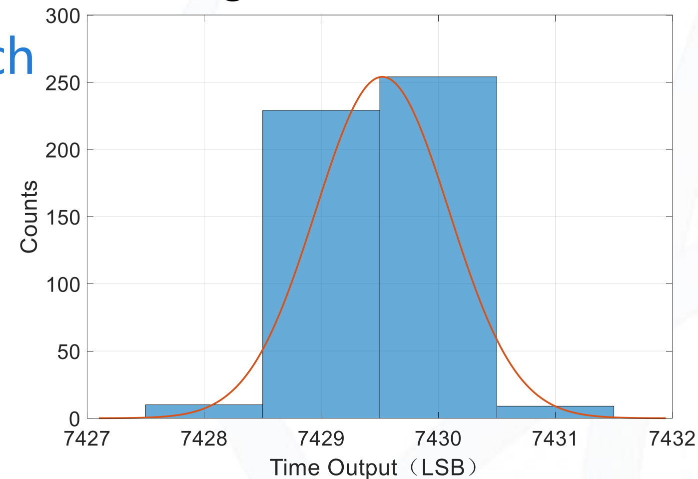
Readout ASIC: TEPIX

清華大学工程物理系
Department of Engineering Physics, Tsinghua University

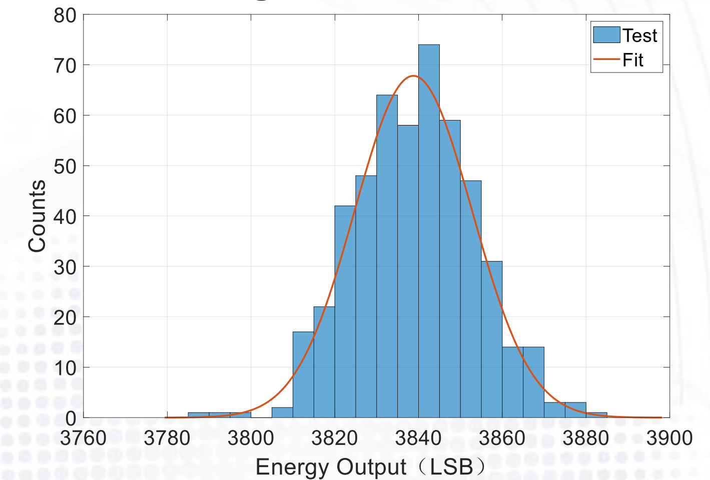
➢ Chip Performance

- ➢ Power Consumption ~ 0.5mW/ch
- ➢ Timing ~ <1LSB(10ns)
- ➢ Noise ~ 300e

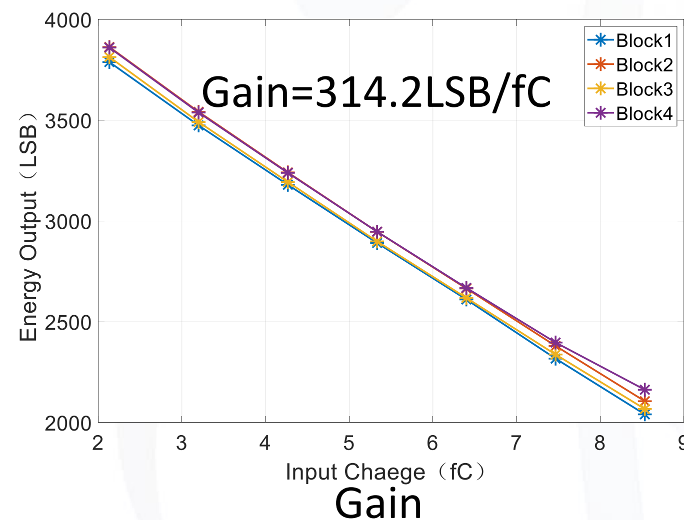
Parameter	Spec
Number of channels	128
Power Consumption	Analog<30mW
	Digital<30mW
ENC	~300 e(high gain)
Dynamic Range	25fC(high gain)
	150fC(low gain)
INL	<1%
Time Resolution	<10ns



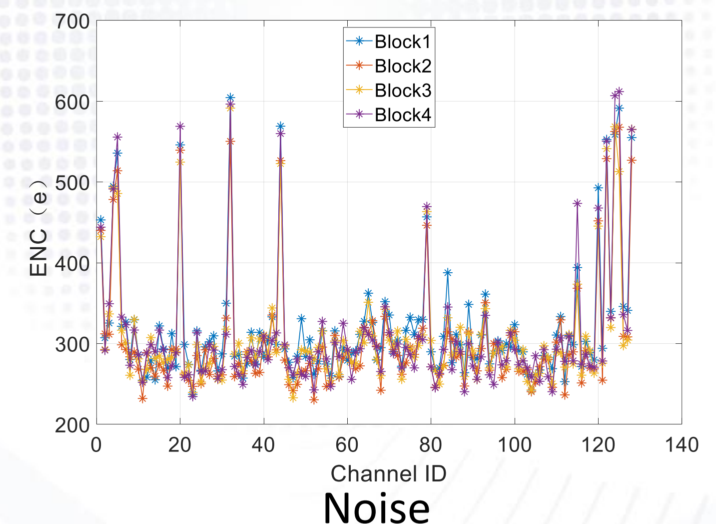
Timing Results



Energy Results



Gain



Noise

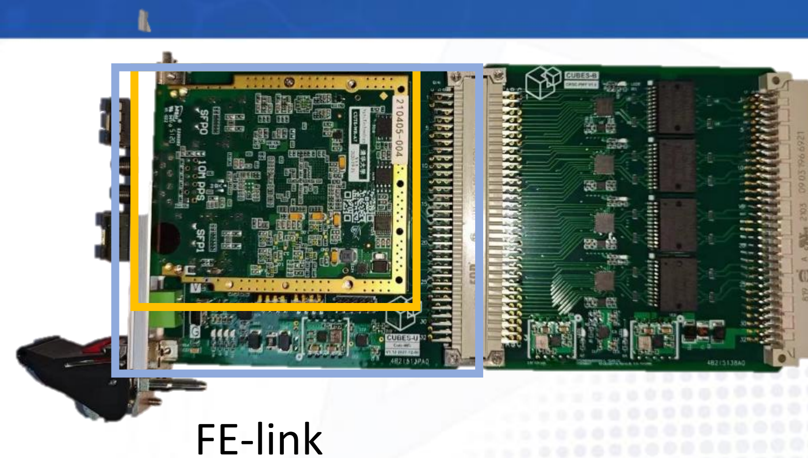
Prototype for beam test

- Pixel size: 0.5mm x 0.5mm pixel
- Pixel number: 5 mm x 150 mm → 10 x 300 channels

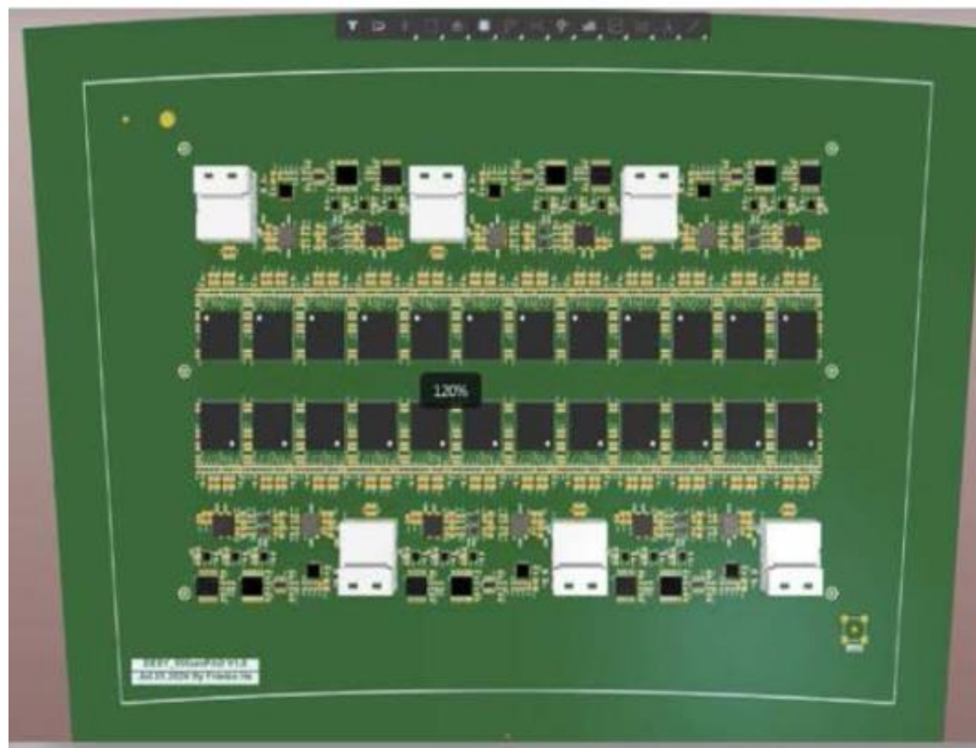
Prototype for beam test

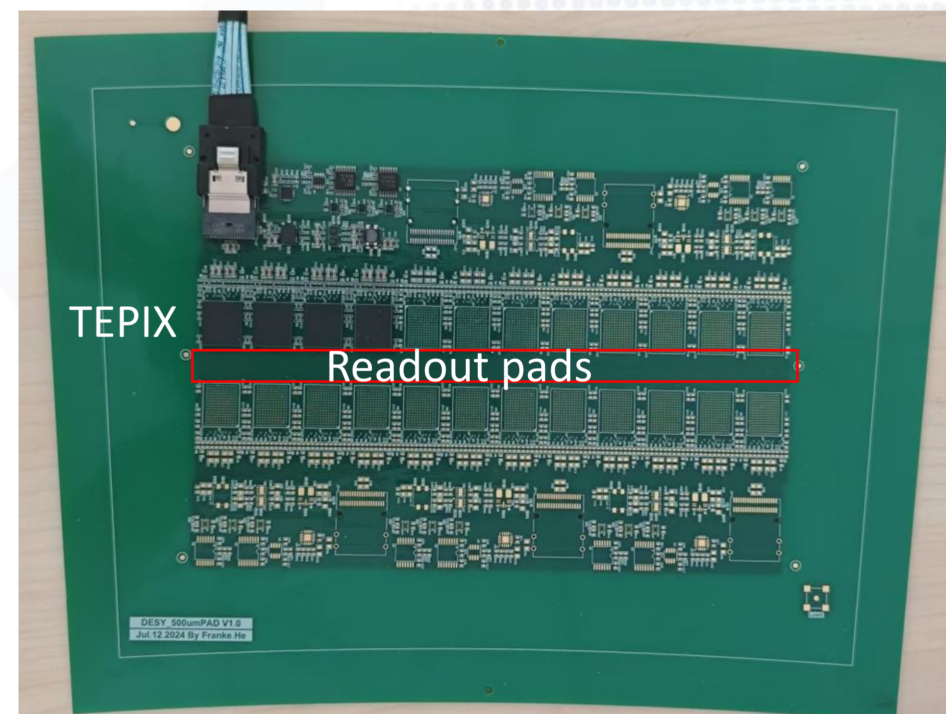
清華大學工程物理系
Department of Engineering Physics, Tsinghua University

- Test board and setup



FE-link





Prototype for beam test

Preliminary test results with calibration signal:

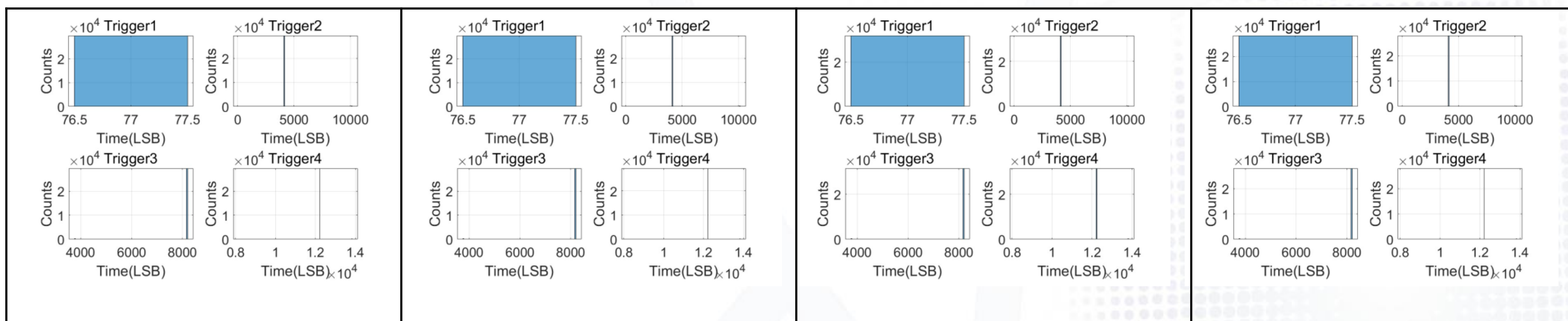
- Charge injected ~6fC;
- 4 triggers, gap between each trigger 40us

Results:

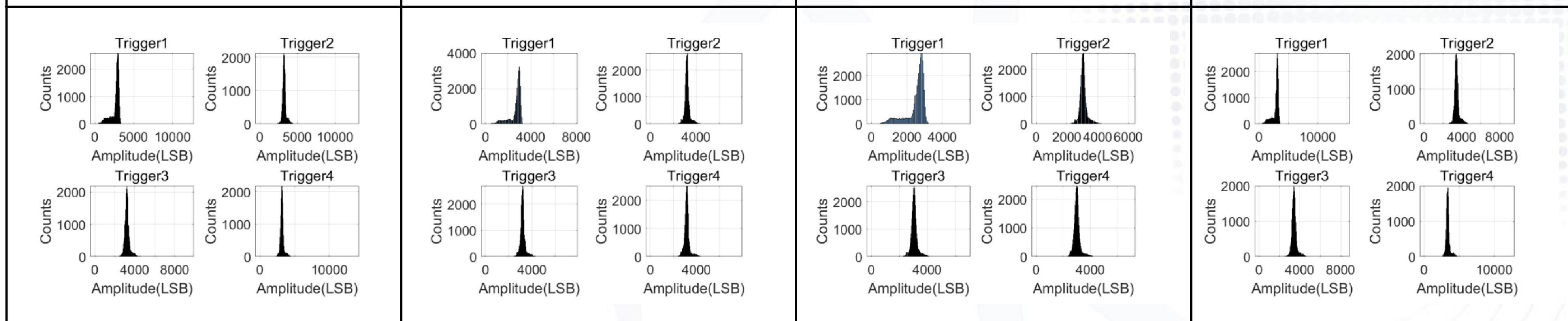
- got expected trigger time.
- got expected energy value according to the charge injected.
- some channels has lower energy of 1st trigger, need further investigation.

Trigger time and energy histogram:

Time:



Energy:



TEPIX1 TEPIX2 TEPIX3 TEPIX4

Summary

- In order to meet the stringent demands on **high rate** and **PID**, **pixel TPC** is essential for CEPC tracking system
- An **interposer based** pixel readout for CEPC TPC has been proposed and a demonstrator of **500um x 500um** pixels was developed, together with a multi-channel readout ASIC – **TEPIX**
- Interposer based pixel readout provides more flexibility, e.g., **pixel size**, **power consumption** etc. And the interposer and ASIC chip can be co-designed or **co-optimized** for the future

THANKS