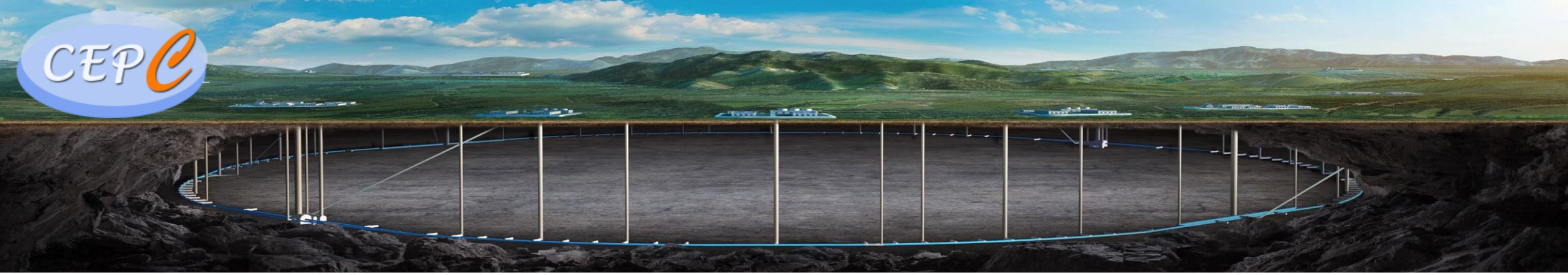

A common project for powering detector front-end electronics

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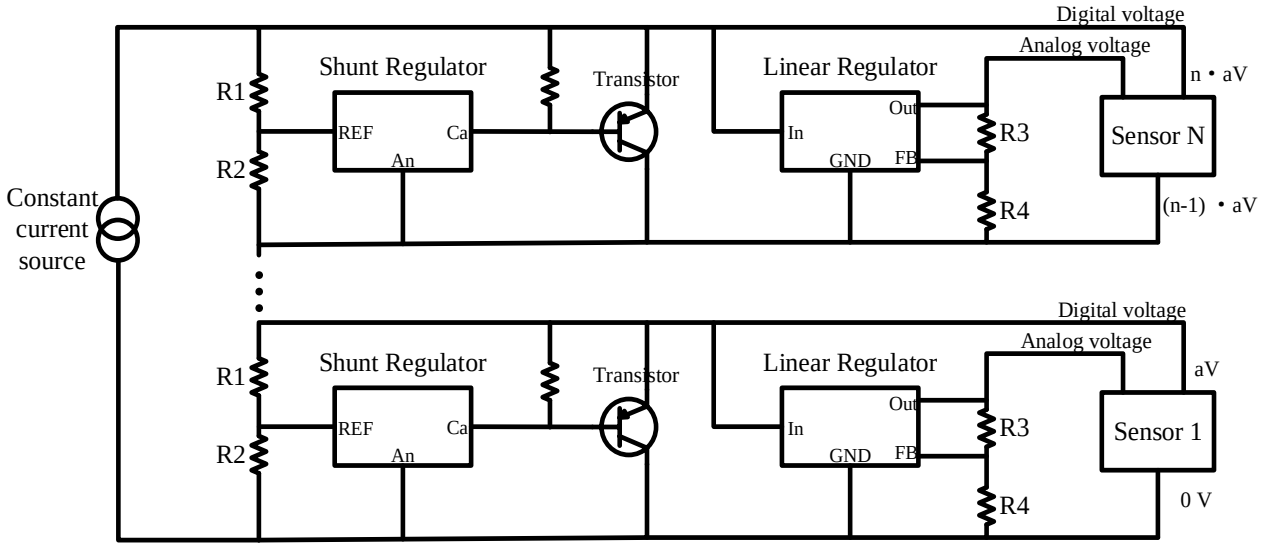
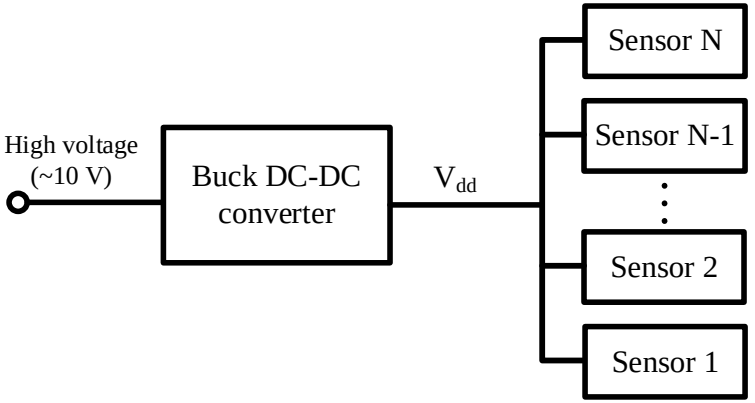
Content

- Introduction
- Preliminary radiation test of GaN transistor
- Measurement results of LDO built-in TaichuPix3
- Structure design of DC/DC buck converter
- Summary and future work

Introduction

- Parallel powering with DC-DC converter VS Serial powering





Serial powering (Backup)

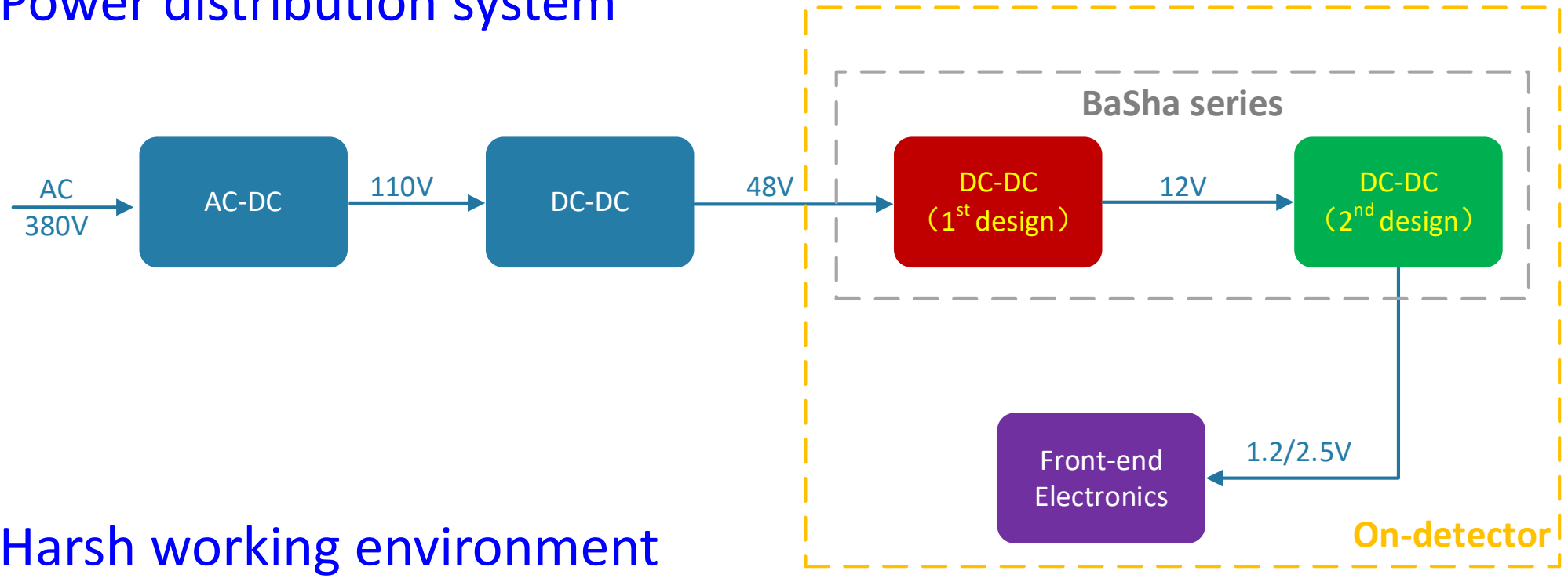
- ✓ Less cable mass
- ✓ Higher power efficiency, more suitable for large current load
- ✓ Low noise
- ✓ Unrequired Magnetic components
- ✗ Many changes with the old power system
- ✗ Lower reliablity
- ✗ Different groud potential -> AC-coupled output, no suitable for stiching chips, very high bias voltage of sensors
- ✗ “Larger” threshold current required to switch on shunt regulator
- ✗ Consistency of shunt regulator and LDO

Parallel powering (Baseline)

- ✓ Compatible with the conventional power system
- ✓ Few changes of readout circuit or sensor required
- ✓ High reliability
- ✓ Unecessary on-chip regulator-> less die area
- ✗ Noisy ripple voltage
- ✗ Large-area air-core inductor
- ✗ EMI

Introduction

- Power distribution system

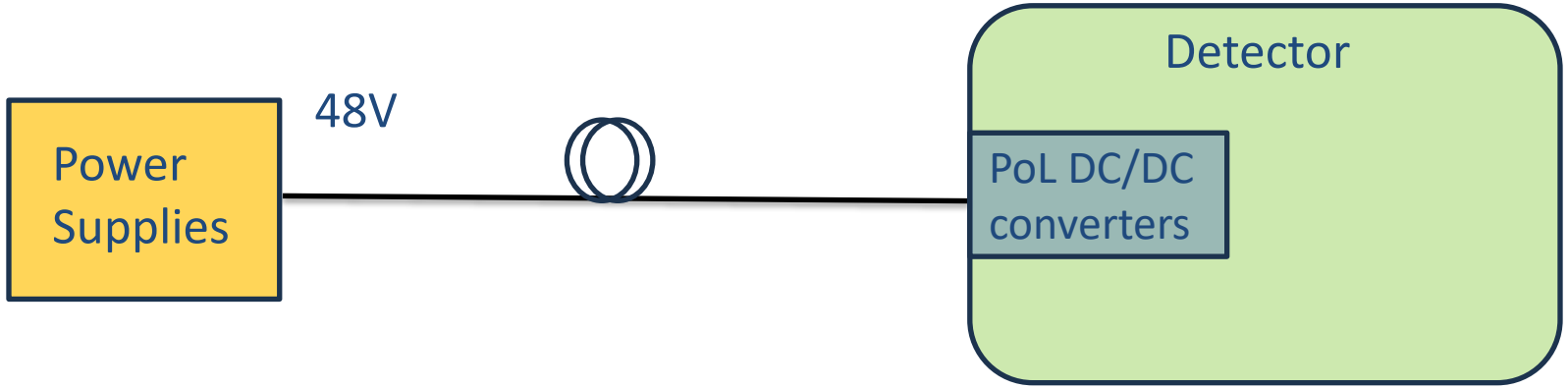


- Harsh working environment
  - ➢ High magnetic field (Up to 3T in CEPC)
  - ➢ High level of radiation will be reached inside the detectors (5 Mrads)

Introduction

Power Distribution System

Point-of-load DC-DC converters are utilized to minimize the losses in the cables and reduce material budget.



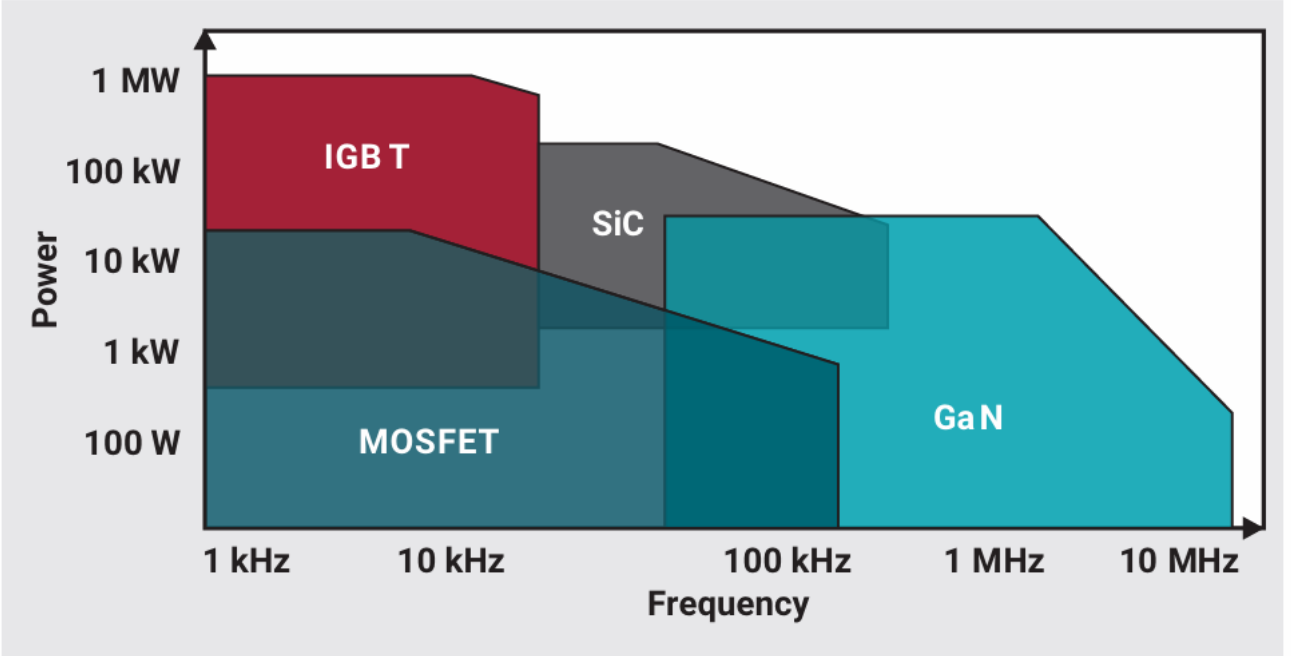
Design Challenges

- Need of high current to power front-end ASICs —> High conversion ratio
- Total Ionizing Dose up to 5Mrad —> Radiation harden design
- Magnetic field up to 3T —> Air core inductors

GaN power transistor

Introduction

- Why GaN(Gallium Nitride) power transistor?
  - Lower size
  - Higher power density
  - Faster switching speed
  - Radiation tolerance



- **Lower On-Resistance (Ron):** Reducing power loss during on-time, which can improve the efficiency of power distribution systems
- **Faster Switching Speed:** Higher operating frequency, which are essential for reducing the size and weight of inductor while maintaining lower ripple voltage.

https://www.ti.com/cn/lit/an/zhct333/zhct333.pdf?ts=1729816468581&ref_url=https%253A%252F%252Fcn.bing.com%252F

Preliminary radiation test of GaN transistor

- Radiation test reulsts of commercial GaN power transistor at CSNS

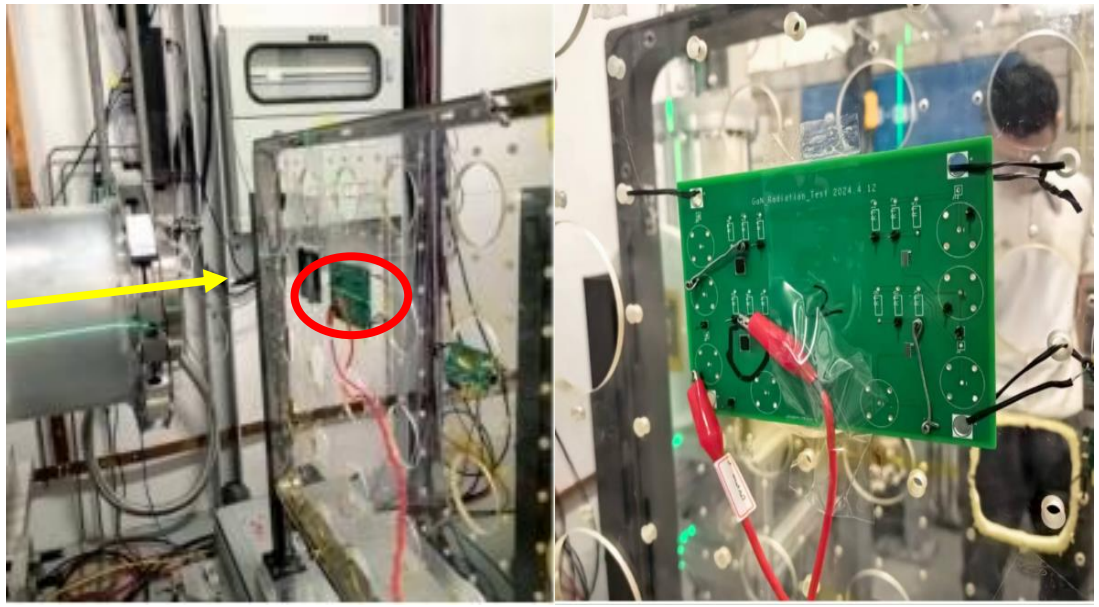
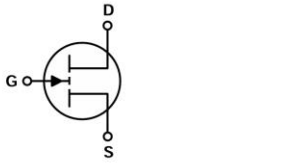
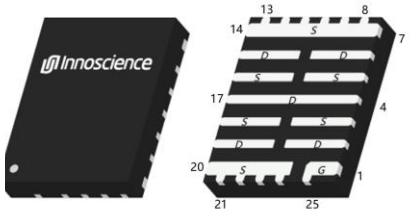


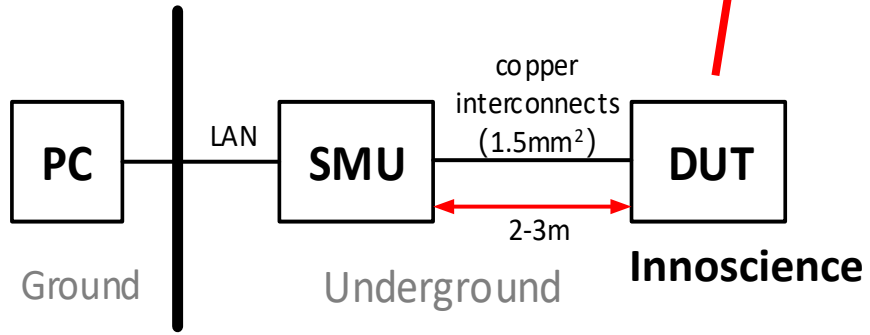
Photo of the PCB fixed to the text platform
(yellow arrow in the left picture is the beam direction)

Parameter	Value	Unit
$V_{DS,max}$	40	V
$R_{DS(on),max}$ @ V_{GS} = 5 V	1.5	mΩ
$Q_{G,typ}$ @ V_{DS} = 20V	28	nC
$I_{DS,Pulse}$	200	A
Q_{OSS}@ V_{DS} = 20V	58	nC





SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Voltage	40			V	V_{GS} = 0 V, I_D = 1.1 mA
I_{DSS}	Drain Source Leakage		0.04	0.9	mA	V_{GS} = 0 V, V_{DS} = 32 V
I_{GSS}	Gate-to-Source Forward Leakage		0.04	0.8	mA	V_{GS} = 5 V
	Gate-to-Source Reverse Leakage		0.04	0.4	mA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage	0.7	1.1	2.3	V	V_{DS} = V_{GS}, I_D = 25 mA
$R_{DS(on)}$	Drain-Source On-state Resistance		1.2	1.5	mΩ	V_{GS} = 5 V, I_D = 15 A
V_{SD}	Source-Drain Forward Voltage		1.25		V	I_S = 0.5 A, V_{GS} = 0 V

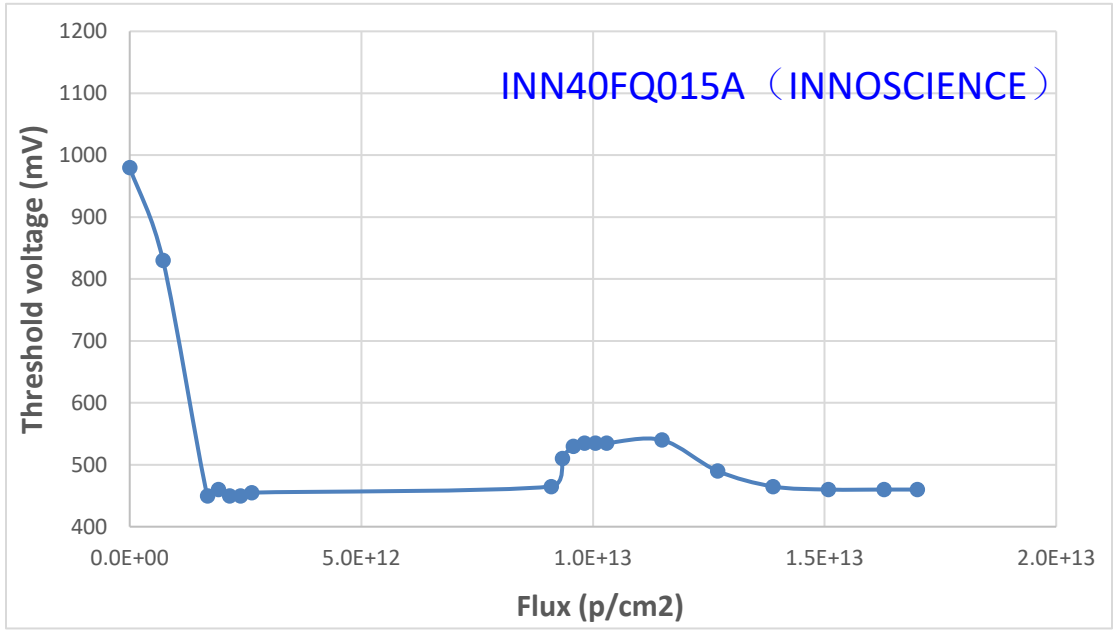


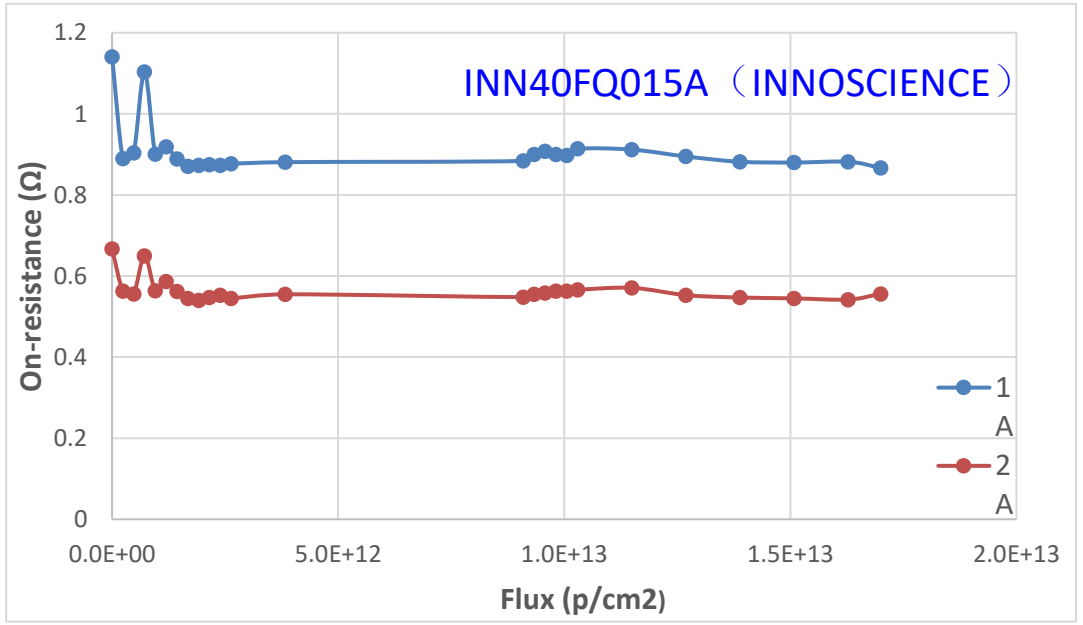
Schematic of the online irradiation testing

Special thanks to the suport of China Spall Neutron Source

Preliminary radiation test of GaN transistor

Radiation test reulsts

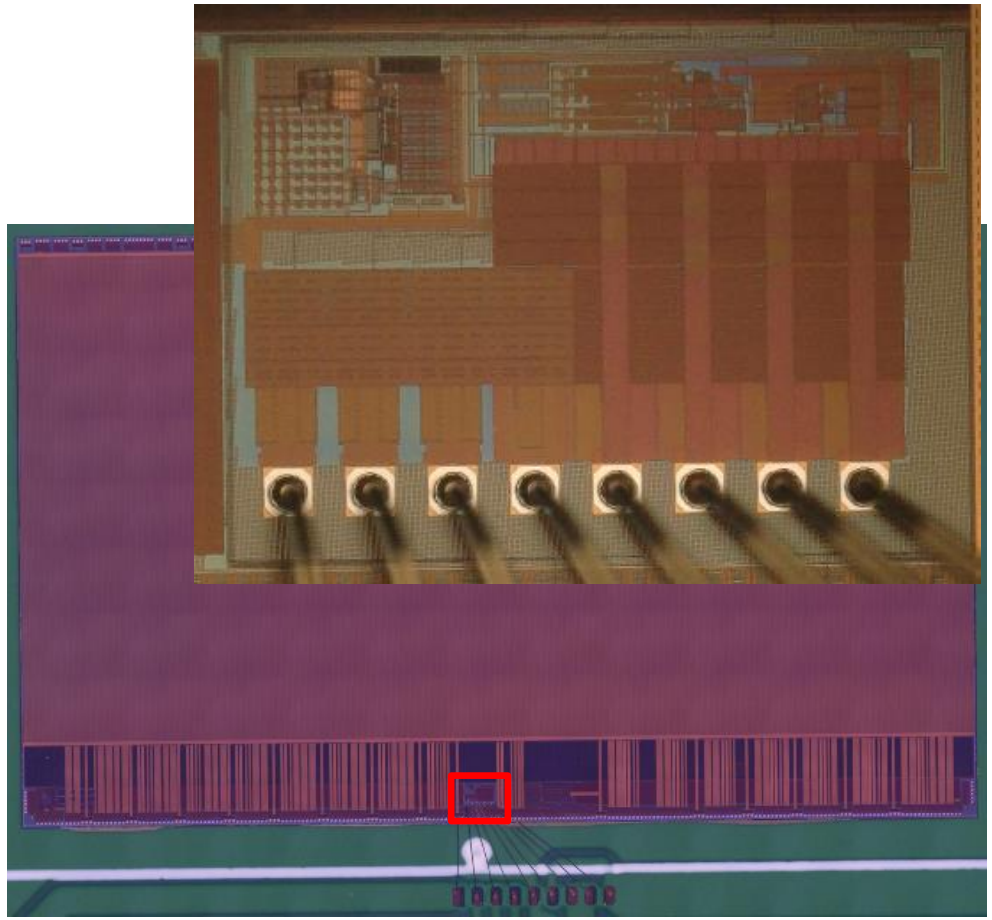


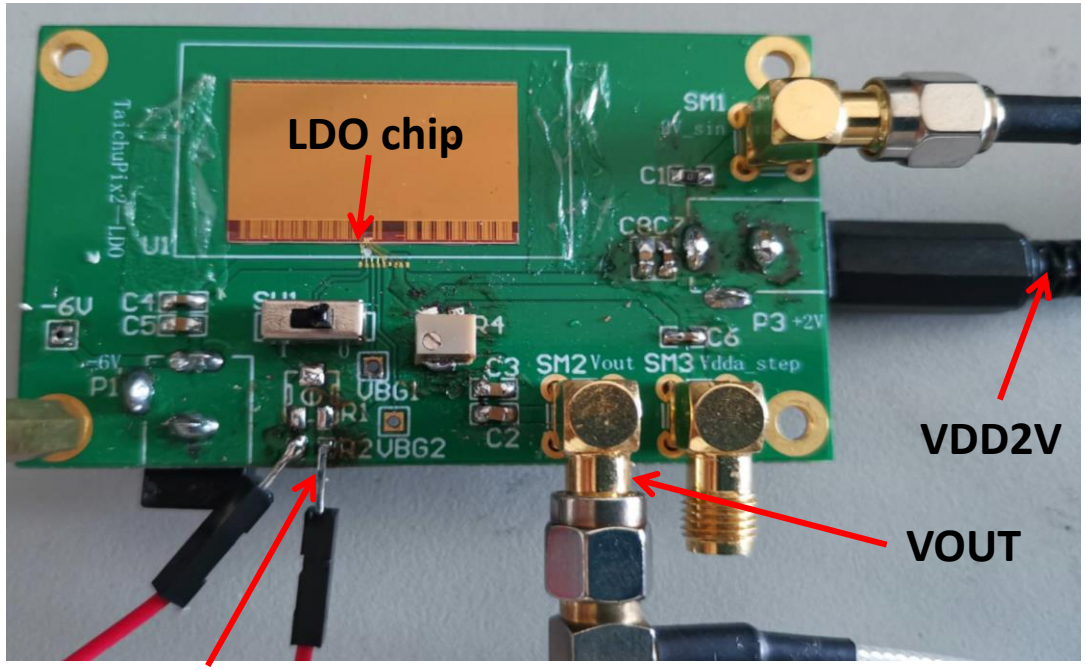


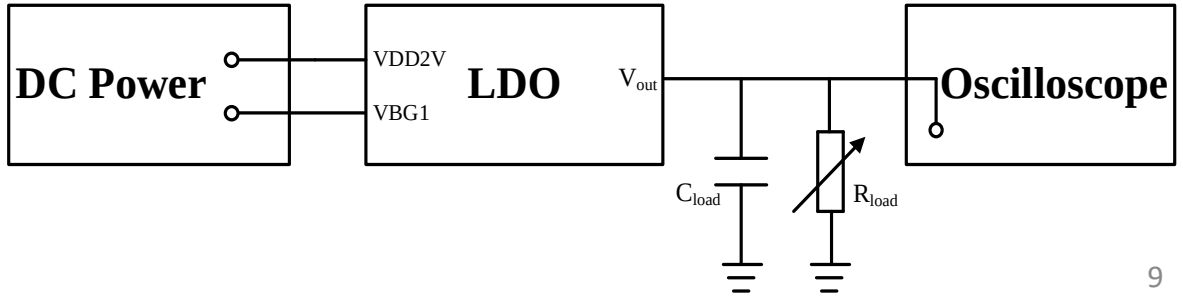
- The threshold voltage of measured transistor decreases to 0.45V when the proton beam is opened with energy of 80MeV.
- The on-resistance of measured transistor decreases to 0.9Ω and 0.55Ω at 1A and 2A currents, respectively.
- Both can be stable till the fulx increases to 1.7×10^{13} p/cm^2.

Measurement results of LDO built-in TaichuPix3

- Micro-photo of chip and measuring setup

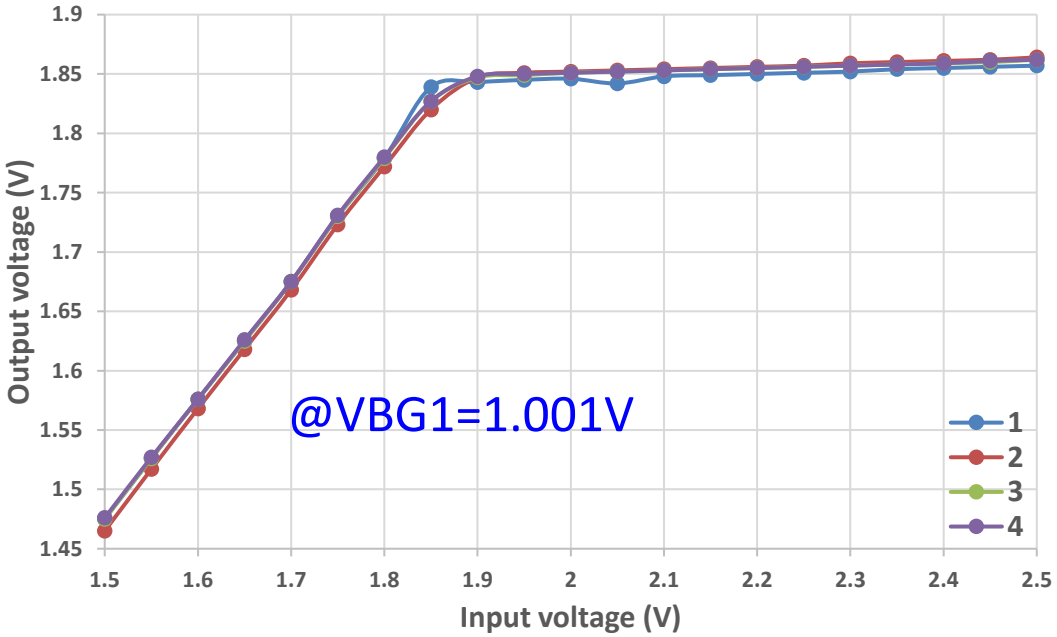




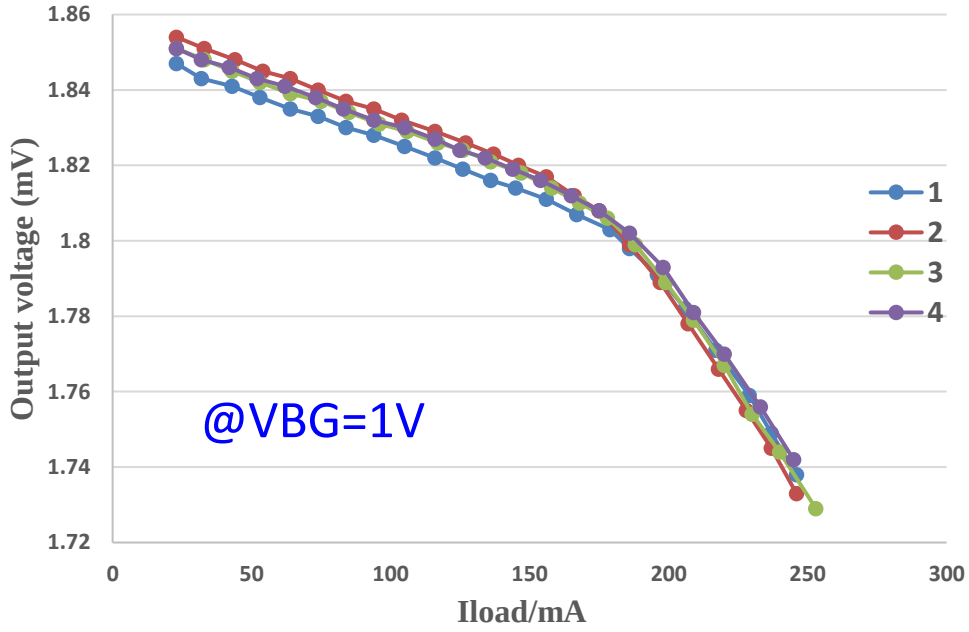


Measurement results of LDO built-in TaichuPix3

- Line regulation and load regulation (4 chips) **external VBG**



1：24.3mV/V (1.9~2.5V)
2：24.8mV/V (1.9~2.5V)
3：22.5mV/V (1.9~2.5V)
4：21.9mV/V (1.9~2.5V)



1：0.282mV/mA (23~179mA)
2：0.294mV/mA (23~166mA)
3：0.283mV/mA (23~168mA)
4：0.283mV/mA (23~175mA)

The chips are still being tested.

Structure design of DC/DC buck converter

- Design specification of the DC/DC converter

Parameter	Value
Input voltage	36-48 V
Output voltage	1.2 V, 2.5 V
Output current	<10 A
Output ripple voltage	<10 mV
power efficiency	85%
Power module size	<50x20x6.7mm^3
TID	5 Mrad
Magnetic field	3T

Structure design of DC/DC buck converter

- Comparison of the loop control methods

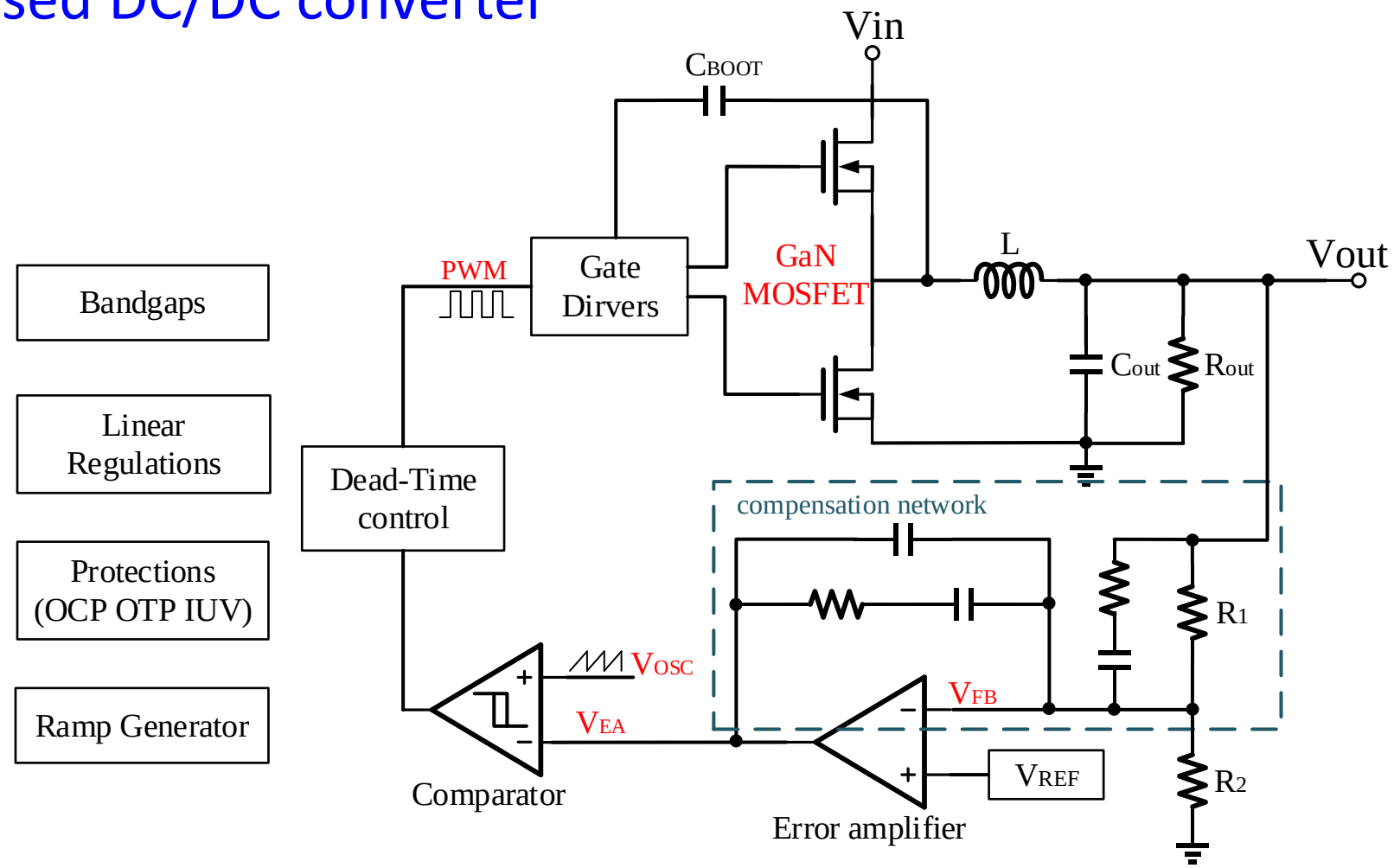
Control type	Transient Response Speed	Noise	Output Voltage Accuracy	EMI	Ripple voltage	Complexity
Voltage PWM	×	√	√	√		√
Current PWM	√	×				
Hysteresis				√	×	√
RBCOT	√			×		
V^2COT	√		√	√		×

Structure design of DC/DC buck converter

- Structure of the proposed DC/DC converter

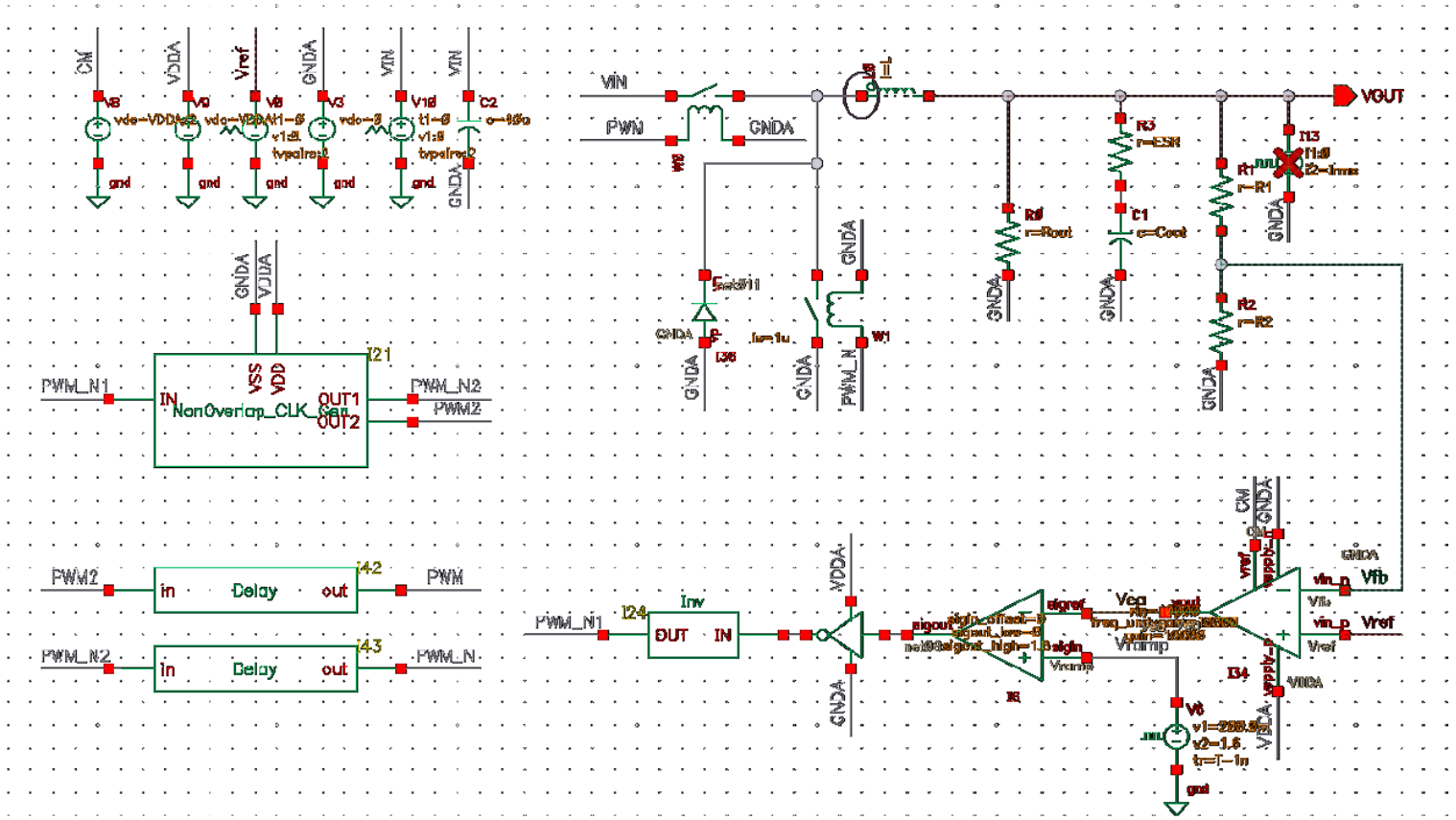
Main circuit blocks

- Air Inductor
- GaN Power FET
- Gate Driver
- Bandgap and LDO
- Error Amplifier
- PWM Comparator
- Level Shifters
- Dead Time Controlling



System design and simulation

- Voltage-Mode PWM DC-DC Converter

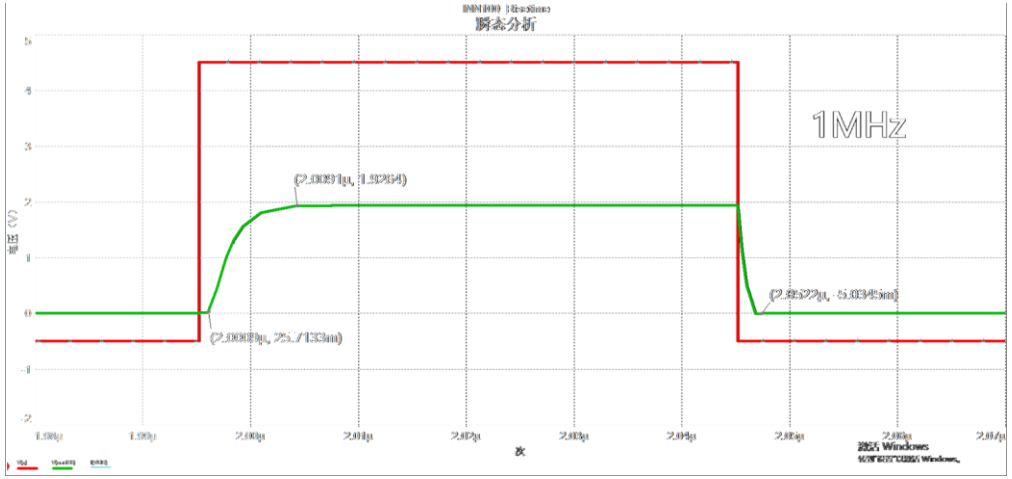


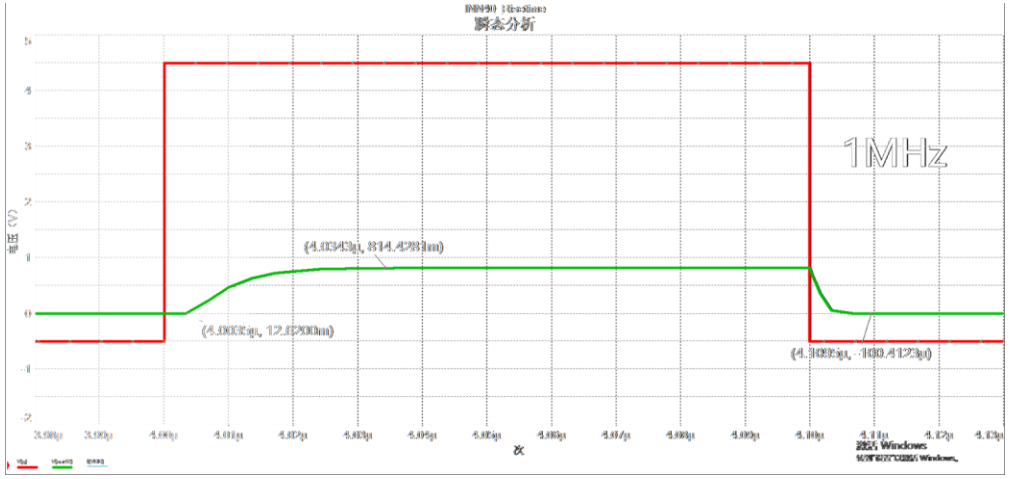
Loop delay = OPA delay + Driver propagation delay + MOSFET ON-delay

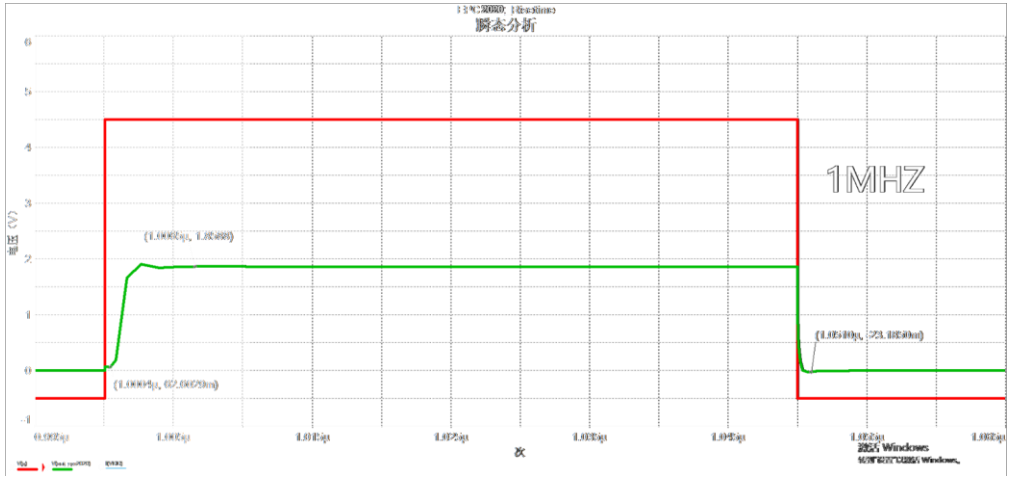
Limited by the loop delay, if the conduction time is less than the loop delay, the loop will be too late to respond, resulting in loop instability

System design and simulation

- Simulation of setup time of Innoscience and EPC GaN







Simulation result with Pspice model of GaN @1MHZ

Table II: Dynamic parameter simulation results

	Input delay	Risetime	Falltime
EPC2020	<1ns	65ns@1MHz 95ns@5MHz	10ns
✗ INN40	3ns	30ns@1MHz 34ns@5MHz	2ns
INN100	1ns	8ns@1MHz 12ns@5MHz	7ns

System design and simulation

- Delay time of GaN

UCC27611	Texas Instruments	4 A/6 A高速5 V、优化的单栅极驱动器				EPC9081
t_{D1}	Turnon propagation delay(1)	C_{LOAD} = 1 nF,	N = 0 V to 5 V		14	25	ns
t_{D2}	Turnoff propagation delay(1)	C_{LOAD} = 1 nF,	N = 5 V to 0 V		14	25	ns

uP1964	uPI Semiconductor	增强型氮化镓场效应晶体管的单通道栅极驱动器					
Rising Propagation Delay Time	T_{PDHLG}	V_{CC} = 5V @load=1nF	--	20	25	ns
Falling Propagation Delay Time	T_{PDLLG}	V_{CC} = 5V	--	20	25	ns

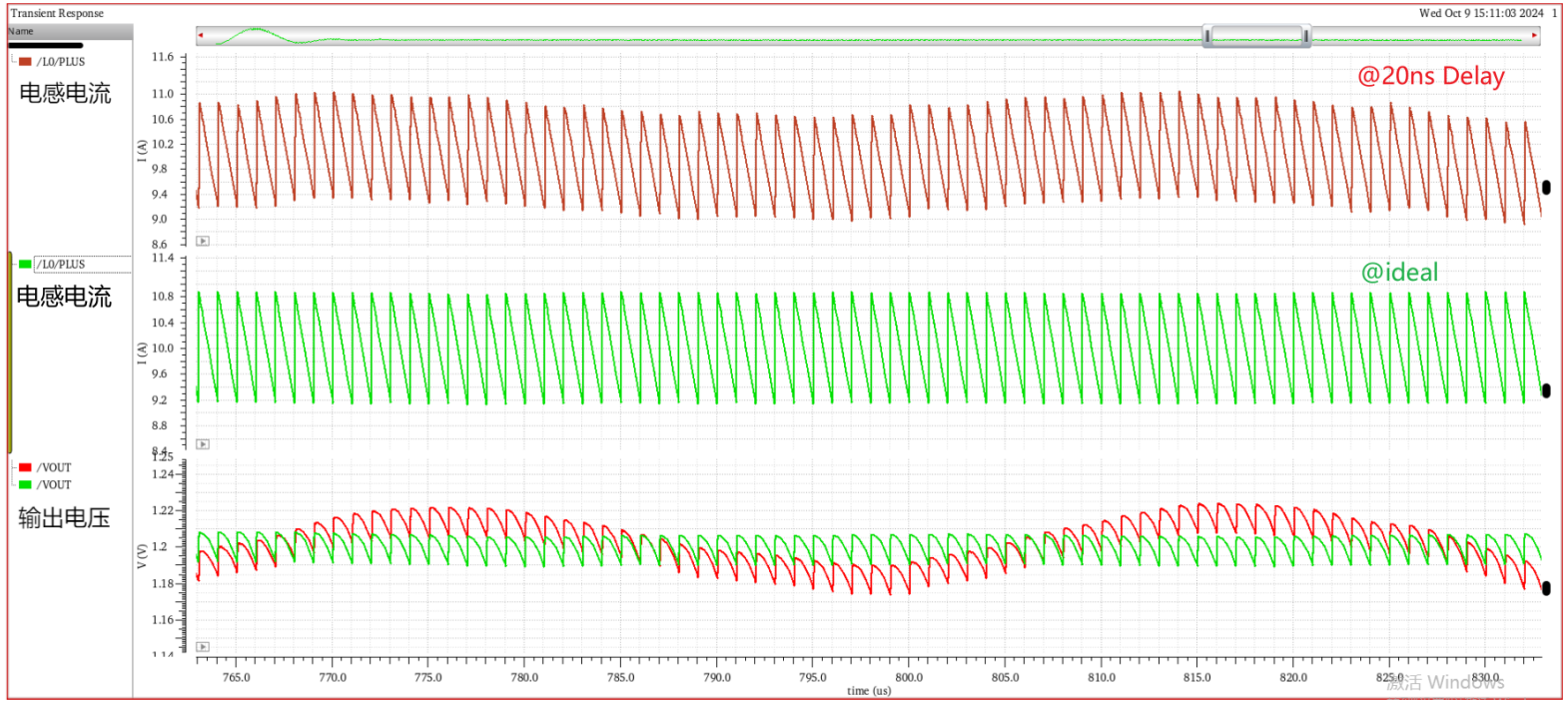
LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-ns Pulse Width Applications

$t_{pd, r}$	Propagation delay, turn on	IN- = 0 V, IN+ to OUTH, 100 pF load	1.5	2.5	4.1	ns
$t_{pd, f}$	Propagation delay, turn off	IN- = 0 V, IN+ to OUTL, 100 pF load	1.8	2.6	4.3	ns

https://epc-co.com/epc/products/gan-drivers-and-controllers

System design and simulation

- 48/1.2V 1MHz Ton=25ns



- A delay of 20ns is added to simulate the delay of the controller.
- The responce speed of loop is low and the output voltage oscillates.

On-time of the power transistor cannot be too short.

Summary and working plan

Conclusion

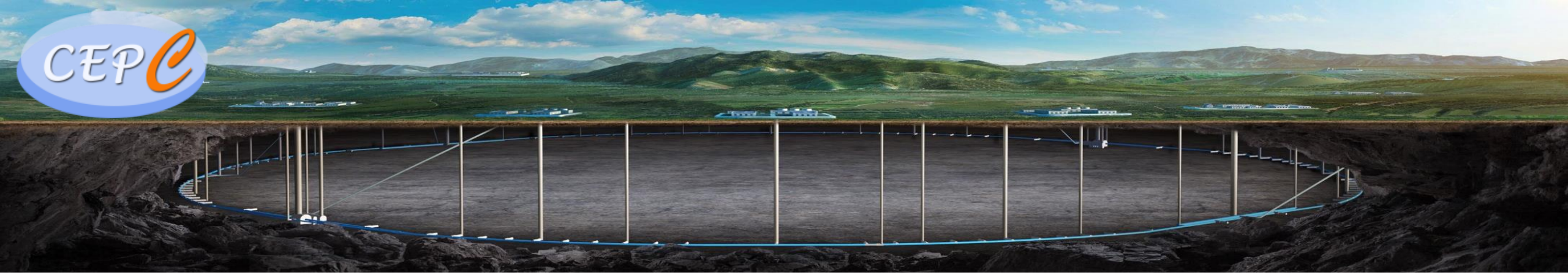
- We chose (conventional) Parallel Powering as the baseline scheme, while consider Serial Powering as the backup scheme.
- Some preliminary radiation tests (GaN MOSFET and LDO) have been completed

  The selected domestic power transistor can ensure no failure in the irradiation environment

  The LDO's test result is promising, and the next step is to improve its radiation tolerance
- The system simulation of the DC/DC converter is completed

Future work

- Design of a DC/DC controller prototype chip
- A functional DC-DC module by 2025
- An radiation tolerant power system(BaSha series) within three years



Thank you for your attention!

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Institute of microelectronics, Northwestern Polytechnical University

System design and simulation

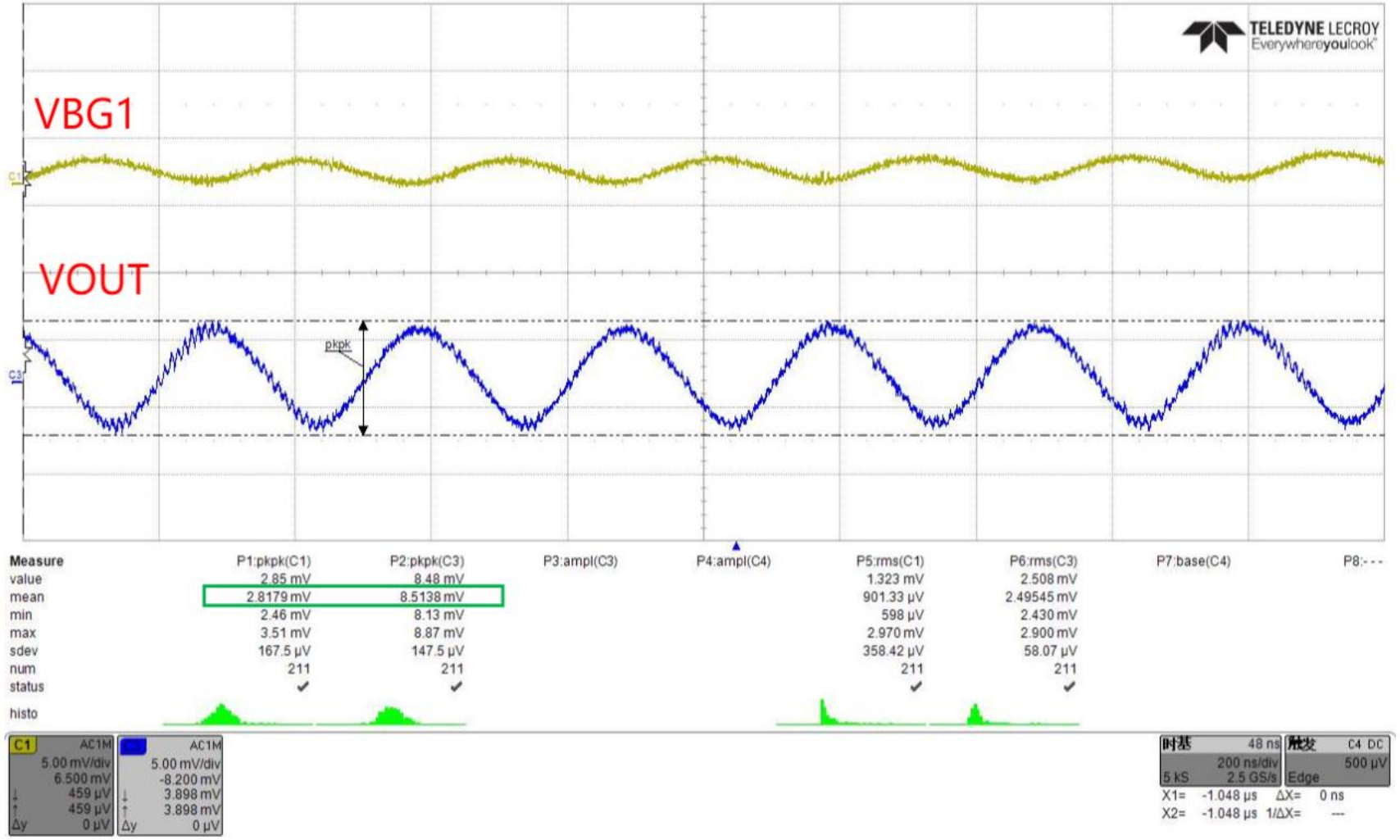
- GaN MOSFET research results

	VDS (MAX)	VGS (MAX)	RDS(on)(mΩ) (MAX)@5VGS	QG(nC) (TYPE)	ID (A)	Pulse Current ID (A)	Package(mm)
EPC2031	60	6	2.6	16	48	450	BGA 4.6 x 2.6
EPC2020	60	6	2.2	16	90	470	LGA 6.05 x 2.3
EPC2202	80	5.75	17	3.2	18	75	LGA 2.1 x 1.6
EPC2204A	80	6	6	5.7	29	125	LGA 2.5 x 1.5
EPC2065	80	6	3.6	9.4	60	215	LGA 3.5 x 1.95
EPC2029	80	6	3.2	13	48	360	BGA 4.6 x 2.6
EPC2218A	80	6	3.2	10.5	60	231	LGA 3.5 x 1.95
EPC2021	80	6	2.2	15	90	390	LGA 6.05 x 2.3
EPC2206	80	6	2.2	15	90	390	LGA 6.05 x 2.3
EPC2016C	100	6	16	3.4	18	75	LGA 2.1 x 1.6
EPC2212	100	6	13.5	3.2	18	75	LGA 2.1 x 1.6
EPC2045	100	6	7	6	16	130	BGA 2.5 x 1.5
EPC2001C	100	6	7	7.5	36	150	LGA 4.1 x 1.6
EPC2901C_55	100	6	7	6.9	36	150	LGA 4.1 x 1.6
EPC2204	100	6	6	5.7	29	125	LGA 2.5 x 1.5
EPC2619	100	6	4.2	8.5	29	164	LGA 2.5 x 1.5
EPC2053	100	6	3.8	11.4	48	246	BGA 3.5 x 2
INN40	40	6	1.5	28	50	200	
INN100	100	6	2.7	13	64	320	

The power loss decreases with RDS(on), and the power pipe establishment time decreases with QG, while RDS(on) and QG are negatively correlated, which requires a performance compromise in practical selection

Back(1)

- VBG1 and VOUT of TaichuPix2 LDO



Control Loop Analysis and stability

Voltage-Mode PWM DC-DC Converter

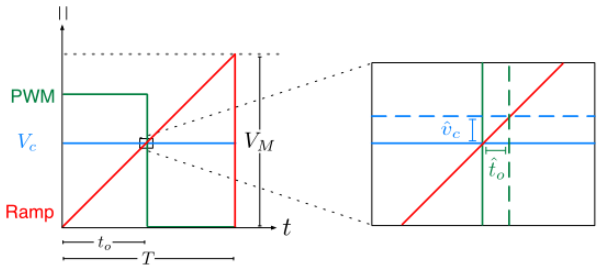
Barkhausen's criterion: the phase shift does not exceed -180° for an open-loop gain of 1

Power-stage transfer function：

$$G_P(s)=\frac{V_{out}}{d}(s)=\frac{R_{Load}(C_o\cdot ESR\cdot s+1)}{L_oC_o\cdot s^2(R_{Load}+ESR)+s\cdot(L_o+R_{Load}\cdot C_o\cdot ESR)+R_{Load}}\times V_{in}$$

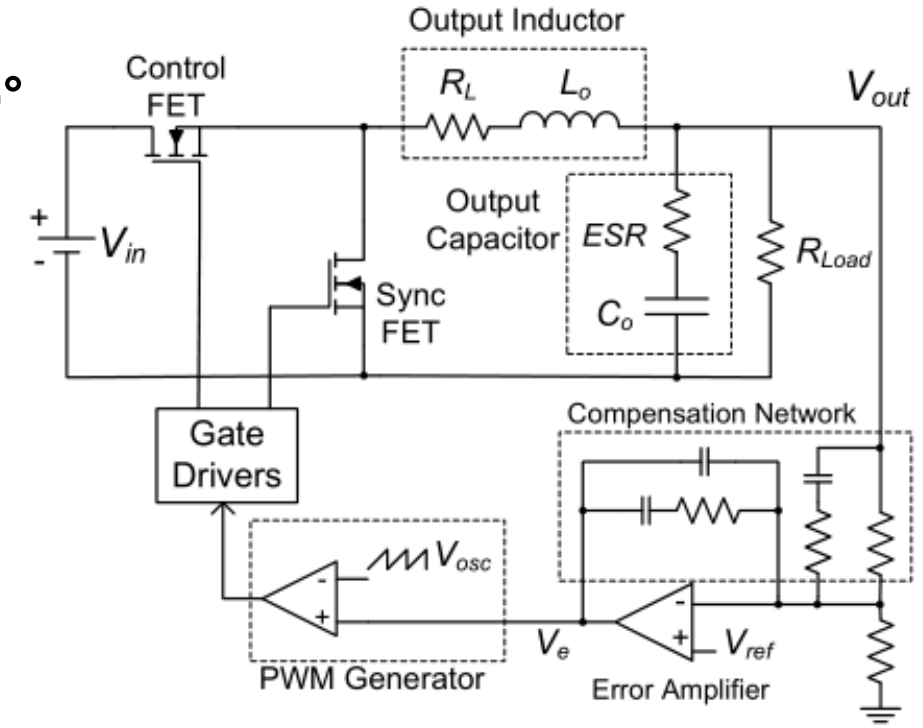
—>double pole

$$G(s)=G_P(s)\cdot\frac{1}{V_{osc}}$$



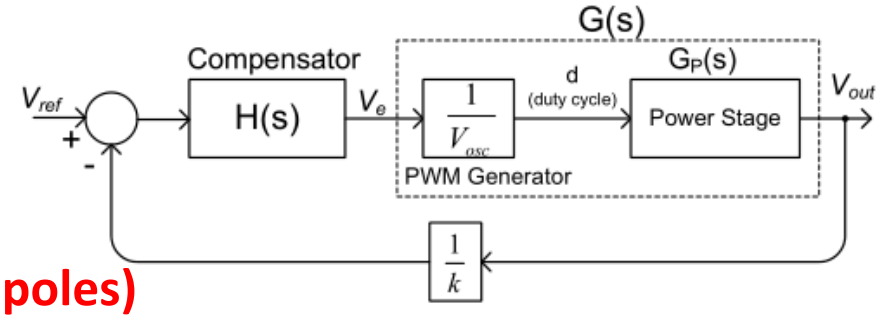
$$\frac{V_M}{T}=\frac{\hat{v}_c}{\hat{t}_o}$$

$$\frac{\hat{t}_o}{T}\frac{1}{\hat{v}_c}=\frac{\hat{d}}{\hat{v}_c}=\frac{1}{V_M}$$



Open-loop transfer function：

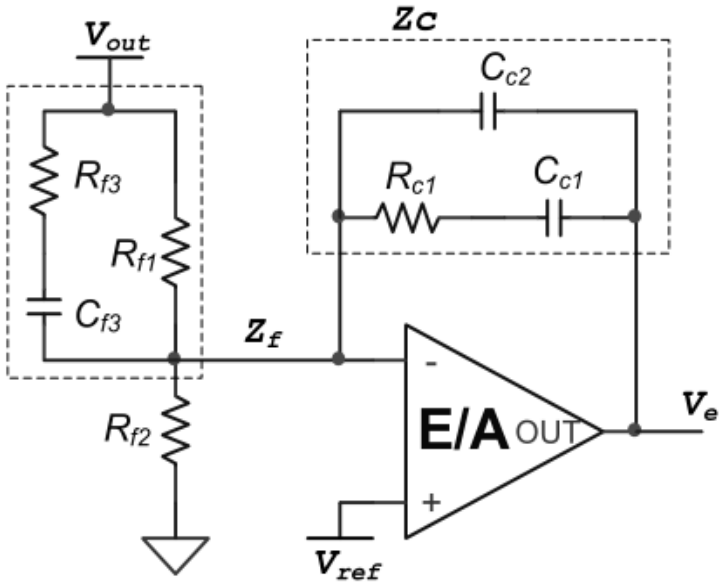
$$M(s)=\frac{1}{k}\times H(s)\times\frac{1}{V_{osc}}\times G_P(s)=\frac{1}{k}\times H(s)\times G(s)$$



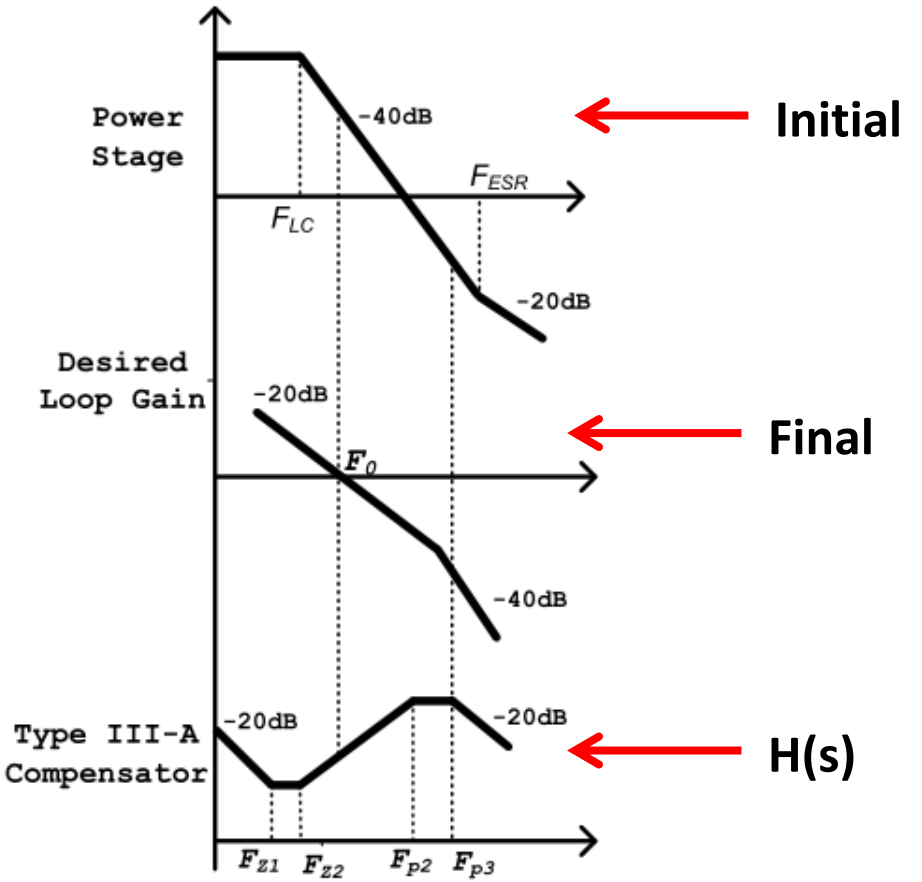
Frequency compensation through H(s) by inserting zeros (and poles)

Control Loop Analysis and stability

- Design of compensate network



Type-III compensate network



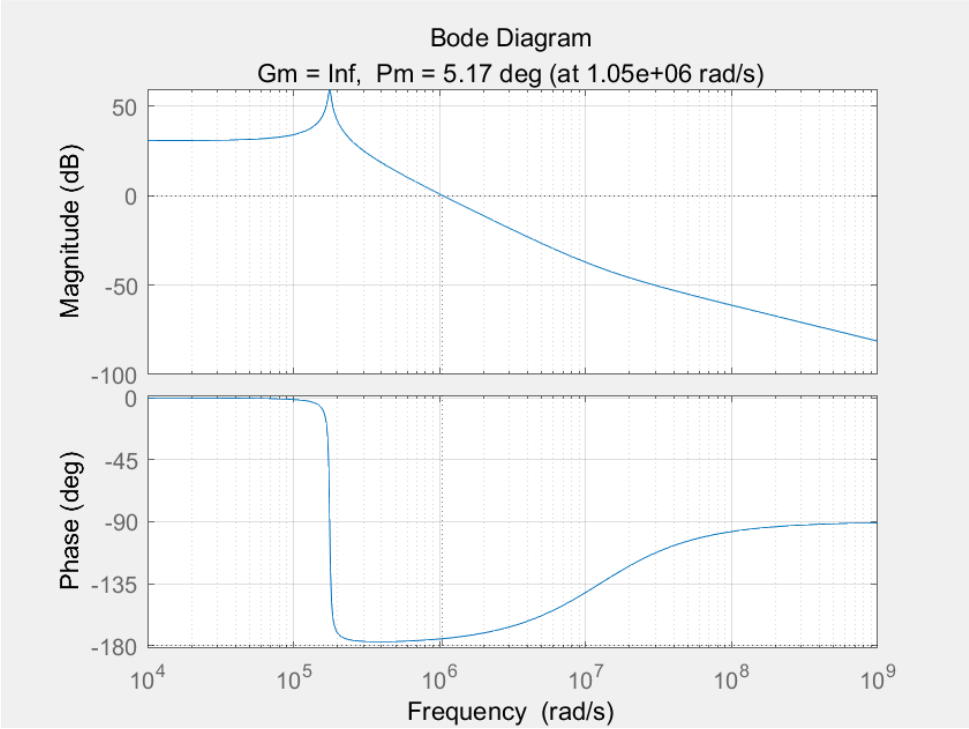
$$H(s) \approx -\frac{(1+R_{C1}\cdot C_{C1}\cdot s)\cdot[1+s\cdot C_{f3}\cdot(R_{f1}+R_{f3})]}{s\cdot R_{f1}\cdot C_{C1}\cdot(R_{C1}\cdot C_{C2}\cdot s+1)\cdot(1+s\cdot R_{f3}\cdot C_{f3})}$$

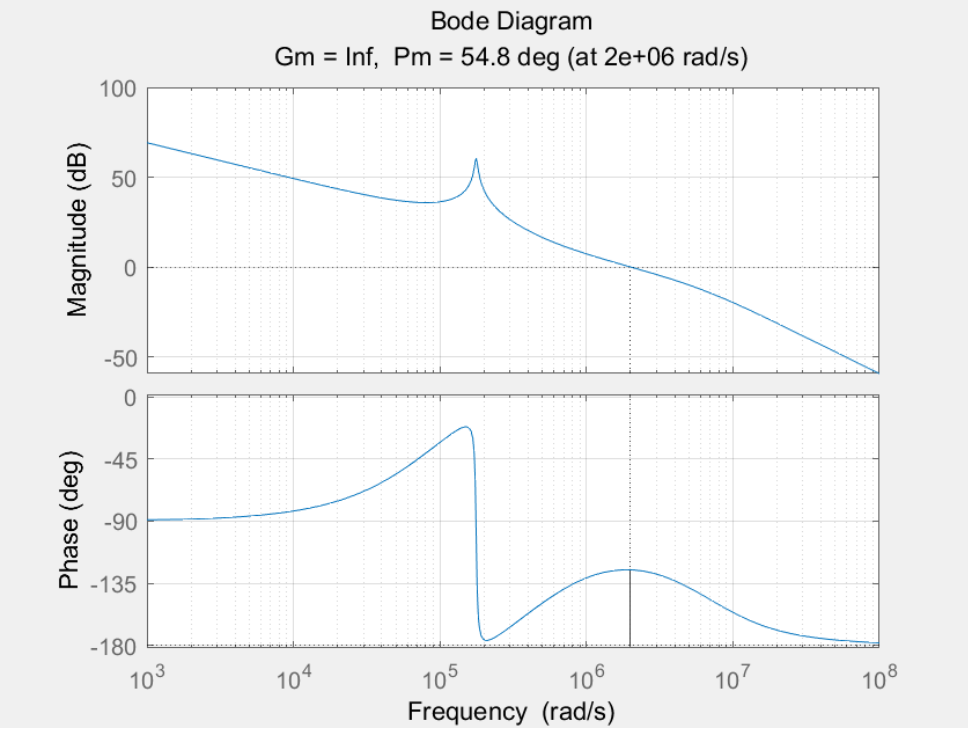
Control Loop Analysis and stability

- Stability simulation of compensated network

Vin=48V，Vout=12V，L=800nH，C=40uF，ESR=2mΩ，fsw=3MHz

```
Type III compensation, method 2.
Phase Margin= 54.8317 deg @ 317.712k Hz
calculated R/C of the compensation network:
 Rf1=104.46k ohm
 Rf2=9.4964k ohm
 Rf3=8.08004k ohm
 Cf3=17.5929pF
 Rc1=100k ohm
 Cc1=113.137pF
 Cc2=1.06103pF
delt_I=3.75
```

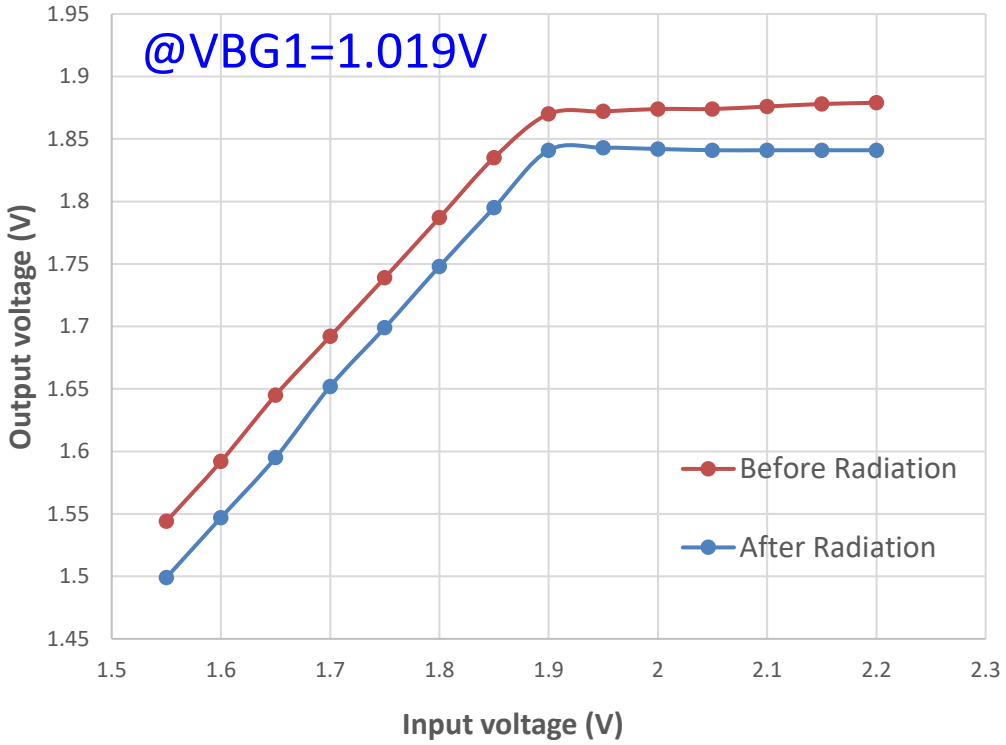




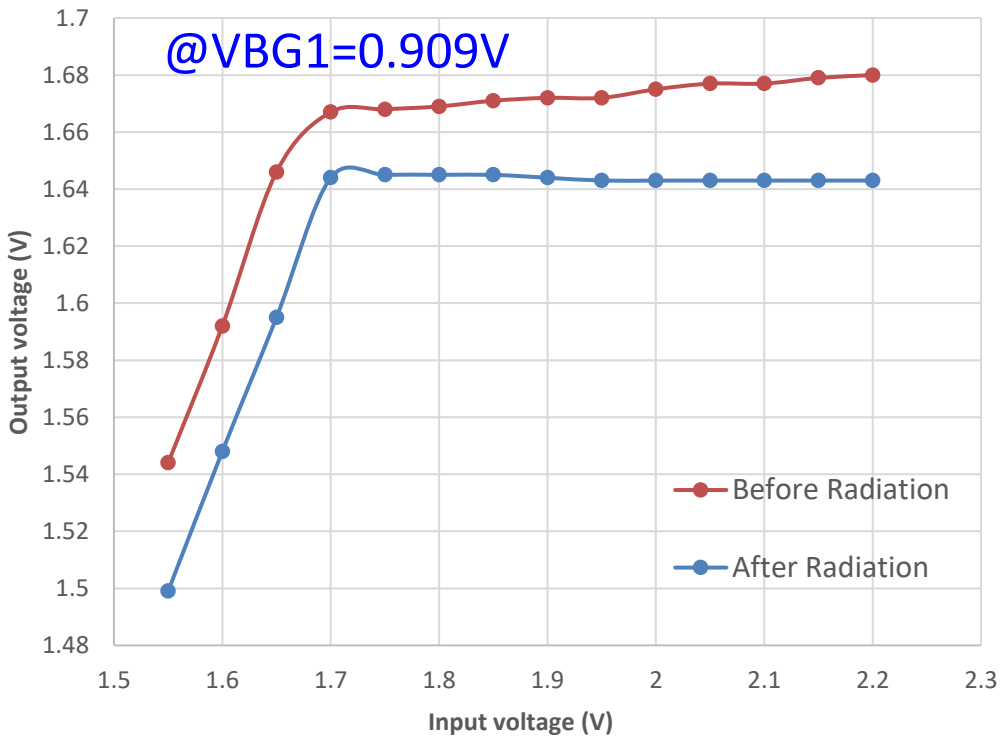
Preliminary radiation test

- LDO—Taichu Pix2

Line Regulation test results



Before radiation: 2.9mV/V (1.9~2.2V)
After radiation: -0.35mV/V (1.9~2.2V)

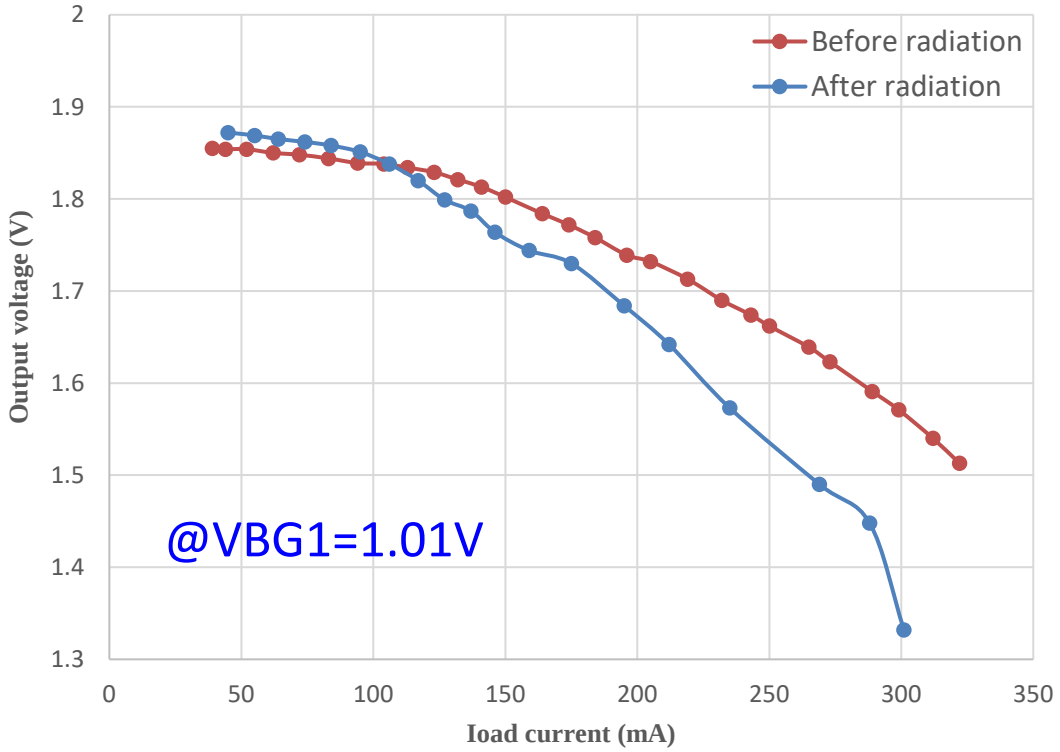


Before radiation: 2.6mV/V (1.7~2.2V)
After radiation: -0.4mV/V (1.7~2.2V)

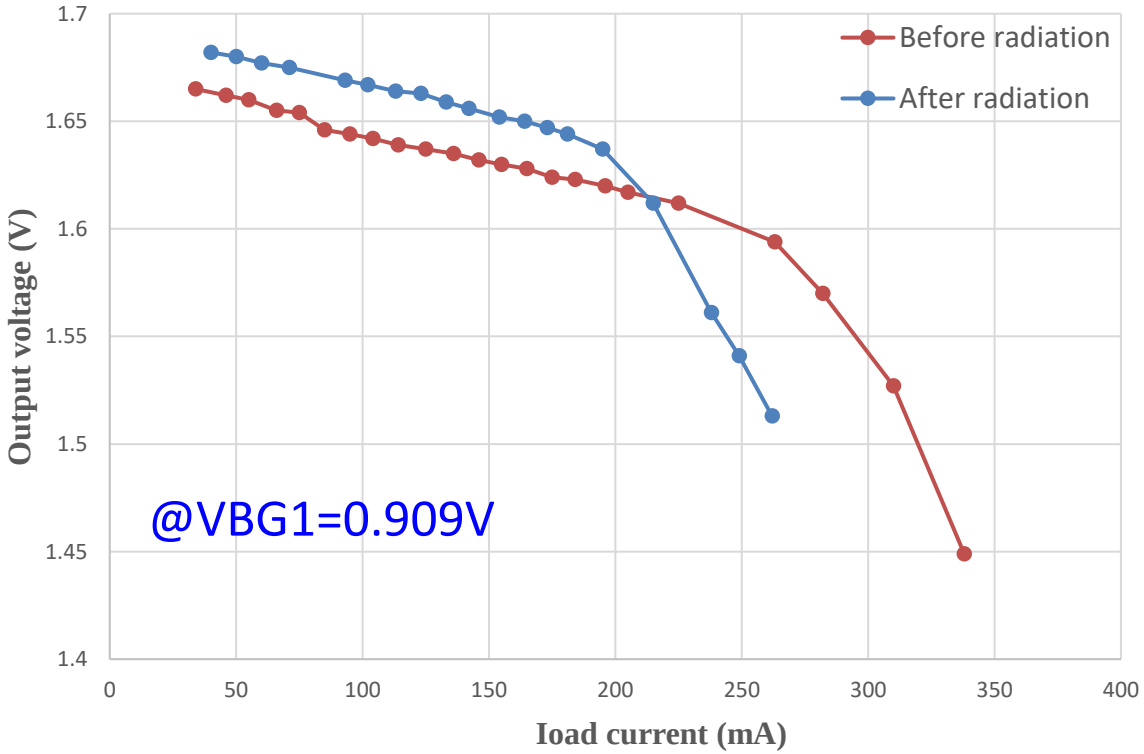
Preliminary radiation test

- LDO—Taichu Pix2

Load Regulation test results



Before radiation: 0.366mV/mA (39~132mA)
After radiation: 0.420mV/mA (45~106mA)



Before radiation: 0.277mV/mA (34~225mA)
After radiation: 0.290mV/mA (40~195mA)