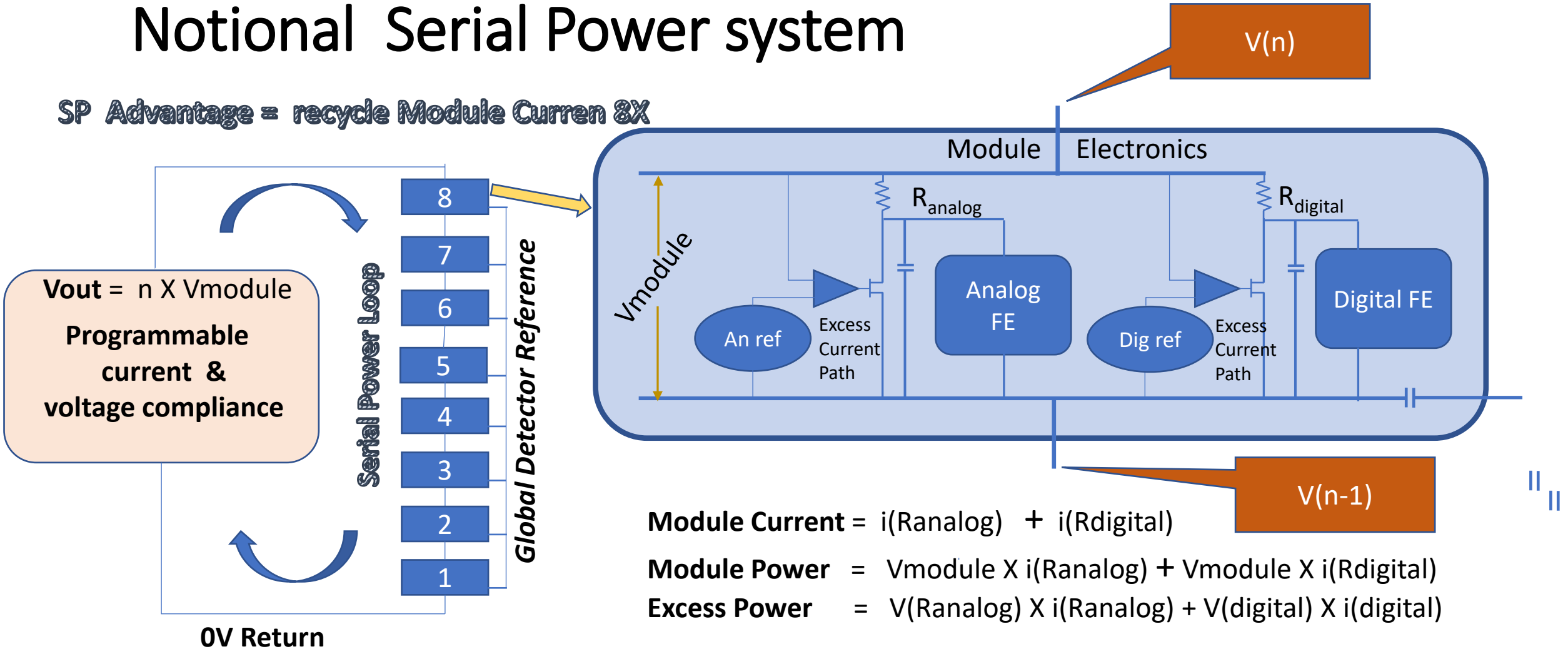
Considerations for Serial Powering

Mitch Newcomer
University of Pennsylvania

Notional Serial Power system

SP Advantage = recycle Module Curren &X



Module Current = i(Ranalog) + i(Rdigital)

Module Power = Vmodule X i(Ranalog) + Vmodule X i(Rdigital)

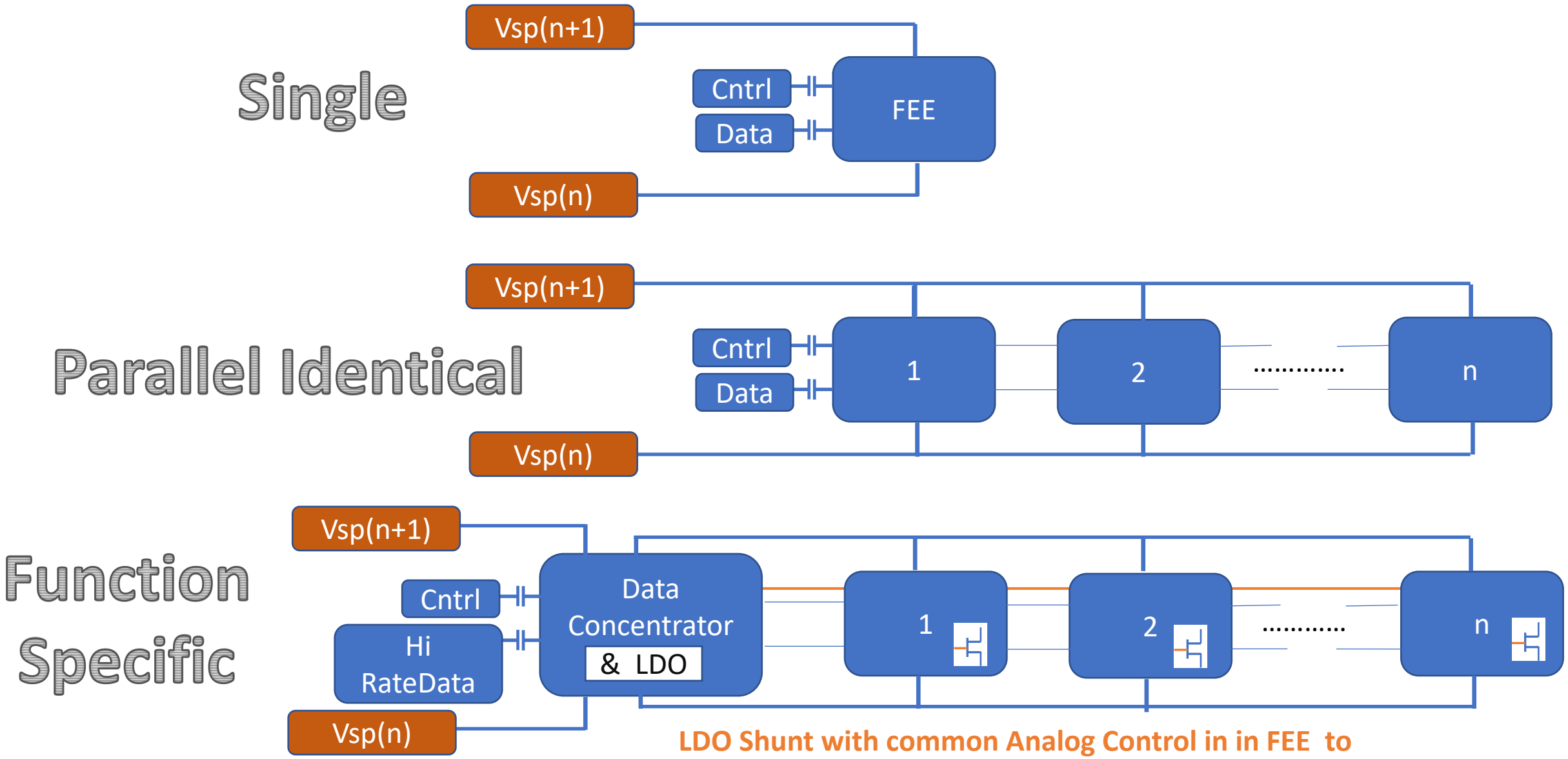
Excess Power = V(Ranalog) X i(Ranalog) + V(digital) X i(digital)

Minimum Loop Current -> **Set by Highest Consumption SP Element** + variations within the loop. (Modules in a loop may have widely varying occupancy eg. along a barrel stave for instance.

Serial Power Implementation Details to consider

- **Number of parallel devices in a voltage Step**
- **Uniformity of Occupancy along Serial power step** especially important for digital logic where power consumption is a *f(activity)*
- **Real time local monitoring** within a step
  - *Can the LDO within the ASIC be externally addressed / controlled?*
- **Realistic Operational Modes**:
  - power up / while powered / power down
    - Ramp UP/Down Speed
    - One of several ASICs powered down …at startup? ….during a run?
  - Architecture for control / data signals within a step

Module organization within a Serial Step



LDO Shunt with common Analog Control in in FEE to ensure even heat distribution.

Advantages of a Serial Powered System

The ADVANTAGE → Material Burden benefit realized by reduced gauge supply & return cables sufficient to provide a **single module** with power a SP loop of ‘n’ modules by increasing the loop voltage ‘n’ times instead of the current.

→ **Simplicity of a nearly DC control structure**.. LDO for each voltage with consideration for Maximum power excursions capacitive filtering for instantaneous current deviations eg clocked logic or trigger response

→**No clocked switching circuits** to generate pattern noise Or Switching Rate related heat.

→**Possibility of aggregating many module consumers in parallel** where detector topology permits.

- **Evens out SP voltage step current loading**. Allows the SP voltage step to take advantage of security in numbers when single units have deviations or may need to be turned off ..
- But this is not magic, simply parallel powering so there is no wire gauge material reduction advantage.

Serial Power Disadvantages

Serial power is **an** ***unfamiliar*** **approach to module powering**

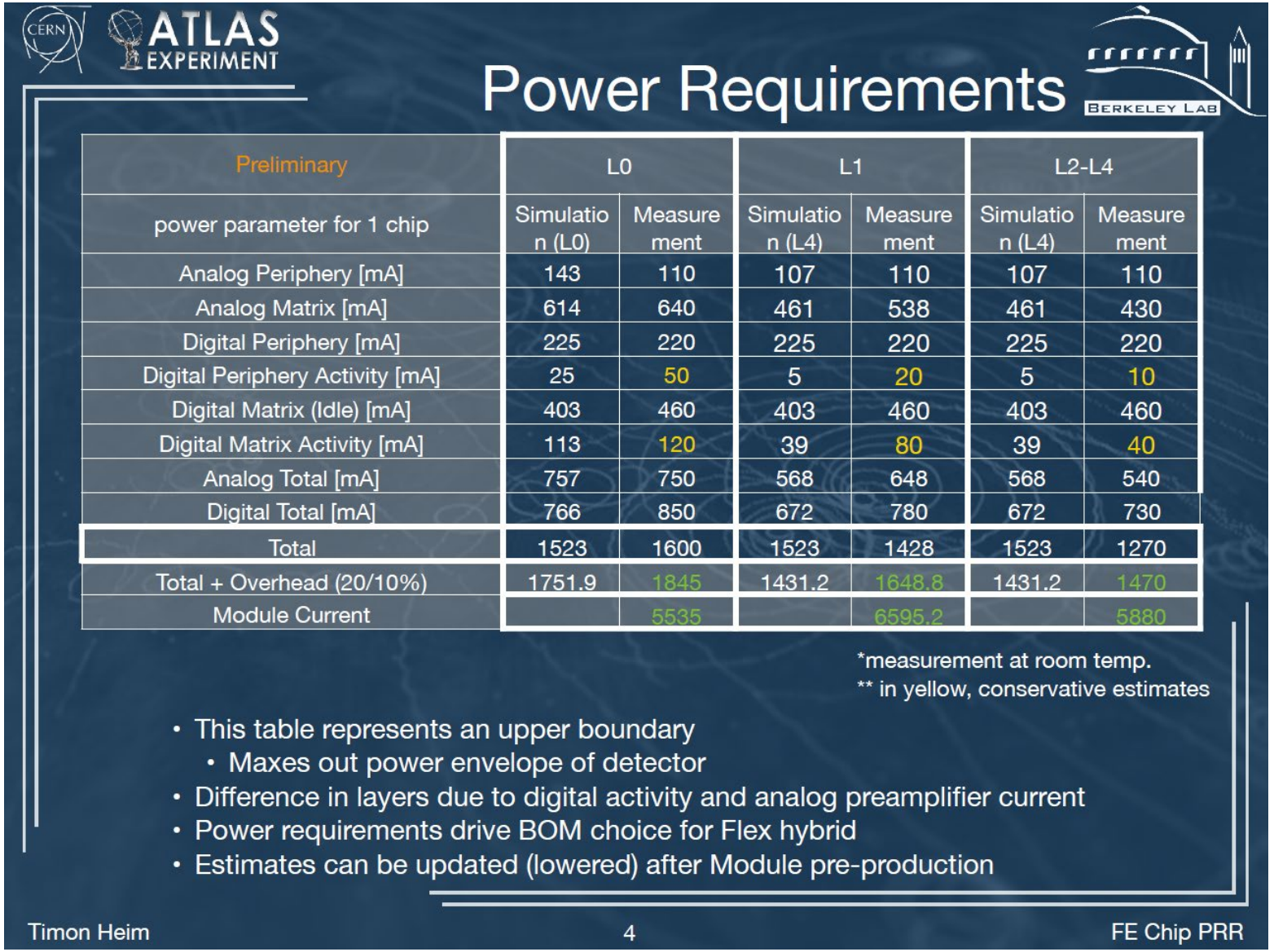
- **Serial power Loop Supply** is **crucial** for fault free operation. Requires a somewhat novel, programmable constant current, programmable voltage compliant approach. An Accelerator driven feed forward control could be advantageous here.
- Communications need to be capacitively coupled **requiring balanced code or receivers with hysteresis and startup procedures**.
- To maintain high levels of operability Module failure modes need to be addressed. Current flow in the SP loop must be maintained. A serial step can be taken out of the loop by shorting the Module with a current bypass element. The time frame is important.
  - Slow changes in voltage steps can result in overheating & damage to current shunt elements.
  - Fast changes can cause cascade communication failures in the Serial Loop

Engineering A stable power efficient Serial Power System

Current Uniformity in the Loop Maximizes Efficiency

- Start with the ASIC. ***Minimize data taking power variations***. For system stability it may be best to shunt unavoidable trigger related readout current in quiescent operational states to avoid data taking spikes.
- Choose loops with common occupancy levels where possible.
- Design with care the reference potential system for proximal read out loops.
- Isolate Communication in Serial Loops with capacitive or optical communication schemes if TID and SEU effects are manageable.
- Co-design a SP Supply with FB from the serial loop and potentially spigots for Feed Forward from the Accelerator control room to provide tuneable increased current during predictable data taking spikes.
- Design in connection redundancy & provision for controlled failure behavior.
- Make sure powered down modules don't present low impedances on bussed communication lines.

ATLAS Pixel Experience with SP systems



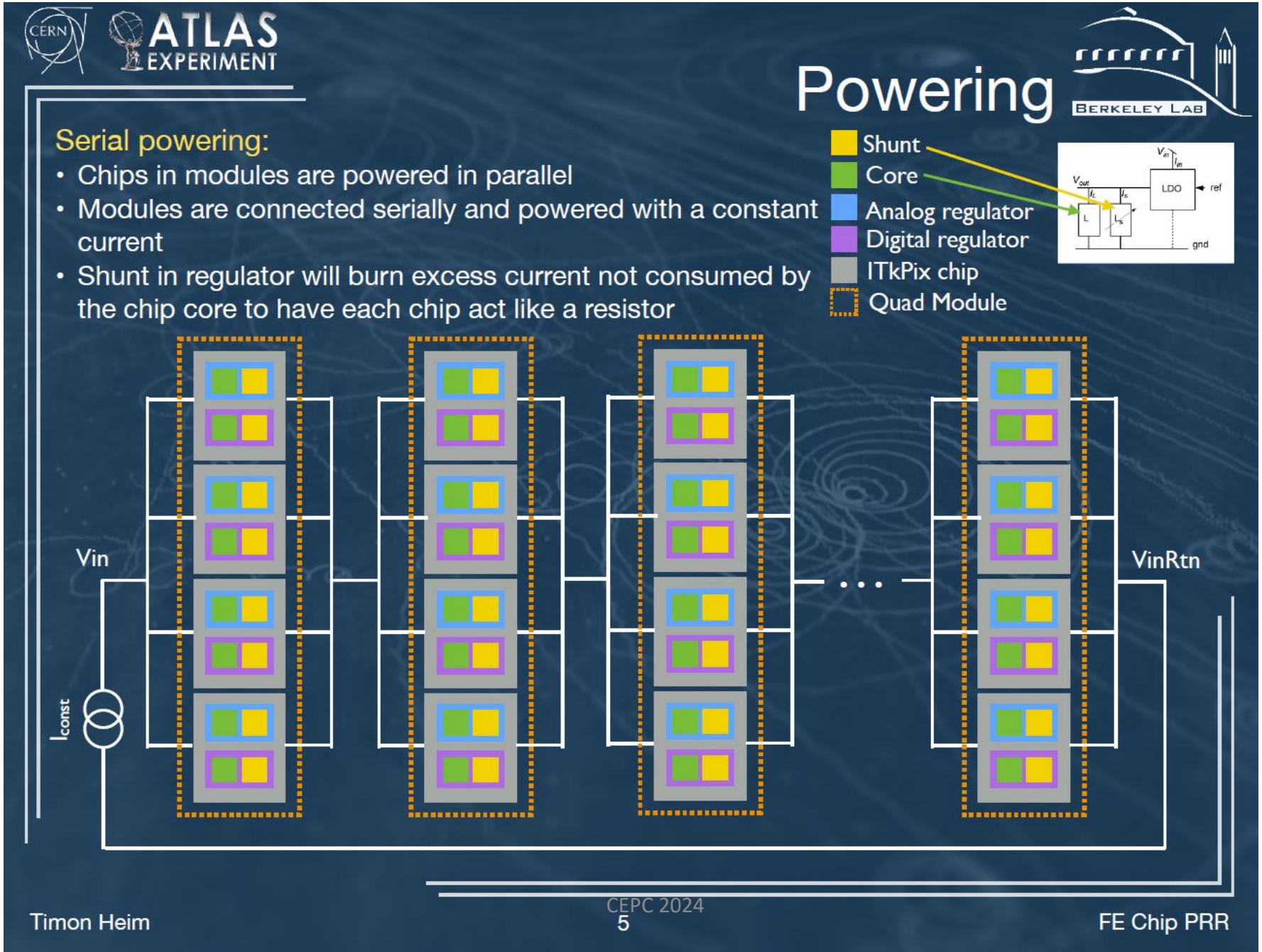
Preliminary	L0		L1		L2-L4	
power parameter for 1 chip	Simulation (L0)	Measurement	Simulation (L4)	Measurement	Simulation (L4)	Measurement
Analog Periphery [mA]	143	110	107	110	107	110
Analog Matrix [mA]	614	640	461	538	461	430
Digital Periphery [mA]	225	220	225	220	225	220
Digital Periphery Activity [mA]	25	50	5	20	5	10
Digital Matrix (Idle) [mA]	403	460	403	460	403	460
Digital Matrix Activity [mA]	113	120	39	80	39	40
Analog Total [mA]	757	750	568	648	568	540
Digital Total [mA]	766	850	672	780	672	730
Total	1523	1600	1523	1428	1523	1270
Total + Overhead (20/10%)	1751.9	1845	1431.2	1648.8	1431.2	1470
Module Current		5535		6595.2		5880

*measurement at room temp.
** in yellow, conservative estimates

- This table represents an upper boundary
  - Maxes out power envelope of detector
- Difference in layers due to digital activity and analog preamplifier current
- Power requirements drive BOM choice for Flex hybrid
- Estimates can be updated (lowered) after Module pre-production

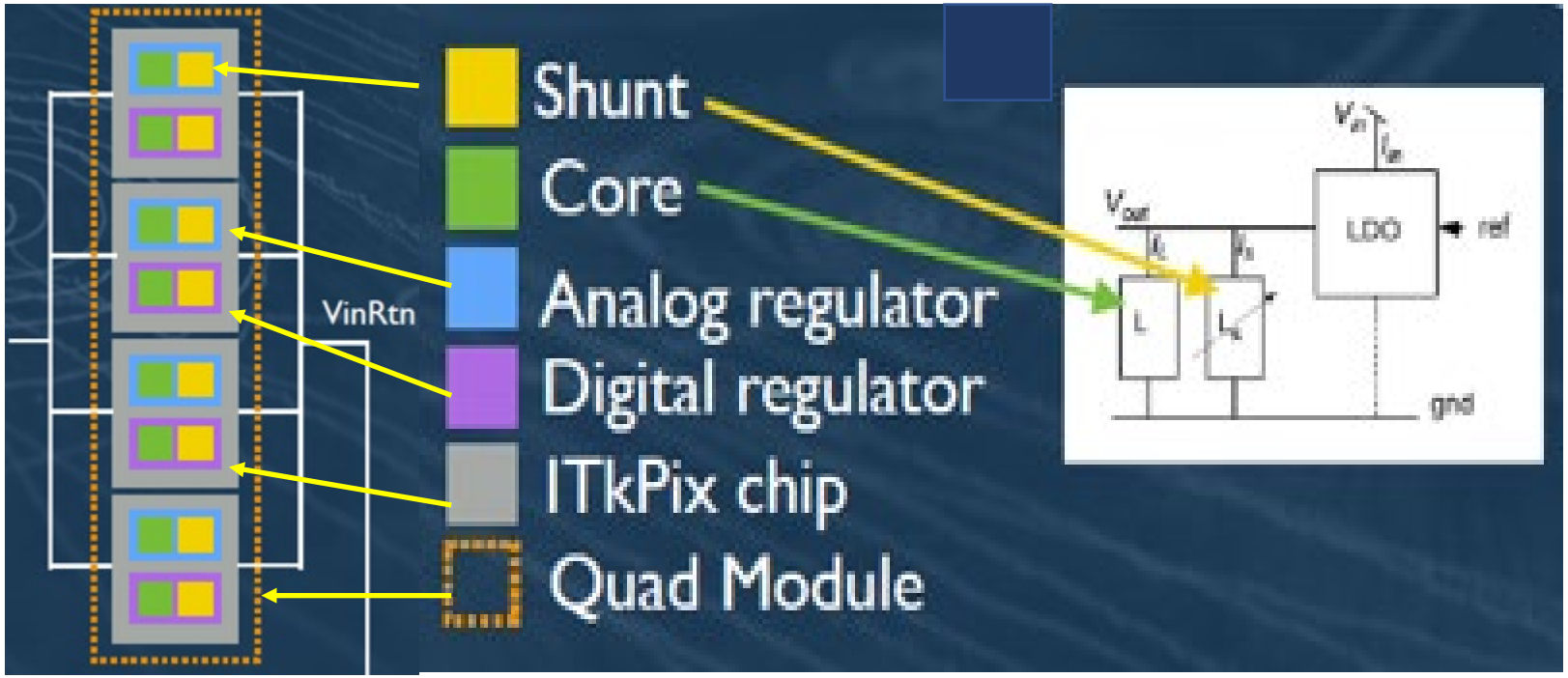
Timon Heim 4 FE Chip PRR

Serial Powered Modules with Multiple Parallelpowered ASICs



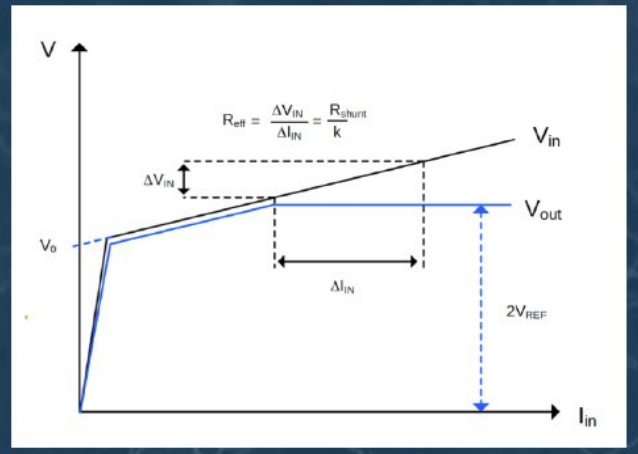
Each ATLAS Pixel Chip has a Analog & Digital Shunt LDO

A Shunt is required to equalize current in each serial step



Powerup Characteristics

SLDO Parameters



Variables:

- Voffset: voltage offset controlled by voltage drop through external resistor from the current reference
- Reff: given by current through external resistor from Vin to local GND multiplied by current mirror

Important aspects for Modules:

- Module through current is split over all chips within
- Current split is given by the equivalent impedance of the chip
- Goal: chip impedances supposed to be as equal as possible to ensure equal current sharing
- Unequal current sharing could lead to a chip not having enough current

Methods to ensure equal Current split:

- Voffset sharing (Voffset connected between all chips in module)
- Equalize resistance on Vin and VinRtn nodes to avoid unequal voltage drops
- High precision resistors (0.1%)
- Main uncertainty on current sharing is current mirror multiplication factor (k-factor) -> have sufficient cut during wafer probing

IV curves show the operating current Stability/Efficiency

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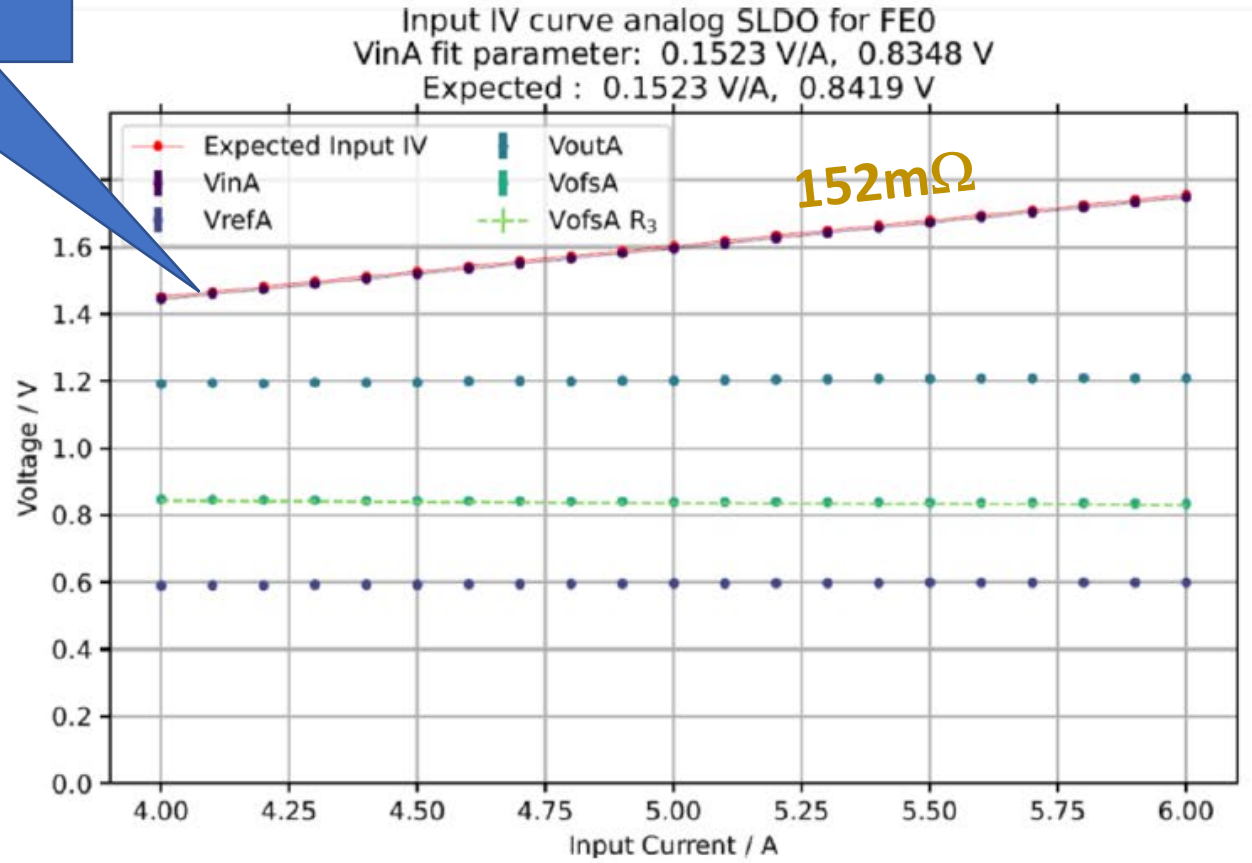
RD53A PLANAR SERIAL POWERING CHAIN – MODULE IV CURVES

- Example: Module SPQ14
  - $V_{IN\_A,D}$ **tied** together on flex
  - > V_{IN} **nearly same** for all SLDOs
- **Good agreement** with expectation

Vin controlled by SP Loop supply



Spice	Full SPQ14
Slope	0.15 V/A

Efficiency of Serial Power Depends on current Overburden

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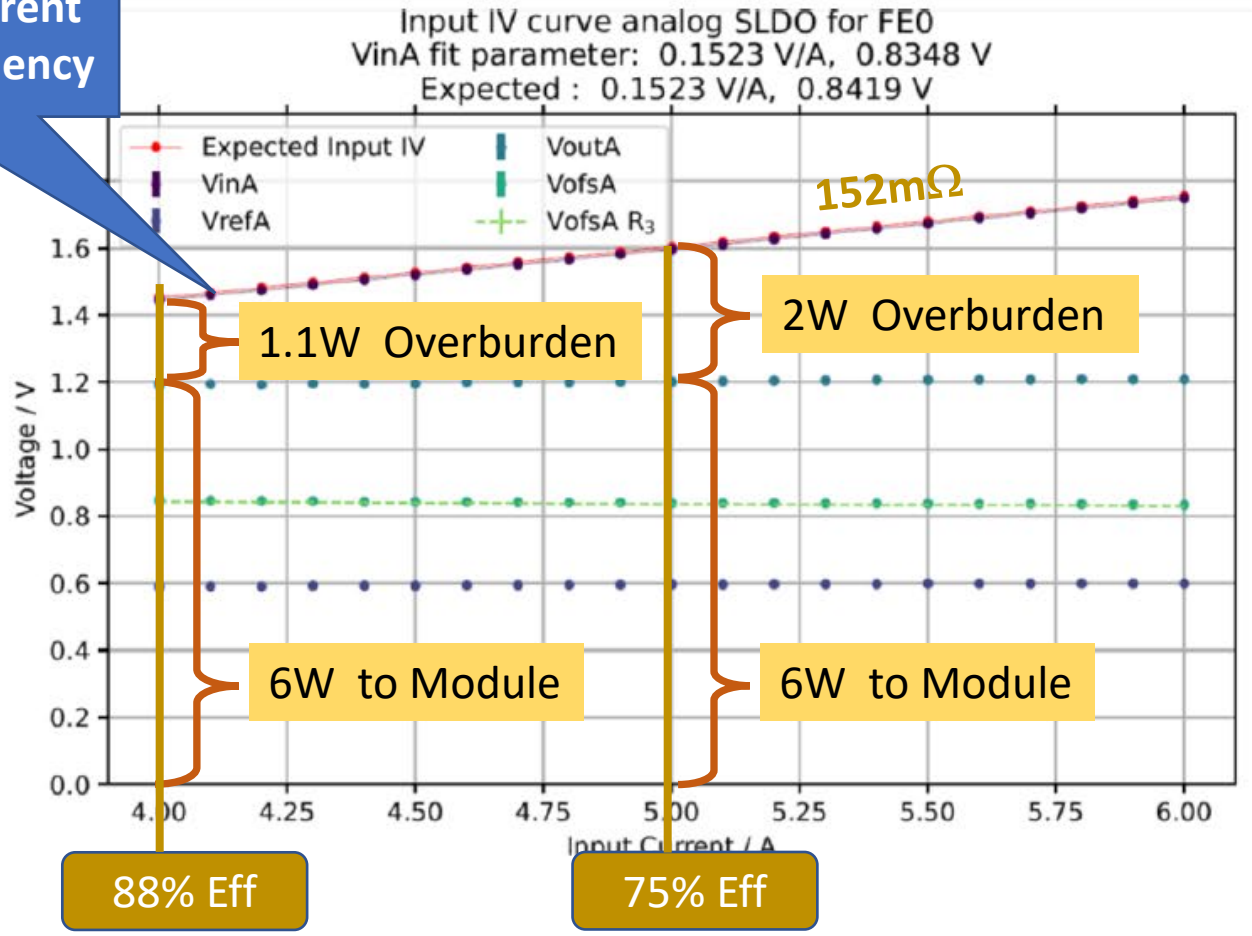
Loop Supply Current Determines Efficiency



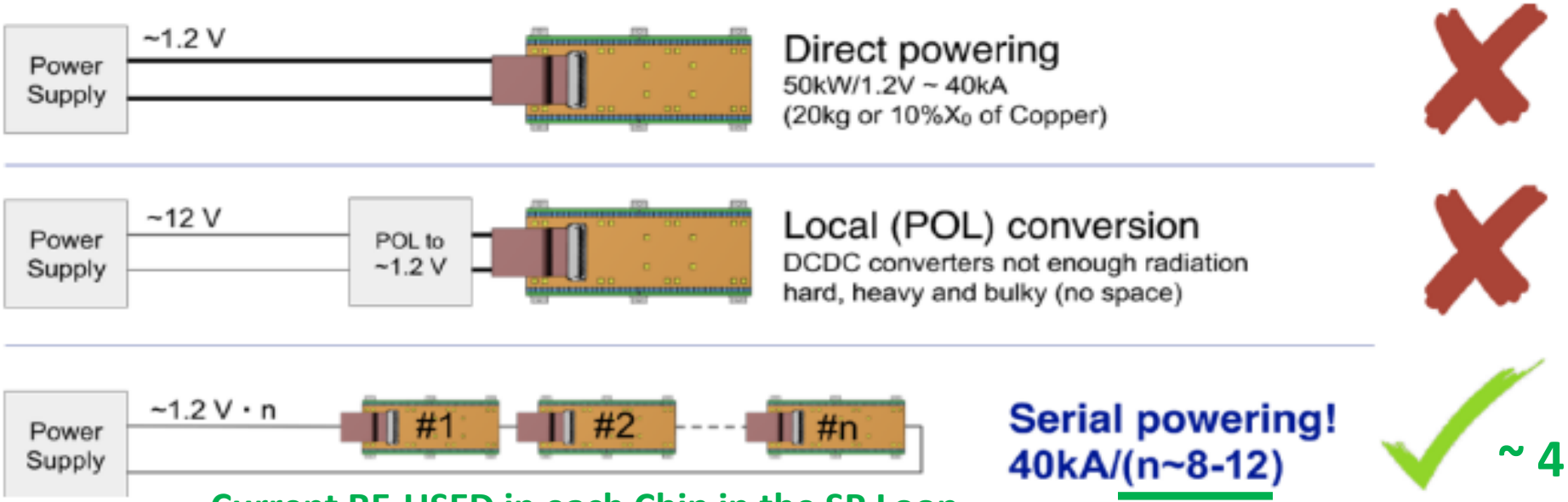
CMS pixel Readout Chip * CROC

- Part of the RD53 joint CMS and ATLAS collaboration to design the pixel electronics of the experiment upgrades for the HL-LHC.
- Designed in 65nm CMOS technology, features 1.5×10^5 pixel channels and
- Consumes about 8 − 10 µA per channel.
- Current per chip is ~ 1.5 A, with a supply voltage of 1.2V.
- Shunt-LDO (SLDO) constant current drain in time, independently of the chip power consumption
- Hit rates of 3Ghz/cm^2 and TID of 500MRad
- Serial powering scheme to provide the ~ 60 kW required by ~ 4000 modular units.

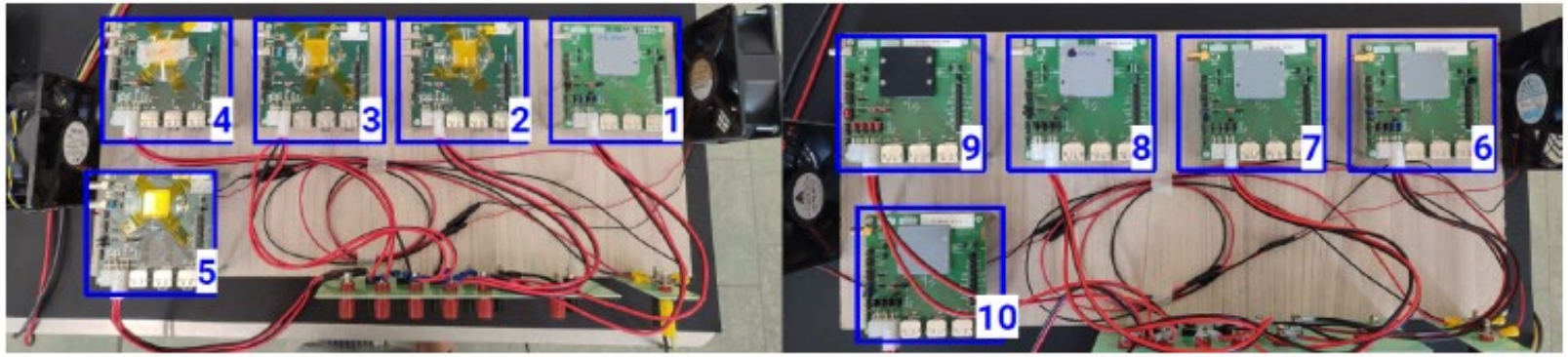
Total current at 1.2V = 50kA

* Jinst 2024 JINST 19 C01056 **Rudy Ceccarelli,** 16th Topical Seminar on Innovative Particle and Radiation Detectors

Evaluating the Powering scheme for the CMS Inner tracker



10 Step CMS CROC Serial Powering Test Setup with a Mix of 3D and Planar Pixel Sensors



Pixel Performance comparison under Serial Power

Serial power step Position 1, 6, 10 of 10 total

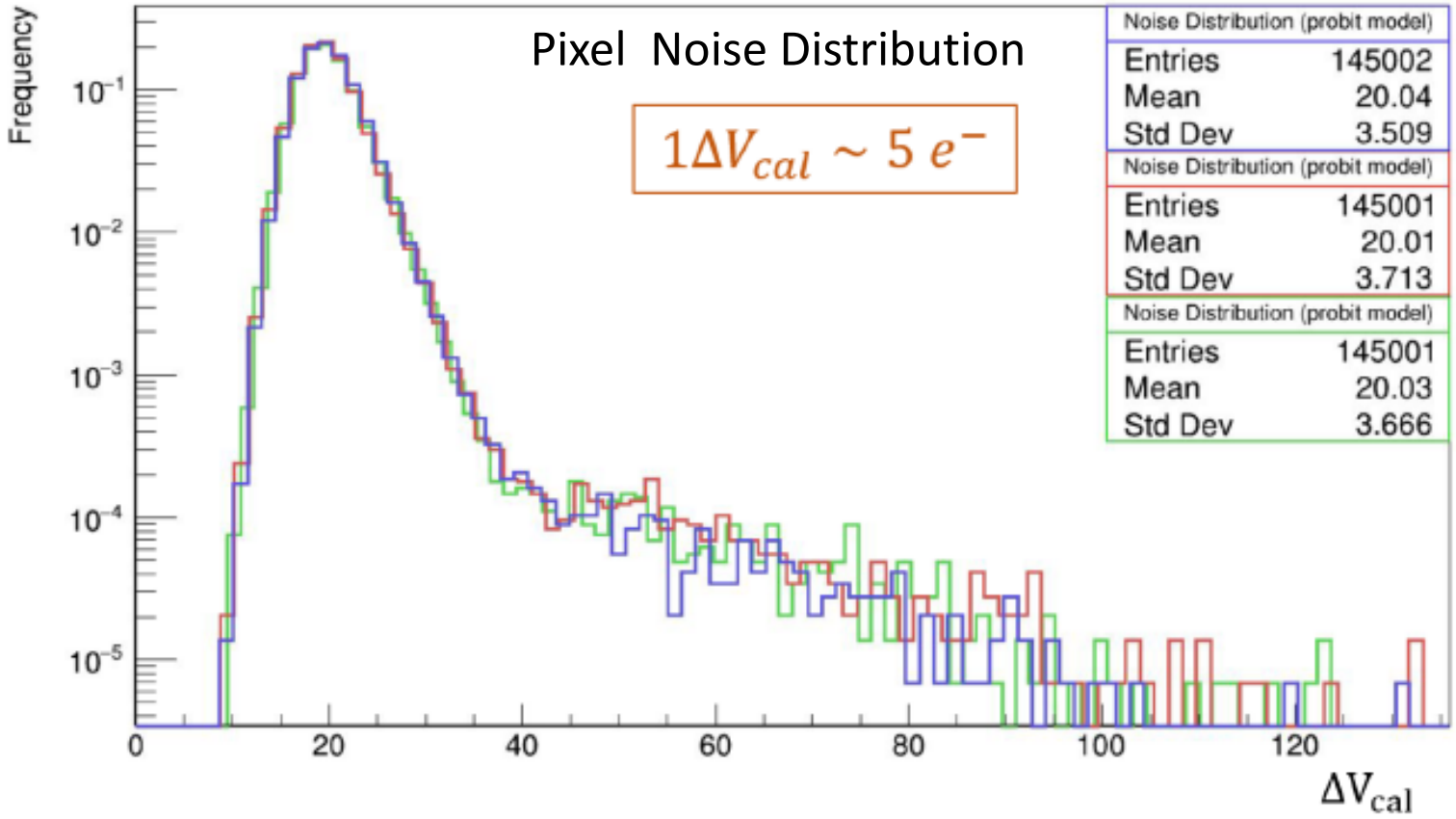


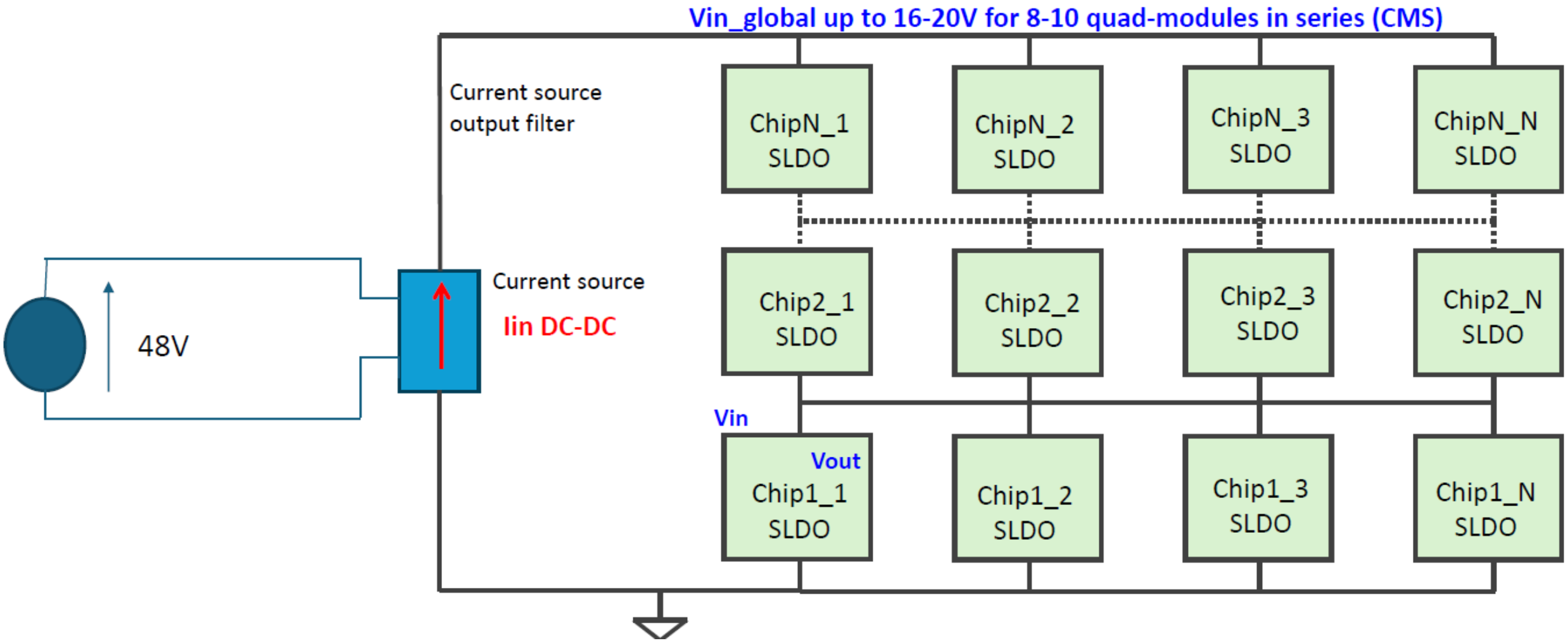
Figure 8. Pixel noise distribution in ΔV_{cal} units (where 1 ΔV_{cal} corresponds to approximately 5 electrons) of the 3D CROC module under test in three different positions of the serial powering chain: blue is the first position, red is the sixth position and green is the tenth position. No significant differences can be observed.

Other tests performed in CROC prototype SP Chain

- Powering up and data taking with some parallel powered ASICS disabled. Demonstrated stable operation with shunts taking up the load of unpowered ASICs.

→ **Missing discussion about live time failure modes.**

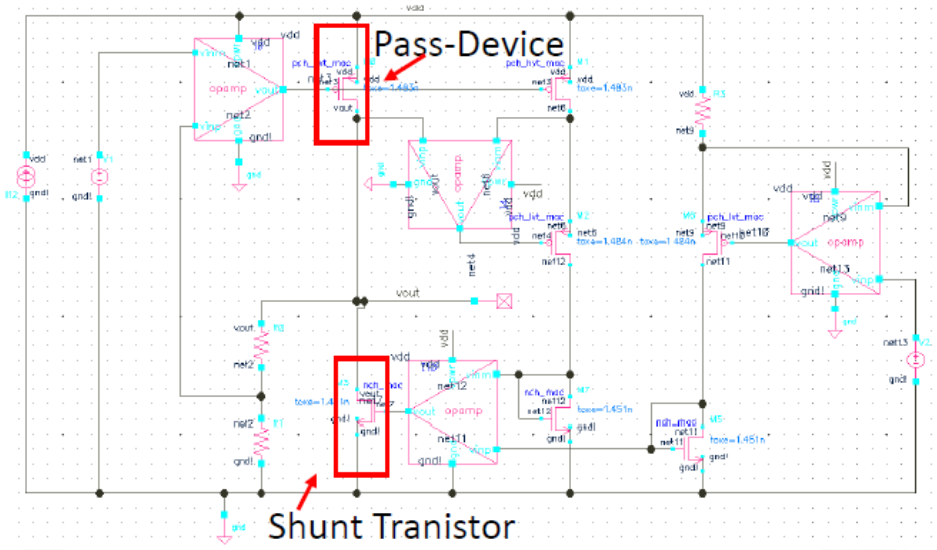
Work in Serial Powering in DRD 7.1b

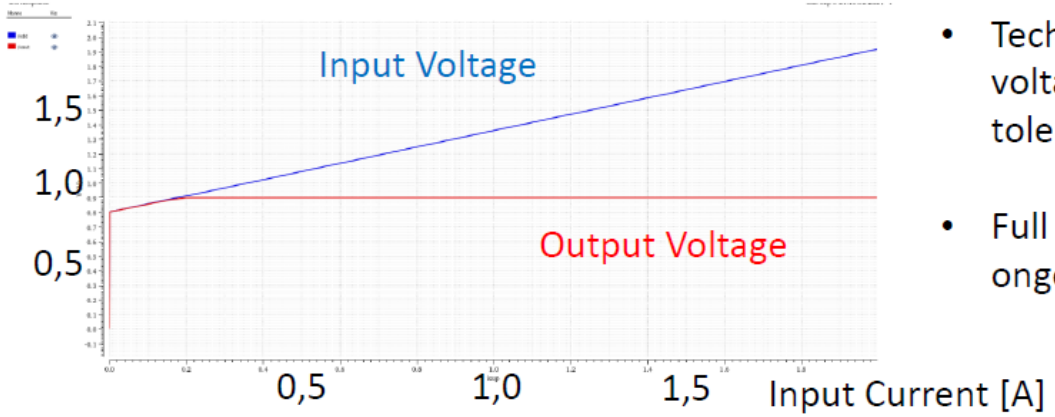


First SP Designs in 28nm process..

Shunt-LDO Design in 28nm

Fachhochschule Dortmund
University of Applied Sciences and Arts





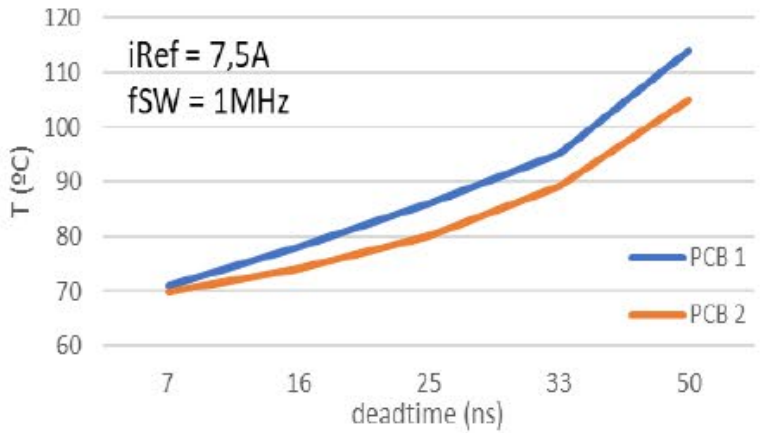
- First simulation studies performed in 28nm based on Verilog-A amplifier models
- Devices types and dimensions studied for shunt and pass-device
- Studies show SLDO thin-gate oxide core transistor implementation feasible in 28nm
- Technology limits maximum input voltage to 1.8V with overvoltage tolerant design (2V @ 65nm)
- Full transistor level implementation ongoing

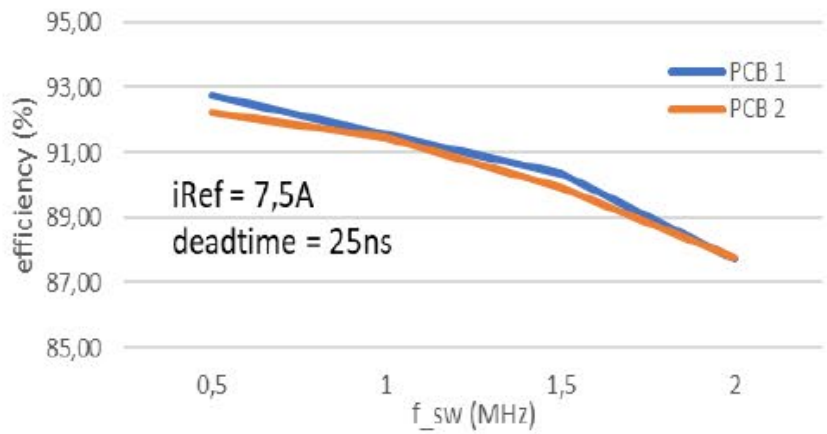
GaN based power converter for Serial Powering

- The main goal of this task is to assess the feasibility of utilizing GaN- based DC-DC converters (current source) for serial powering applications.
- Several critical issues have been identified to optimized the design of these units
  - Design implications associated to GaN switching
    - High frequency (MHz) and short transition times (ns)
    - Precise Duty Control & deadtimes (High Resolution PWM modulator)
  - EMI filter design : Filter embedded in the PCB & magnetic components
  - Radiation hardness
  - Modular /Multiphase concept
- Several activities focused on the development of 200W / 2MHz GaN-based DC-DC have been carried out
  - **Design & Develop a preliminary prototype, which includes (2023)**
  - **Perform a performance evaluation, encompassing efficiency and EMI testing (2024)**
    - **This evaluation will also involve combined EMI testing in radiation environments (on going)**
  - Design printed circuit boards (PCBs) that incorporate embedded filters and magnetic components.
  - Design & develop a new prototype based on a modular concept, incorporating identified improvements.(2025)

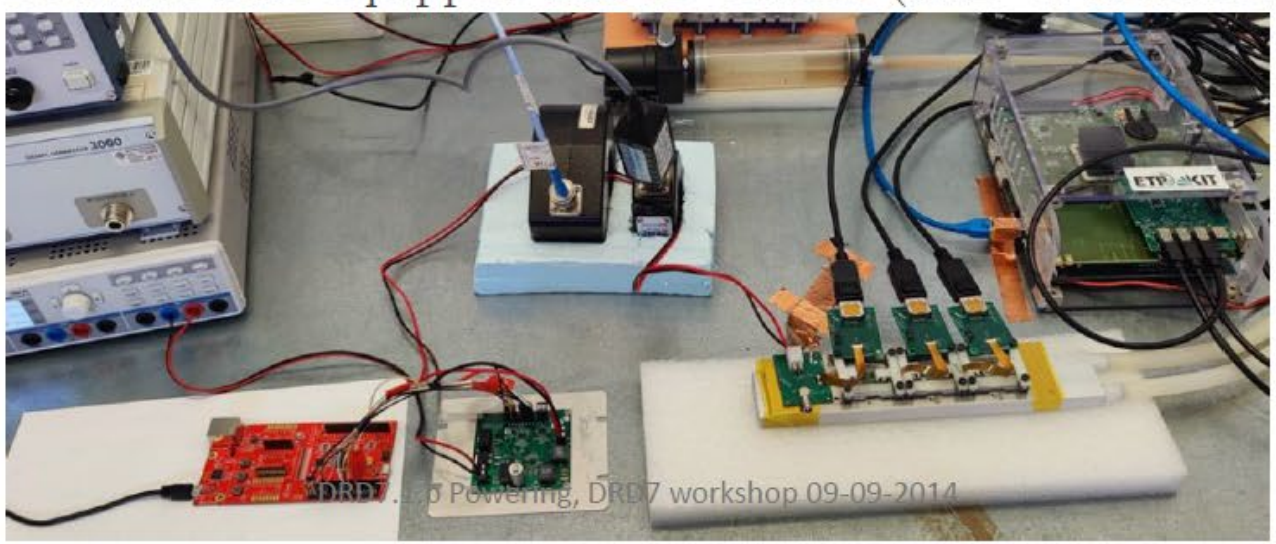
GaN based power converter for Serial Powering

- The performance assessment of the preliminary prototype is almost finalized.



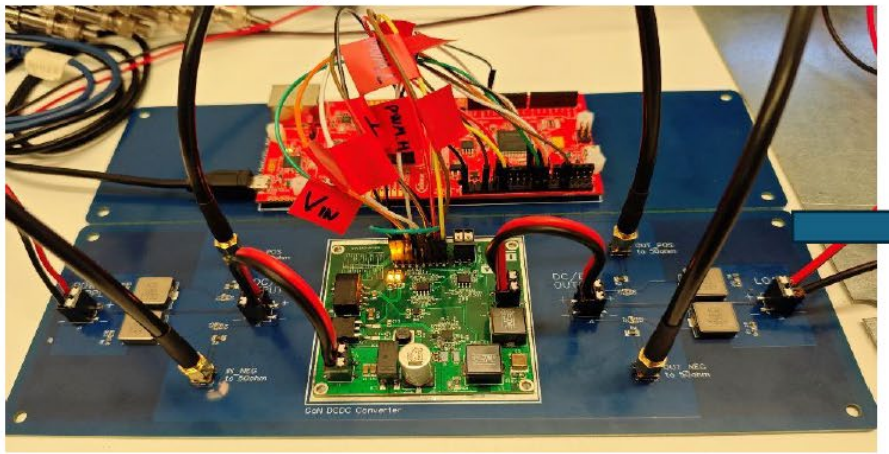


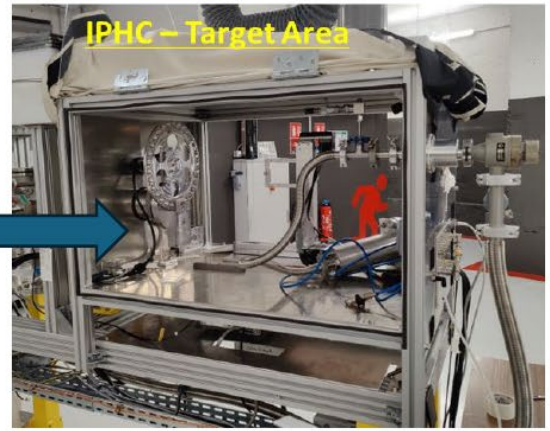
- The preliminary prototype was also tested on a real serial power chain during the noise Transfer Function characterization of 1x2 RD53A modules equipped with 3D sensors (IMB-CNM Barcelona) – CMS IT – Phase II



GaN based power converter for Serial Powering

- The EMI evaluation of the prototype was conducted using a specialized setup developed under the AIDAINNOVA project.
  - The setup is portable and fully automated, allowing both time and frequency domain measurements.
    - It is highly effective for measuring transients related to power supplies (PS)
  - The system can also perform noise measurements during radiation campaigns (Measurements are planned at IPHC-Strasburg).





- Measurements of the noise emission of the DC-DC has been already performed

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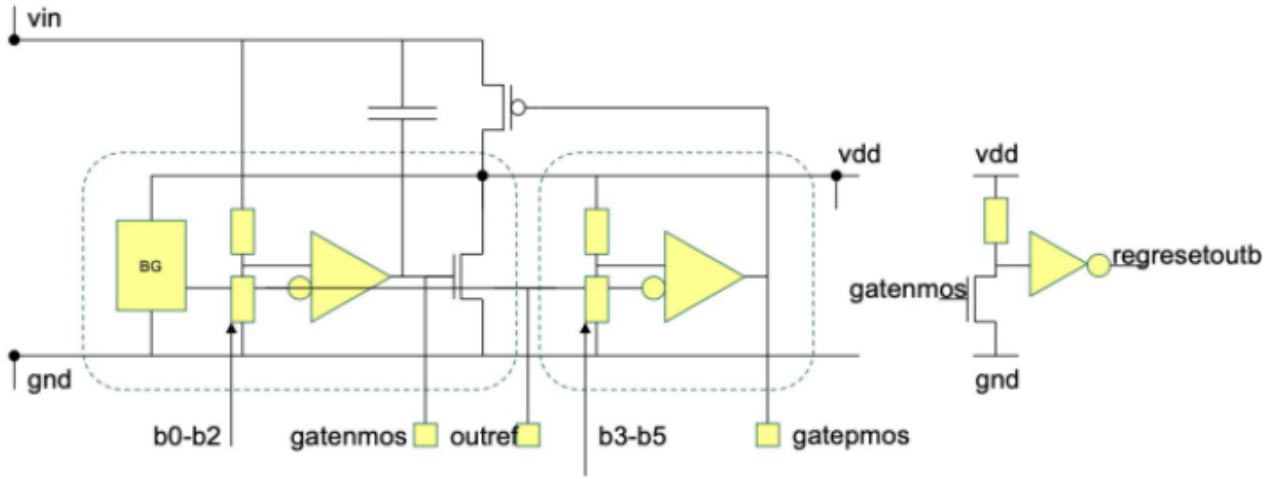
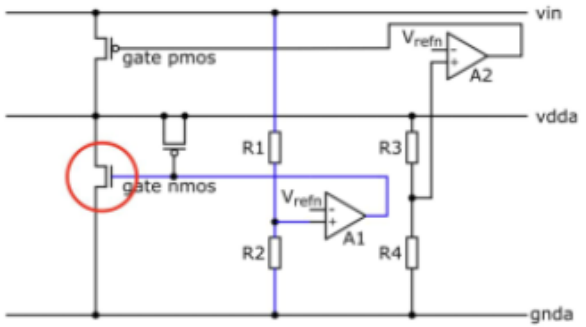
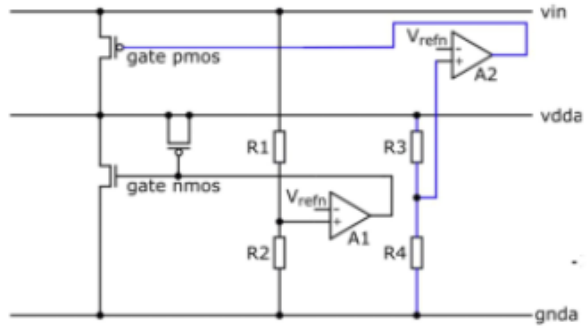
ATLASPIX3.1 Serial Powering

- ATLASPIX3 is a full reticle size monolithic pixel sensor
  - I. Peric (KIT) main designer
- Version ATLASPix3.1 has possibility for serial powering through two shunt/low dropout regulators
  - digital and analog (VDDD/A)
  - 3 bits to tune threshold of shunt regulator
  - 3 bits to tune VDD
  - gatenmos, outref, gatepmos are for monitoring
  - regresetoutb can be used as power on reset
- Possibility to use a single power supply line for all the 6 biases needed to operate the chip





- First loop defines **shut regulators**



- Second loop **regulates VDDD/As**

180nm HV CMOS process Active Pixel Sensor Compatible with Serial Powering.

Summary

- Serial Power is a serious candidate for delivering power with low mass cabling without adding the overhead of high frequency conversion process that may affect near by sensitive electronics.
- It can be configured in a variety of way to suit detector implementations.
- Efficiency is maximized by tight control of the module to module current differences.
  - These may include part to part quiescent power differences
  - Minimizing/understanding the occupancy differences during data taking
- Communications must be capacitively coupled and will likely require utilizing balanced code transmissions.
- Early Implementation in the design cycle is essential although the same FEE parts complatible with Serial Powering can be used with parallel powering.