COMPARING ELECTRONIC SYSTEMS FOR PRECISION TIMING IN ATLAS AND CMS EXPERIMENTS

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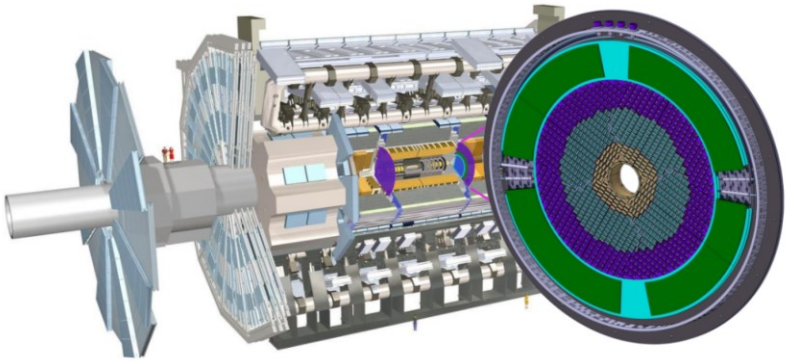
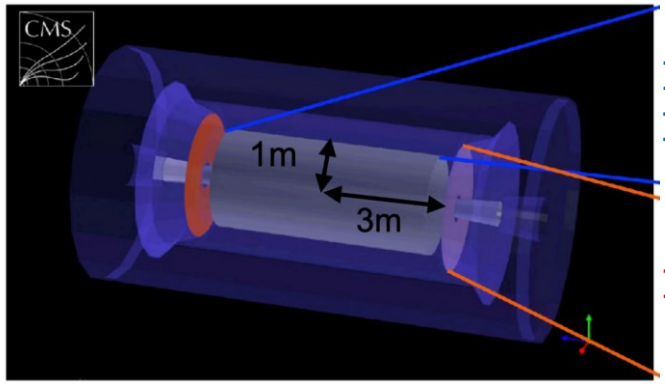
2024 International Workshop on the High Energy Circular Electron Positron Collider

at Hangzhou, Oct. 26, 2024

TIMING DETECTOR: ETL (CMS) AND HGTD (ATLAS)



ATLAS High Granularity Timing Detector (HGTD)



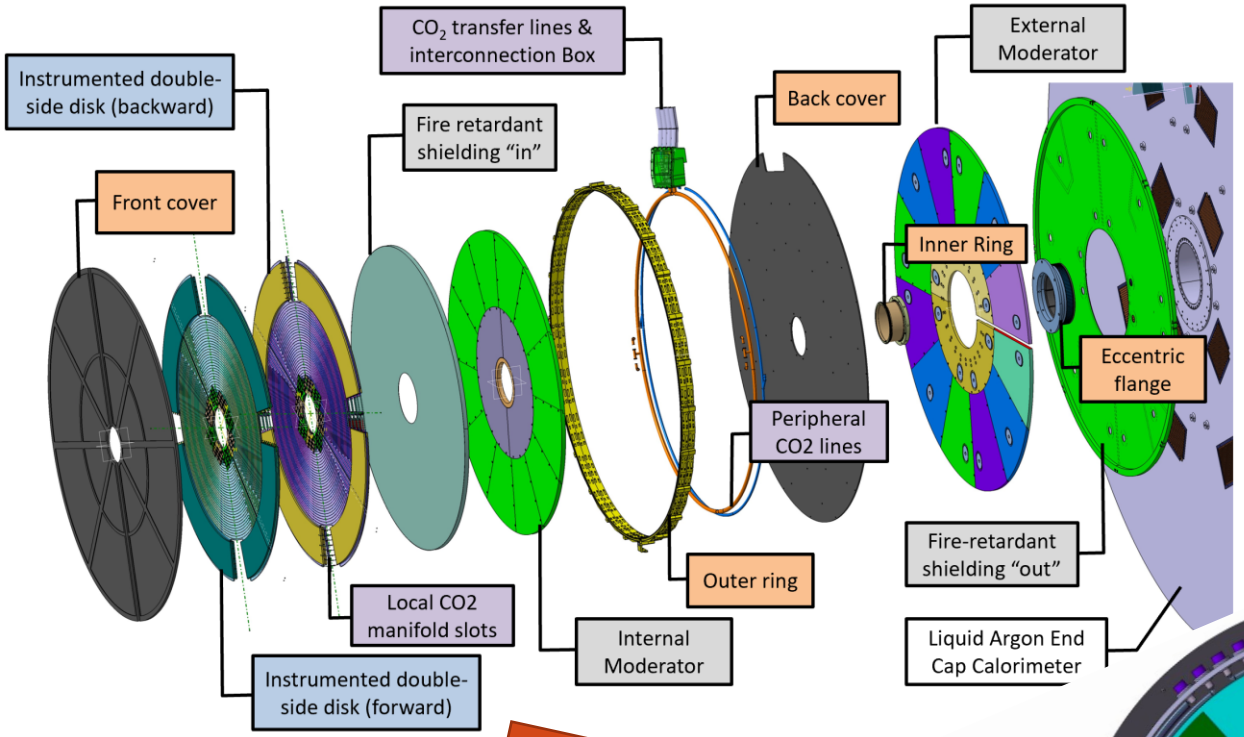
Barrel Timing Layer (BTL):
LYSO bars + SiPM readout

Endcap Timing Layer (ETL)

CMS MIP Timing Detector (MTD)

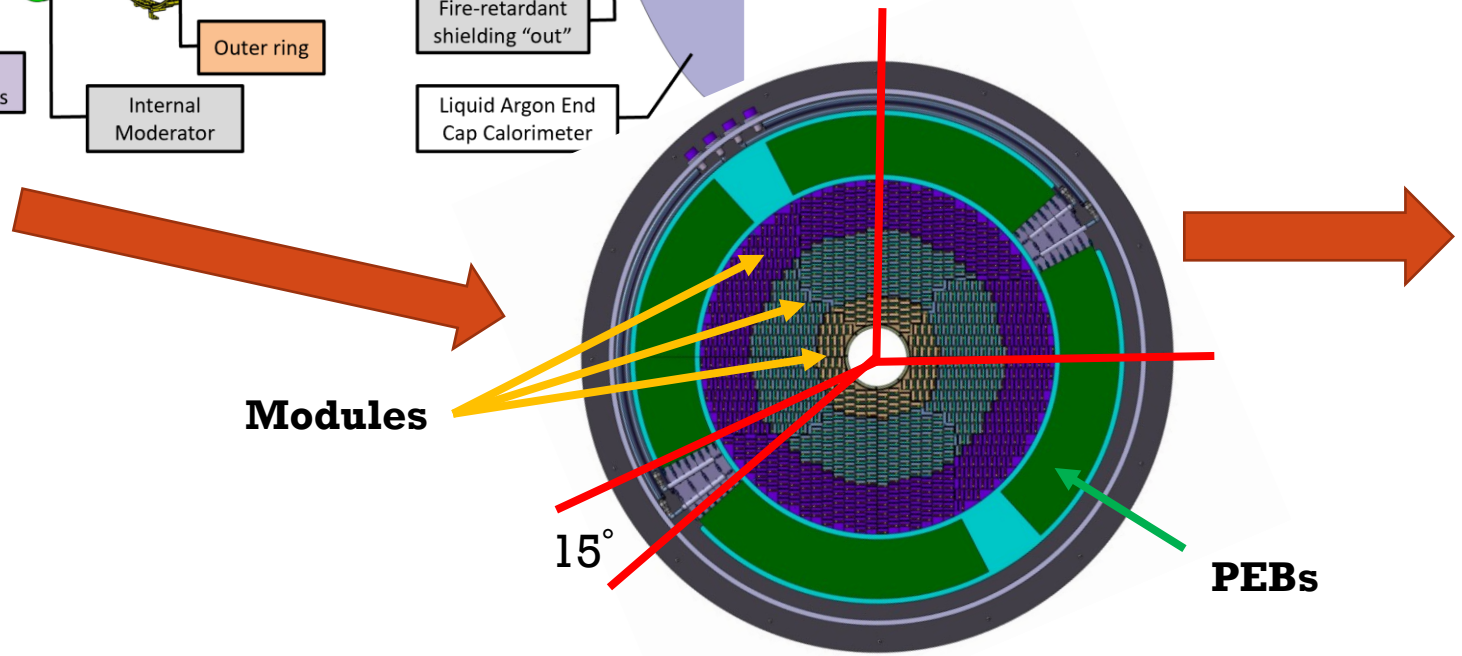
	HGTD	MTD ETL
Position	120 < R < 640 mm or 2.4 < |η| < 4.0	315 < R < 1200 mm or 1.6 < |η| < 3.0
	z ± 3.5 m	z ± 3.0 m
Active area	~6.1 m^2	~14 m^2
Pixel in total	~3.6 M	~8.5 M
Occupancy	Up to 7 %	Up to 5%
TID	Up to 200 Mrad	Up to 100 Mrad
NIEL	Up to 2.5 x 10^{15} n_{eq}/cm^2	Up to 2 x 10^{15} n_{eq}/cm^2
MIP	from 4 fC to 25 fC	from 10 fC to 25 fC
Time resolution	35 - 70 ps / hit, 30 - 50 ps / track with hits from two detector layers	40 - 50 ps / hit, 30 - 40 ps / track with hits from two detector layers
Sensor(LGAD)	15x15, IHEP and USTC IME sensors with carbon	16x16 HPK or FBK or IHEP-IME,…, undecided yet

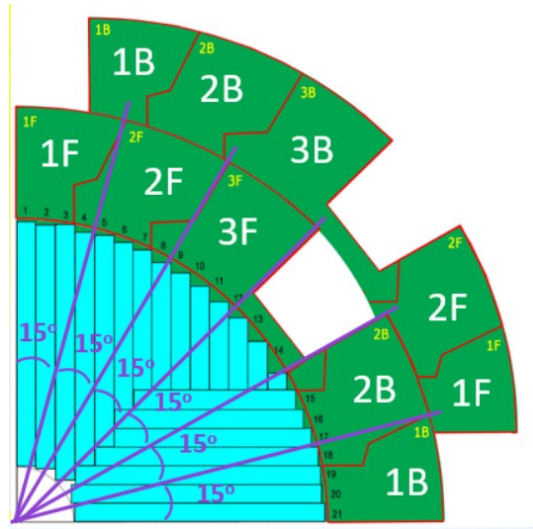
HGTD DETECTOR STRUCTURE



Each end-cap

- Two instrumented disks, rotated by 15°
- On each disk:
  - Double-sided layers mounted on a cooling plate
  - 3 ring layout for front-end modules
  - Each quadrant is exactly the same

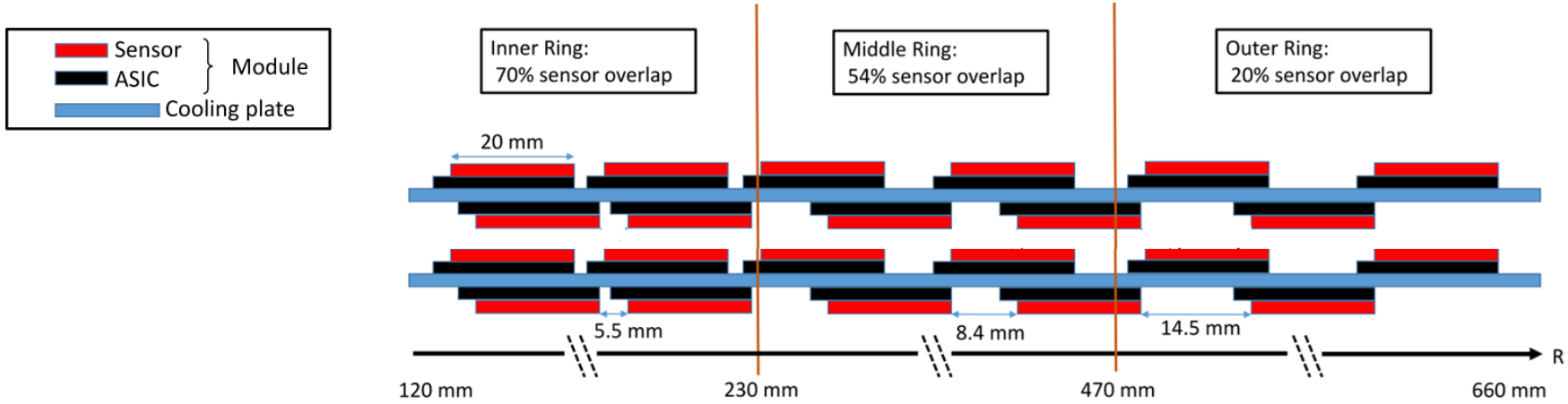




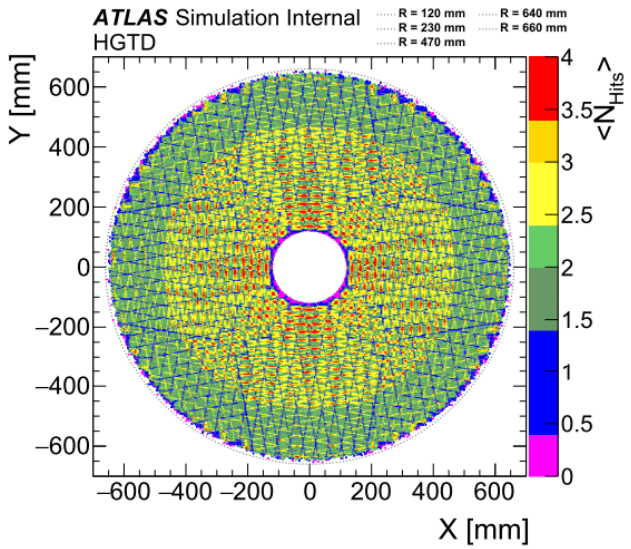
One quadrant

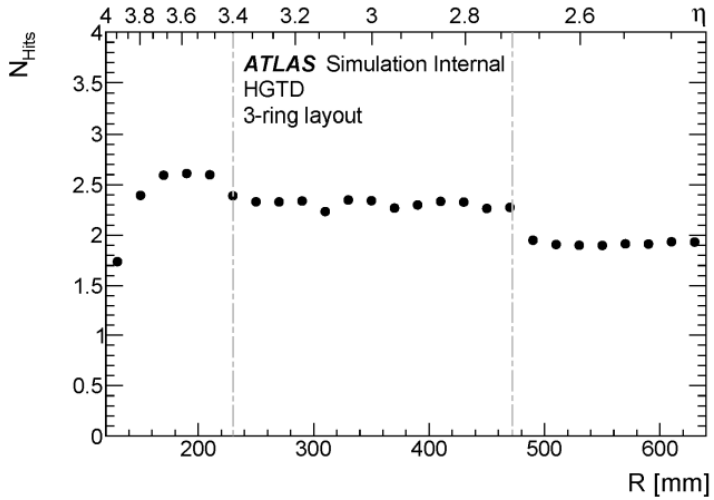
SENSOR OVERLAP IN HGTD

- 4-layer sensors with overlap from 20% up to 70%
  - Balance between timing resolution per track Vs the average number of hits

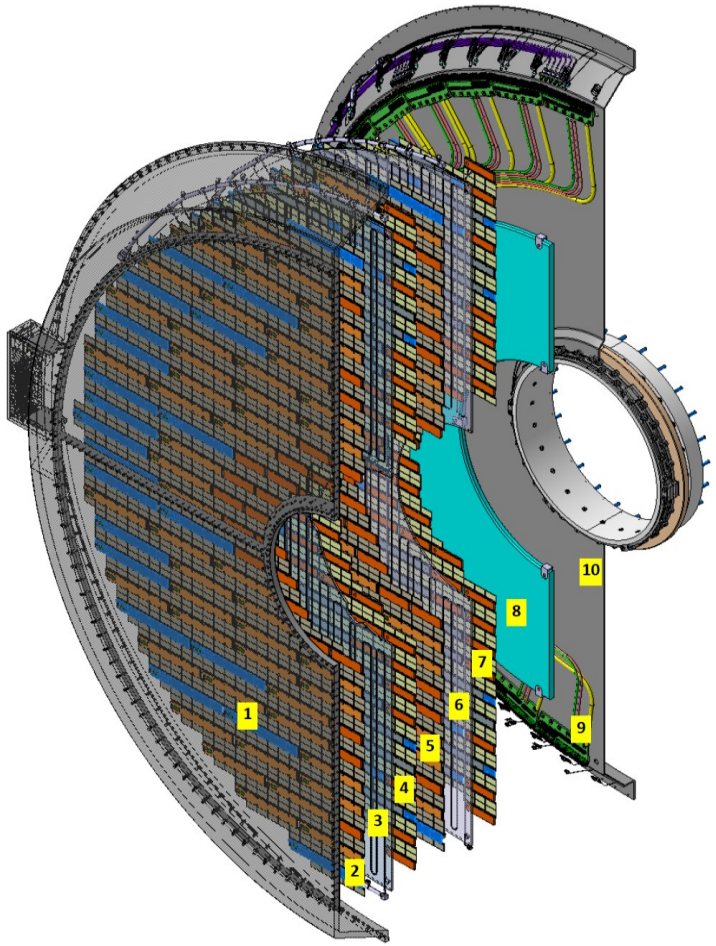


Hit multiplicity as function of x, y (left) and r (right)

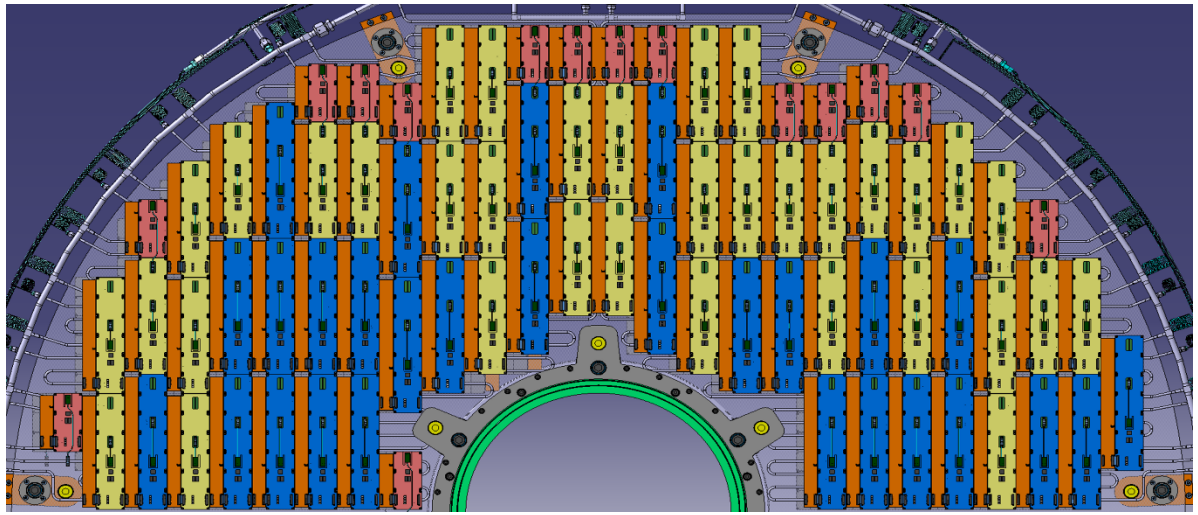




ETL DETECTOR STRUCTURE



1. Thermal screen
2. Front face of electronics of front disc
3. Front disc
4. Rear face of electronics of front disc
5. Front face of electronics of back disc
6. Back disc
7. Rear face of electronics of back disc
8. Polyethylene Moderator (PM)
9. Patch panels and cables
10. Back support plate



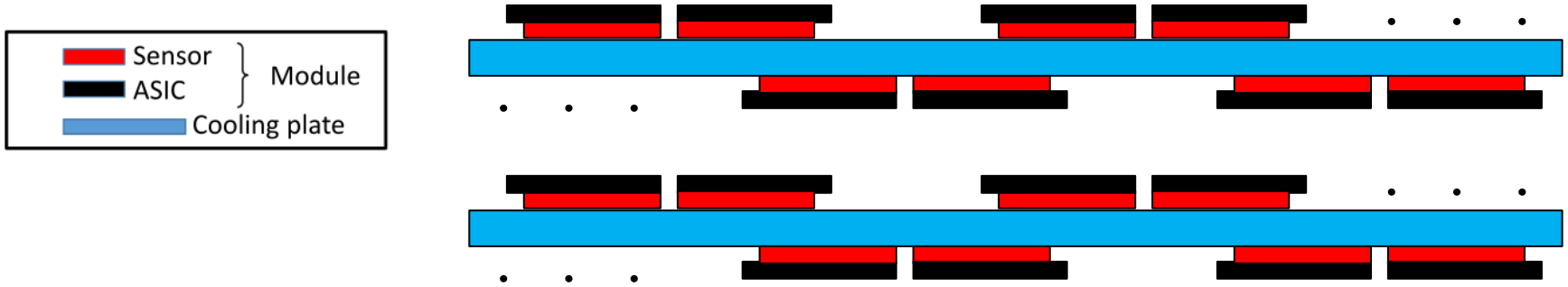
- Top half of an ETL disk (front)
  - Power boards are shown in orange
  - Three flavors of readout boards shown in red, yellow and blue interface to 3, 6, and 7 modules, respectively.

- Each endcap of the ETL detector contains 2 Al disks with embedded cooling loops.
- Each half disk is exactly the same

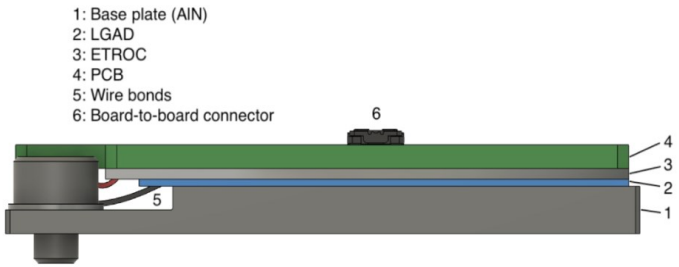
Ref: CMS MTD TDR
https://cds.cern.ch/record/2667167
https://etl-rb.docs.cern.ch/

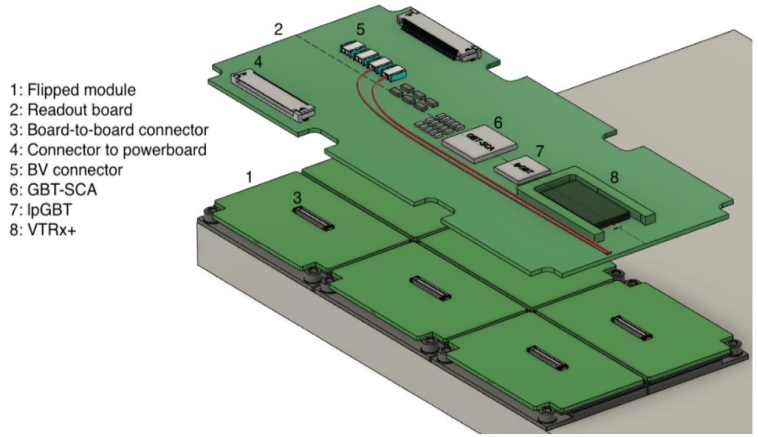
SENSOR OVERLAP IN ETL

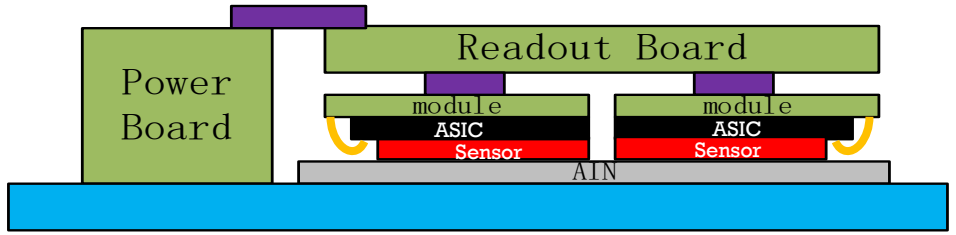
- 4-layer sensors with overlap about 33%



- Low density arrangement -> More space to install the readout board and power board
  - Fiber and 12V power cable are close to the front-end module





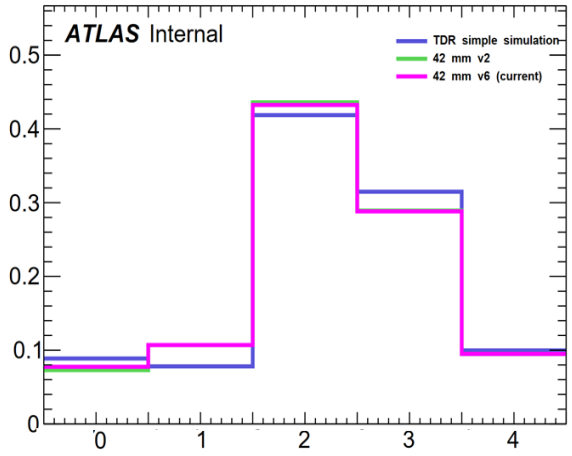


- Cross section of ETL readout unit

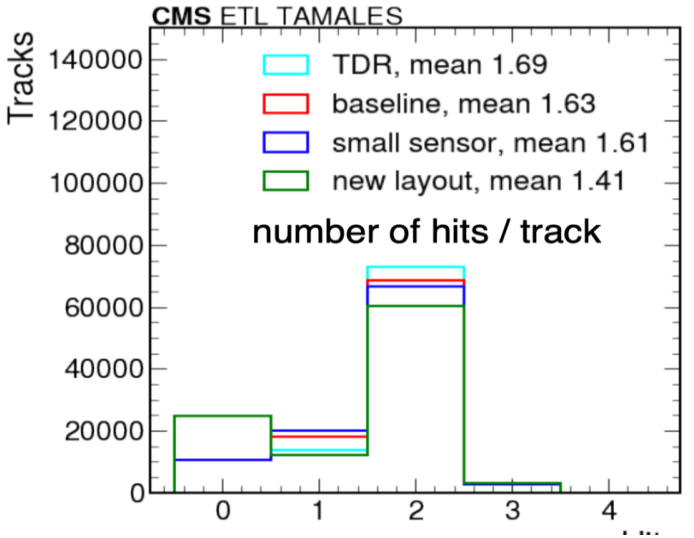
The TAMALES module (left) and service hybrid (right) designs

https://etl-rb.docs.cern.ch/

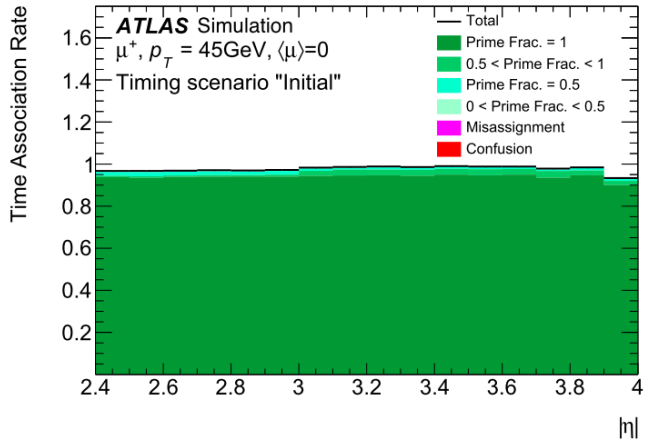
HITS PER TRACK IN HGTD AND ETL



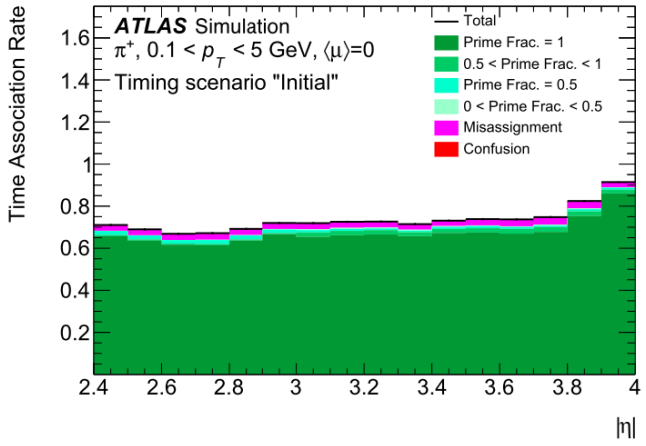
HGTD



ETL

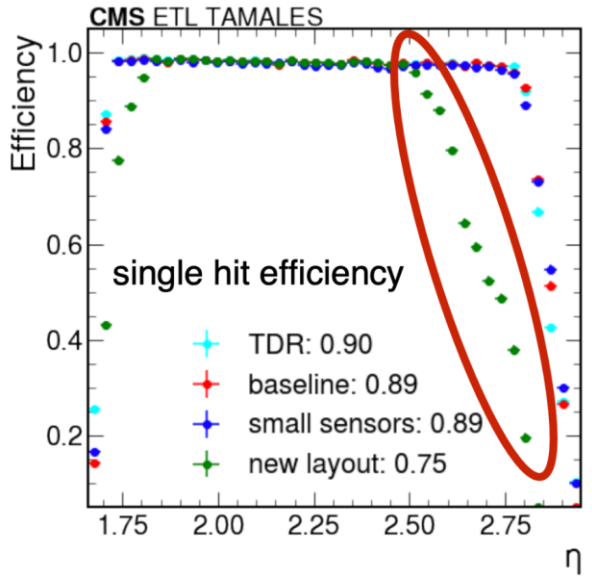


(a) Single-muon events

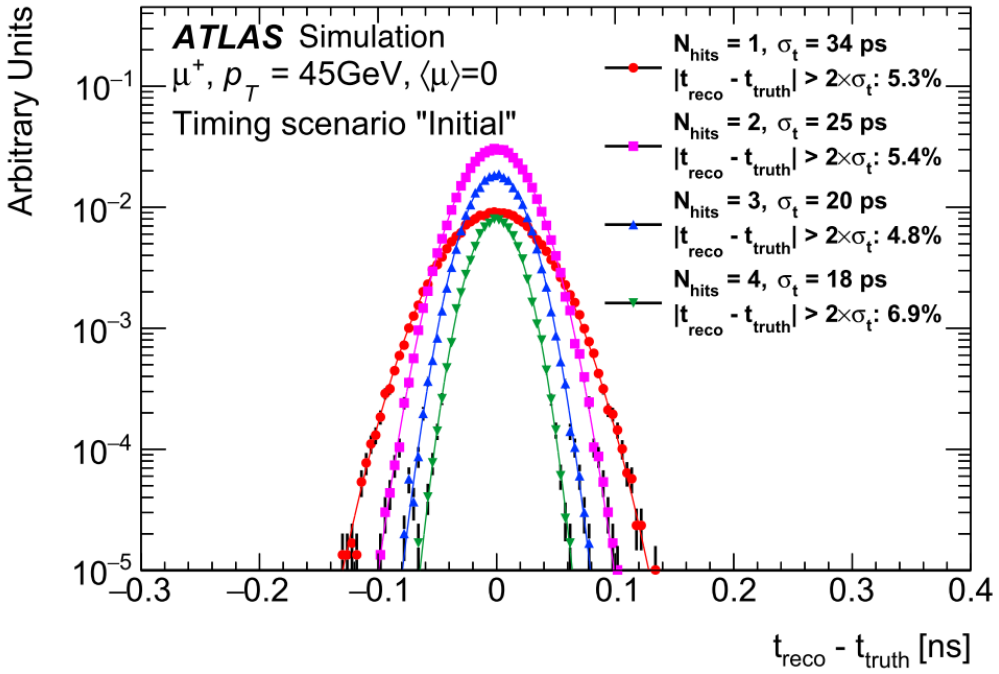


(b) Single-pion events

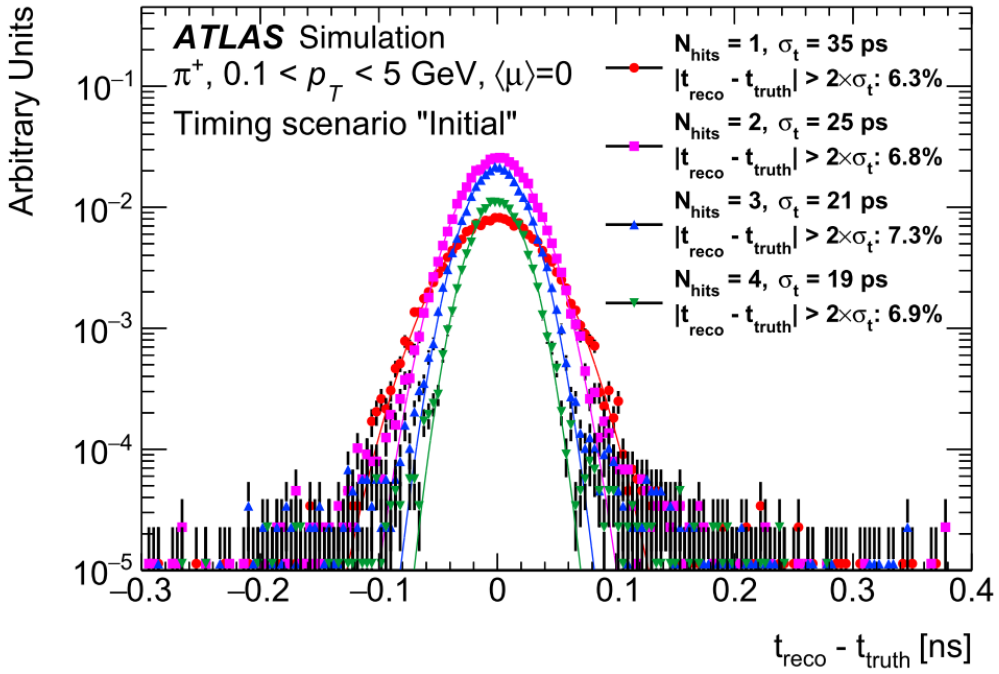
Figure 3.12: Overall time association rate for tracks as function of pseudorapidity for (a) single-muon and (b) single-pion events without pileup. A bin-by-bin breakdown of correct (green shades) and incorrect (red/magenta) hit associations is also shown. https://cds.cern.ch/record/2719855



TRACK-TIME RESOLUTION



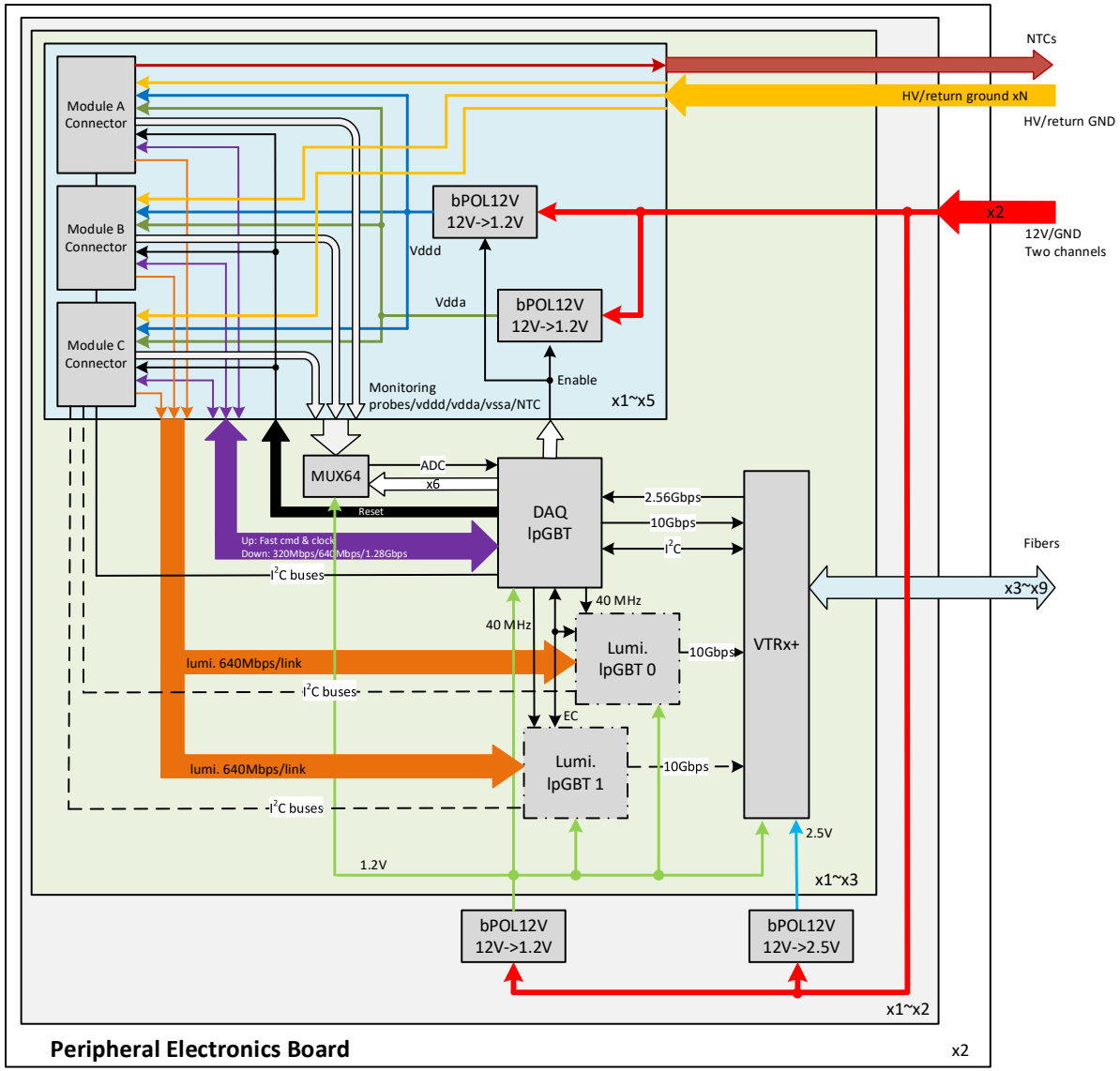
(a) Single-muon events



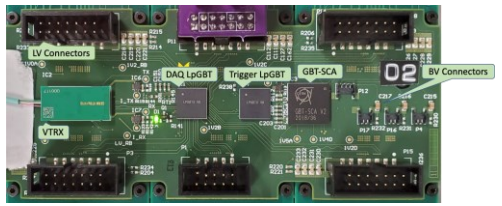
(b) Single-pion events

- The resulting track-time resolution, i.e. the difference between the measured and true track-times ($t_{reco} - t_{truth}$), is calculated for tracks extrapolated with one, two, three and four associated HGTD hits separately
- Benefit from more hits per track
  - More hits per track, better track-time resolution
- Ref: ATLAS HGTD TDR https://cds.cern.ch/record/2719855

CONSEQUENCE FOR ELECTRONICS DESIGN



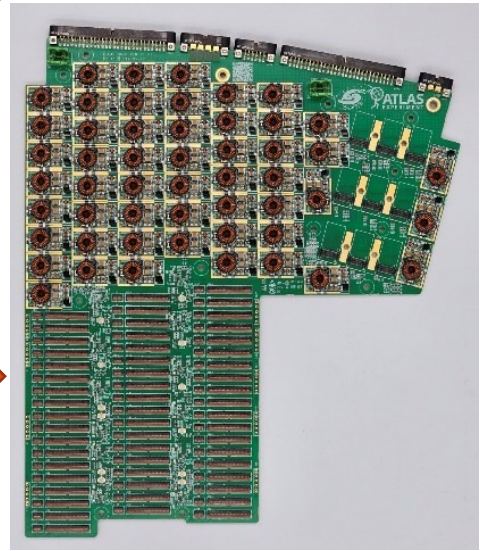
- Higher sensor overlap
  - No enough space for data aggregation, clock distribution and fast control (lpGBT, VTRx+, fiber) and power distribution (bPOL) near the sensor range
  - Readout board
    - 1~2 lpGBT -> up to 12 lpGBT
    - BUT pcb complexity is more than 12 times
      - 8 layers -> 22 layers
      - Longer transmission line for 10 Gbps
      - More IR drop for power distribution -> Need to compensate the voltage drop



Readout board prototype for 3 module service hybrid in ETL

Power board prototype in ETL

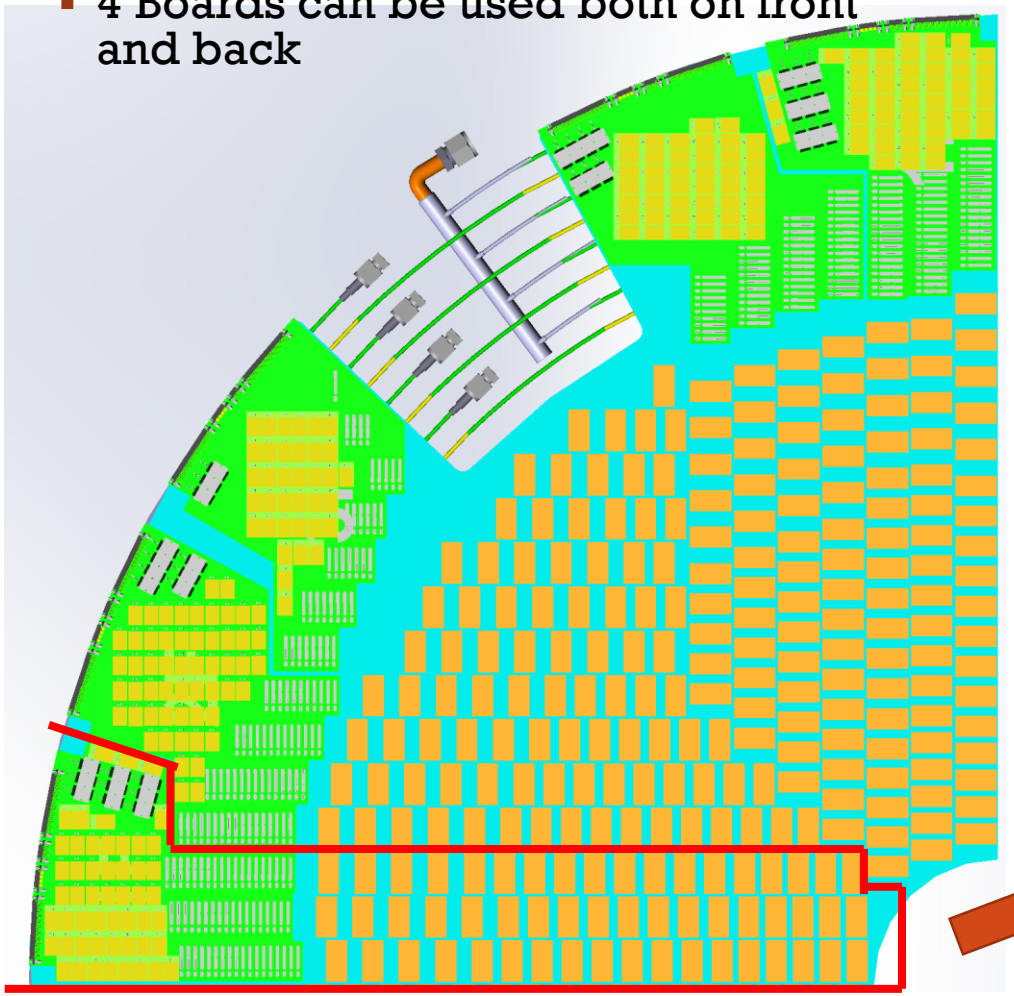
×6



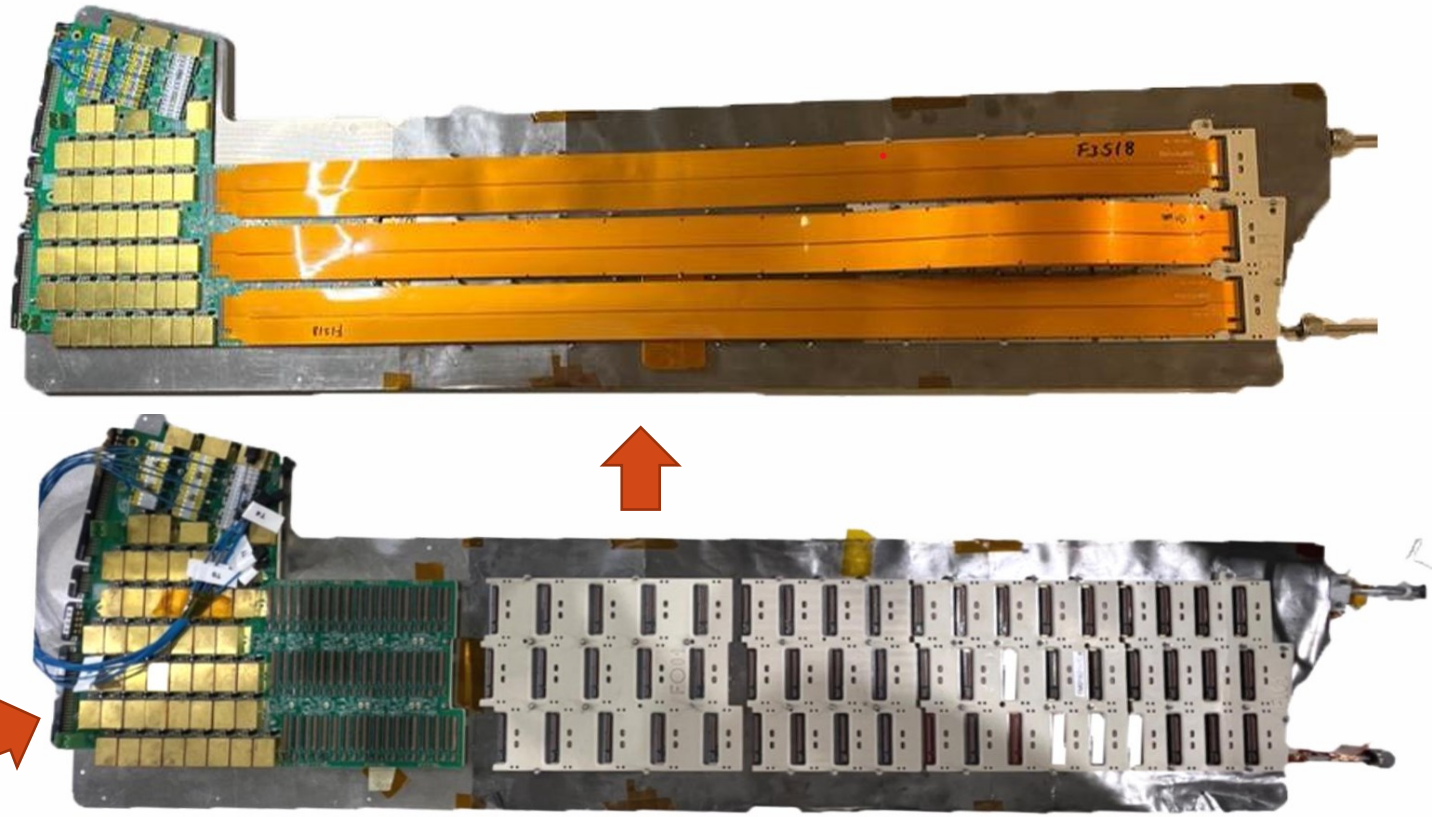
Peripheral electronics board prototype in HGTD

IN-DETECTOR CONNECTIONS IN HGTD

- Six types of PEB to be designed
  - 4 Boards can be used both on front and back

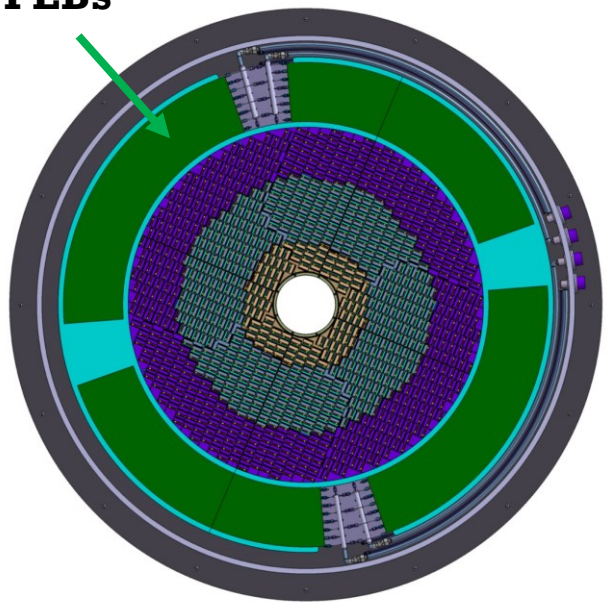


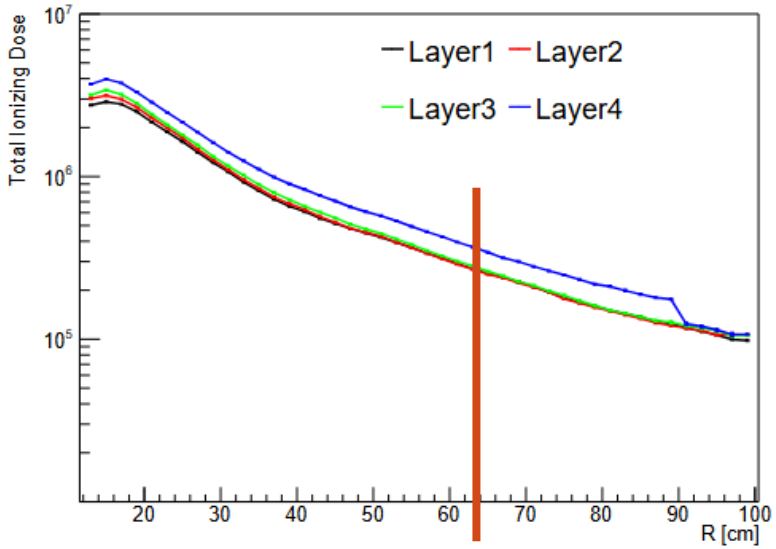
- Flex-tails use to connect the front-end modules and PEB
  - Up to 19-layer stack-up flexes in one row
  - Lengths range from about 3 to about 70 cm
  - Full detector: 77 different lengths



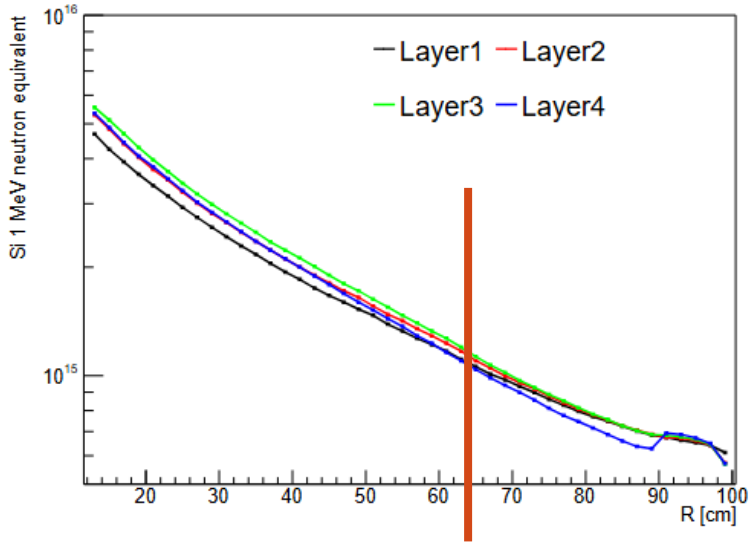
CONSEQUENCE - BENEFIT

PEBs





(b) Total Ionizing Dose $(G\gamma)$(Genat4)



(d) Si 1MeV Neutron equivalent (cm^{-2})(Geant4)

- Lower radiation requirement for data aggregation, clock distribution and fast control (lpGBT, VTRx+, **fiber**) and power distribution (bPOL)
- PEB could survive during HL-LHC Run4 (3~4 years)?

SUMMARY

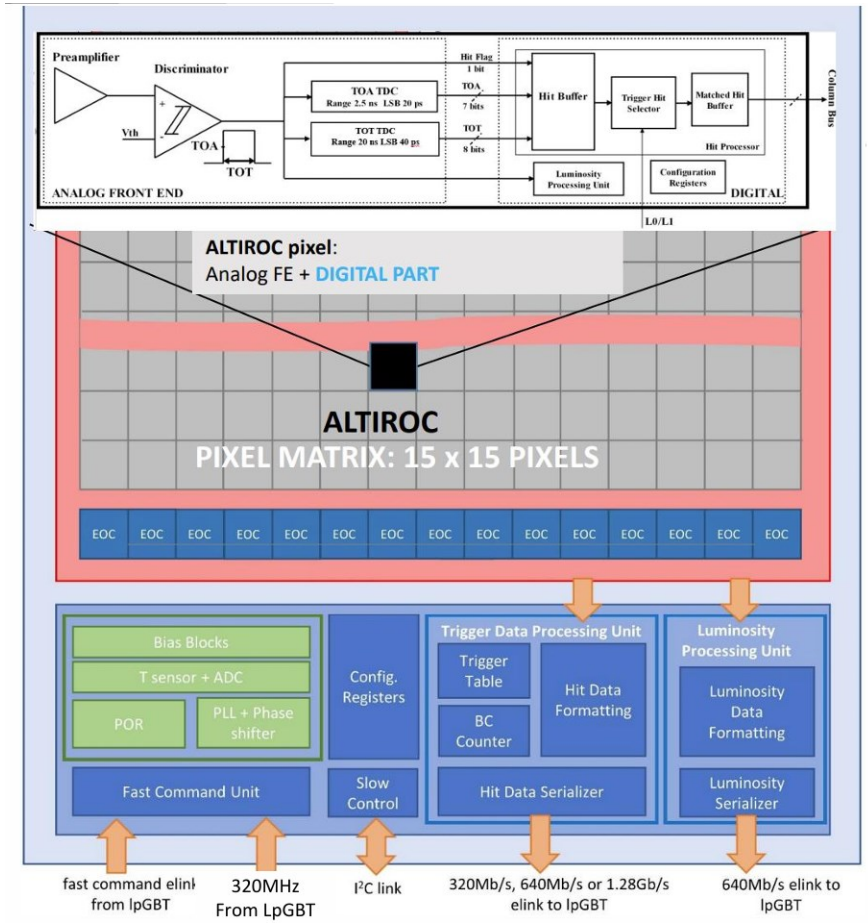
- In-depth analysis and comparison of the electronic systems of the ATLAS HGTD and CMS MTD timing detectors
- Exploring their differences and similarities in terms of design concepts and technological implementations

- In fact, there is no absolute solution that is good or bad
- Solution that suits the project requirements is the best one

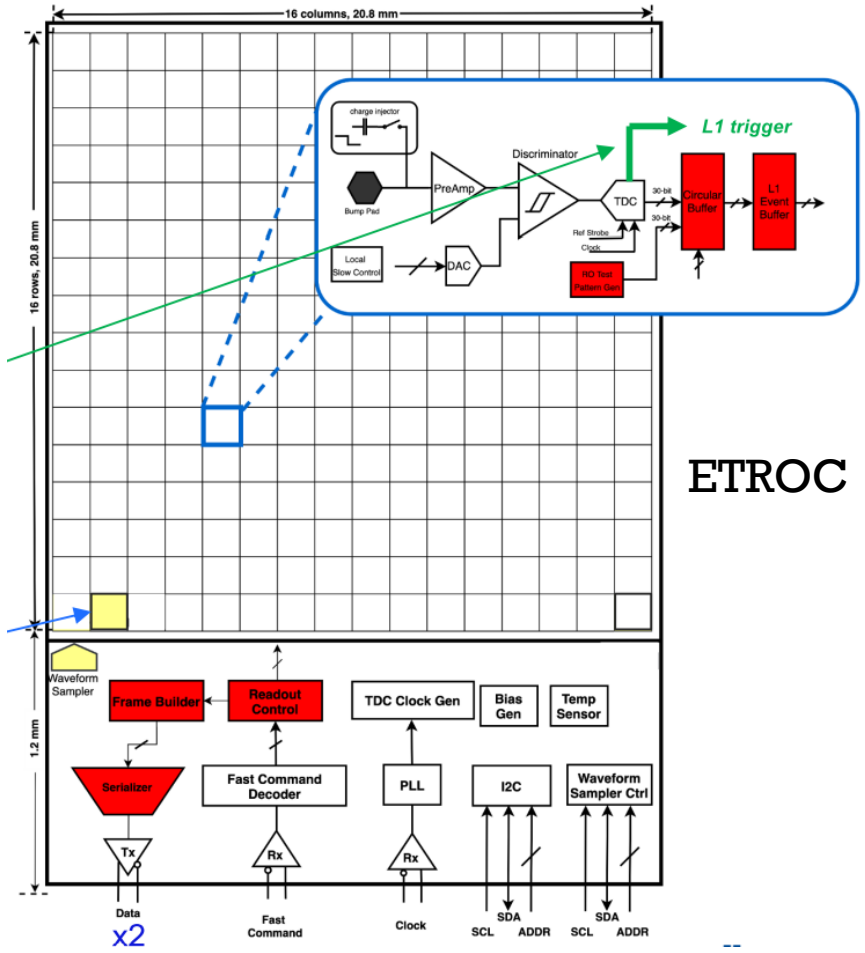
THANKS TO YOUR ATTENTION

READOUT ASIC

	ALTIROC	ETROC	Remark
Process	130 nm	65 nm	• Smaller power consumption for the digital part of ETROC • More room for decoupling caps and SRAM for ETROC
Architecture	Similar architecture with same front : TZ amplifier+ discri + TOA and TOT TDC + SRAM (10 µs for ETROC, 35 µs for ALTIROC)		
TDC	Vernier lines	"digital" TDC with a single delay line and "self calibration"	



From
https://indico.cern.ch/event/1381495/contributions/5988493/attachments/2869323/5163702/TWEPP2024_Soulier.pdf

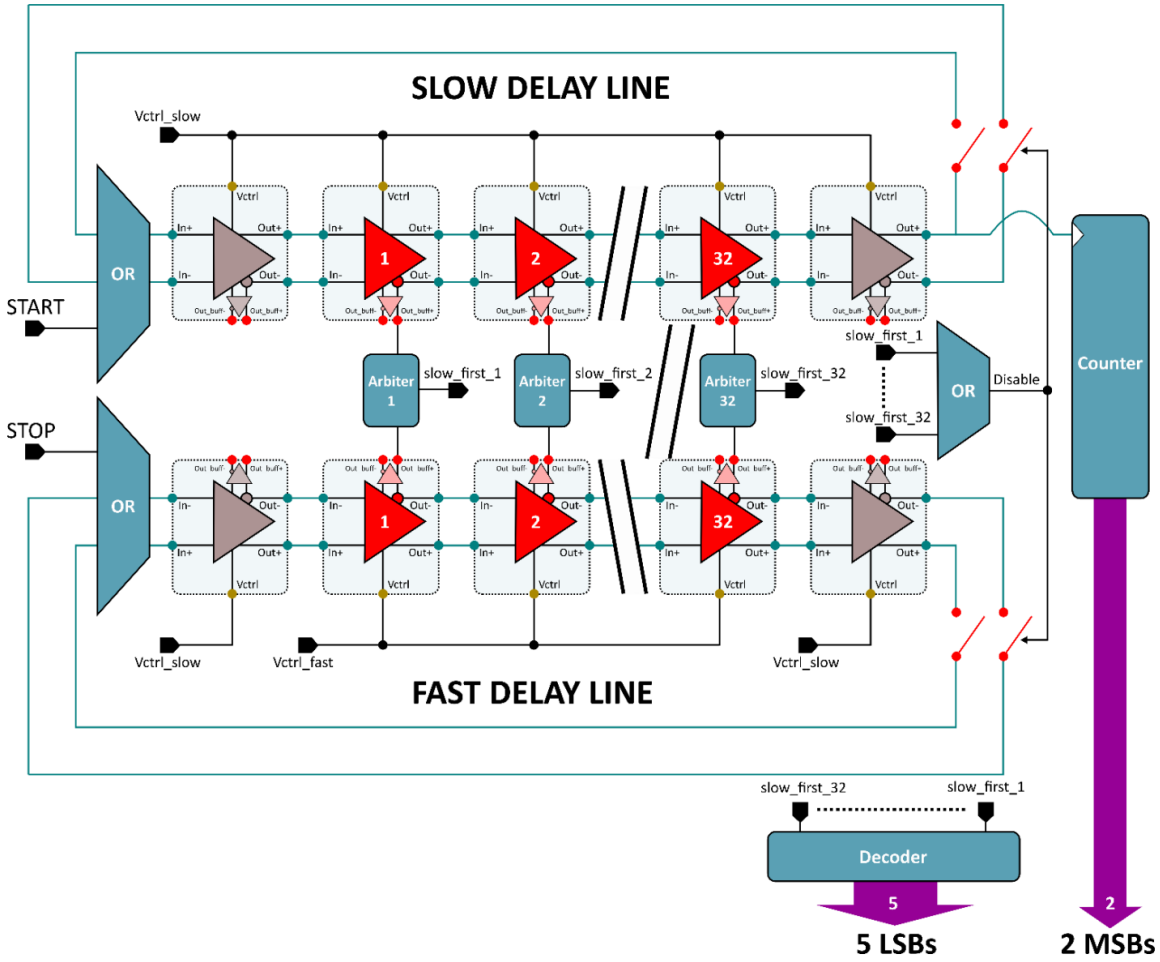


ETROC

From
https://indico.cern.ch/event/1381495/contributions/5988475/attachments/2938155/5161178/ETROC2-TWEPP-2024-final.pdf

ALTIROC TDC

ALTIROC TOA TDC: Cycling Vernier Delay Line



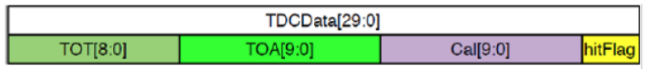
- Resolution: 20ps - Range: 2.5ns – 7 bits
  - 130 nm=> 20 ps below the gate-propagation delay in 130nm technology => Vernier delay line configuration
- Cycling configuration used in order to reduce the total number of Delay Cells.
- DLLs needed to set automatically the Vctrl of the delay lines and to compensate for temperature, power variation

ETROC TDC

ETROC TDC

1984 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 68, NO. 8, AUGUST 2021

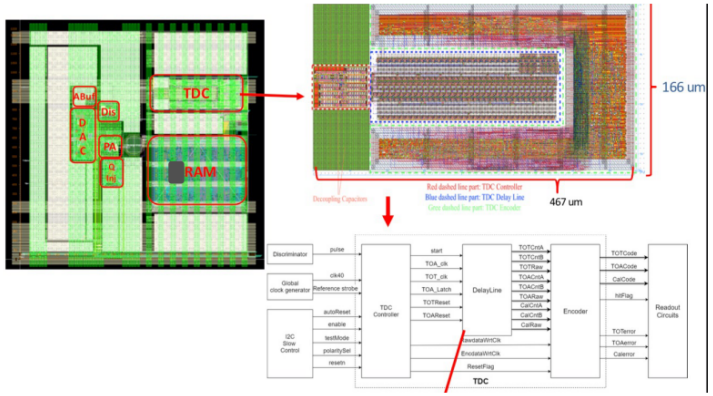
A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade



hitFlag: discriminator is fired or not

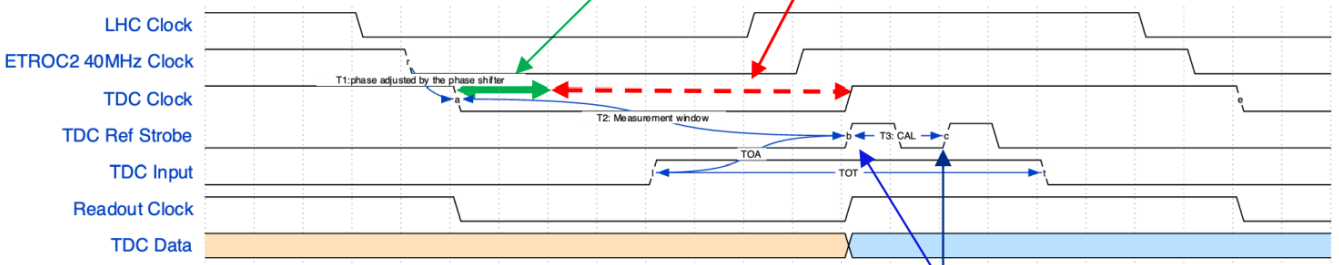
- ❑ bin= T3/Cal_code
- ❑ TOA=12.5 - bin*TOA_code

T3 is programable with 3.125 ns by default.



Normal TOA window for prompted particles from collisions

extended TOA window for long lived particles



Double time-stamps for self-calibration "on the fly", to calibrate TDC bin size in real time for every hit (very important feature of this TDC design)

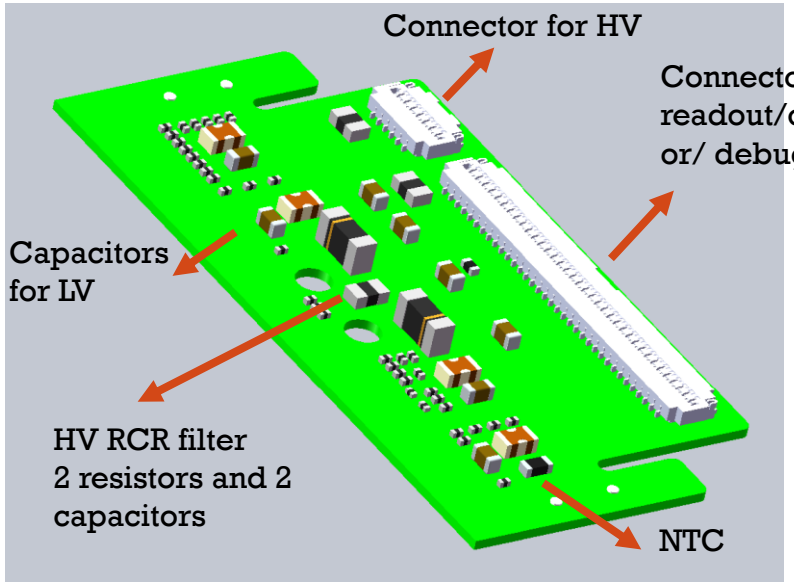
https://ieeexplore.ieee.org/document/9446843

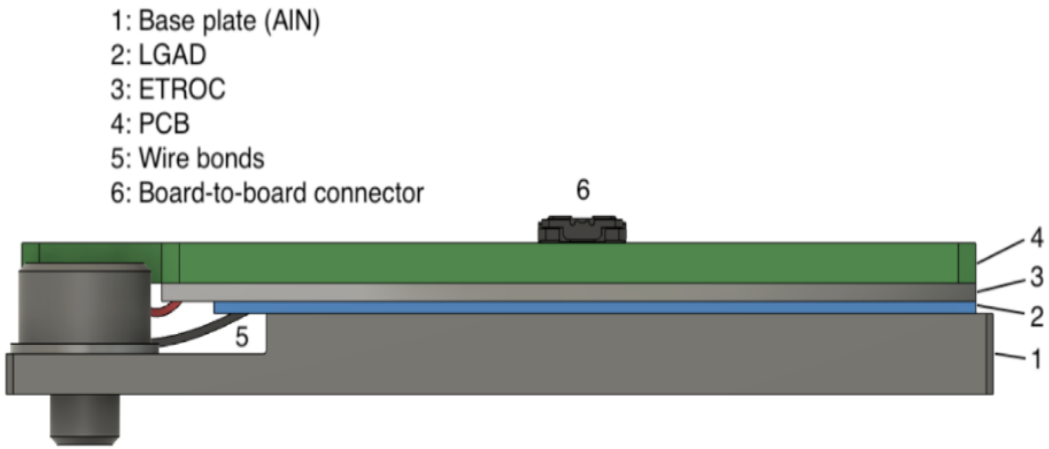
Less sensitive to temperature changes, IR drops, radiation etc…

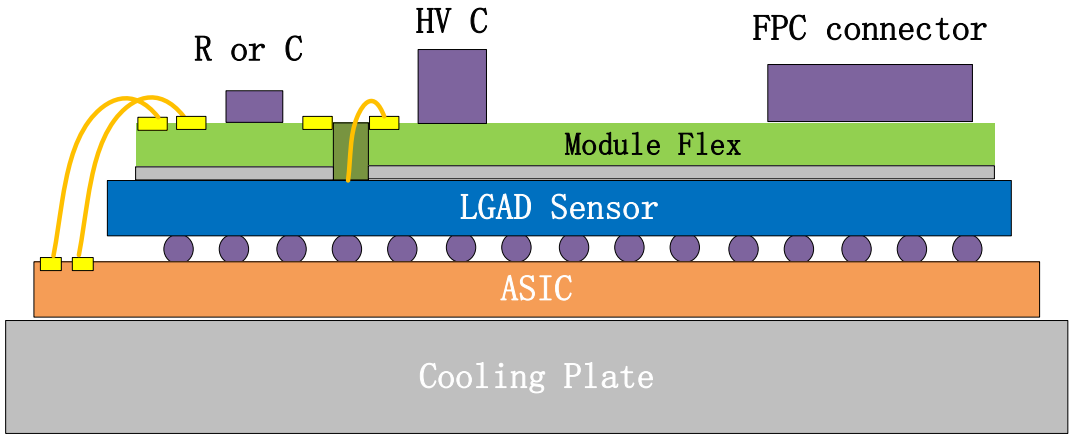
Fermilab

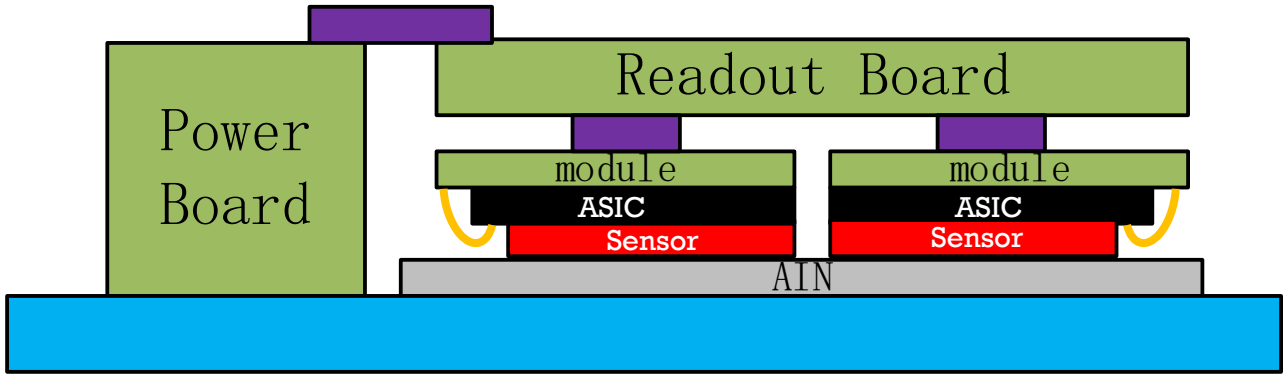
From https://indico.cern.ch/event/1381495/contributions/5988475/attachments/2938155/5161178/ETROC2-TWEPP-2024-final.pdf

FRONT-END MODULE





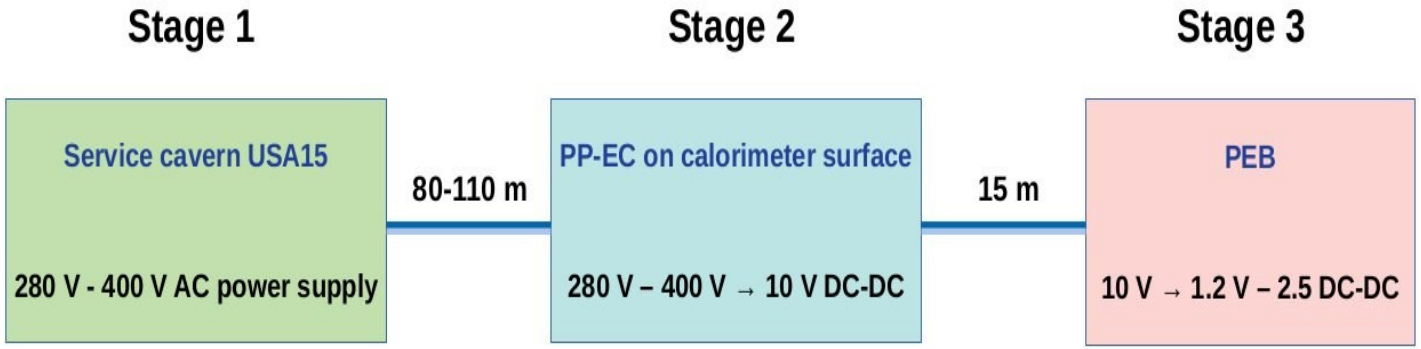




- HGTD
- ETL

LV POWER DISTRIBUTION

- HGTD



- ETL

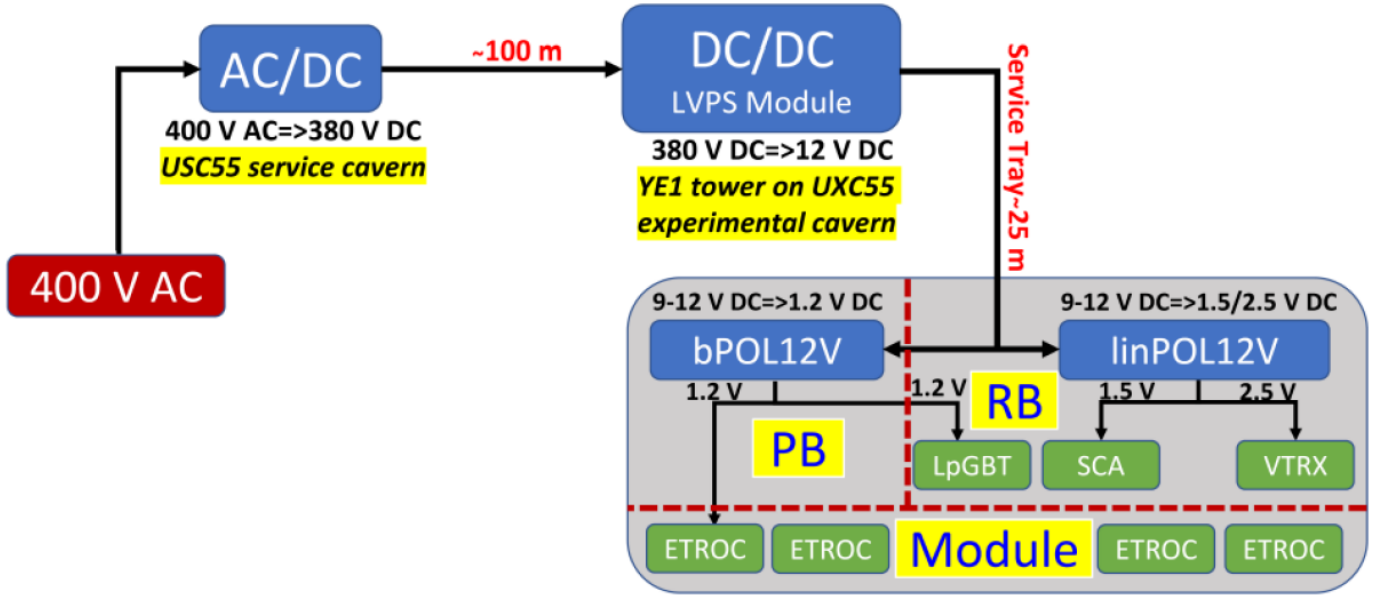


Figure 3: LV conversion scheme for ETL detector