



## The Integration of Feedback System with Machine Learning

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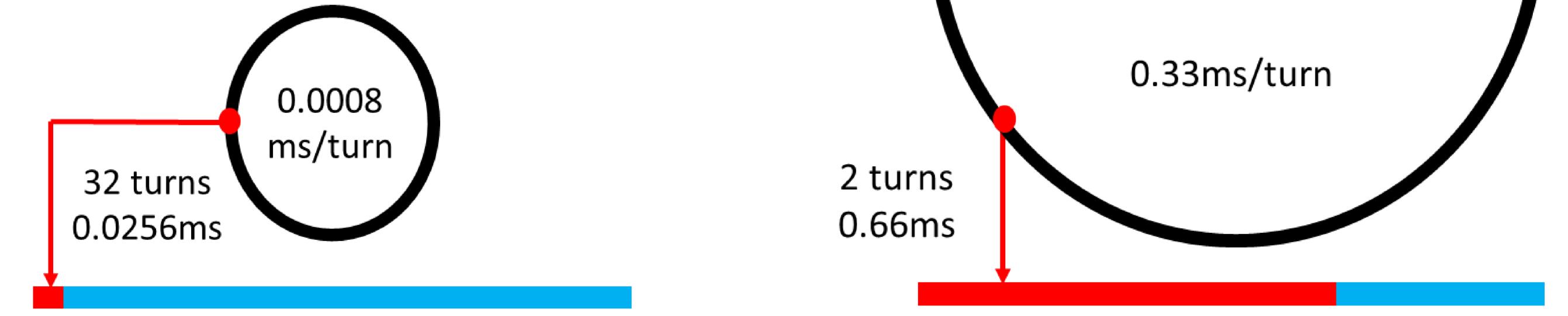
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## Abstract

For accelerators like CEPC, which have extremely large storage rings, there is a significant issue with beam instability, By utilizing appropriate machine learning techniques, it is possible to train on a large dataset of beam oscillation signals to directly compute the feedback signals required for the beam, significantly shortening the data acquisition time, achieving faster damping times than traditional feedback systems, and even realizing single-turn feedback.

## Introduction

The damping time that feedback system can provide includes the time for signal acquisition and processing. In traditional bunch-by-bunch feedback systems, the filter processes signals that require data collection over multiple turns. The effect of this data acquisition time on the damping time is not prominent in smaller circumference storage rings, but it can become a major issue in the CEPC, potentially resulting in damping times comparable to the instability growth times.

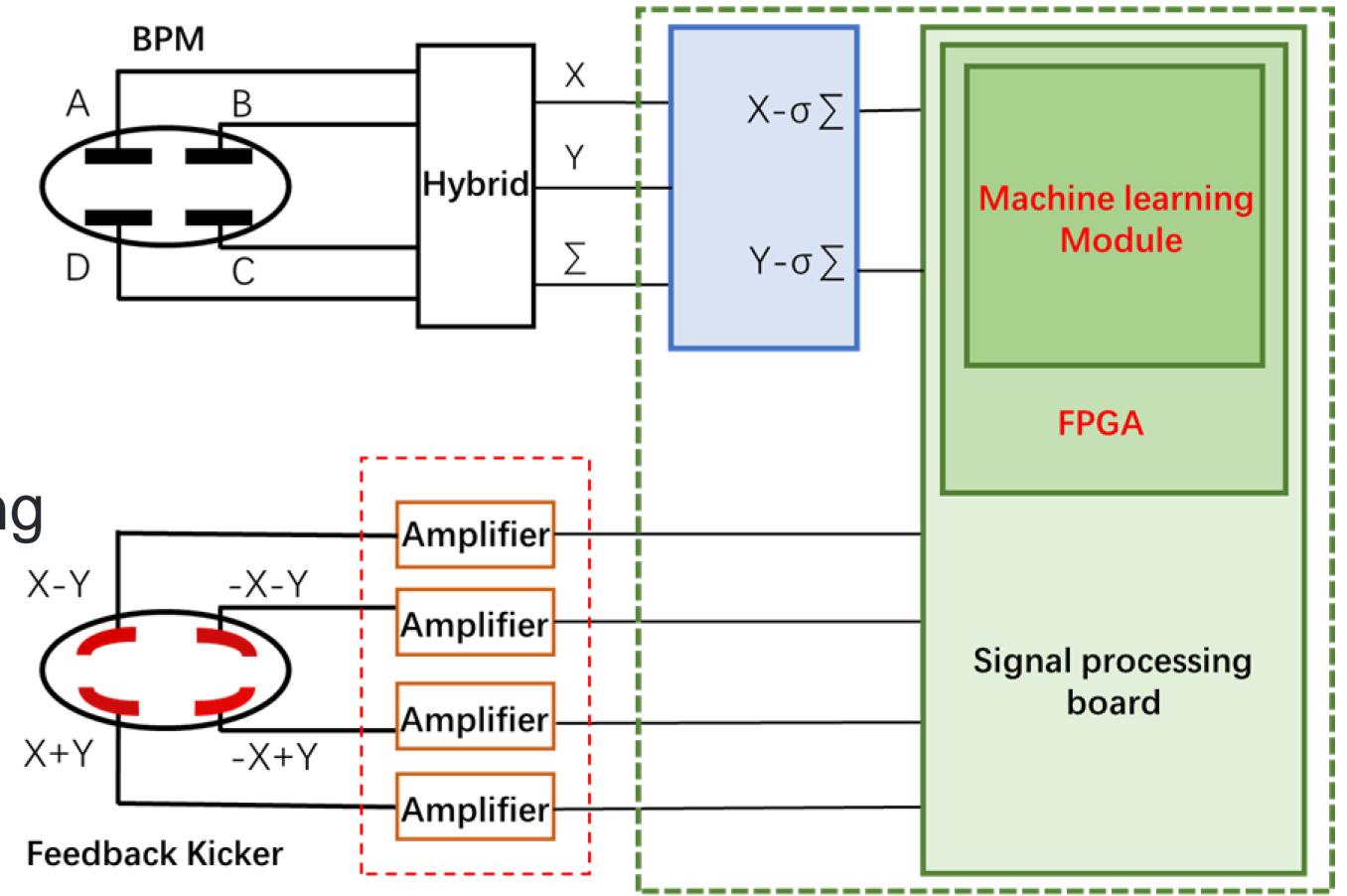


Using traditional feedback methods, the time taken for data acquisition will occupy at most 2/3 of the damping time.

CEPC Damping Time 1ms BEPCII Damping Time 0.5ms Comparison of the time taken for data acquisition by the feedback systems in small rings (BEPCII) and large rings (CEPC) relative to the damping time.

## Method

Implementation of Closed-orbit Signal **Cancellation based on Digital/Analog Circuits** Oscillation Information Acquisition Based on **Machine Learning** Acquire the dataset of X and Y direction signals



calibrated by the oscillation signals, and select an appropriate neural network to perform machine training on the dataset. Establish a suitable machine learning model, test its signal processing effectiveness in software, and compare it with actual signals. Subsequently, optimize the processing speed and the machine learning model. Debugging of the Signal Processing Card and Implement the machine learning model in the FPGA **FPGA Implementation** 

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