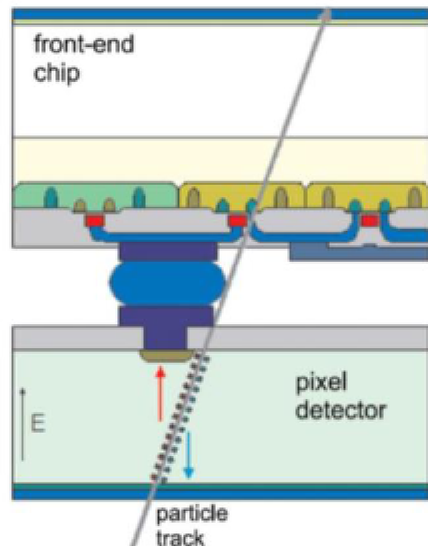
Development of Hybrid*
4(- 5?) D**
Prototyping Tools & Techniques

Discussion Topic for Mixed Electronics & Tracking Session

Friday Afternoon @ CEPC



Readout
ASIC chip

The sensor

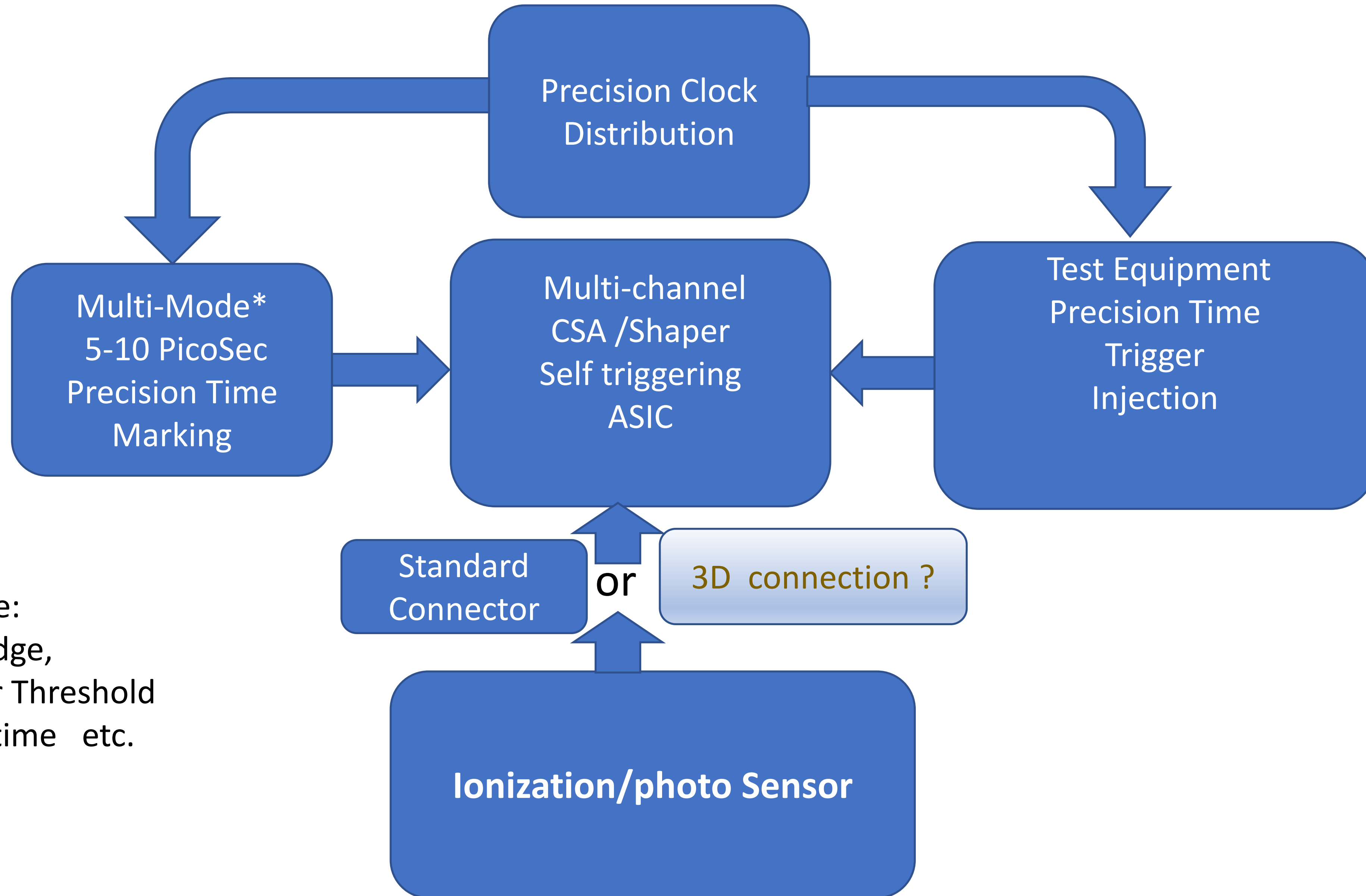
Hybrid detectors

Yang ZHOU -CEPC workshop
Hangzhou 23-27/10/2024

* Hybrid : Readout and Sensor separately fabricated.

** 5D (x, y, z, t, q)

Elements of a common 3-4D tracking detector Prototype



* Multi-mode:
  Leading Edge,
  Time Over Threshold
  Or Peak time etc.

Discussion to explore the benefits of a common Test bench for both electronics and sensors

- Common Readout
- Sensor to Electronics Connectors /packaging
- ASIC interface

Non Standard Detectors

Many Interesting sensor materials are not CMOS ASIC compatible

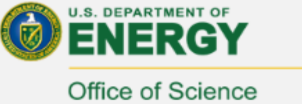
- Continued exploration of LGAD Silicon.. . + Rad Hard variants
- GaN band gap 3.39eV large displacement energy 110eV N, 45eV Ga (with gain?)
- Diamond (3D posts? , with gain?)
- GaAs, CdTe, CZT

Hybrid Electronics developments

Characterization of the BigRock 28 nm Fast Timing Analog Front End

Amanda Krieger[1], Kennedy Caisley[2], Maurice Garcia-Sciveres[1], Carl Grace[1], Timon Heim[1], and Zhicai Zhang[1]

[1]*Lawrence Berkeley National Laboratory, Berkeley, CA (USA),* [2]*University of Bonn (Germany)*

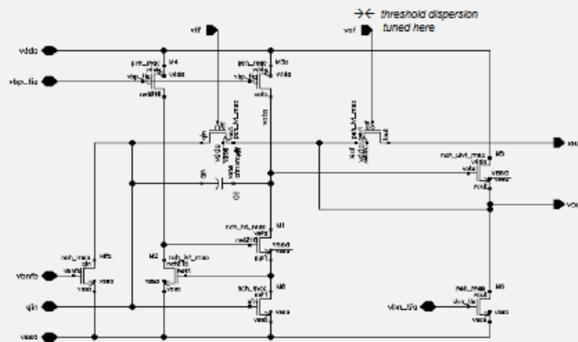


Summary

A succession of design refinements have been implemented in a common 2x2 mm 28 nm testbed ASIC series—BigRock, Pebbles, and MetaRock. **Pebbles**, the device now being characterized in the lab, implements an array of on-chip input capacitor loads for characterizing the BigRock AFE performance from 0 to 100 fF. Noise, ToA and ToT timing dispersion, ToT-vs-Qin, and timewalk are covered herein. MetaRock (FY24) is the final prototype in the series. It features a more efficient, faster revision of the BigRock CSA, and includes a full timing and charge readout AFE with a new low power analog TDC suitable for implementation in a next-generation pixel readout ASIC for HL-LHC upgrades or other 4D tracking applications.

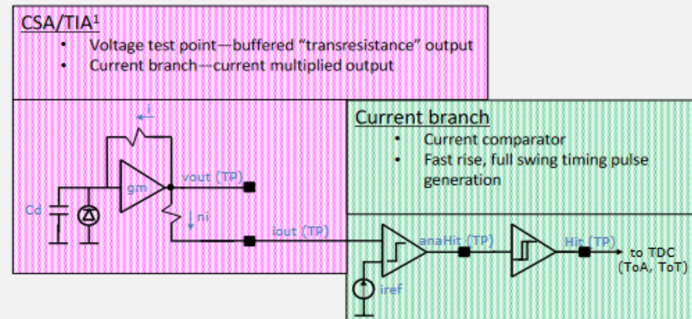
BigRock CSA

- The CSA is a typical regulated cascode design
- The input current pulse (charge) is mirrored forward to the current comparator as the signal
- The mirror factor is determined by ratio of *vaf, vff*



BigRock Analog Front End (AFE)

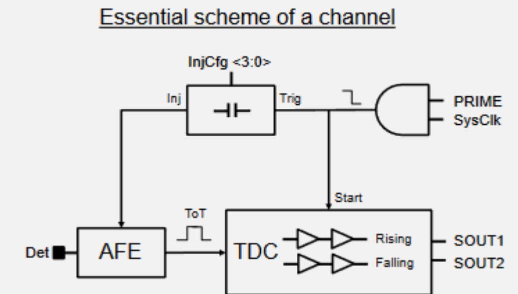
- The CSA topology follows the design described in ref. 1
- "Pseudo-TIA" (very fast pulse peaking time (3-10 ns) that is optimal for low jitter)
- The signal current presented to the current comparator is multiplied by ratio "n", where "n" is implemented as a transistor ratio and control voltage differential



1. Pierre Jarron, et. al, *A transimpedance amplifier using a novel current mode feedback loop*, 1996

On-chip testbench

- TDC and programmable charge Injection circuit
- Charge injection is synchronized with TDC start



BigRock, a Fast Timing Front End for Future Pixels in a 28 nm CMOS Process , Zhicai Zhang, TWEPP 2022

Timespot-1 *28nm 32 X 32 sensor RO matrix*

Test setup consists of five tracking layers in a row each having 3mm² area .

* *3 layers with trench silicon layers*
* *2 layers with 3D column diamond sensors*

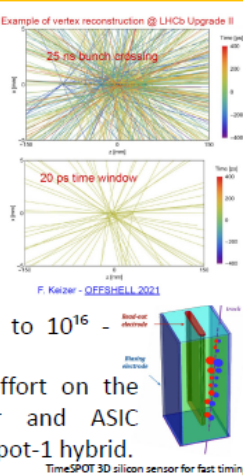
A prototype 4D-tracking demonstrator based on the TimeSPOT developments

Angelo Loi, on behalf of the IGNITE and TimeSPOT Experiments

INFN · IGNITE · TimeSPOT

Introduction: We present first results obtained with a prototype 4D-tracking demonstrator, using sensors and electronics developed within the TimeSPOT project, and tested on a positive charged pion beam at CERN SPS. The setup consists of five small tracking layers in a row, having area of about 3 mm squared each, three of which equipped with 3D-trench silicon sensors and two with 3D-column diamond sensors. The five layers are then read-out by a KC705 Xilinx board on a PC. We describe the demonstrator structure and operation and illustrate results on its tracking capabilities.

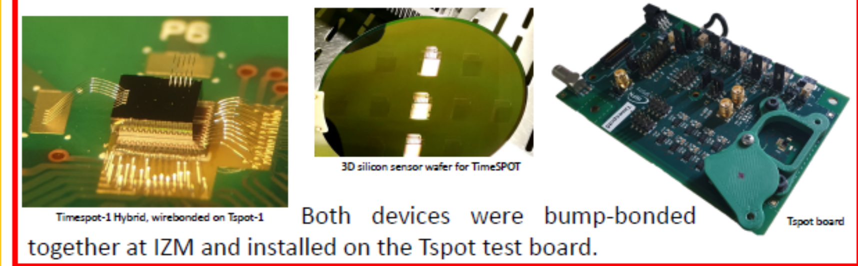
Context: At future experiments at the Hi-Lumi LHC, 4D (space and time) tracking is a crucial ingredient, necessary to avoid high event pile-up which inevitably would decrease overall detector efficiency.
The requirements for a future LHCb-VELO like 4D tracking detector are a space resolution around 10 µm, a time resolution better or equal to 50 ps, as well as a radiation hardness up to 10^{16} - 10^{17} MeV neq/cm².
The TimeSPOT project focused its effort on the development of innovative sensor and ASIC technologies, culminating in the Timespot-1 hybrid.



TimeSPOT 3D silicon sensor for fast timing

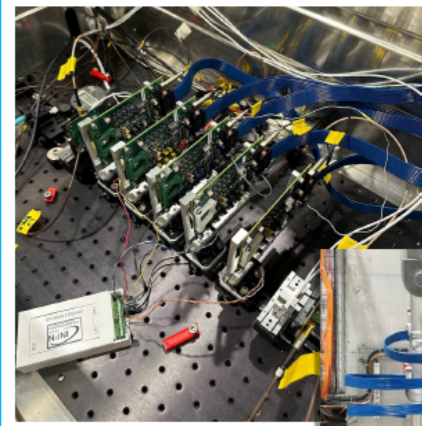
Device under test: Within TimeSPOT, the hybrid Timespot-1 has been developed and fabricated. The ASIC is a 32x32 pixel matrix with each channel having its own TDC and pitch of 55 µm. It is connected on a 32x32 sensor matrix in 3D silicon sensor technology.

Timespot-1 ASIC Layout and single channel architecture


Timespot-1 Hybrid, wirebonded on Tspot-1 · 3D silicon sensor wafer for TimeSPOT · Tspot board

Both devices were bump-bonded together at IZM and installed on the Tspot test board.

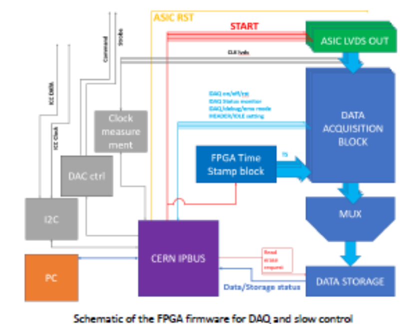
Setup: Test-beam campaign performed during May 2023. Setup consisted in 5 tracking stations, 3 made of Timespot hybrids with silicon matrix and 2 with diamond pixel matrix.


Inner view showing 5 Tspot boards used as tracking stations

Each station was controlled by an independent IIC interface board.

DAQ and system sync has been implemented within a customised firmware implemented on a KC705 fpga board, which also has a IIC interface as backup.

External view of the setup, diplaying FPGA and mezzanine (green boards), IIC interface (white boxes) and clock generator (blu board)



Schematic of the FPGA firmware for DAQ and slow control

The firmware of the DAQ was developed around the ipbus firmware (https://ipbus.web.cern.ch/) which allowed a fast development and easy communication with the FPGA.

The ipbus software package allowed the development of a custom graphical user interface used to control DAQ and system synchronisation.

A prototype 4D-tracking demonstrator based on the TimeSPOT developments, **Angelo Loi (INFN, Cagliari), TWEPP 2023**

The INFN - IGNITE initiative

Integrated system composed by a LARGE hybrid 28nm CMOS ASIC and pixel Sensor MATRIX

considering all the challenges in realizing such a device:

- Obtain uniform timing performance over a large area
- Minimize power consumption
- Distribute data to the read out etc.

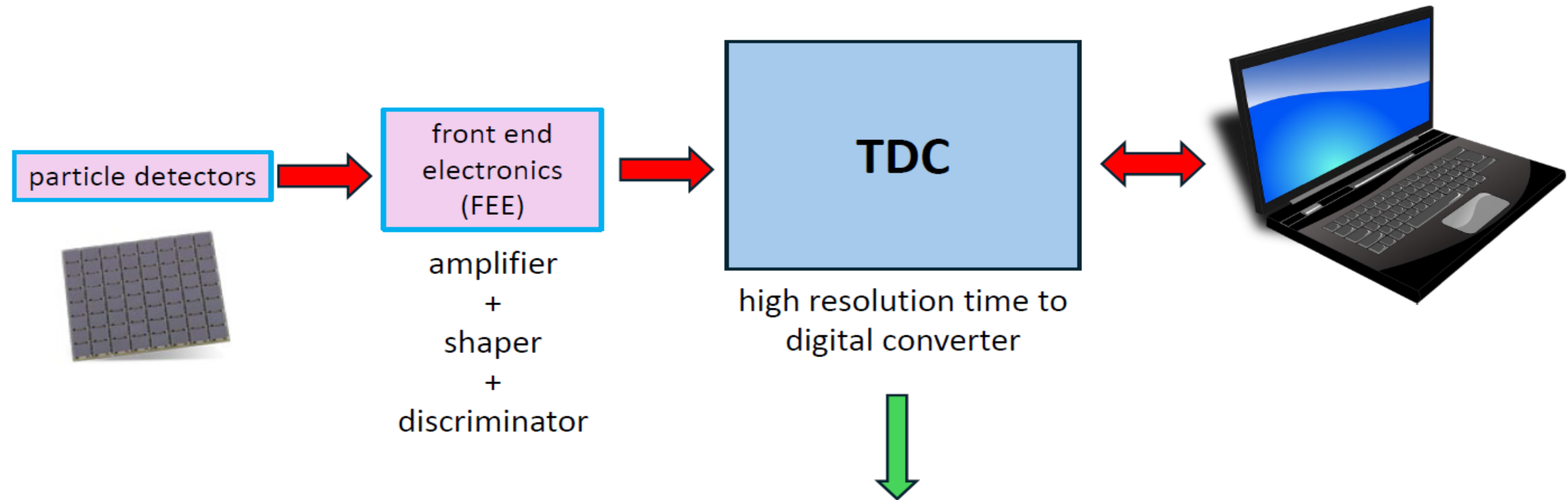
GOAL: DEVELOP A TRACKING SYSTEM SUITABLE FOR HIGH LUMINOSITY CONDITIONS

Take advantage of the experience obtained from the previous INFN R&D projects (Timespot, Falaphel etc..)

Explore innovative 3D technologies and vertical connections (TSVs, Face2Face or Face2Back bonding)

First results on the Ignite-0 test ASIC in CMOS 28-nm technology, Gian Matteo Cossu (INFN, Cagliari), TWEPP 2024

Pico TDC



Our goal was to build **a flexible high resolution timing measurement device** able to:

- connect to multiple detector types + FEE with standard connectors
- provide high data bandwidth towards a PC via standard interfaces (Ethernet + USB3)
- provide the best achievable timing resolution on a lot of channels (128)

Design, test and performance of a PicoTDC based board, Davide Falchieri (INFN, Bologna*)*, TWEPP 2024

The picoTDC ASIC from CERN

40 MHz clock

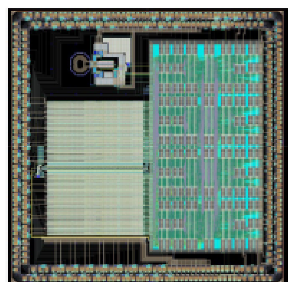
trigger

64 channels

4 8-bit readout ports

sync clock

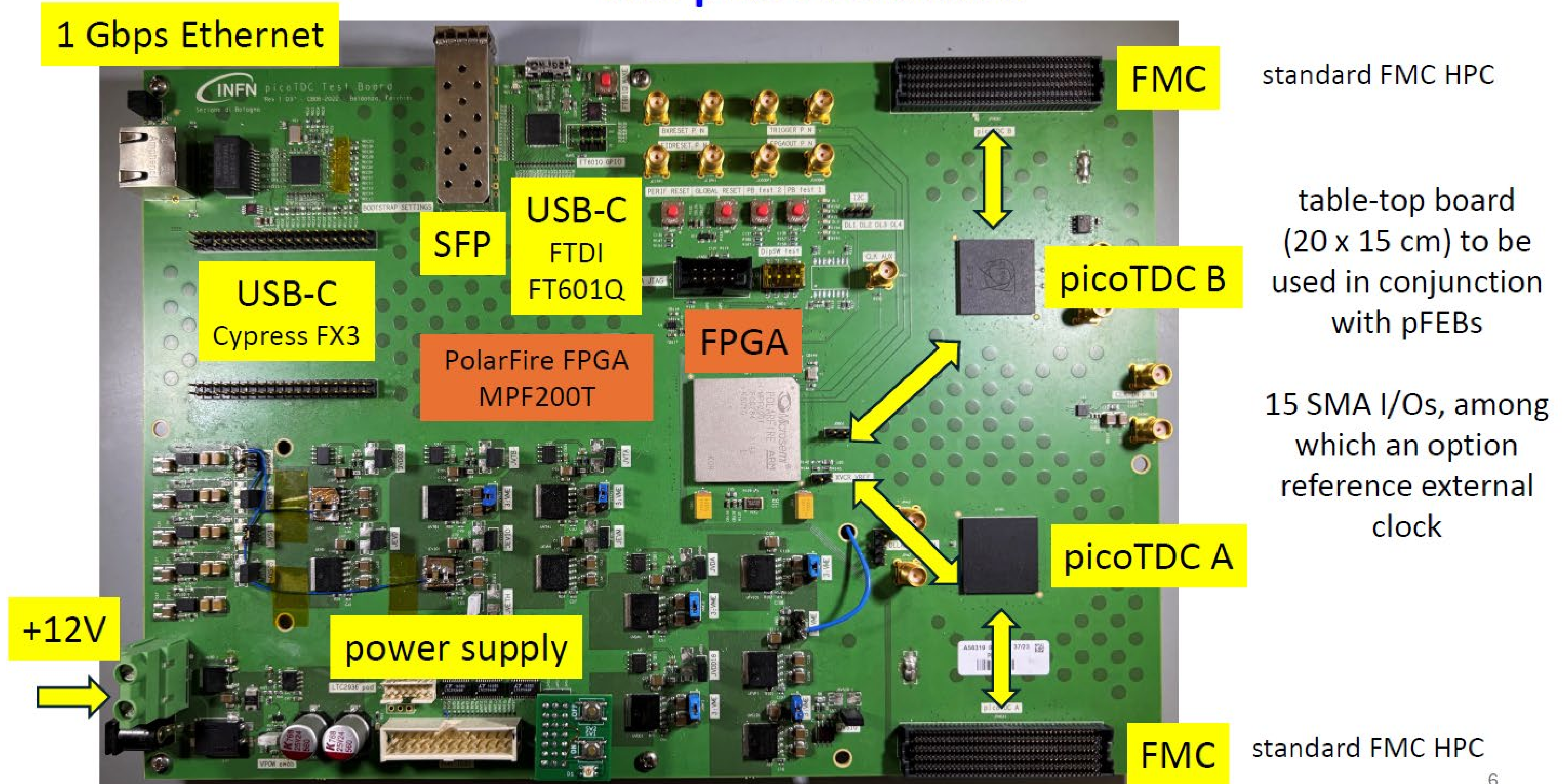
40MHz Ext ref.
PLL
40MHz
80MHz
160MHz
320MHz
1.28GHz
1.28GHz ... 40MHz
Counters
Trigger interface
Trigger buffer: 512
Trigger, Resets
Control, Programming, Monitoring
I²C
320MHz
Hits x64
Leading
Trailing
TOT
x16
Hit register
Interpolation decoder
TDC channel
Buffer: 512
Trigger matching
x16
Readout buffer: 512
8 Bit 40,80,160,320M
x8
Readout 1/4 Ports
Data rate 320Mbps -10Gbps (4MHit/s per channel)
Sync



picoTDC main features:

- bin size: 3.05 ps (fine resolution) or 12.2 ps (coarse resolution)
- single shot resolution: <3.3 ps in fine mode or <4.2 ps in coarse mode
- measurement range: 204.8 μs
- measurement scheme: triggered or un-triggered time-tagging

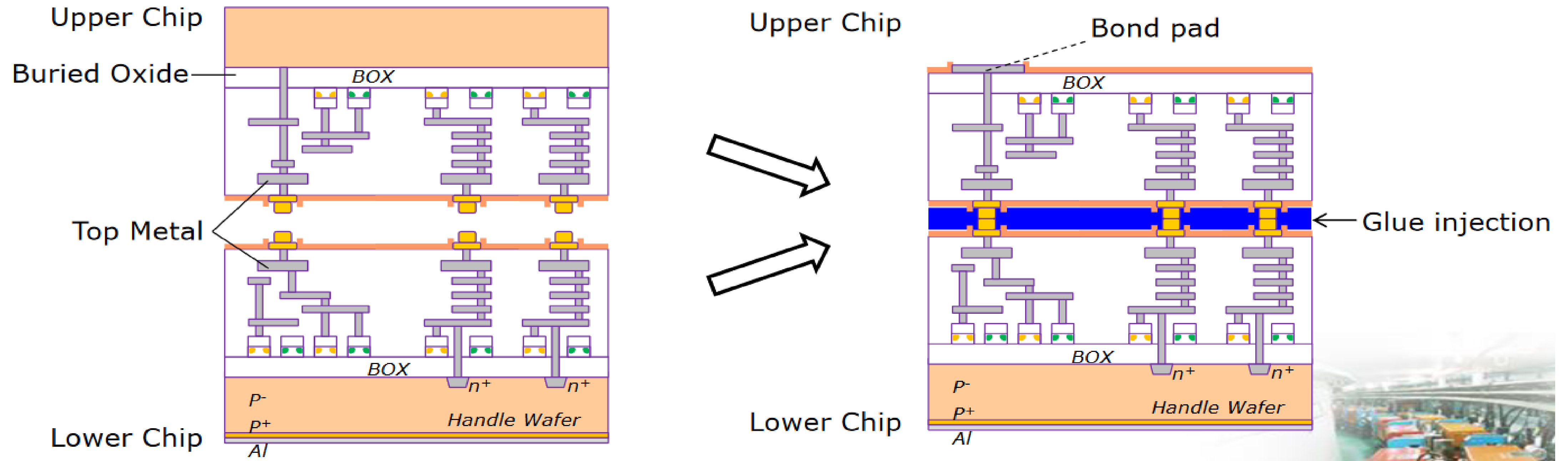
The picoTDC board



3D-SOI vertical integration

Originally developed by T-micro and KEK in Japan and demonstrated on the SOFIST 3D chips for the ILC

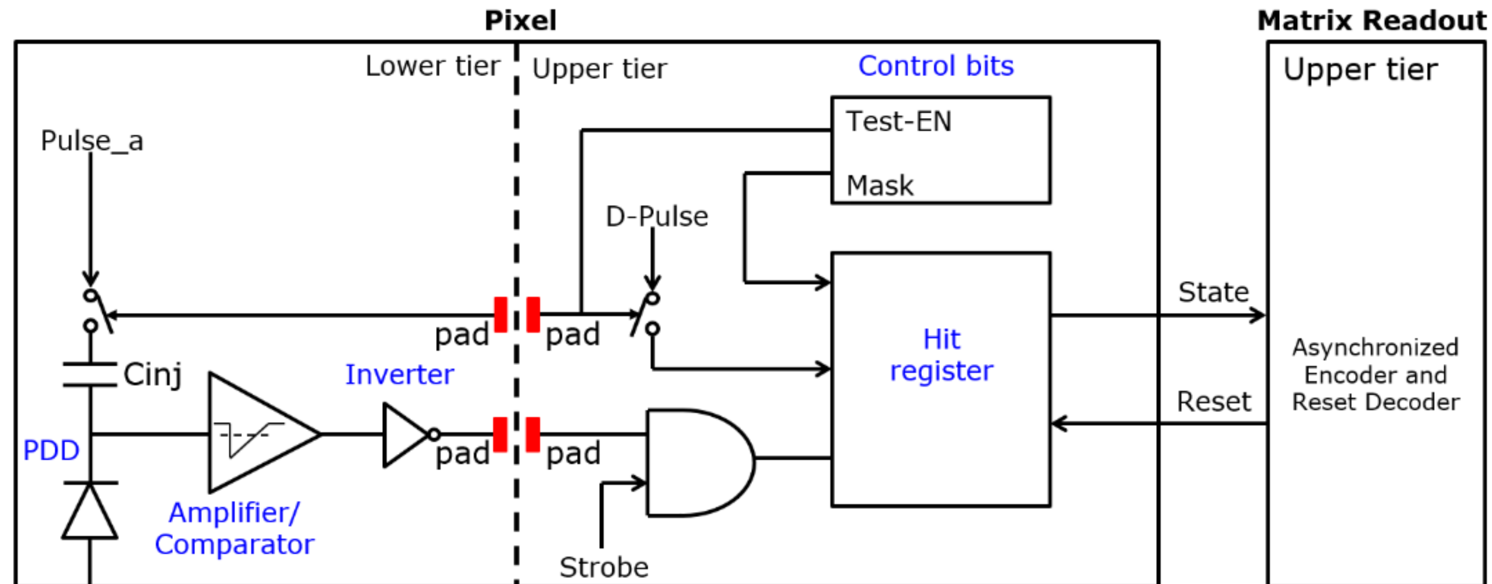
- Essentially, flip-chip and micro bump connections
- Au bump, diameter ~ 3.5 um, pitch ~ 7 um, resistance 0.3 ~ 0.4 Ω
- **Multiple bumps in each pixel**, for signals and power/ground connections
- Glue injection for mechanical strength



3D-integrated pixel circuit for a low power and small pitch SOI sensor, Yunpeng Lu, IHEP China, TWEPP 2023

CPV-4 design scheme

- Lower tier: PDD sensing diode + amplifier/comparator
- Upper tier: Hit register + 2 Control bits + Matrix readout
  - Bit 1 for mask, bit 2 for pulse test
- **2 vertical connections** in each pixel: comparator output and configuration bit for pulse test
  - Transition from Analog to Digital domain at the Inverter
  - Analog power/ground has dedicated connections in the chip peripheral



DRD 4 Presentation SiPM's at FBK Alberto Gola May 15, 2023

Fondazione Bruno Kessler
Silicon Photomultipliers

Detector-grade clean-room, 6 inches, class 10 and 100

Single photon sensors (SiPM) account for a significant portion of the detectors fabricated here.

Private Research Foundation

- ~400 researchers in different fields, ranging from Microelectronics to Information Technology
- 50% funding from local government
- 50% self-funding rate
  - 25% from publicly funded research
  - 25% from collaboration with companies

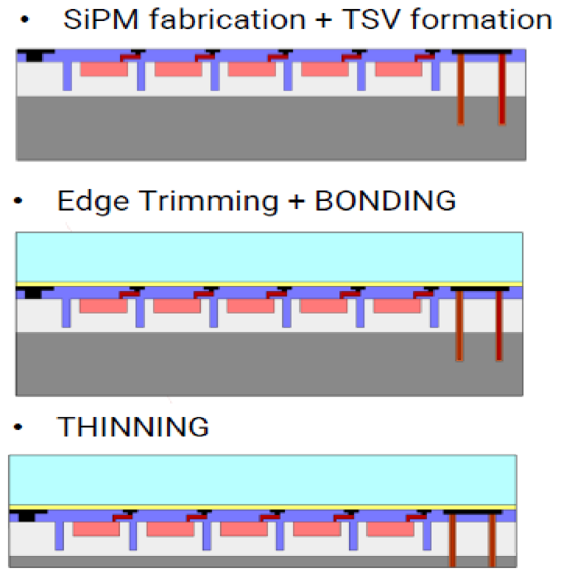
Being a research center, FBK is typically interested in R&D activities and collaborations to improve and customize SiPM technology for specific applications.

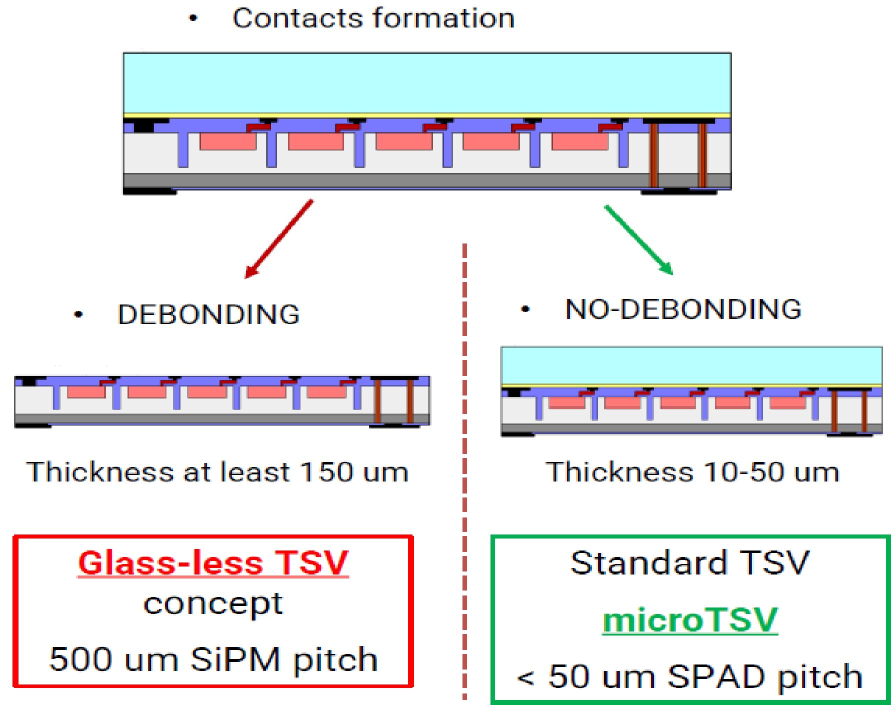
Large area productions can be carried out in FBK (up to ~5 sqm) or relying on external partners: success stories of technology transfers.

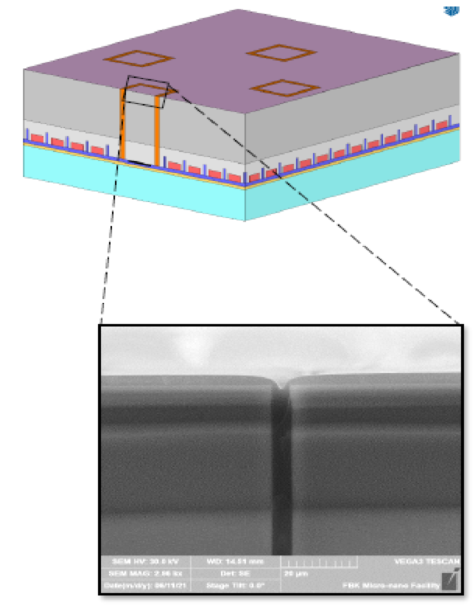
2.5D and 3D Integration
TSV – via mid: process flow

IPCEI on Microelectronics

In the via-mid process, the *TSV is formed during the fabrication of the SiPM, modifying its process flow*.





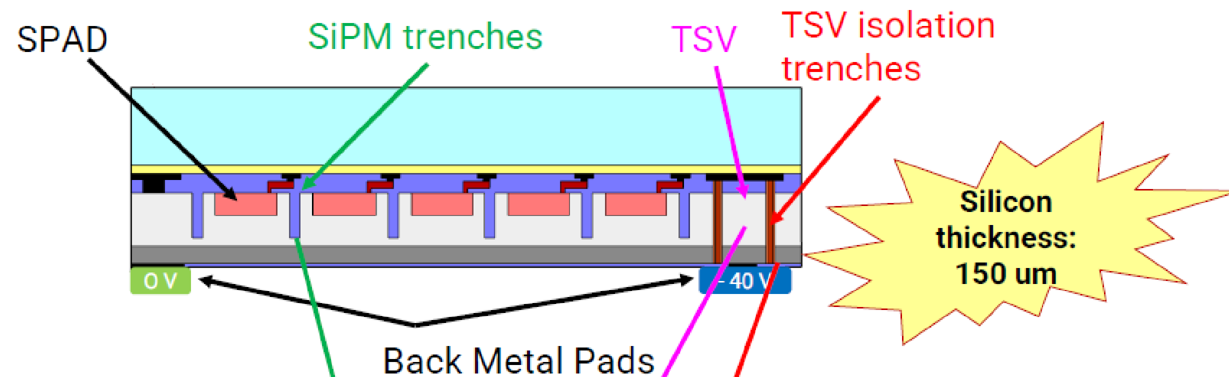


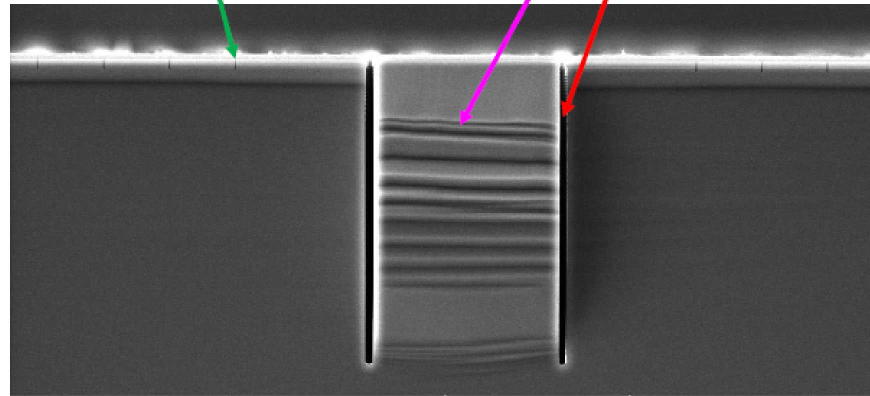
Interconnects

2.5D and 3D Integration
TSV – via mid: first results

IPCEI on Microelectronics

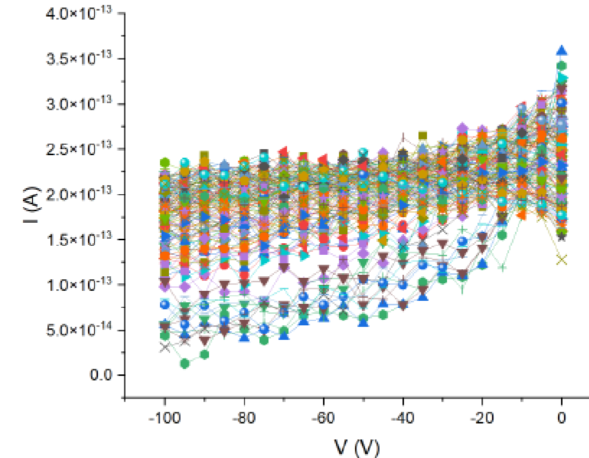
Preliminary results on TSV via-mid development, with partial SiPM process, to *check isolation and continuity* (no Geiger-mode multiplication).





At **-100 V** of bias applied the intensity varies from **30 to 200 fA**

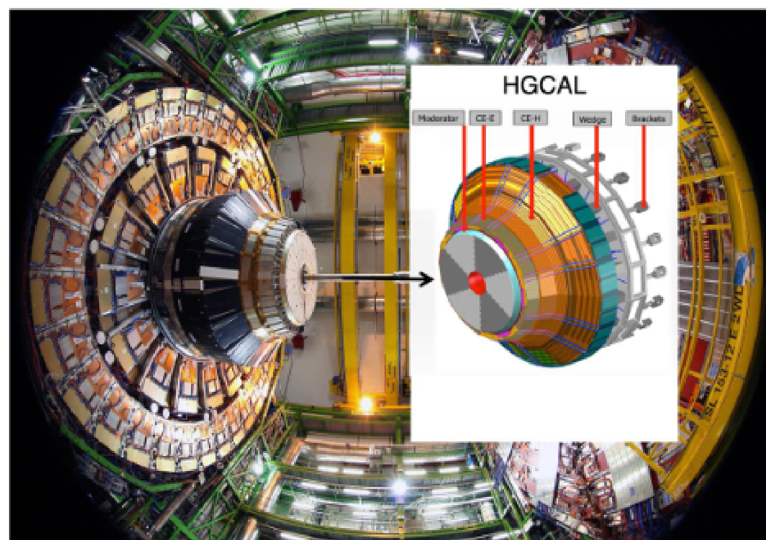
Trough Silicon Vias – Via Mid are isolated from the bulk silicon contact

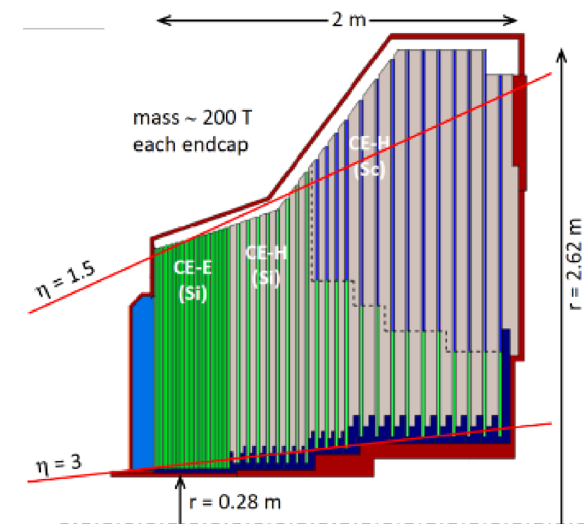


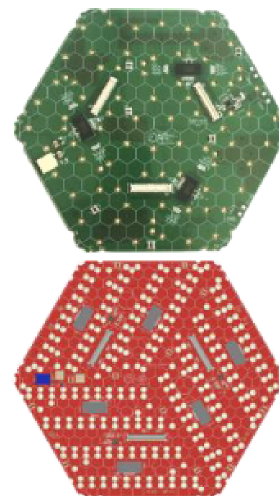
HGCAL: CMS EndCap Calorimeters for the LHC Phase-II upgrade

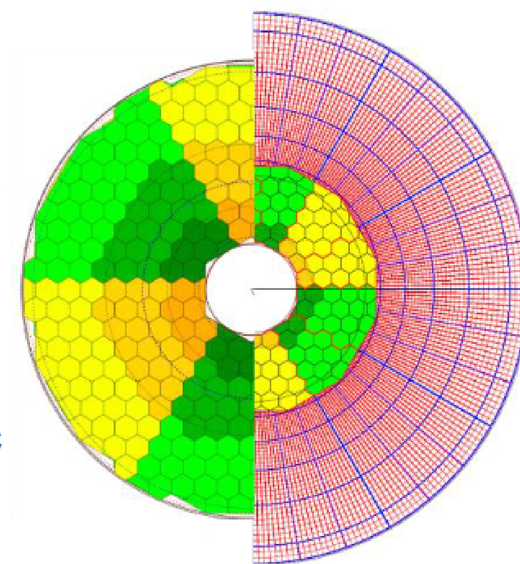
[No Title]

- HGCAL covers 1.5 < eta < 3.0
- Full system maintained at -30°C
  - ~ 640 m² of silicon sensors, 6.1M Si channels, 0.5 or 1.1 cm² cell size
  - ~ 370 m² of scintillators, 240k scint-tile channels
- Data readout from all layers
- Trigger readout from alternate layers in CE-E and all in CE-H
- Active Elements
  - Electromagnetic calorimeter (CE-E): Si, Cu/CuW/Pb absorbers
  - Hadronic calorimeter (CE-H): Si & scintillator, steel absorber
- New Front-end electronics
  - Two versions: Silicon and SiPM
  - Rad.tolerant (200 Mrad, 1.1016 neq / cm²)
  - Power consumption: 20 mW per channel
  - Noise: 0.4 fC
  - Charge: 0.2 fC to 10 pC
  - Pileup mitigation: Fast shaping (peak < 25 ns), precise timing capability (25 ps)









HGCROC2 overview

The possibility for an International Forum

- To share ideas on Hybrid Detectors.
- Evaluate sensor technologies using standardized comparisons.
- Explore interconnect technologies (eg. 3-D attachment).
- Develop full systems with a limited number of channels to explore realistic implementation / reliability issues.