Poster ID: 15

Installation and operation of LHCb Upstream Tracker

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Abstract

The Large Hadron Collider (LHC) began its third run, known as Run 3, in 2023. During this phase, the LHCb detector operates at a higher instantaneous luminosity ($\mathcal{L}_{inst} = 2 \times 10^{33} cm^{-2} s^{-1}$), which is five times increase from Run2, and use a separate sentence for software trigger. The increase in luminosity is very demanding on the detectors. To address these challenges, LHCb has undergone a major upgrade, replacing nearly all of its subsystems. The all-software trigger relies on real-time readout, reconstruction and selection of events. Fast and efficient track reconstruction is particularly crucial. The Upstream Tracker (UT), a new silicon microstrip detector located upstream of the dipole magnet, replaces the old tracker TT and is a critical component of LHCb tracking system. The UT consists of four silicon microstrip planes and read out with 128-channel SALT ASICs. Installed in LHCb in 2023, the UT has recently started physics data-taking globally after a few months of commissioning. This poster will cover the installation and commissioning of the UT and will also include the operation during data-taking.

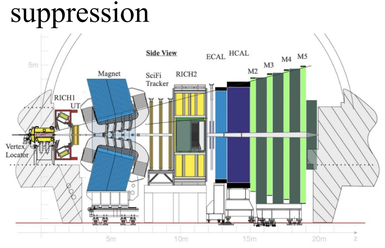
Introduction

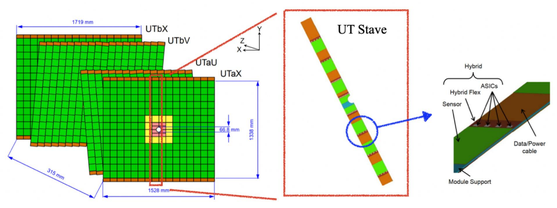
The Upstream Tracker (UT)

- A silicon strip detector with four layers, located upstream of the LHCb bending magnet
- Full angular coverage
- Higher segmentation sensors in the region surrounding the beam pipes[1]
- An important component of LHCb track system

UT front-end readout, SALT (Silicon ASIC for LHCb Tracker)

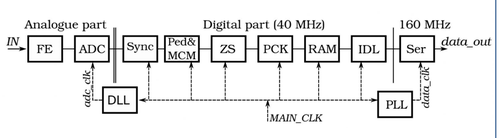
- 128 Channels with 6-bit ADC, 40MHz readout
- CMOS 130nm technology
- Fast shaping time: Tpeak < 25ns
- Digital signal processing providing pedestal & common mode noise subtraction, zero-suppression





UT Commissioning

UT was the last detector to be installed in the LHCb, leaving very limited time for commissioning

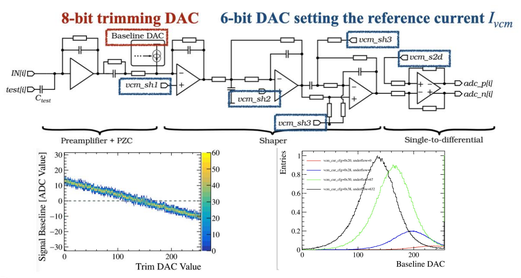


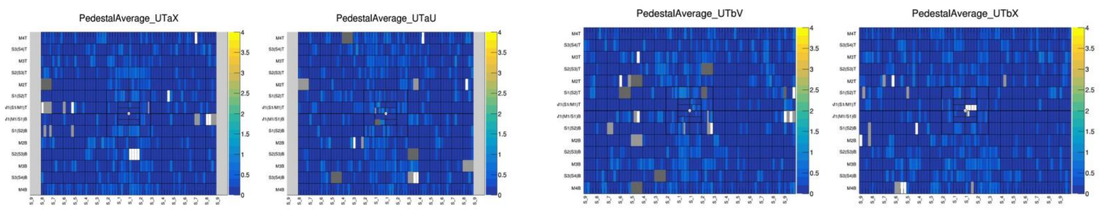
UT Calibration steps:

Tune DLL/PLL, Scan serializer delay, Tune e-link phase on GBTx, Tune ADC, Tune deserializer, TrimDAC scan, Pedestals, Tune ZS threshold, Tune MCM thresholds, Gain scan, Run DAQ with random triggers @ 30MHz

TrimDAC Scan

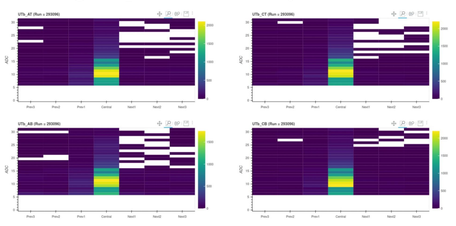
- Each ASIC channel contains an 8-bit trimming DAC for a precise baseline setting[2]
- The single common mode voltage setting couldn't cover all cases: apply 4 different setting for all ASICs
- 99.97% channels work properly at the TrimDAC scan stage

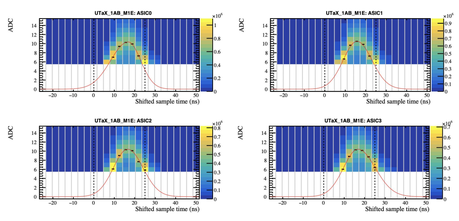




Time Alignment

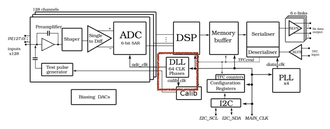
- Time alignment was done using the TAE events produced by the LHC during its 2024 luminosity ramp-up
- Coarse time alignment was done per DCB (Data Control Boards). It makes sure that all ASICs correctly identify a bunch crossing with its corresponding bunch crossing ID within the LHC orbit
- Fine time alignment was done by scanning the ADC sampling phase, which adjusting the delay for each ASIC by fitting a known signal shape to the actual detector signals, resulting in precise time synchronization across the detector

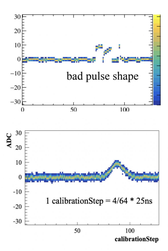




Pulse Scan

- Check the whole processing chain in the SALT chip
- SALT contains a dedicated internal Delay Locked-Loop (DLL) block to provide 64 independent clock phases selection
- Generate test pulse and take data with different clock phase (adc_clk_sel)
- Most of ASICs have the correct pulse shape
  - Recorrected adc_sync_sel bit setting for ASICs with bad pulse shape (32 out of 4048 ASICs)



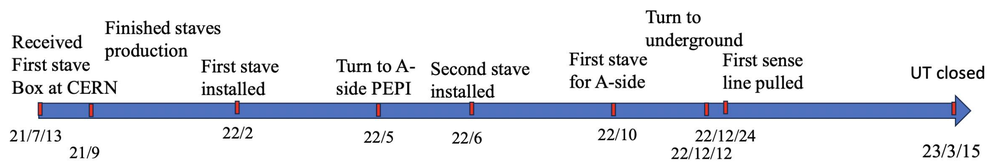


adc_clk_sel	adc_sync_sel	time shift [ns]
0 – 7	1 (falling edge)	$adc\_clk\_sel \cdot \frac{25}{64} + 25$
8 – 39	0 (rising edge)	$adc\_clk\_sel \cdot \frac{25}{64}$
40 – 63	1 (falling edge)	$adc\_clk\_sel \cdot \frac{25}{64}$

Default setting

UT installation

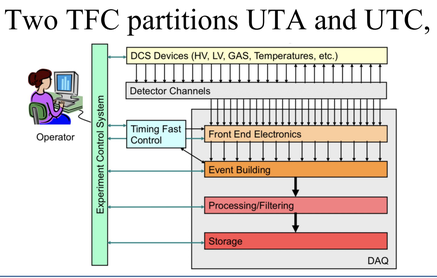
- The Installation started in July 2021 and completed in March 2023
- Chinese groups have significant contributions in design validation, detector installation, and system commissioning
  - HV patch panel, LV splitter, PEPI patch panel, HV cable designed and produced by HNU & IHEP
  - IHEP/HNU/CCNU/LZU/THU/UCAS/SCNU all participated in installation

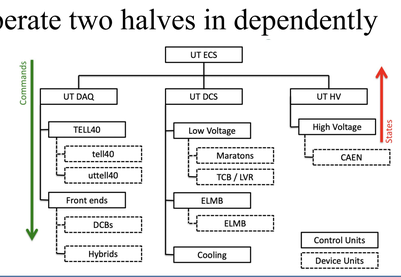


UT Control System

LHCb Experiment Control System (ECS)

- Supervisory Control and Data Acquisition System (SCADA) based on WinCC-OA
- Each tree is a Finite State Machine (FSM)
- UT ECS implemented following LHCb rules
  - Two TFC partitions UTA and UTC, operate two halves in dependently





Working in global

The UT is already taking data smoothly at nominal rates with the rest of LHCb

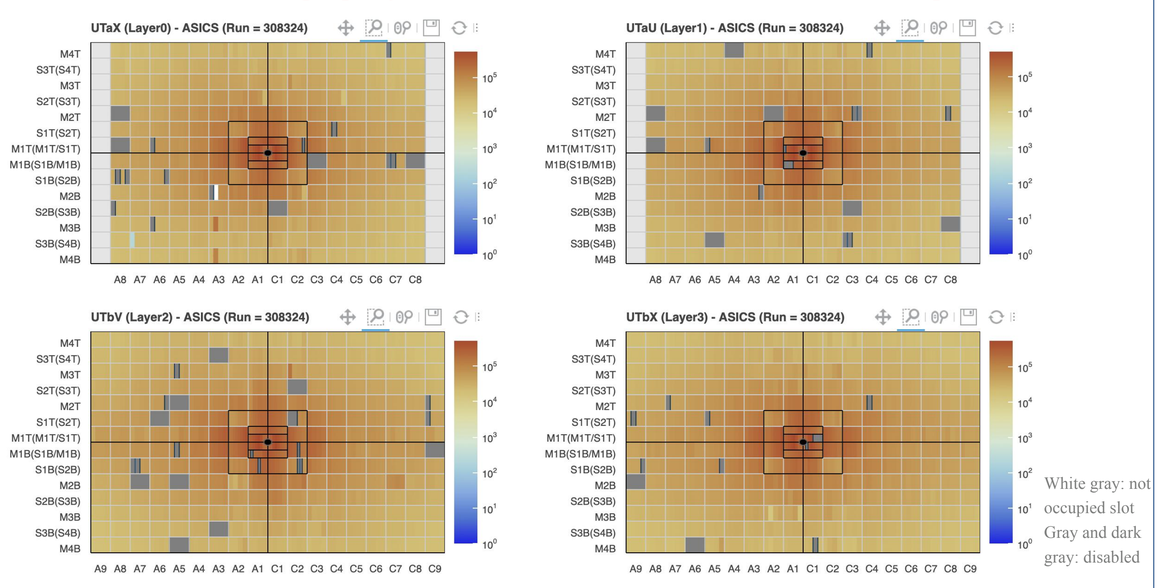
The UT features 4192 ASICs of 128 channels each, with a total of 536,576 strips in 4 layers

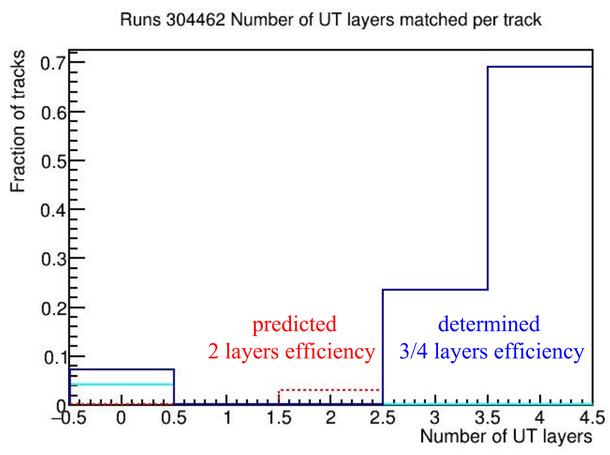
A typical fill of proton-proton collisions at nominal luminosity

The 2D plot for 4 UT layers shows number of hits in each UT chip

Those plots are computed in real time during data taking, so it can timely reflect whether the detector is working properly

Most of the ASICs work properly, and the hit distribution is consistent with expectations!





- The determined efficiency of UT layers (3+4) that match the long track ~ 96.9%
- The predicted UT layers (2+3+4) efficiency ~ 99.8%

Reference and links:
[1]Jianchun Wang et al., The upstream tracker for the LHCb upgrade, https://www.sciencedirect.com/science/article/pii/S0168900216300407
[2] M. Firlej et al., SALT3 chip documentation, https://twiki.cern.ch/twiki/pub/LHCb/StripAsic/salt_v5_spec.pdf

The 2024 International Workshop on the High Energy Circular Electron Positron Collider
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AMSL0 Ladder Production

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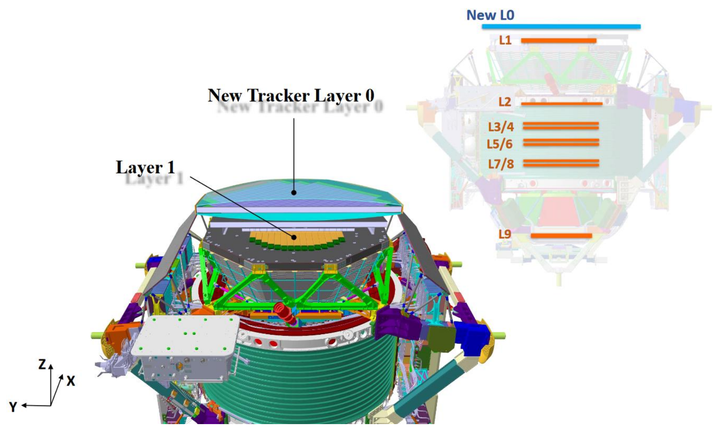
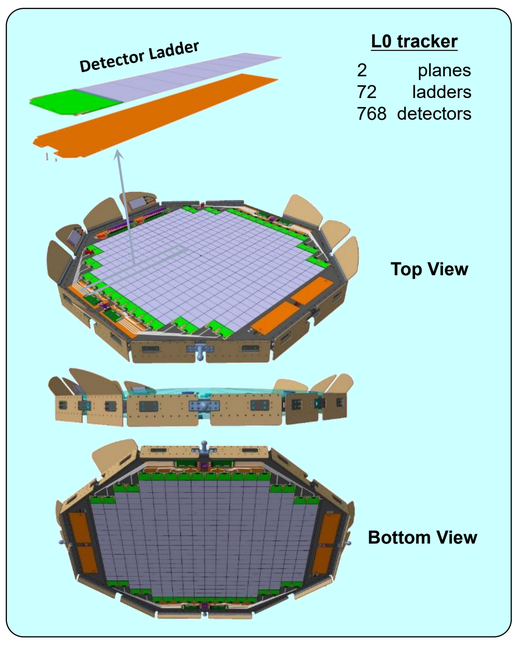
Institute of High Energy Physics, CAS

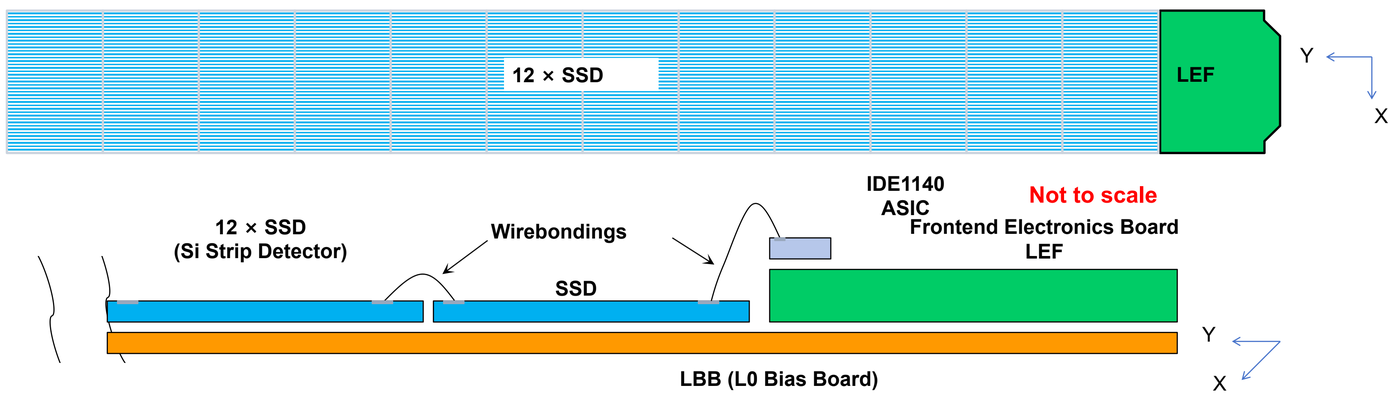
AMS-02 and L0 upgrade

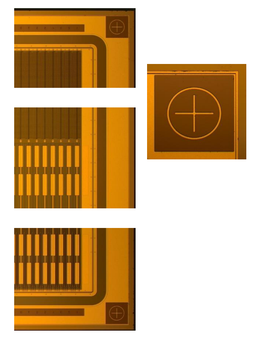
AMS is a multipurpose particle physics detecor installed on the International Space Station. The objective of the experimental includes search of dark matter, the primordial anti-matter, and the origin and propagation of cosmic rays. AMS-02 detector has a large acceptance and is designed to provide precise measurement of charged cosmic rays. Components of the detector include: a silicon tracker, four planes of TOF scintillation counter, a transition radiation detector, a ring imaging Cherenkov detector, an electromagnetic calorimeter, and permanent magnet.





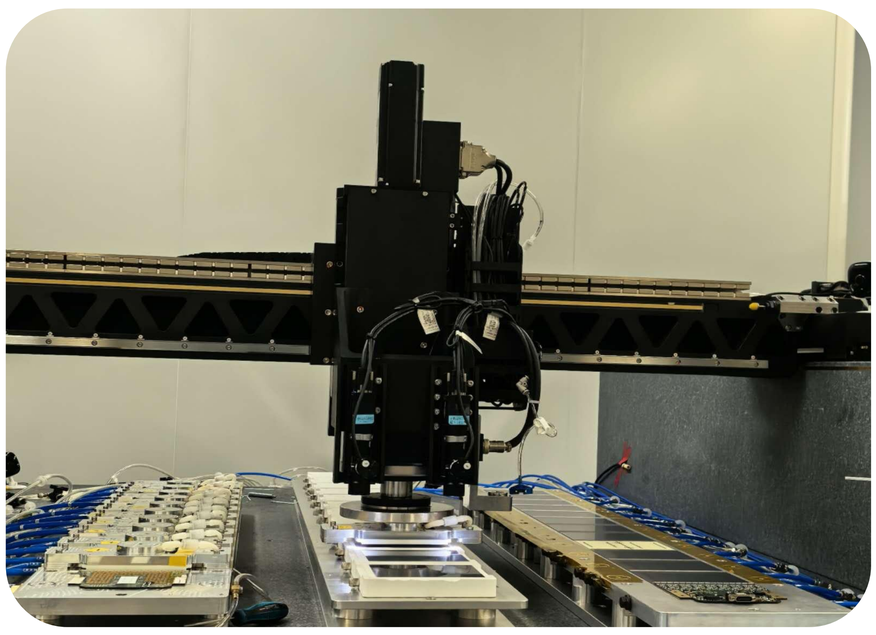
AMSL0 increases the acceptance of cosmic rays by 300% and significantly improves the ability of identifying heavy ions. The L0 layer has two planes, each consists of in total 36 ladders of three different types: 8, 10, 12-SSD(Si Strip Detector). The main responsibility of IHEP is to produce all 72 high quality ladders.(Si Strip Detector)

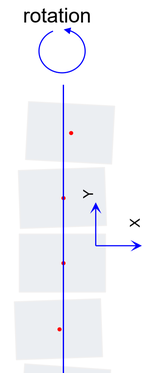


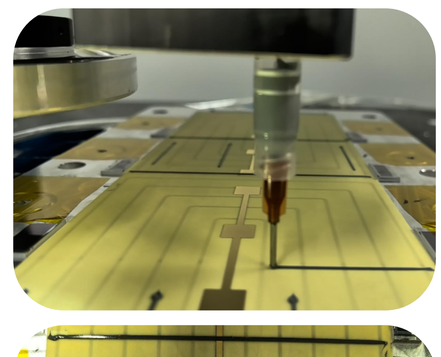


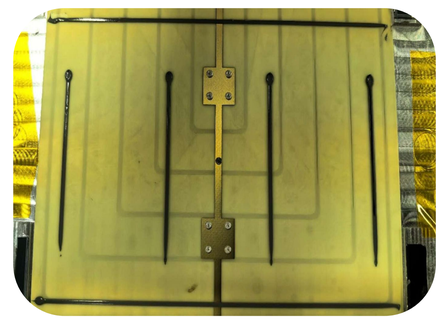
Ladder assembly procedure

Chinese team (IHEP and SDIAT) use a custom designed robotic gantry to achieve high precision assembly, the sigma of positions in x axis is better than $5\mu m$, which is the highlight of the work. The gantry can move in four dimensions: x, y, z, θ with $1\mu m$ and 10^{-6} rad precision. There are two high resolution cameras on the gantry head that can recognize two fiducial marks on one SSD at the same time, they provide real-time coordinates information of SSD.

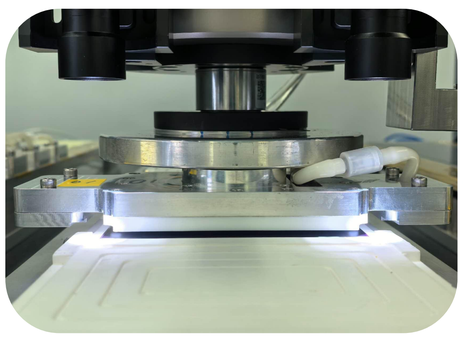


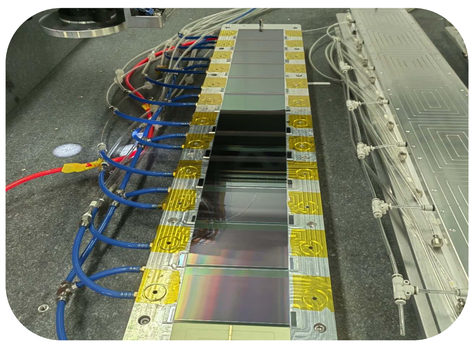




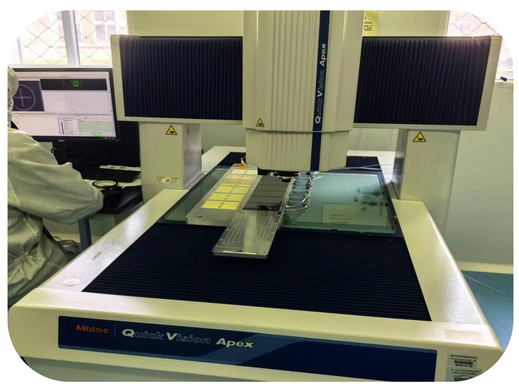


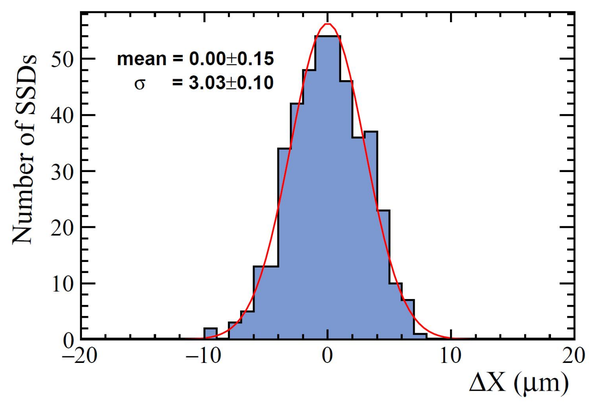
Designated vacuum pick up tool is attached to the gantry head to suck up SSD, and bring SSD to the desirable location on the top of LBB(L0 Bias Board), where the structure and conductive glue is already dispensed by the vacuum devices on the gantry head. After putting down one sensor, adjust the position by controlled movements of gantry head, then cut the vacuum of gantry head and turn on the vacuum under the pick up tool, finally leave the pick up tool pressing down the SSD on LBB, now one SSD is done. When the glue is cured, remove the pick up tools.





Once the ladder is assembled, an optical metrology system is used to measure all the fiducial marks and fit the coordinates to give the sigma in x axis.





By September 10th, we have finished all high quality ladders.

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Beam Test For The AMS-02 Layer0 Tracker Upgrade

Dexing Miao(缪德星) on behalf of AMSL0 team
Institute of High Energy Physics (IHEP), Beijing, China

1. Introduction

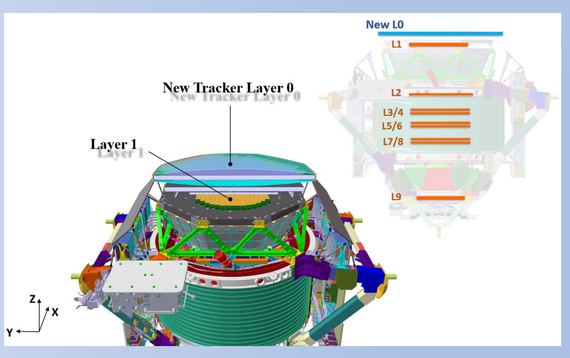


Fig. 1:AMS-02 and new Tracker Layer0

AMSL0 Project:

- Increase the acceptance of cosmic rays by 300%
- Significantly improves the ability of heavy ion particle ID
- The largest single detection Si detector Unit (100cm*11cm)
- The first large Si Detector for major international experiment that the **Chinese team play a leading role**

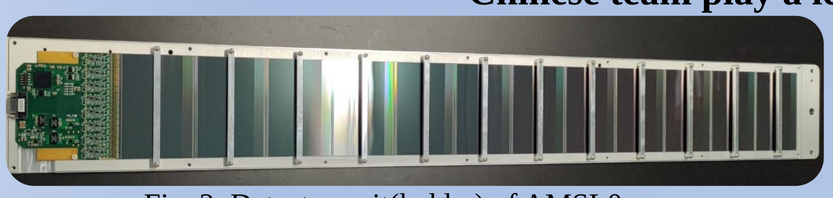


Fig. 2: Detector unit(ladder) of AMSL0

Ladder is formed by 8/10/12 SSDs are connected in series

- Large detection area with small electrical power budget
- Each readout channel corresponds to a very long (~1m) strip
- Requires high precision placement of the SSDs on each ladder, and precise SSD position measurements after assembly with optics and **beam tests**

2. Beam test setup

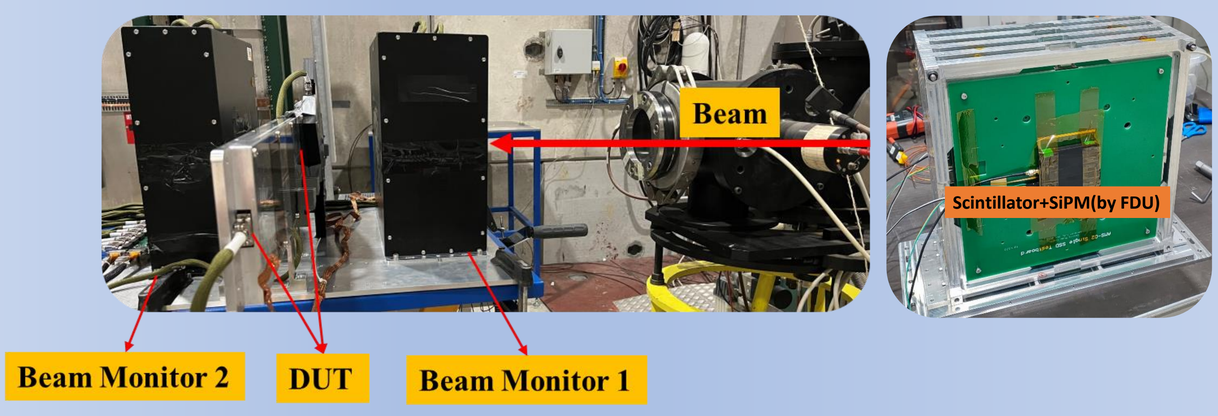


Fig. 3: Photo of beam test setup

- Performed several beam tests at SPS, BSRF with muon, proton, electron and mix heavy ion beams
- Study the spatial resolution, efficiency, heavy ion PID …
- With 12 beam telescope boards using the same SSD and electronics

3. Sensor efficiency

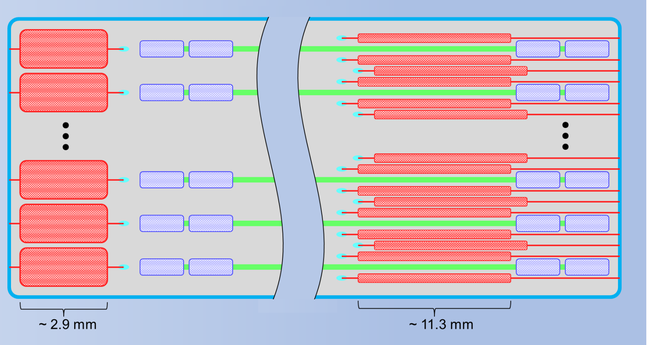


Fig. 4 Schematic of one SSD Unit: 3 bias strip + 1 readout strip(green), 4 bias resistors(red), 4 bonding pads(purple) on the readout strip only

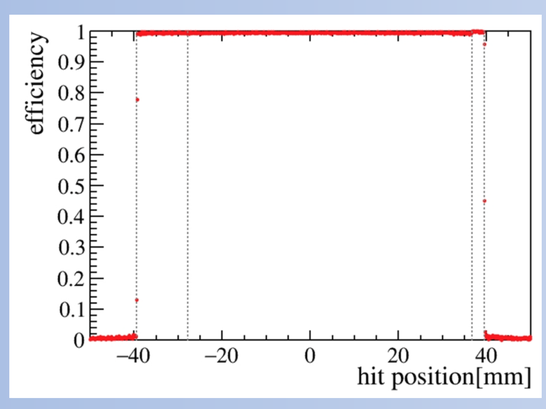


Fig. 5 The detection efficiency of MIP along strip direction

Special design of the SSD

- A large resistance (~100MΩ) is needed to achieve impedance matching
- The bias resistor and strip located on different layers
- The detection efficiency, especially in region of the bias resistors, was studied at test beam

- Fig.5 shows the entire sensor exhibits high detection efficiency(>99.9%)

4. Spatial resolution

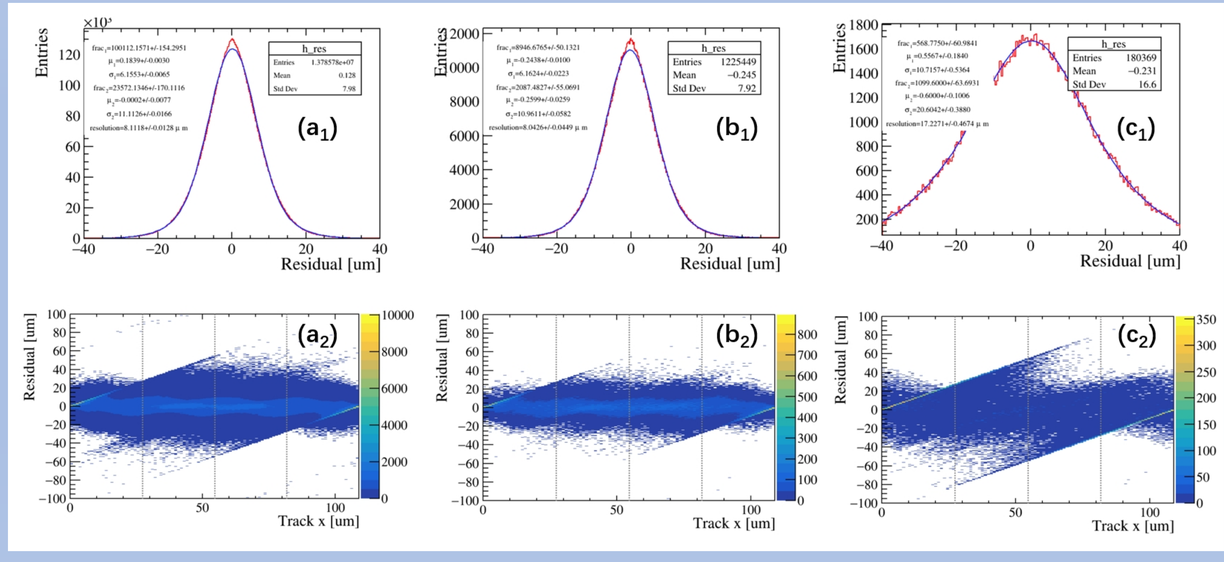


Fig. 6: Residual distribution and residual of in-strip hit position distribution of different regions: (a_1)(a_2) normal region; (b_1)(b_2) bias resistor region; (c_1)(c_2) no intermediate strip region.

- A new position finding algorithm(PFA) is developed to eliminate the channel switching caused by noise
- Get spatial resolution of the SSD of MIP is 7.5um, the bias resistor did not affect the spatial resolution
  - Readout pitch=109um, strip pitch=27.25um
- The design of 3-intermedia strips significantly improve spatial resolution

5. PID and tracking for heavy ions

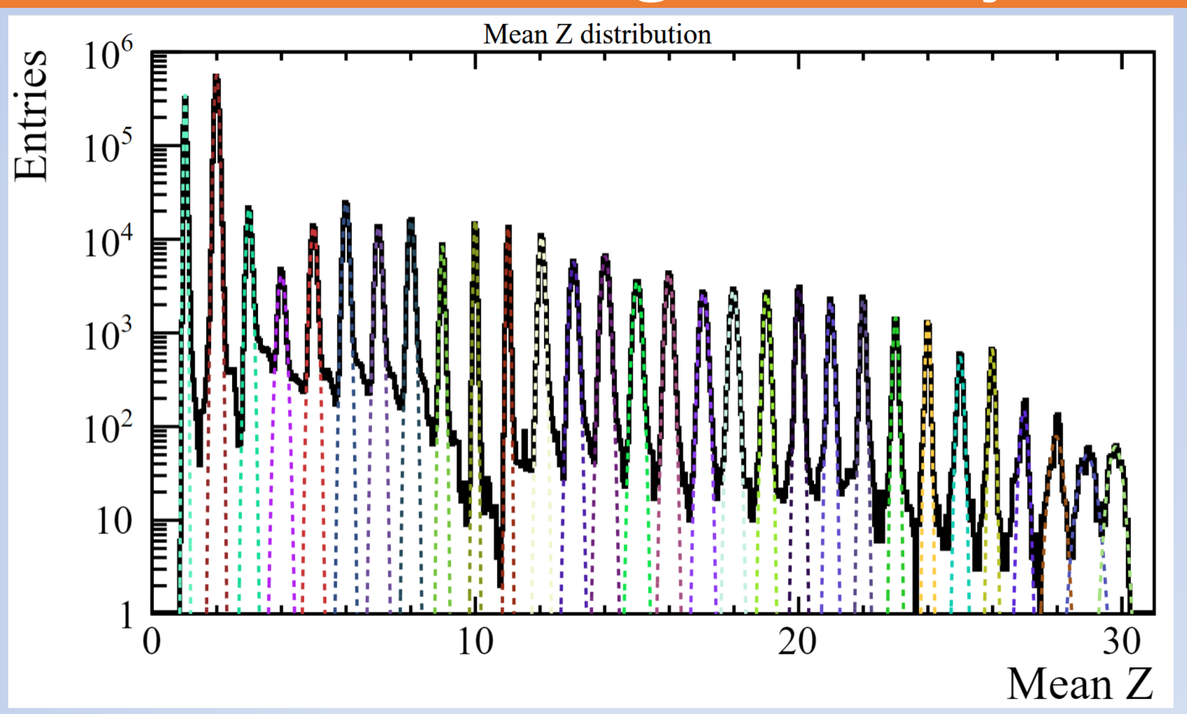


Fig.7 The mean Z-values predicted by the 9-layer telescope

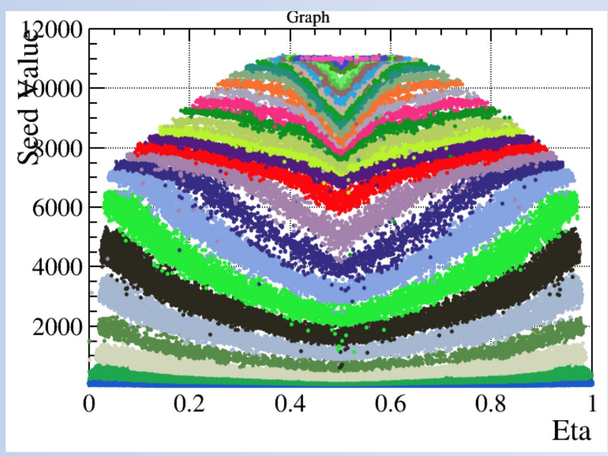
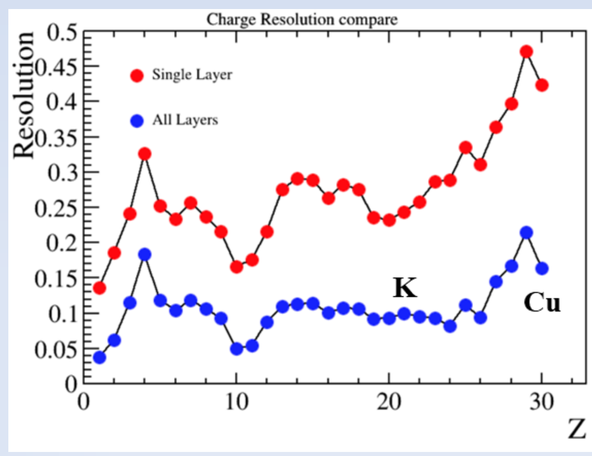


Fig.8 BDT Z-tag display of one layer



Charge resolution of single layer and telescope

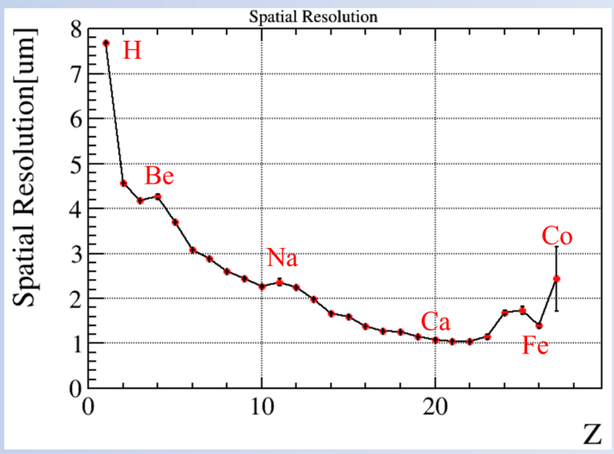


Fig.9 The spatial resolution of the nucleic up to Z=27

- Use BDT to get z-tag of every event, calculate mean Z of 9 layers of each track
- Get ~0.1 charge unit resolution of the telescope up to Cu(Z=30) nuclei
- Obtained the spatial resolution of single layer for heavy nuclei up to Co(Z = 27)
  - Best resolution ~1um

Contact: Dexing Miao e-mail: miaodx@ihep.ac.cn
The 2024 International Workshop on the High Energy Circular Electron Positron Collider,
October 23-27, 2024, Hangzhou

Institute of High Energy Physics
Chinese Academy of Sciences

Poster ID: 20

MAPS-based Upstream Tracker for The LHCb Phase-II Upgrade

Ji Peng (彭吉) on behalf of the LHCb UT upgrade team
Institute of High Energy Physics (IHEP), Beijing, China

01 Introduction

01. LHCb Detector

The LHCb detector, illustrated in Fig. 1, is designed for studies in flavor physics and functions as a forward general-purpose detector:

- The forward single-arm spectrometer features a unique coverage in pseudo-rapidity ($2 < \eta < 5$).
- It observes 40% of the heavy quark production cross-section within only 4% of the solid angle.
- Precision measurements are conducted in the beauty and charm sectors.
- It also investigates topics such as QCD, EW, and heavy ion collisions.

02. Upstream Tracker

The Upstream Tracker (UT) is located upstream of the LHCb bending magnet. Since 2023, LHCb has been operating at a maximum luminosity of $\mathcal{L}_{\max} = 2 \times 10^{33}\ cm^{-2}s^{-1}$ due to an upgraded detector. It is expected to collect data at a higher luminosity of $1.5 \times 10^{34}\ cm^{-2}s^{-1}$ starting from around 2035, which represents an increase approximately 7.5 times compared to Run 3 and Run 4 (as shown in Fig. 2). The current UT is struggling to handle the increased data rate and high occupancy levels.

03. Upgrade-II UT

The Upgrade-II UT (UP) detector will utilize CMOS Monolithic Active Pixel Sensors (MAPS) technology. In this poster, we outline the proposed design, performance studies, and R&D plan.

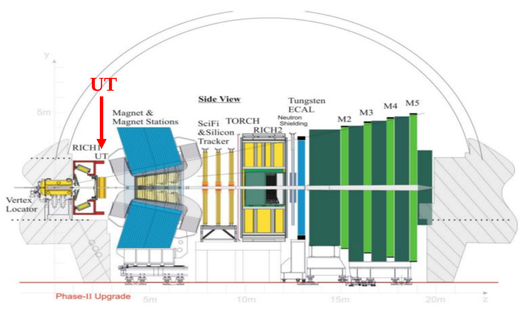


Fig. 1: LHCb Detector at Upgrade II

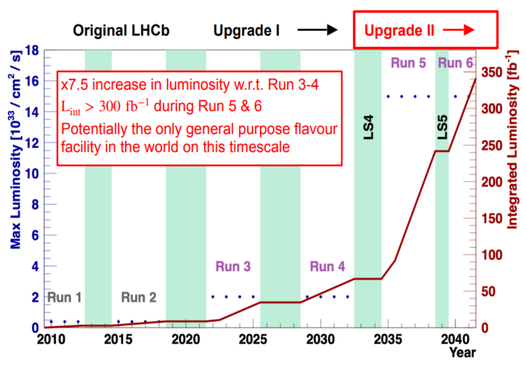


Fig. 2: Upgrade II timeline

02 Detector Design

01. Detector Structure

A potential detector layout is shown in Fig. 3. Each plane consists of 12 staves, with each stave made up of multi-MAPS modules.

- Each module features 14 chips arranged in a 7 × 2 array, interconnected through a flexible circuit.
- The lpGBT ASIC, which is radiation tolerant and serves functions such as data, timing, trigger, and control for the HL-LHC, will be used for data acquisition.
- A total of 36 modules are installed alternately on both sides of a supporting bare stave, resulting in 12 staves for each plane.

A four-plane detector based on HVCMOS is proposed. Layout using other MAPS technology like CMOS with low fill-factor is similar.

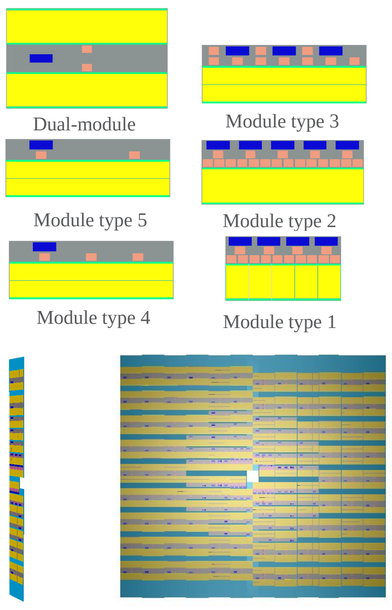


Fig. 3: Geometry construction using DD4hep

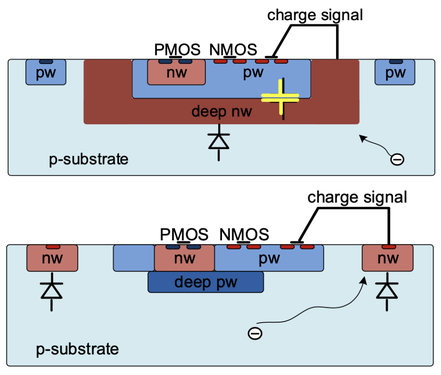


Fig. 4: The schematic of HV-CMOS (top) and CMOS with low fill-factor (bottom)

02. CMOS Sensor

The ongoing R&D studies suggest that monolithic active pixel sensors are promising candidates for the UP.

To enhance the depletion in the sensing volume and improve the speed and radiation tolerance of the detector, DMAPS (Depleted Monolithic Active Pixel Sensors) implementations adopt two distinct approaches: one is high fill-factor or high-voltage (HVCMOS), and the other is CMOS with low fill-factor.

03 Software Simulation

01. Software Development

The detector description has been developed using both the DetDesc and DD4hep frameworks. The "fake digitization" study was conducted at the MCTruth level. A material budget scan was carried out in both frameworks, yielding consistent results.

Fig. 6 illustrates the radiation length of the first layer of the UP plane in both x/y and η/ϕ views. The final plot presents the projection map along the η axis.

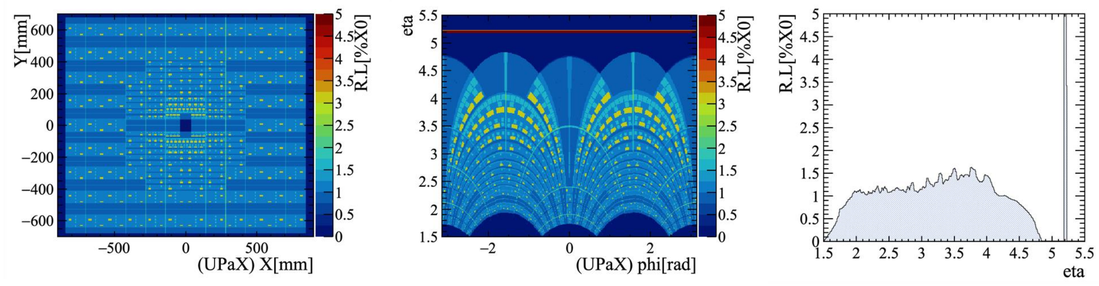


Fig. 6: Radiation length in DD4hep

02. Performance of UP

The performance studies of the UP detector utilize simulation samples generated under Upgrade II conditions, described using the DD4hep framework within Gauss/Gaussino. The proton-proton collision sample contains minimum bias and inclusive b-hadron events generated by Pythia, simulating HL-LHC conditions with a center-of-mass energy of $\sqrt{s} = 14$ Tev. Fig. 7 shows average hit densities in proton-proton collisions at HL-LHC, up to ~ 4.5 hits/cm²/BX. There are 2574 colliding bunches and the baseline instantaneous luminosity is $1.5 \times 10^{34}\ cm^{-2}s^{-1}$.

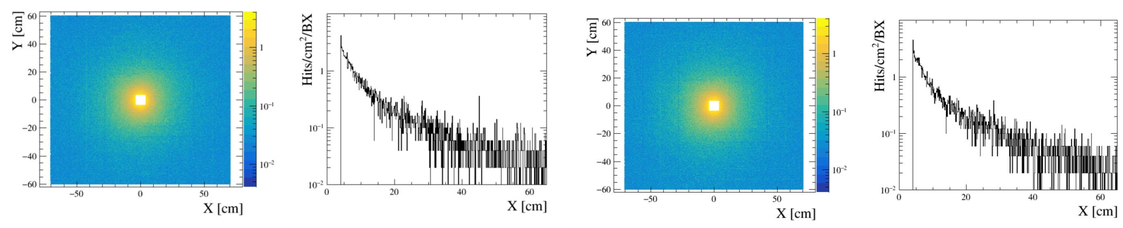


Fig. 7: Mean UP hit density per bunch for (left) minimum bias and (right) inclusive b events.

Related studies are accomplished at Boole:

- **Pixel Occupancy** : The maximum pixel occupancy was estimated to be 0.256% using 1.2K miniBias MC events, which aligns with the estimates provided in the FTDR.
- **Reconstruction Efficiency**: Fig. 8 shows the reconstruction efficiency for the Velo-UP tracks and the Velo-UP-SciFi tracks. In this study, the Velo and SciFi are in their Run 3 configurations. The efficiency is at the same level as the current detector.

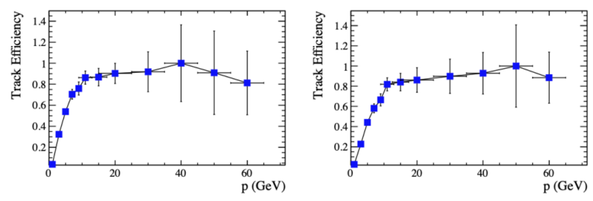


Fig. 8: The tracking efficiency as a function of the total momentum, for (left) the Velo-UP tracks and (right) the Velo-UP-SciFi tracks.

04 Updated baseline

During the studies for the scoping document, the baseline of a UP plane has evolved towards a reduction of the outer acceptance for cost reduction with minimal impact on physics, shown by the red dashed box in Fig. 9.

UP new geometry model:

- The UP features four detector layers at Z positions similar to the current UT.
- Coverage reduction:
  - Number of staves decreased from 12 to 10.
  - Number of modules reduced from 36 to 32.
  - Overall detection area reduced by 26%.
- The central 4×4 chips are removed for beam pipe, covers (±39 mm) ×(±37 mm).

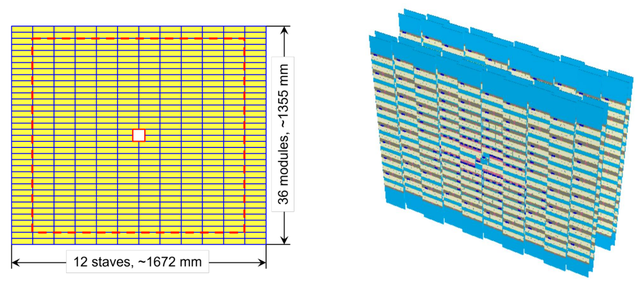


Fig. 9: Layout of a plane (left) and 4-layer detector (right) of updated baseline with reduced coverage.

Reference and links:

[1] “Framework TDR for the LHCb Upgrade II Opportunities in flavour physics, and beyond, in the HL-LHC era”, CERN, Geneva, LHCb Collaboration, CERN (Meyrin)

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The 2024 International Workshop on the High Energy Circular Electron Positron Collider
October 23-27, 2024, Hangzhou

Test of HVCMOS sensor using 55nm process [1]
(Poster 21)

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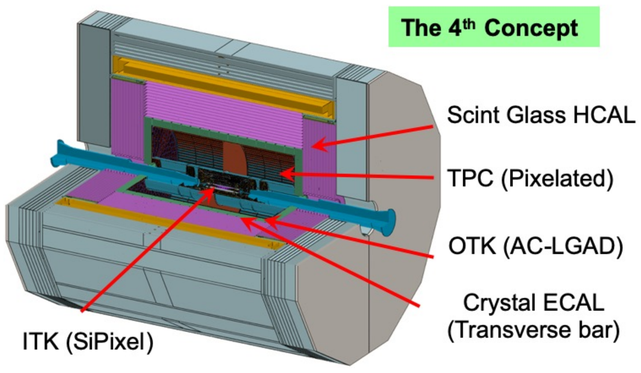
CEPC workshop 2024, 22-27
October, Hangzhou

1 Introduction

CEPC plans to utilize a large-area and economic silicon-based tracker to achieve exceptional spatial resolution.

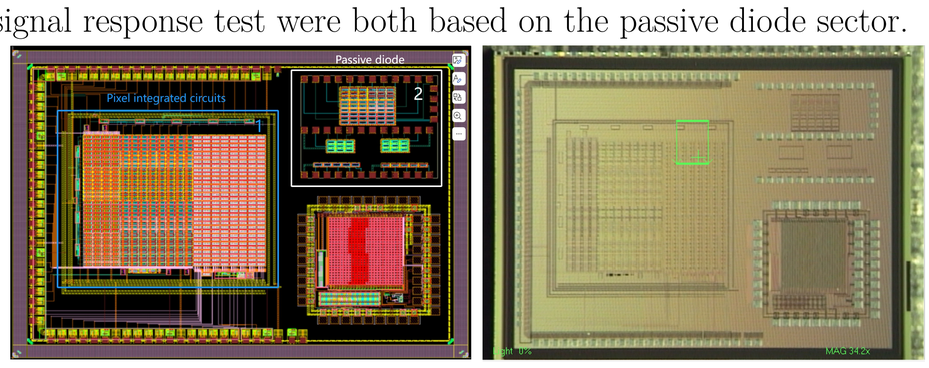


The CEPC tracking system conceptual design.

CMOS technology presents an appealing solution due to its high performance and cost-effectiveness. The commercially available high resistance wafer based High Voltage CMOS (HVCMOS) is intrinsically radiation hard and has large capacitance for signal acquisition, it has been used in such as Mu3e or ATLASPix. Current research and development mainly focus on 150/180nm processes while 55nm helps integrate more functions and reduce power consumption within the same pixel area.

2 COFFEE2 chip

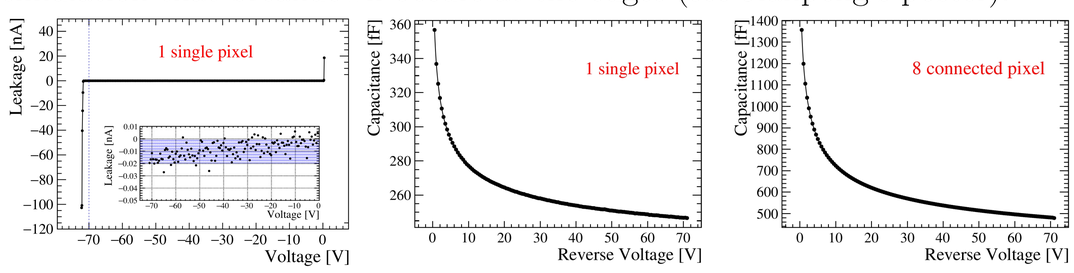
The CMOS sensOr in Fifty-FivE nm procEss (COFFEE) has been designed and evolved. COFFEE2 chip, size of 4×3 mm^2, consists of a passive array sector and a pixel array (40×80 μm^2 for each pixel) with integrated circuits. Though the high resistance substrate was not yet available, the pixel array is already a true verification of the complete structure. The analog amplifier, switch circuit and variant diode structures were integrated in sector 1 while sector 2 only contains passive diode. The following IV/CV and signal response test were both based on the passive diode sector.



The layout of design (left) and photo (right) of COFFEE2 chip

3 IV/CV test

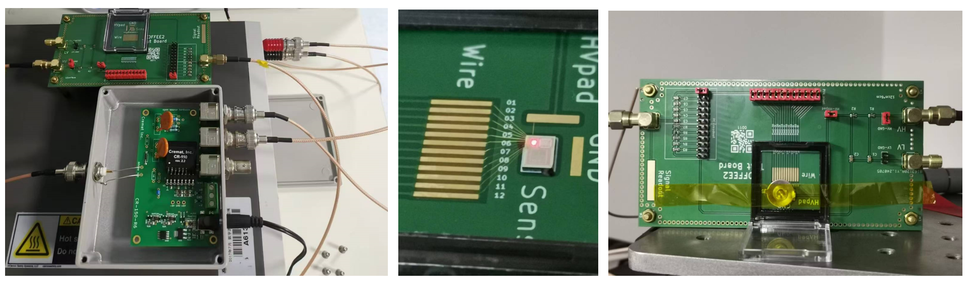
For COFFEE2 chip, the IV test results show very good diode behavior with low leakage $\sim$ 10 pA for different pixel array. Clear positive conduction and gradually reverse breakdown begins as voltage increases to 70V. Under the same voltage, the capacitance variation of 8 pixels array is 8 times that of a single pixel. Considering deducting parasitic parameters of metal routing wire, the capacitance of single pixel is about 30-50 fF. It is evident that the pixel have not been completely depleted and it can be inferred from the simulation that breakdown occurs at the edges (see Jianpeng's poster).



The typical IV result (left) and CV curves for single pixel (middle) and 8-pixel parallel structure (right)

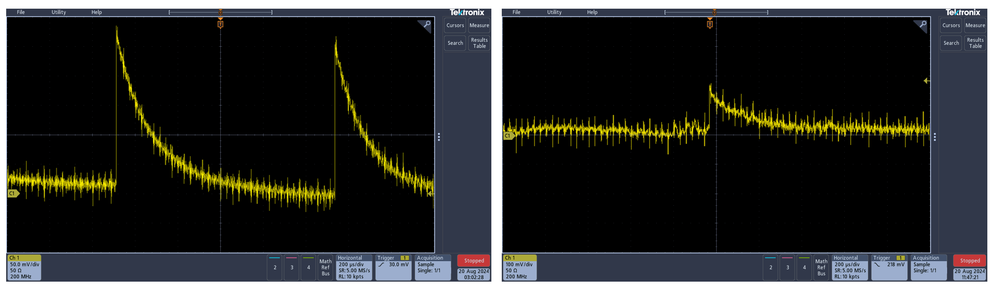
4 Signal response test

The signal response test was performed with laser or radioactive sources to verify the reliability of the COFFEE2 CMOS sensor with 55nm process. An external charge sensitive amplifier, with the gain of 1mV/fC, was used to test the passive diode array response to red laser ($\lambda \sim 650$nm) or radioactive sources (i.e. α, β source).



The setup for external CSA connect to COFFEE2 (left), the red laser focusing on chip (middle) and illuminate the chip with an α source

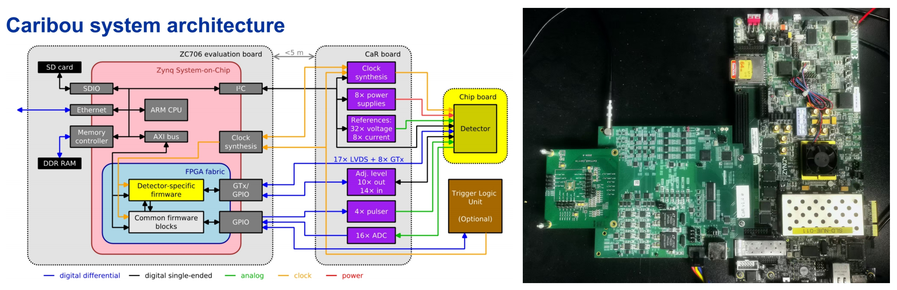
With the high voltage applied, the response of pixel array (54 pixels) to red laser is proportional to the magnitude of the high voltage. Under 70V, on average, each pixel is excited by 5fC charge due to red laser energy deposition. For α source, the signal response of pixel can reach up to 100fC due to the α complete deposition. The β and X-ray source also tried, ^{90}Sr and ^{55}Fe, but no clear signal was found at existing noise level. Due to the high noise level of the external amplifier, the pixel integrated amplifier will be used in the next to observe the signal.



Under 70V, the response of an array consisting of 54 pixels to red laser (left) and α source (right)

5 Circuit test

The ZC706 + Caribou boards form the circuit testing system and a dedicated carrier board is designed for COFFEE2 chip. The circuit test verified the expected digital circuit functionality (row-column gating and DAC unit), demonstrating the feasibility of the digital circuit design.



The Caribou system architecture (left) and the circuit test setup (right)

6 Summary & plan

Promising test results from CMOS chip using 55nm process indicate the possibility of future applications. For the verification of radiation resistance, nucleon beam in SNS, DESY or CERN can be chosen. The results of COFFEE2 testing provide important input for future chip design.

[1] Zhuojun Chen, Ruoshi Dong, Leyi Li, Yiming Li, Weiguo Lu, Yunpeng Lu, Ivan Peric, Jianchun Wang, Zhiyu Xiang, Kunyu Xie, Zijun Xu, Hui Zhang, Mei Zhao, Yang Zhou, Hongbo Zhu **and** Xiaoyu Zhu. "Feasibility study of CMOS sensors in 55 nm process for tracking". **in***Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*: 1069 (2024), **page** 169905. ISSN: 0168-9002. DOI: https://doi.org/10.1016/j.nima.2024.169905.

Poster ID: 43

CMOS Strip Chip Simulation with RASER

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2. University of Chinese Academy of Science, Beijing, China.

Hangzhou, Oct 23-27, 2024

Abstract

The CMOS strip sensor is a key component of the CEPC Inner Tracker. We have simulated CMOS Strip Chip (CSC), including the electric properties of the sensor, the front-end electronics and the detector responce of beta ray and laser.

Simulation Work Flow

First, a detector geometry is designed, from which a suitable mesh is created. Using the open-source TCAD software DevSim, the electric field and carrier distribution can be calculated.

Next, an incoming particle is generated by Geant4, and the deposited energy is converted into carrier excitation. After the charge carriers drift and diffuse, an induced current is generated on the readout electrode, followed by amplification and waveform shaping simulated by NGSpice front-end electronics.

With noise simulation, statistical results for arrival time, hit position, and dE/dx can be evaluated, allowing for the determination of the detector's time, spatial, and energy resolution.

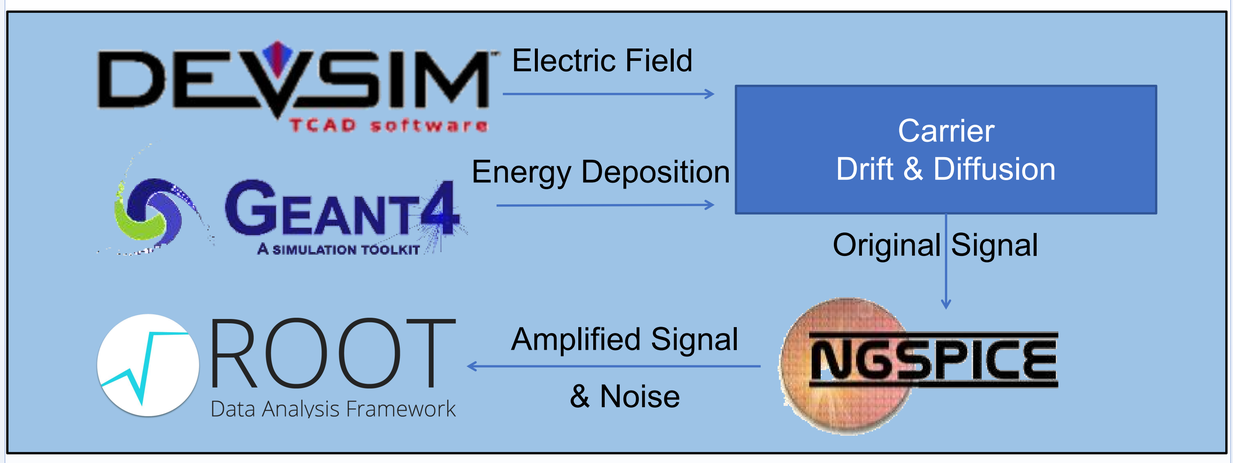

Figure 1. Simulation work flow by RASER [1].

CSC Detector Modelling

We have developed a strip detector model based on [2], integrated with a CMOS processing design, as illustrated in Fig. 2. In our simulation, each strip readout is equipped with an n-plus well connected to the cathode, along with two p-stops shared by neighboring readouts to reduce the charge sharing effect.

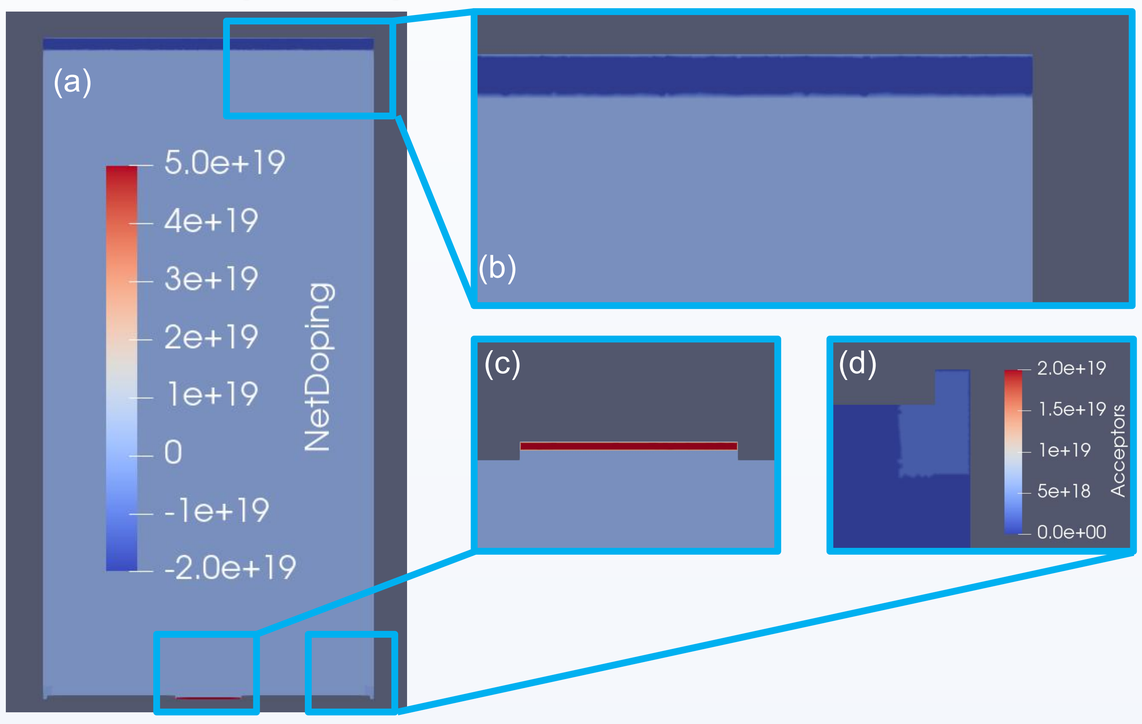

Figure 2. Doping profile of (a) the sensor, (b) p-contact (c) n-well, (d) and p-stop.

Electric Performance

We have evaluated the in-circuit properties of the detector, including the current-voltage (I-V) and capacitance-voltage (C-V) relations. The C-V relationship indicates that the detector reaches full depletion at 30 V. Meanwhile, the I-V relationship shows a relatively mild leakage current of 1 μA at operating voltages.

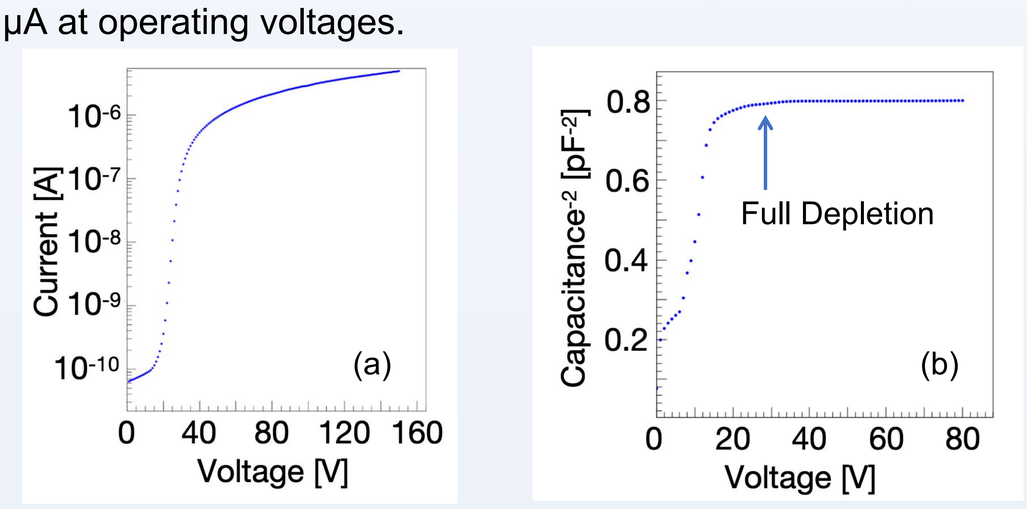

Figure 3. (a) I-V and (b) C-V relations of CSC sensor.

Electronics

We have simulated the ATLAS ABCStar amplifier, which consists of three stages: a preamplifier, a first boost amplifier, and a second amplifier with a shaper. This design is with good noise tolerance.

The circuit achieves a gain of 87.7 mV/fC, a rise time of 21.7 ns, and a waveform full width at half maximum (FWHM) of approximately 32 ns. These results are consistent with the ABCStar data, which reports a gain of 85 mV/fC, a rise time of 22 ns, and an FWHM of 34 ns.

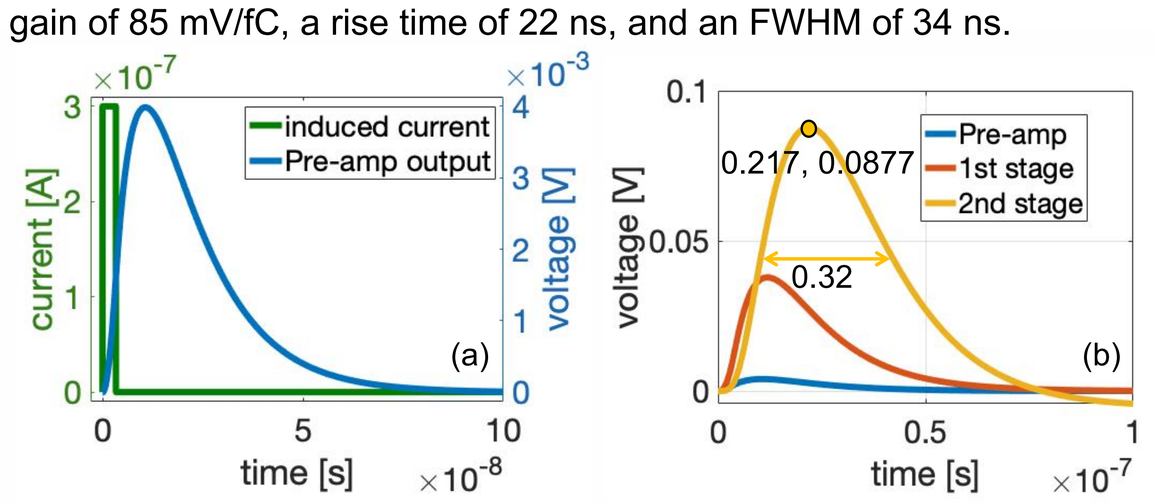

Figure 4. Signals (a) before and after the Pre-amp, (b) after every stage. Input 1 fC.

Responce Simulation

We use a ^{90}Sr beta source in Geant4 as minimum ionizing particle (MIP) source, with the emitted electrons having an energy of 0.546 MeV.

Similarly, we also simulated the response of the detector to a 660 nm wavelength laser. The laser is incident from the n-well side of the detector, with a beam width of 5 μm and a pulse duration of 5 ns.

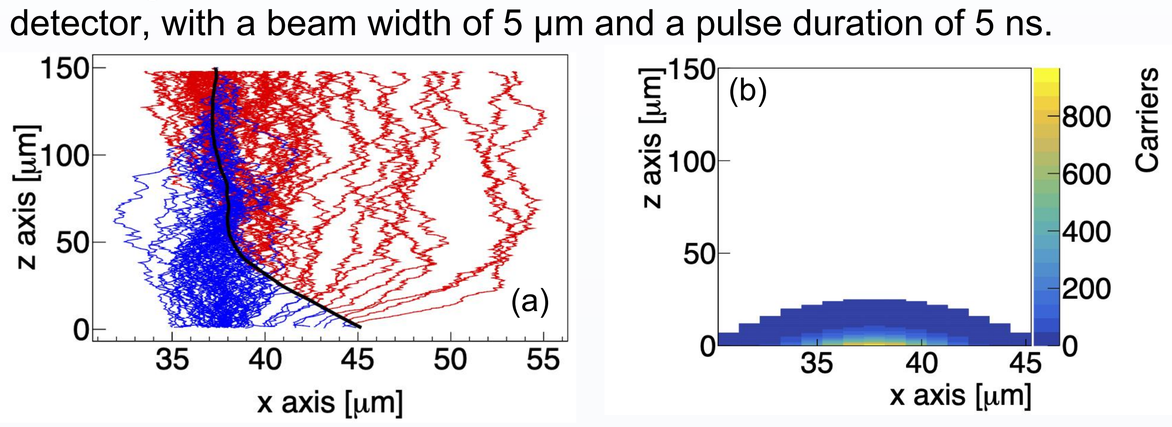

Figure 5. Visualization of (a) carrier drift paths after beta ray injection and (b) carrier distribution after laser injection.

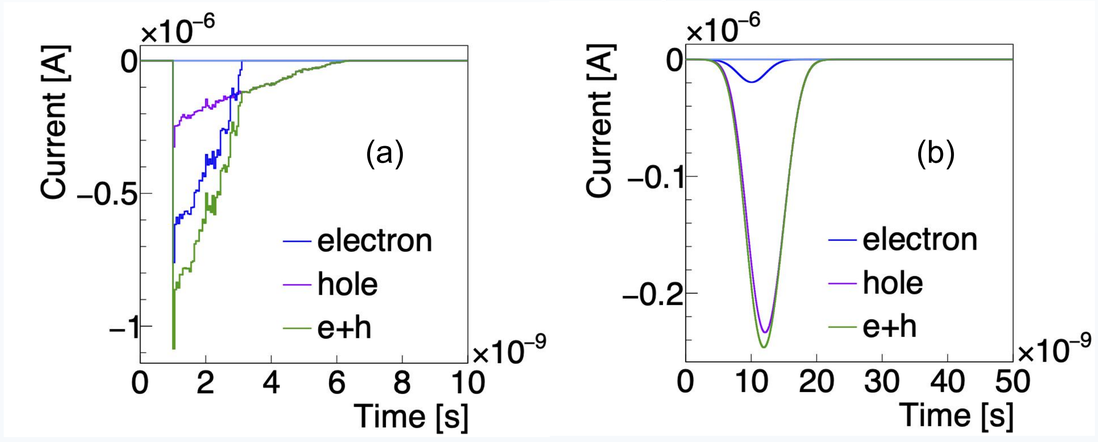

Figure 6. Sensor responce of (a) beta ray and (b) laser injection.

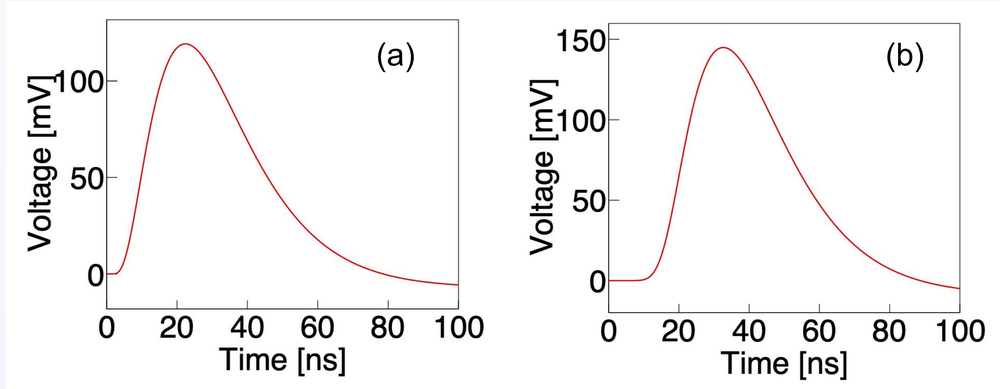

Figure 7. Amplified waveform of (a) beta ray and (b) laser injection.

Summary

Based on the fully open-source software RASER that we developed, we conducted a comprehensive simulation of the minimum ionizing particle (MIP) and laser response signals for the CMOS Strip Chip used in the CEPC inner tracker. This simulation provides an effective reference for the subsequent development and testing of the device.

Reference

[1] raser, https://pypi.org/project/raser/.

[2] Diehl, L., et al, 2022. Characterization of passive CMOS strip sensors. Nucl. Inst. Meth. A. 2022, 166671.

[3] Cormier, K.J.R., et al, 2021. Development of the front end amplifier circuit for the ATLAS ITk silicon strip detector. J. Inst. 16, P07061.

Poster #49

Design of AC-LGAD for CEPC Outer Tracker (OTK)

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1.Institute of High Energy Physics, CAS 2. University of Chinese Academy of Sciences

The Circular Electron Positron Collider (CEPC) is a future collider experiment which has huge potential for the precision measurement of standard model and exploration for the new physics. The Gas detector (dE/dx) for CEPC suffers separation problem for k/pi and k/p at low energy range which is important for the flavor physics. **Timing detector** based on the LGAD technology is proposed to improve the separation ability which is complementary to gas detector. The timing detector would have **30 ps to 50 ps** timing resolution and the **10 μm** spatial resolution at the same time due to application of the AC-LGAD technology. **Low Gain Avalanche Diode** (LGAD) has **high-precision time performance**, and the time resolution can reach 30 ps, IHEP has designed a LGAD strip prototype to verify the technical validity.

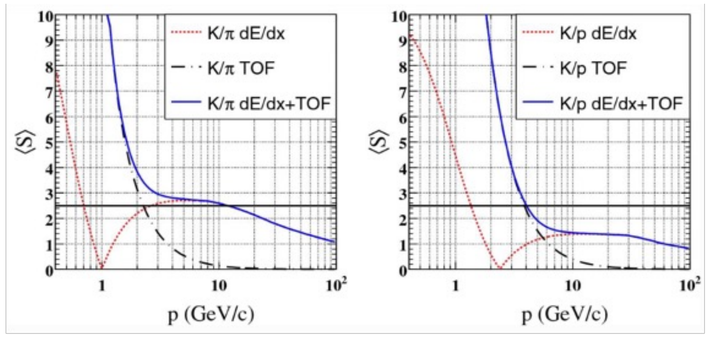
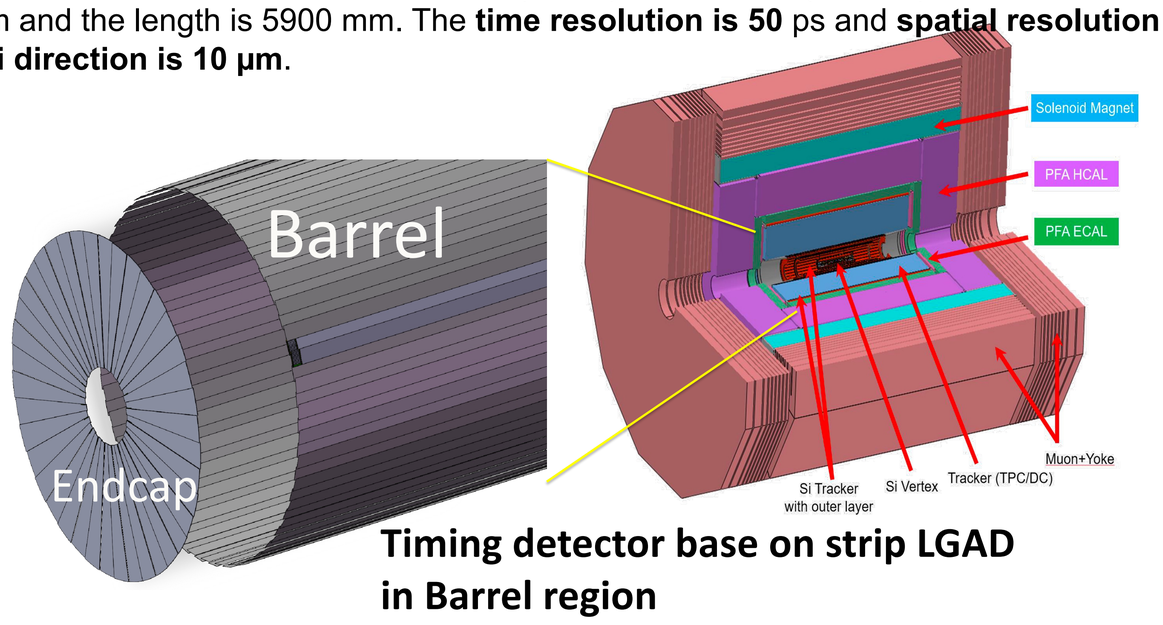
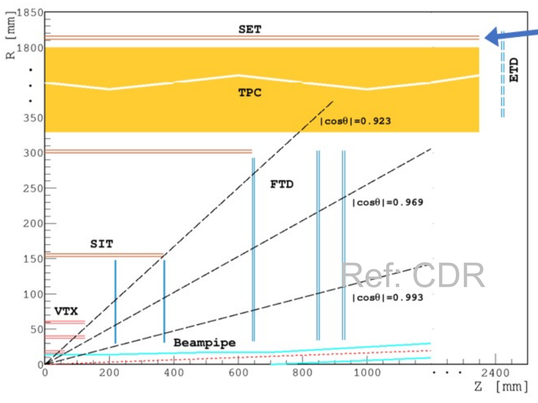


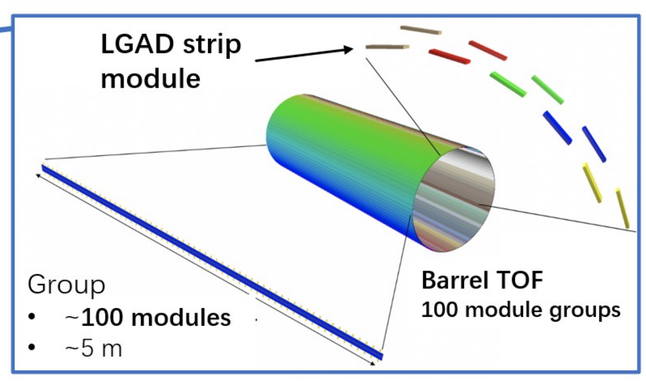
Figure 1:（left）Simulation results of the separation power for the K/pi with and without ToF，
（right）Simulation results of the separation power for the K/p with and without ToF.
(From CEPC simulation group)

Time of flight & out Tracker would be placed between the TPC and ECAL which could provide the time and spatial information for the particle track. The total coverage area would be **~90 m²** which included **70 m²** (barrel) and **~20 m²** (endcap). The radius is 1800 mm and the length is 5900 mm. The **time resolution is 50** ps and **spatial resolution at r-phi direction is 10 μm**.



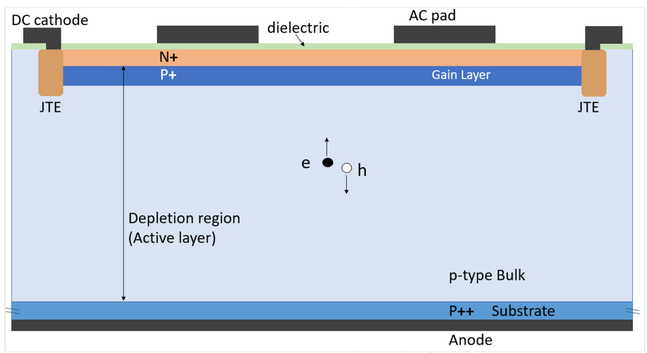
Timing detector base on strip LGAD in Barrel region



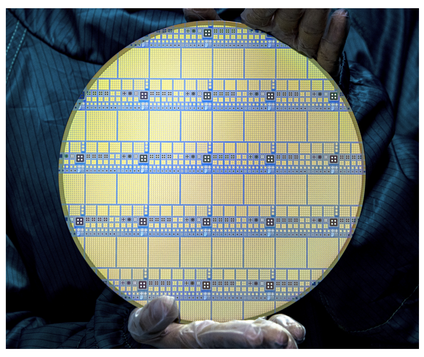


AC-LGAD (AC-coupled LGAD)

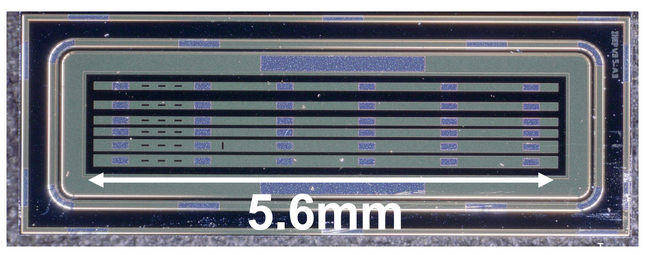
Continuous gain layer



Structure of AC-LGAD



IHEP-IME LGAD wafer



Strip AC-LGAD

Testing Results

The left figure shows the relationship between the laser intensity used for testing and the distance. The laser spot diameter is approximately 3 micrometers. The right image shows the signal waveforms read from four channels when the laser hits on the sensor surface. It can be observed that the signal peak values differ due to the varying distances between the laser incidence point and the strips.

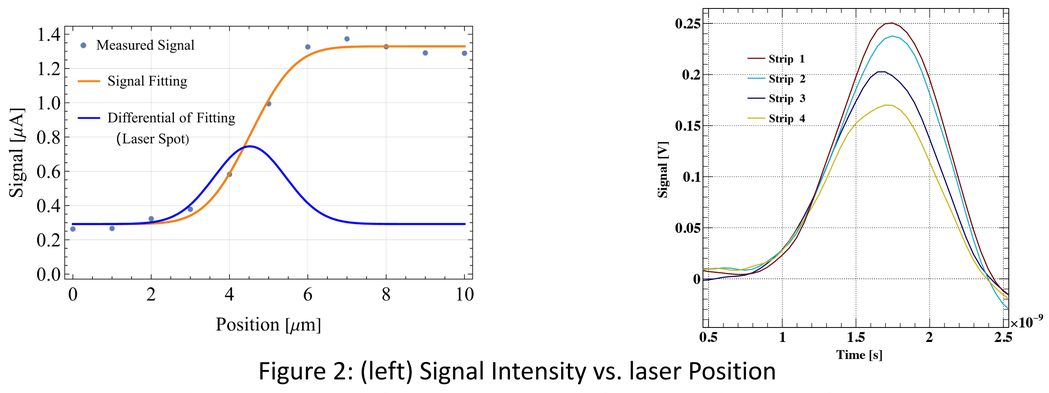
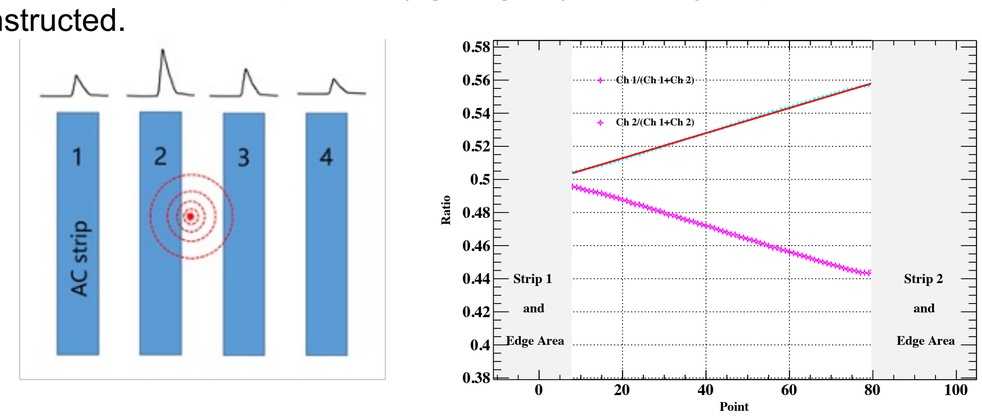


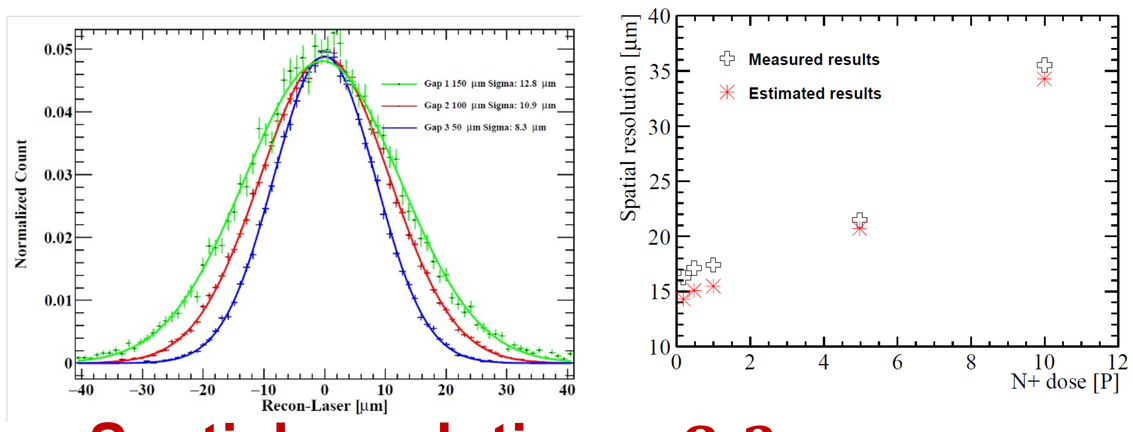
Figure 2: (left) Signal Intensity vs. laser Position
(right) Waveforms induced by a laser hit readout from 4 strips.

The method for position reconstruction is based on amplitude difference (left figure). Distribution of fraction of amplitude $\frac{Amp_2}{Amp_1+Amp_2}$ of adjacent strips has linear distribution based on the position (right figure), whereby hit position can be reconstructed.



Fugure 3: (Left) : Amplitude difference due to propagate distance.
(Right): Distribution of $\frac{Amp_2}{Amp_1+Amp_2}$ with position, showing a good linear relationship.

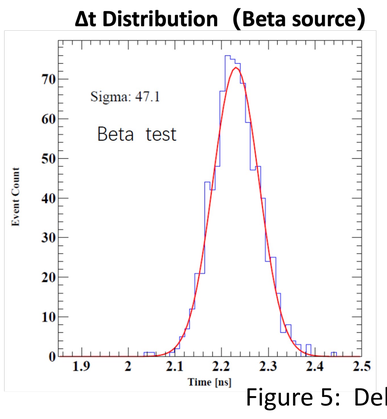
The spatial resolution of the strip AC-LGAD were tested by the Laser. The spatial resolutions of strip AC-LGADs with different pitches (150 μm, 200 μm and 250 μm) are 8.3 μm, 10.9 μm and 12.8 μm



Spatial resolution： 8.3 μm with 150 μm pitch

Figure 4: (Left) Distribution of the difference between the reconstructed position and the true position under different pitches.
(Right): Relationship between spatial resolution and gain layer concentration.

The time performance of the strip AC-LGAD were tested by the Beta source. The delta t was the difference between the arrival time of the trigger and the AC-LGAD. The sigma of the delta t distribution is combination of the time resolution of trigger and AC-LGAD. Thus according to the formula, the time resolution of **the whole AC-LGAD** is 37.5 ps.



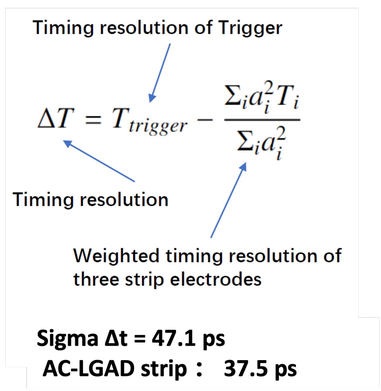


Figure 5: Delta t distribution of AC-LGAD at the Beta test

Time resolution: 37.5 ps

Summary:

AC-LGAD based Timing and out tracker detector for the CEPC is important for the flavor physics of CEPC. ToF & out tracker detector is complementary for the gas detector and help improving the k/pi,k/p separation at low energy part. It also would provide additional spatial resolution for the track due to the application of the AC-LGAD sensor technology. The total area would be about 90 m^2. The readout channels would be about 10^7. The time resolution and spatial resolution is **30-50 ps** and 10 μm (R-phi direction). In the future, the large area and very long strip AC-LGAD would be designed and produced which is very challenging.

References:

[1] CEPC Conceptual Design Report: Volume 2 - Physics & Detector
[2] Mei Zhao, et al. Low Gain Avalanche Detectors with good time resolution developed by IHEP and IME for ATLAS HGTD project.
[3] Mengzhao Li, et al. The Performance of Large-Pitch AC-LGAD With Different N+ Dose.
[4] Weiyi Sun, et al. The performance of AC-coupled Strip LGAD developed by IHEP.
[5] Weiyi Sun, et al. Development of the strip LGAD detector with double-end readout for future colliders

Poster ID: 53

Design of COFFEE2: a pixel sensor prototype in 55nm high-voltage CMOS process

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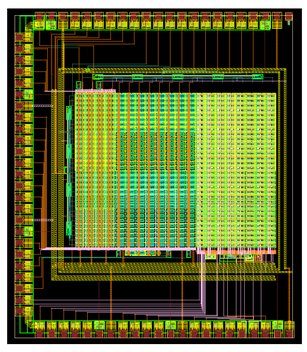
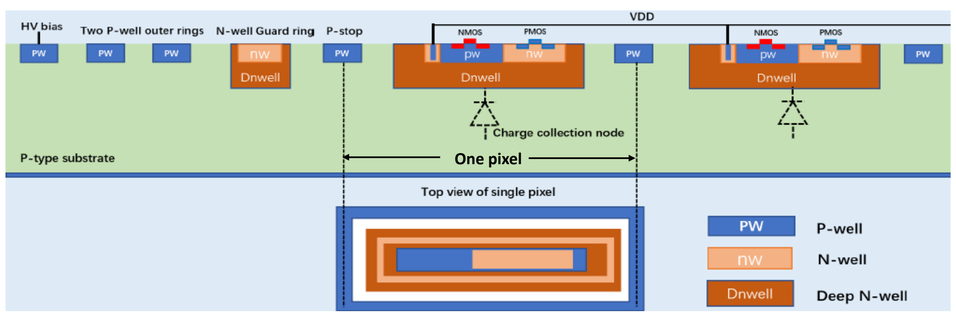
Introduction

To explore HV-CMOS processes with smaller design nodes and meet the requirements of the CEPC inner tracker, a series of chips named "COFFEE" is currently under development. This report presents the design and simulation results for COFFEE2 , which is the first prototype developed to verify the process and circuit module in SMIC High-voltage 55 nm technology. COFFEE2 features a small scale (2.2 × 2.7) mm^2 chip divided into (20 × 32) pixels with 3 variations of pixel design.



HV-55nm process

- Large electrodes: Dnwell-Psub junction as collection electrode
- Triple-well process: N-well/P-well/Deep n-well
- Low P-type substrate resistivity: 10 Ω·cm
- Guard ring: one inner N-well ring, with two P-well outer rings
- Substrate breakdown Voltage > 50V with frontside HV bias



COFFEE2 architecture & design

To quantitatively evaluate the "X-talk" issue of HV-CMOS pixel sensor technology in the new process and guide the overall design of the future detector chip, COFFEE2 includes both analog and digital readout pixel designs. The digital readout pixels incorporate two different comparator structures for comparative verification. The schematics are shown below, peripheral modules including bandgap, analogue buffer, DACs and row/column selection.

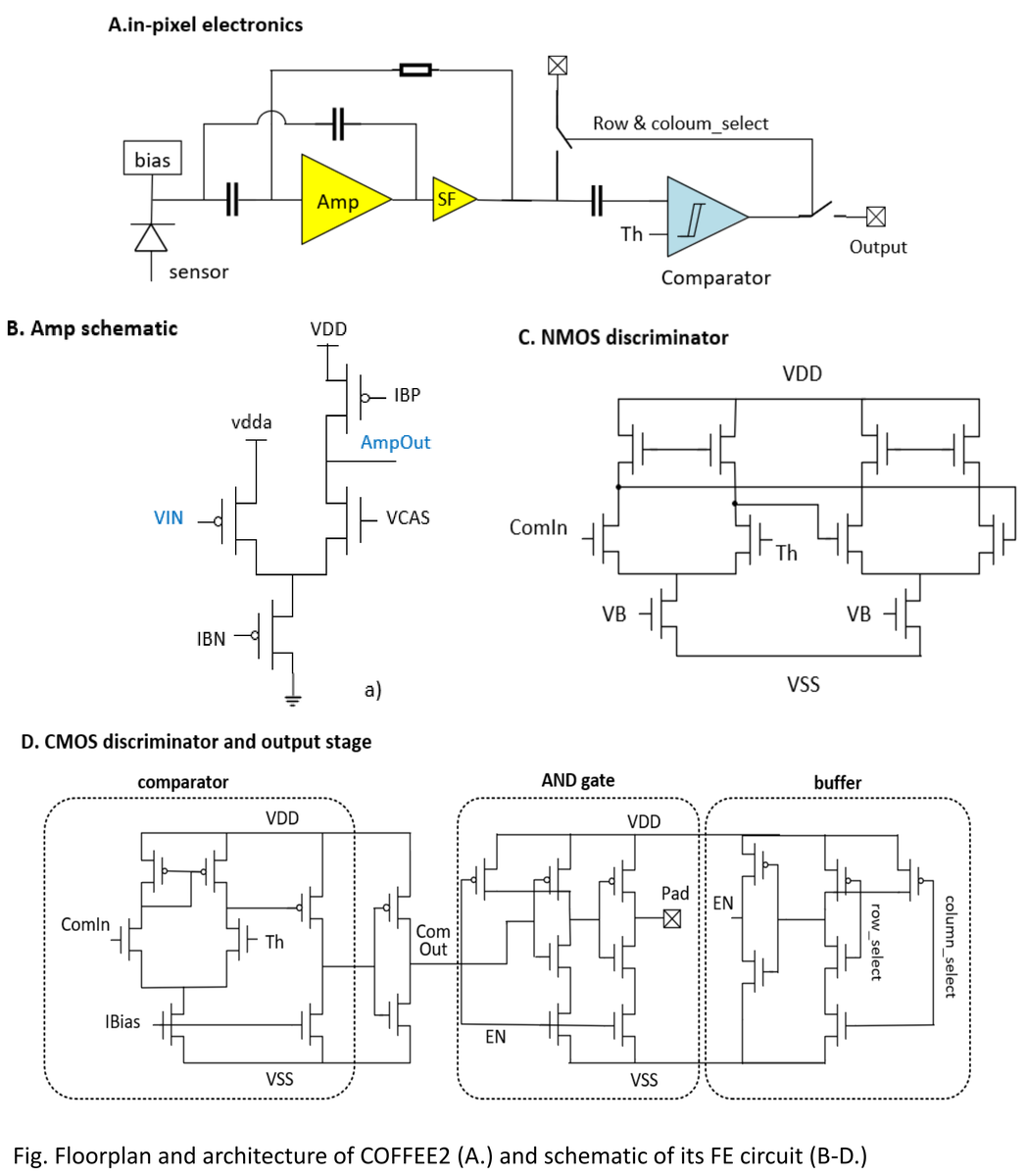


Fig. Floorplan and architecture of COFFEE2 (A.) and schematic of its FE circuit (B-D.)

Simulation results

CSA: noise and gain

Simulated noise and gain for preamplifier, as a function of detector capacitance. The estimated sensor capacitance, derived from TCAD for the three different pixel designs, ranges from 80 to 100 fF. Due to discrepancies between actual fabrication and simulation, also to provide a reference for future modifications, the simulation range has been expanded to 50-150 fF. The bias current is approximately 4.6 μA for the preamplifier.

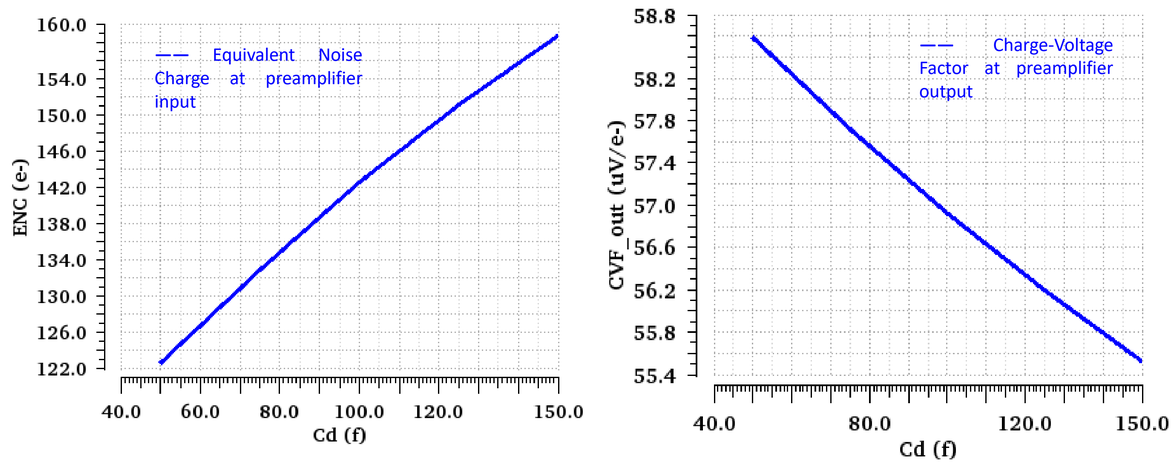


Fig. The input equivalent noise (ENC) of the preamplifier (left) and the gain in CVF (right)

CMOS/NMOS Comparator: time-walk

Figure shows the simulated waveforms of the comparator output (“ComOut”) and the CAS output (“PreAmp”), with the input charge ranging from 2k e− to 20k e−. The simulated time-walk of CMOS comparator is ~ 2 ns, for NMOS comparator has a larger value of ~ 9 ns. The bias current are ~ 15 μA and 8.5 μA, for the CMOS and NMOS comparator, respectively.

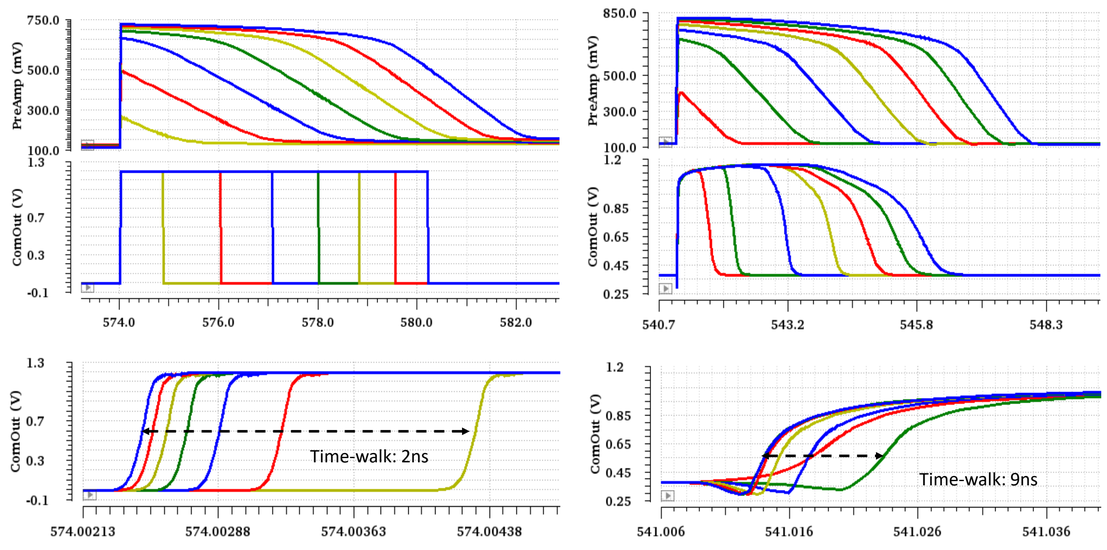


Fig. Simulated waveform of CMOS comparator (left) and NMOS comparator (right) output and time-walk

Summary & outlook

A pixel sensor prototype, COFFEE2, was designed using SMIC's 55 nm HV-CMOS technology to explore next-generation process nodes. COFFEE2 includes various in-pixel preamplifier and comparator designs. Simulations show the preamplifier’s gain and noise as functions of the input detector capacitance, while the time-walk for the two comparators is 2 ns and 9 ns, respectively, across a signal range from 2 ke^- to 20 ke^-. The testing and verification of the COFFEE2 chip are still ongoing, with preliminary test results in Zhiyu Xiang’s poster. The design of the next version, COFFEE3, is also underway, with the submission for fabrication planned for early next year.

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Poster ID: 55

TCAD Simulations of HV-CMOS

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Abstract

Technology Computer-Aided Design (TCAD) simulations were conducted on High Voltage CMOS (HV-CMOS) sensors with varying substrate resistivities. The simulations investigated how changes in substrate resistivity affect leakage current, breakdown voltage, the depletion region, and the distribution of high electric field areas within the sensor. The effects of pixel gap and p-stop on capacitance were evaluated, with simulation results agreeing with experimental measurements. Furthermore, Allpix2 simulations provided insights into the sensor's response to Minimum Ionizing Particles (MIPs), facilitating an analysis of signal collection and charge sharing phenomena across different substrate resistivities.

Structure of HV-CMOS (COFFEE2)

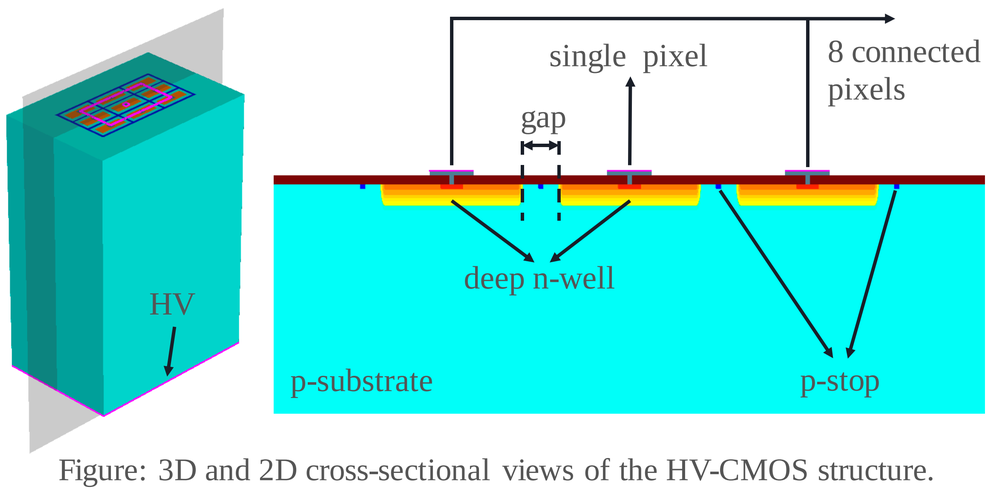


Figure: 3D and 2D cross-sectional views of the HV-CMOS structure.

- **gap**: 10/20/30 μm
- **p-substrate**

Resistivity: 10/100/500/1000/2000 Ωcm
Depth: 500 μm

- **deep n-well**

Gauss profile: $5*10^{17} \sim 1*10^{17}$ cm^{-3}
Depth: 5 μm

- **p-stop isolation**

Concentration: $1*10^{19}$ cm^{-3}
Depth: 2 μm

A simplified three-dimensional structure based on COFFEE2 (CMOS sensOrs in Fifty-FivE nanometer procEss) is simulated with varying substrate resistivities. The diode configurations include 3 gap sizes and the presence or absence of p-stop between pixels. The 8 peripheral pixels are connected in parallel for output, with HV bias applied from the bottom in the simulations.

Depletion Depth and Breakdowm Voltage

Resistivity (Ωcm) / N_A (cm^{-3})	10	100	500	1000	2000
HV (V)	1.36e15	1.33e14	2.66e13	1.33e13	6.64e12
-10	3.0	9.0	16.1	21.3	35.6
-50	6.1	19.2	37.6	53.8	76.8
-100	--	31.3	55.7	77.2	100.3
-200	--	--	--	100.3	147.1

Table: Depletion depth (μm) for varying substrate resistivities and voltages.

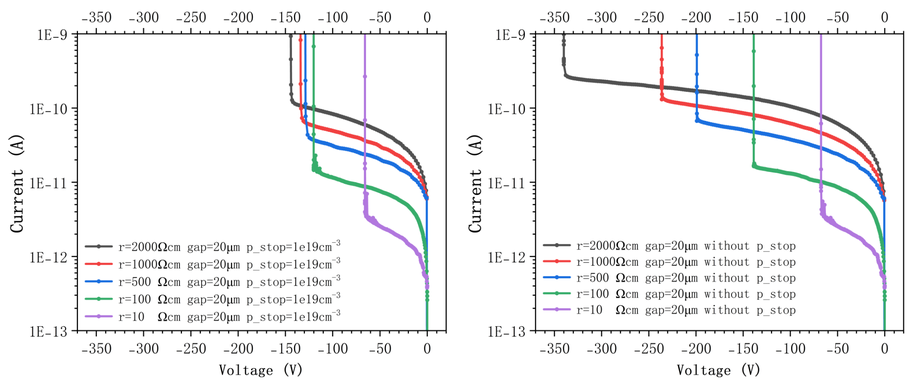


Figure: IV curves for varying resistivities, with and without p-stop.

The Depletion region depth generally follows the formula $D \propto \sqrt{V_{bias}\frac{N_A+N_D}{N_A \cdot N_D}}$. The IV curves indicates that increasing resistivity results in higher leakage current and breakdown voltage. Since this simplified model lacks complete structures like guard rings, the presence of p-stop may cause an earlier breakdown voltage.

Effects of Gap and P-stop on Capacitance

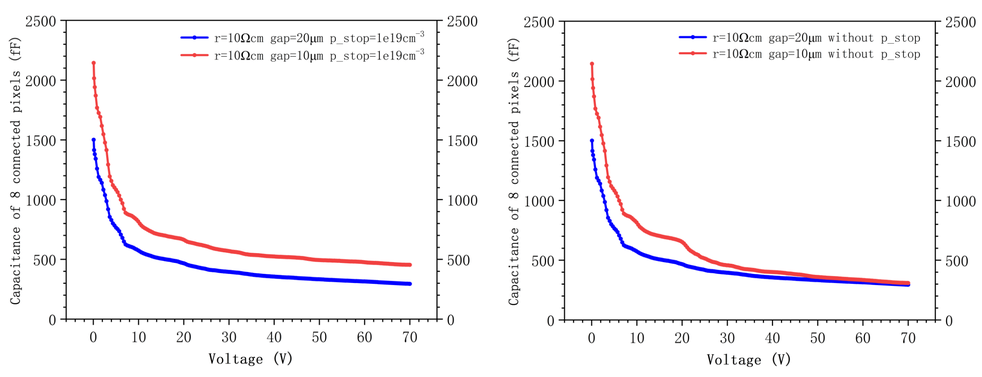


Figure: CV curves for r = 10 Ω·cm, gap = 10/20 μm, with and without p-stop.

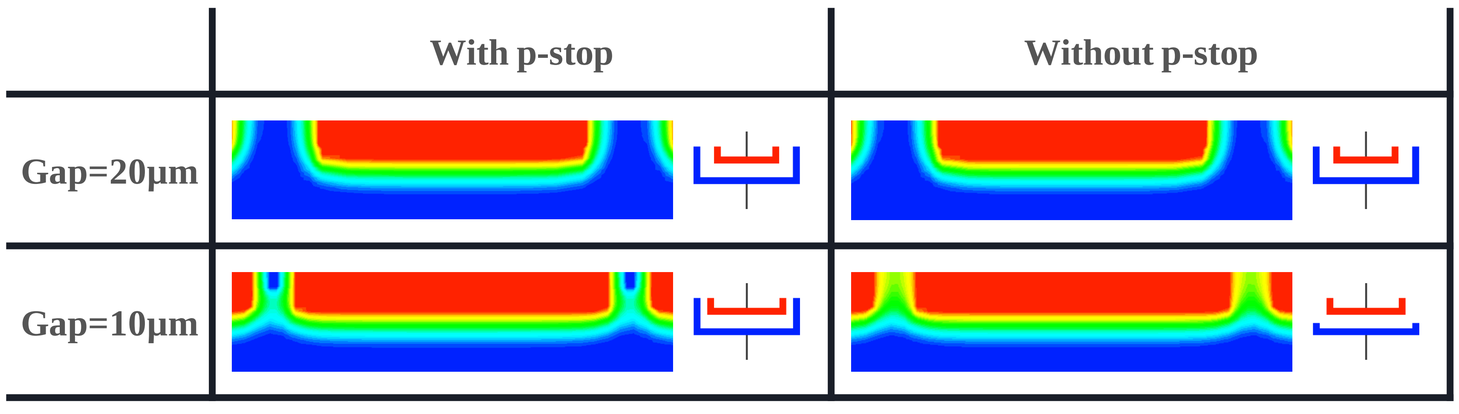


Figure: Electric potential diagram for gap sizes 10/20 μm, with and without p-stop, at HV = -70 V

The figures above are based on a substrate resistivity of 10 Ω·cm. At low bias voltages, pixels with smaller gaps have greater bottom and side areas of the DNW, resulting in higher capacitance, unaffected by p-stop. However, as bias voltage increases and the depletion region extends into the adjacent pixel, p-stop prevents a decrease in side capacitance, leading to a higher capacitance than pixels without p-stop.

MIP Test and Charge Sharing Simulation

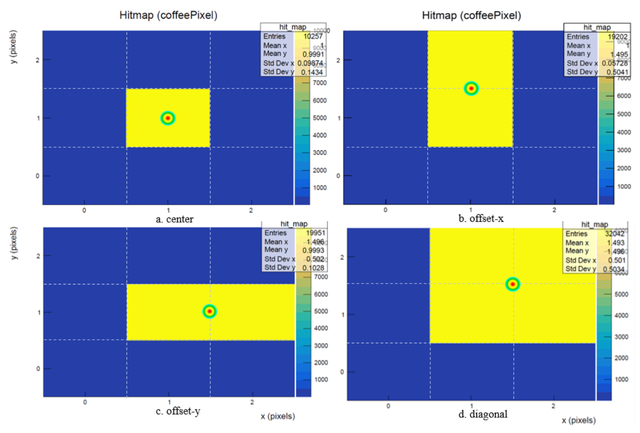


Figure: Hitmap at 4 different incident positions.

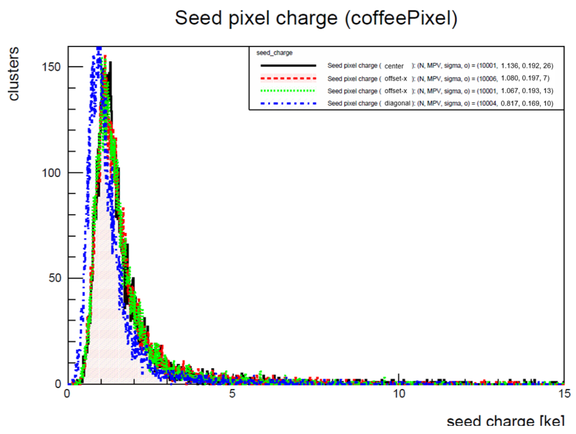
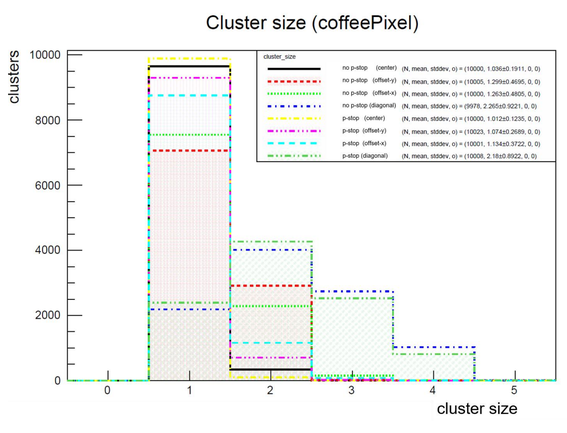


Figure: Distribution of the seed pixel signal.



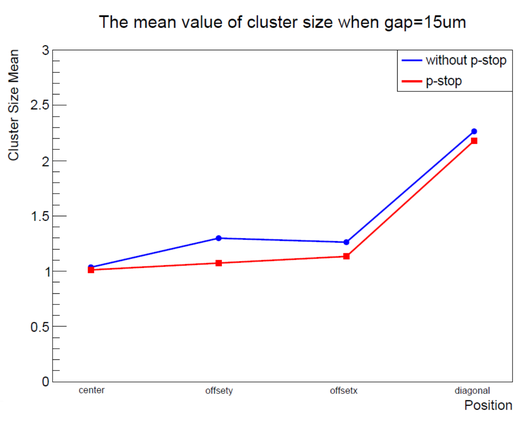


Figure: The distribution of cluster size at a threshold of 120 e-, and the mean value of cluster size.

A 3x3 pixel array on a 10 Ω·cm resistivity substrate (gap=15μm) is simulated by integrating a detailed TCAD electric field model into the Allpix2 framework. A 4 GeV proton beam (MIPs) incident on the array is modeled, and the seed pixel signal for different impact positions (center, offset-x, offset-y, diagonal) is shown. The MPV of the Landau distribution ranges from 0.8 to 1.1 ke-. The cluster size is approximately 1 for center incidence, reaching 2.3 for diagonal incidence. The average cluster size indicates that the p-stop structure effectively reduces charge sharing.

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Poster ID: 61

Beam Background Study for the CEPC Silicon Tracker

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Introduction

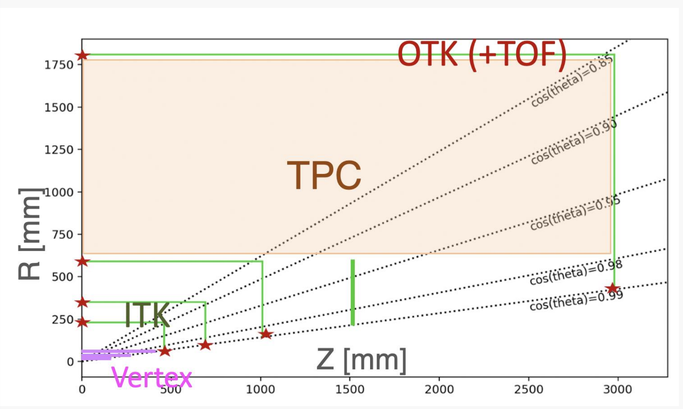
- The hit rate of the CEPC silicon tracking system, induced by beam background processes, will impact irradiation, data rates, and the design of the detector.
- The study of hit rate can also help develop methods to decrease the hit rate resulting from beam induced background.
- Pair production background represents the most important detector background at CEPC, as induced particles position is near IP and difficult to be shielded.

Pair Production

- Pair production [1] : electron-positron pairs are produced via the interaction of beamstrahlung photons with the strong electromagnetic fields of the colliding bunches.
- Electrons and positrons of pair production are generated near IP, with low generated momentum (~0.12GeV) and close to beampipe (cos(θ)~0.99).

CEPC Silicon Tracker

- CEPC silicon tracker consists of Inner Tracker Barrels (ITK-Bs), Inner Tracker Endcaps (ITK-Es), Outer Tracker Barrel (OTK-B), and Outer Tracker Endcaps (OTK-Es), as shown in Fig.1. The detailed positions of the detector layout are tabulated in Table.1.



Fig,1 The layout of CEPC tracker system

Endcap	Z [mm]	R_{in} [mm]	R_{out} [mm]
ITK-E1	500.5	75	240
ITK-E2	715	101.9	350
ITK-E3	1001	142.6	600
ITK-E4	1500	213.7	600
OTK-E	2903	406	1810

Barrel	R [mm]	Half Z [mm]
ITK-B1	240	500.5
ITK-B2	350	715
ITK-B3	600	1001
OTK-B	1800	2000

Table.1 The position of CEPC silicon tracker

Introduction to CEPCSW

- The silicon tracker background evaluation is based on CEPC offline software, CEPCSW [2], developed based on Geant4 and edm4hep, within the Gaudi framework.
- CEPCSW incorporates precise description of detector geometry, comprehensive simulation of physics processes, detector digitization, and reconstruction.

Silicon Tracker Hit Rate

- The pair production generator is provided by MDI group. The detector hit rate is defined as the number of particle hits per area per second. The estimated results of maximum and average hit rates for individual silicon tracker detector are shown in Fig.2.

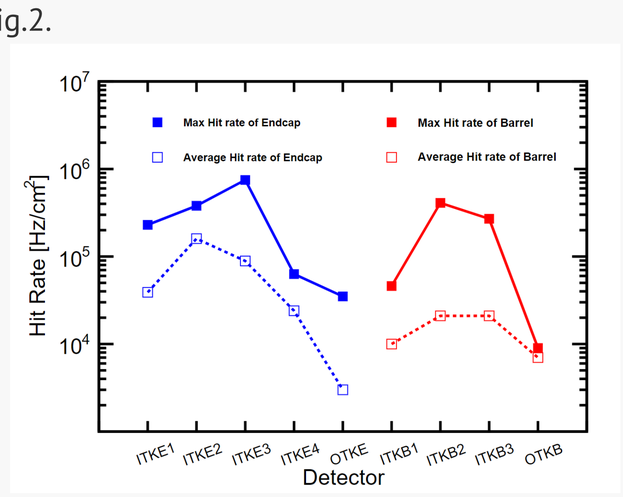


Fig.2 The hit rates for individual silicon tracker detector

- As shown in Fig.2, for ITK, the highest max hit rate region is the 3rd layer of endcap (ITK-E3), while the highest average hit rate is the 2nd layer of endcap (ITK-E2).
- The detailed investigation of maximum hit rates appeared on ITK-E3 induced by beam background will be elaborated in the next section.

ITKE3 Hit Map

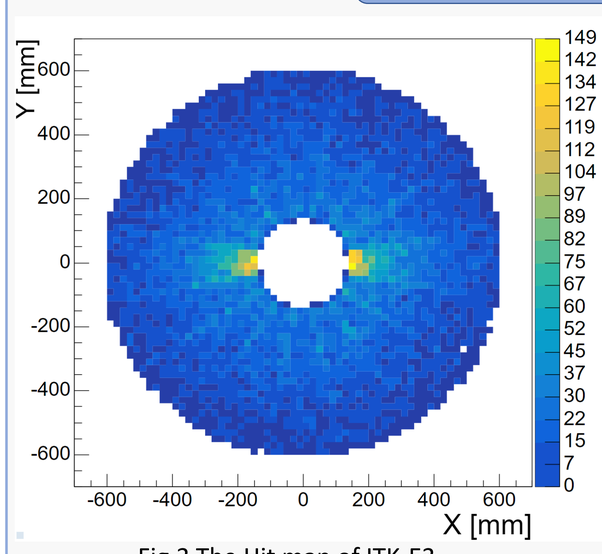
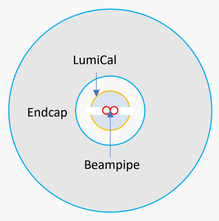


Fig.3 The Hit map of ITK-E3

- As shown in Fig.3, the highest hit region in ITK-E3 near phi=0 and phi=π is caused by the gap structure of LumiCal at z~1000mm.



- This results shows that material distribution close to beampipe has great impact on hit map.

Impact from beampipe

- The magnet in the beampipe leads to the increase of the material budget and the interaction background particles, as shown in Fig.4.

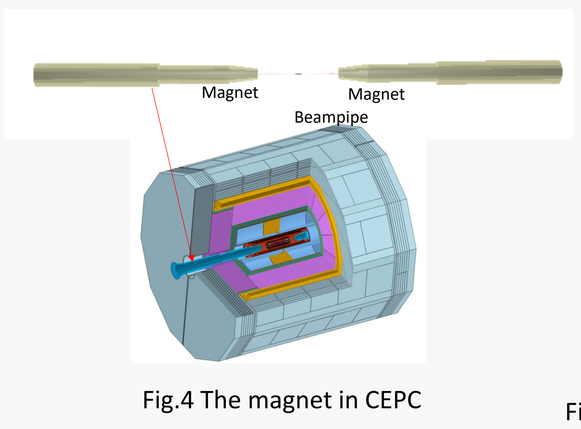


Fig.4 The magnet in CEPC

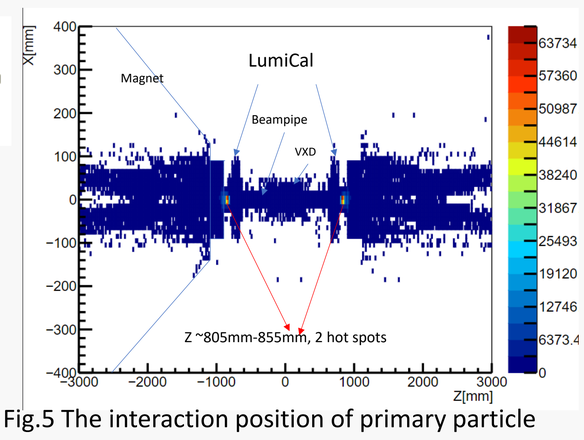


Fig.5 The interaction position of primary particle

- The interaction of background particles mainly occur between 805mm and 855mm in z axis, as shown in Fig.5.
- After interaction, the background particles might be absorbed, or create more tracks and secondary particles.

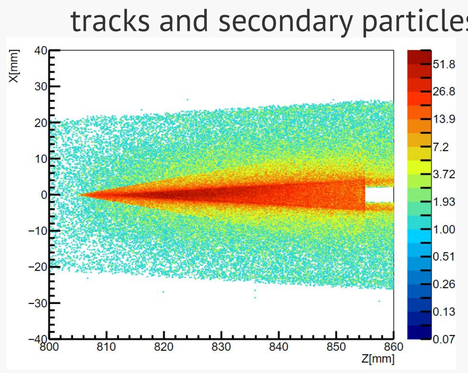
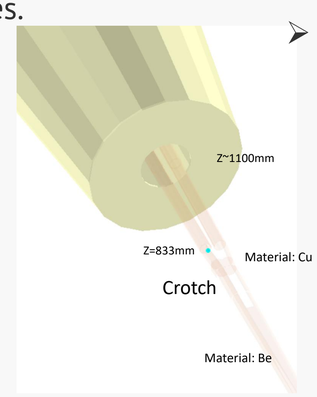


Fig.6 most particles end in crotch region



- At 805mm, the particle will hit the crotch of the beampipe, with the transition from light material Be to heavy material Cu. We can call them "crotch particles
- Since ITK-E3 is at z~1000mm close to the beampipe, the secondary particles generated between 805mm and 855mm are more likely to hit ITK-E3.

Hit by beampipe crotch particles

	Z [mm]	Average hit rate [10^4 Hz/cm^2]		Crotch Particle Fraction [%]
		All particles	No Crotch particles	
ITKE1	500.5	3.9	3.1	20.5
ITKE2	715	16	12	25.0
ITKE3	1001	8.9	6.6	25.8
ITKE4	1500	2.4	1.8	25.0
OTKE	2903	0.30	0.23	23.3

- The particles that interacts in crotch region (only about 50mm length) bring about 25% of the hit on the sensors in the detector region, as shown in Table.
- Optimization of shielding to reduce the beam background will be performed in future study.

Summary

- The max hit rate and average hit rate study for the CEPC silicon tracking system, induced by beam background processes has been studied.
- The crotch of the beampipe with heavier materials, introduces more particle interaction.
- The particles that interact in crotch region bring about 25% more hits, mainly on ITKE3, which can be reduced by shielding optimization in future.

Reference

[1] Dong, M., et al.: CEPC Conceptual Design Report: Volume 2 - Physics & Detector (2018) arXiv:1811.10545 [hep-ex]

[2] CEPCSW, https://code.ihep.ac.cn/cepc/CEPCSW

Geometric Optimization Simulation of the CEPC Vertex Detector

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Institute of High Energy Physics, CAS

Poster ID: 67

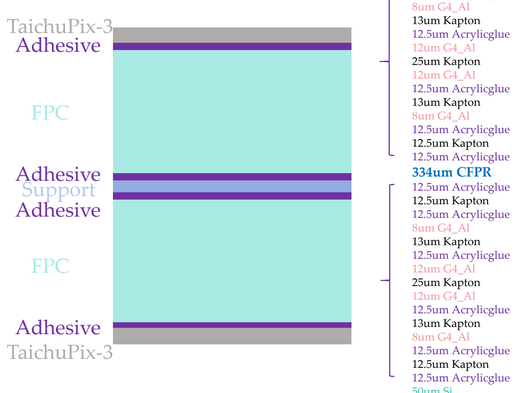
Introduction

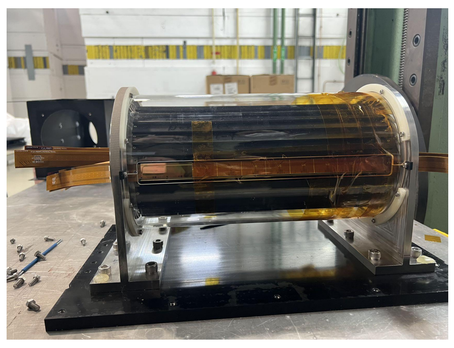
The identification of heavy-flavored quarks and τ leptons is an important physics goal of the Circular Electron Positron Collider(CEPC). The vertex detector of the CEPC is capable of obtaining precise track parameters of charged particles in the vicinity of the Interaction Point to reconstruct the decay vertex of short-lived particles. The CEPC vertex detector currently adopts two schemes, one based on the MOST2 prototype Long Barrel scheme, and the other based on the bent MAPS Stitching Mixing scheme. Both structures currently cover a polar angle of 8.1° along the length of the z-direction using a chip with a single-point spatial resolution of 5um. Based on the radius of the beam pipe of 10 mm in the CEPC-TDR, the minimum radii for the Long Barrel scheme and the Stitching scheme are 12um and 11.06um, respectively.

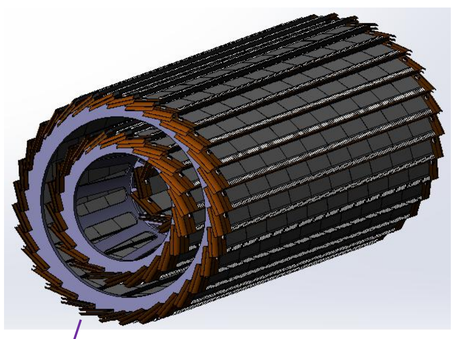
Structure

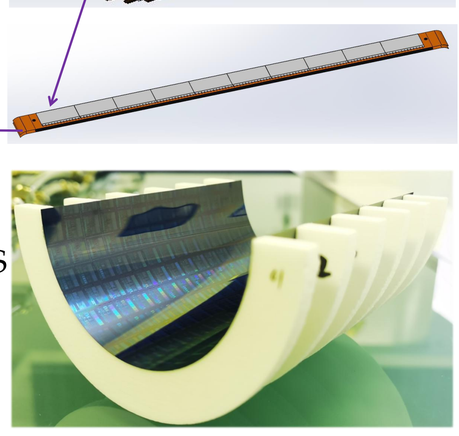
Long Barrel scheme

- Ladders using TaichuPix-3 chips **on both sides** as repeating units for each layer;
- TaichuPix-3 adopts a 180 nm CIS process with sizes of 15.9mm * 25.7mm;
- Carbon fiber, along with flexible circuit boards, is affixed to both sides as a support structure.









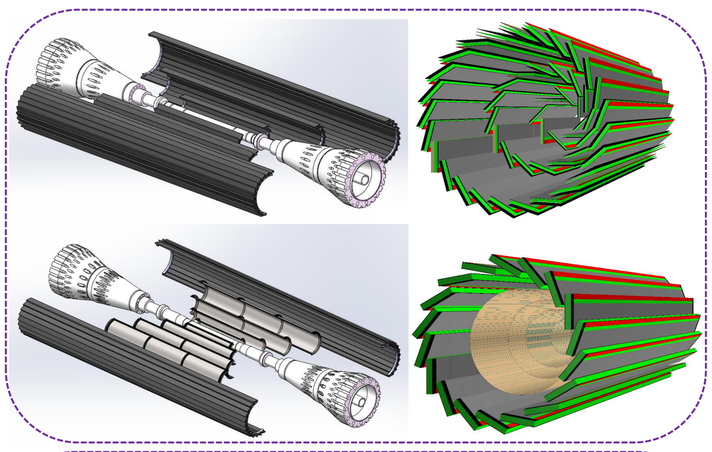
Stitching Mixing scheme

- A bent MAPS sensor adopts a 65nm CIS process with sizes of 17.277 mm * 20.2mm;
- Chips are fixed on the support.

Details of the two schemes placements

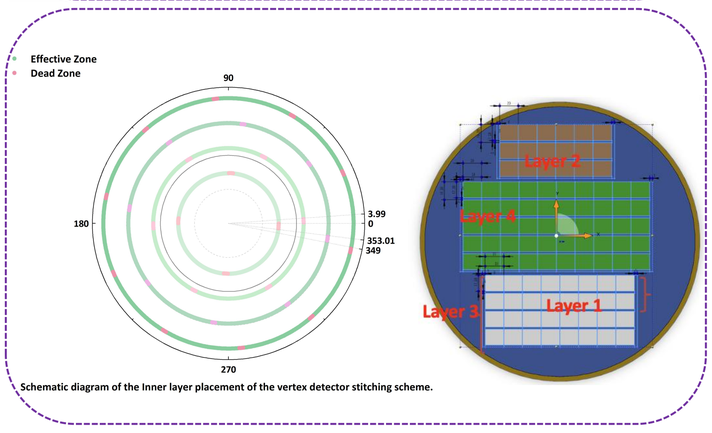
Long Barrel features:

- Innermost layer radius: ~12mm;
- Three layers of ladder from inside to outside (total of six layers of chips);
- Different thicknesses of support structure for load-bearing consideration.



Stitching Mixing features:

- Innermost layer radius: ~11mm;
- Specific starting angle for each chip layer to ensure that outgoing particles pass through at most one dead zone in a straight line;
- Utilizing four layers of curved chips and one ladder layer.



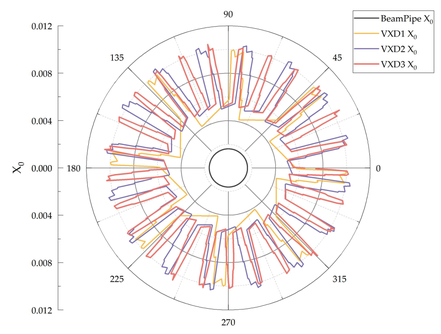
Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.

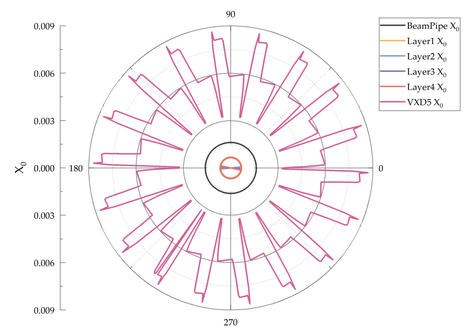
	layer/VXD X	radius .mm	length .mm	arc length .mm	height .mm	support thickness .um
Long Barrel	VXD1	12.46	260.0		1.7	334
	VXD2	27.89	494.0		2.5	358
	VXD3	43.79	749.0		3.2	370
Stitching Mixing	layer 1	11.06	161.4	69.108		45
	layer 2	16.56	242.2	103.662		32
	layer 3	22.06	323.0	138.216		31
	layer 4	27.56	403.8	172.770		29
	VXD5	34.74	500.0		2.8	363

Material budget

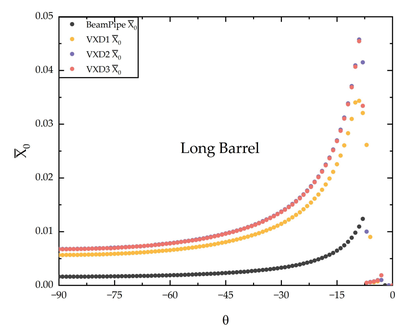
Long Barrel scheme:

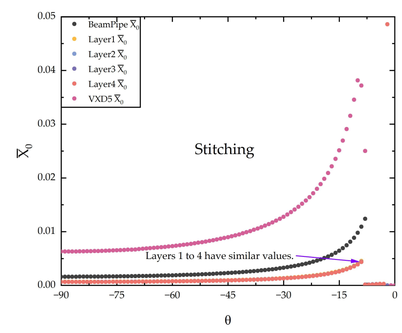
- More chips used in middle and outer layers, so additional four layers of aluminum in each for stability and to prevent significant deformation.





The material budget X_0 of the long barrel structure varies with φ when $\theta = -90°$.

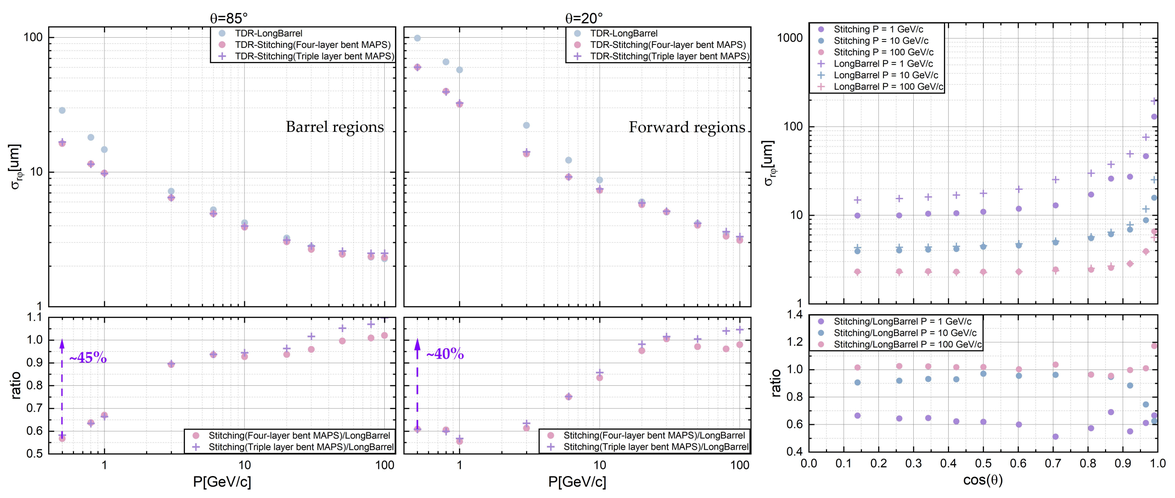




The average value $\overline{X_0}$ within the range of $\varphi \in (0, 360)$ varies with θ.

Mat	BeamPipe	Layer /VXD 1	Layer/VXD 2	Layer/VXD 3	Layer 4	VXD5
Long Barrel	0.162%	0.565%	0.676%	0.672%		
Stitching	0.162%	~0.06%	~0.06%	~0.06%	~0.06%	0.629%

Performance



- When the momentum of the outgoing particle μ^- is lower than 40 GeV/c, the TDR-Stitching Mixing scheme uses four-layer bent MAPS to perform better than the TDR-LongBarrel.
- The TDR-Stitching Mixing scheme employs triple-layer bent MAPS and four-layer bent MAPS in the low momentum range, with nearly identical performance in terms of the impact parameter d_0.
- In the low momentum range, the TDR-Stitching Mixing scheme uses four-layer bent MAPS to improve d_0 by nearly 40% compared to the TDR-LongBarrel for particles emitted at any angle.

Summary

- The TDR-Stitching Mixing scheme features a reduced material budget compared to the TDR-Longbarrel scheme, resulting in a smaller d_0 resolution in the low momentum range;
- The TDR-Stitching Mixing scheme utilizing triple-layer bent MAPS demonstrates performance nearly equivalent to that of the four-layer MAPS;
- Further detailed simulation and optimization of the TDR-Stitching Mixing scheme are planned for the future.

Reference

I. Chengdong Fu, “Silicon Tracking at CEPC ”, The 2023 international workshop on the High EnergyCircular Electron-Positron Collider, 23-27 October 2023, Nanjing.
II. Hao Zeng, “Optimization of Silicon Pixel Vertex Detector for CEPC”, Joint Workshop of the CEPC Physics, Software and New Detector Concept, 14-17 April 2021, Yangzhou.
III. http://code.ihep.ac.cn/cepc/CEPCSW

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Poster ID: 88

Design and Optimization of the CEPC Tracking System

Geng Qinglin, Li Gang

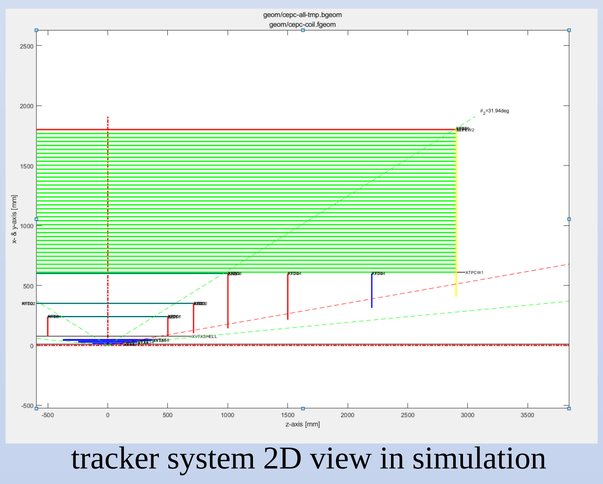
Abstract

The Circular Electron Positron Collider (CEPC) is specifically designed for in-depth studies of Higgs, W, and Z bosons, as well as heavy flavor particles. The precision tracking system is pivotal for the success of these physics studies. This presentation will delve into the software tools include fast simulation as well as optimization standards that have been meticulously selected, and applied it to achieve best performance. The presentation will showcase the impact of these optimizations on key performance indicators such as momentum resolution, tracking efficiency, and the robustness of the track fitting process.

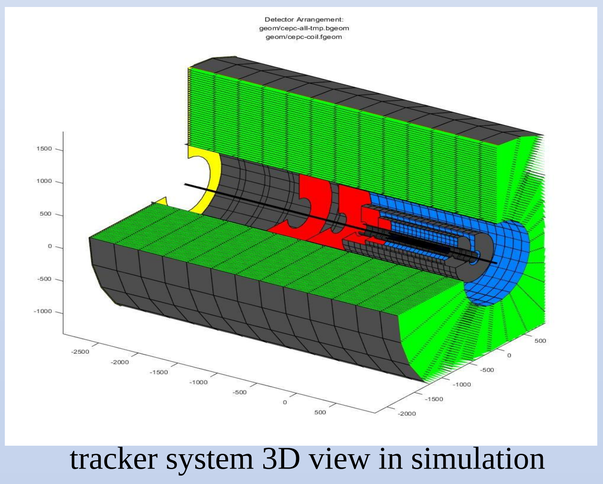
Details

Simulation Tool

Introduction: The "LiC Detector Toy" (LDT) software tool which has been developed for detector design studies, aiming at investigating the resolution of reconstructed track parameters for the purpose of comparing and optimizing detector set-ups. It consists of a simplified simulation of the detector measurements, based on a helix track model and taking into account multiple scattering, followed by full single track reconstruction using the Kalman filter. The software runs under Matlab and Octave, with an integrated GUI.



tracker system 2D view in simulation



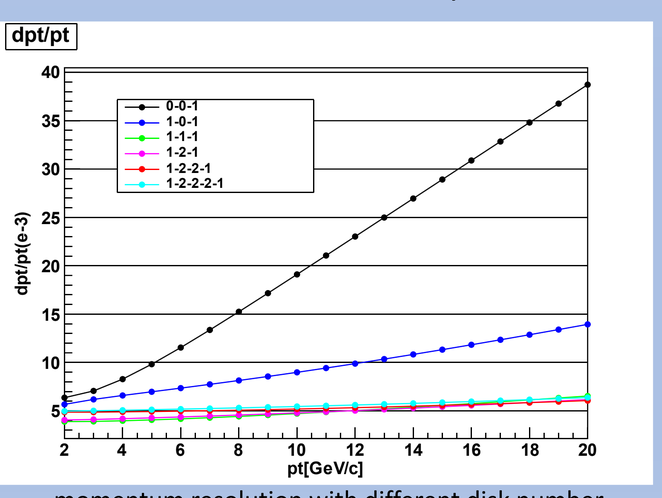
tracker system 3D view in simulation

Simulation method: Based on LDT software, we can change the layout, material budgets, spatial resolution, and hit efficiency of each sub-detector in the tracking system to achieve optimal performance.

Optimizations for Momentum resolution

The momentum resolution of tracking system is influenced by various factors, among which the layout of inner tracker(ITK) is one of its important factors.

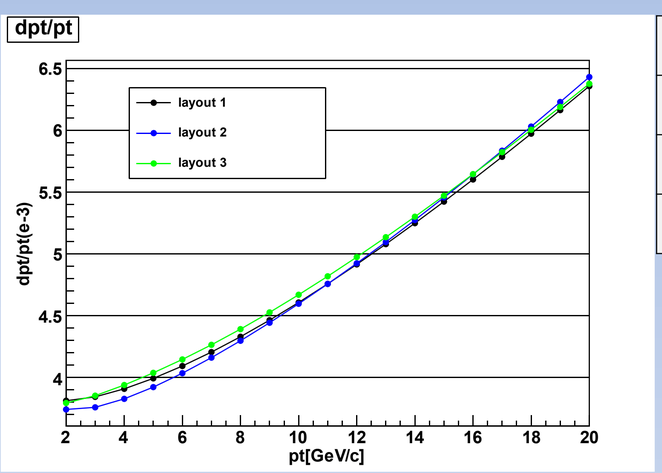
ITK endcap : The key to the impact of endcap layout on momentum resolution lies in its number and position. we tried different combinations of ITK endcap positions and numbers, compared the momentum resolution of each different combination, and selected the optimal layout.



momentum resolution with different disk number

We fixed the position of OTK and simulated the performance of different numbers of endcaps from 0 to 4. (the legend "-2" represents double layers)

The results show that no disk and one disk have poor performance; Two, three, and four disk perform well and are similar.

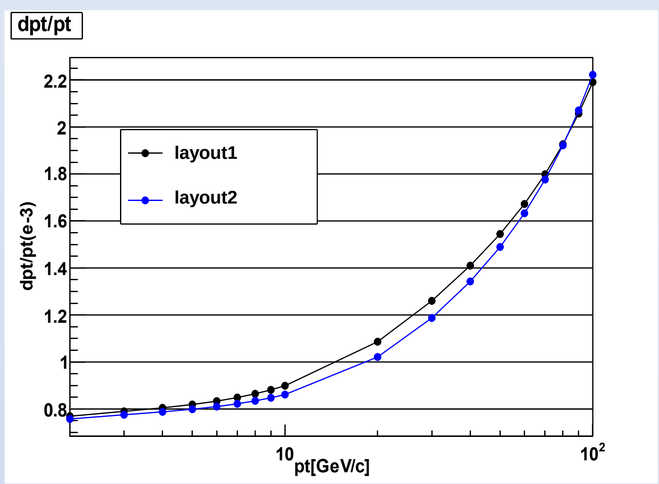


momentum resolution with optimized layout

	Disk z position(mm)		
layout1	1750	2680	2830
layout2	1125	2500	
layout3	500	1750	2680

After comparing the layouts of different combinations, we selected the best three .And they have little difference from each other

ITK barrel : Similar to endcap, we select the one with the best momentum resolution from different combinations of position numbers.

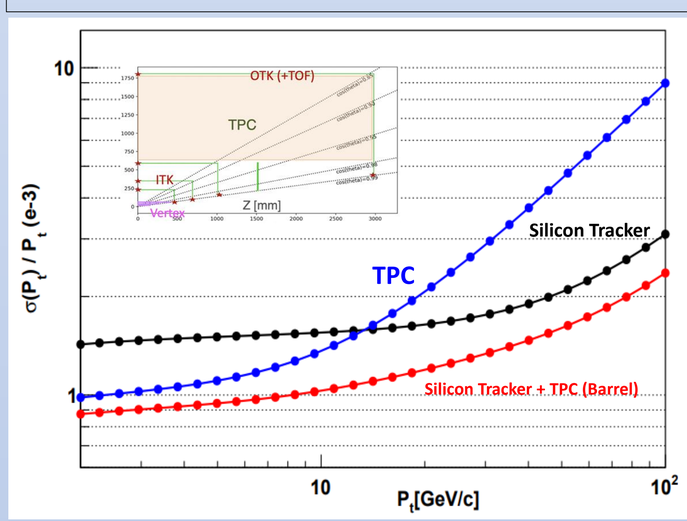


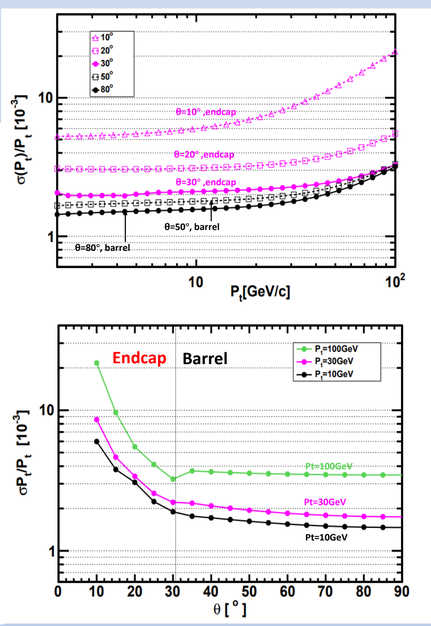
momentum resolution with different barrel layout

	ITK barrel R position(mm)		
layout1	90	364	500
layout2	90	310	400

The layout of ITK has a relatively small impact on momentum resolution, with dibarrelfferences within 0.1 ‰ for different combinations.

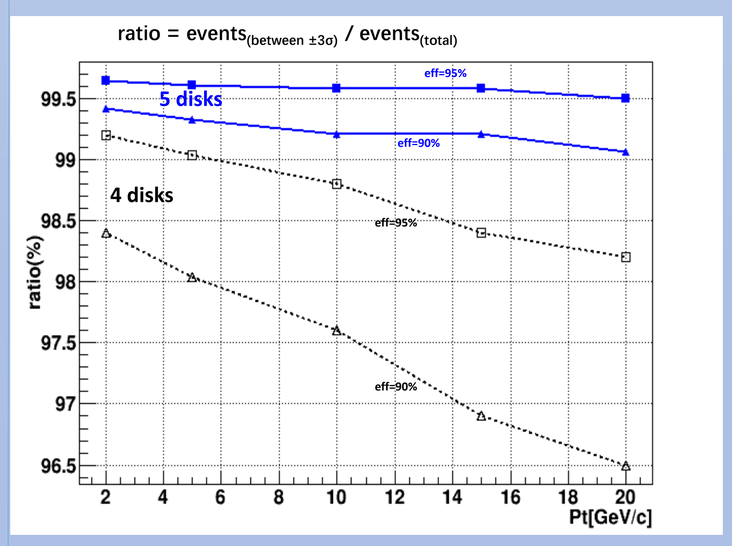
Tracking performance from fast simulation





Optimizations for tracking efficiency

For each sub-detector of tracking system, we set different hit efficiencies and observed their residual distribution of momentum resolution. Then take the events ratio within 3 σ as the tracking efficiency, and observe the impact of layout on it.



tracking efficiency in different disk number

We simulated the problem of decreased tracking efficiency caused by the loss of measurement points. And the effect of increasing the number of endcap layers on reducing this impact.

Summary:We studied the effects of different layouts on momentum resolution and tracking efficiency using fast simulation tools. For the endcap region, increasing the number of layers can improve tracking efficiency, but it can also increase scattering effects and lead to decreased resolution; Due to the presence of TPC in the barrel region, the impact of layout is relatively small. And we also give the performance of momentum resolution in current tracking systems. We will verify it through more detailed simulations in the future.

ID: 106

Transition-Edge Sensor Microcalorimeter Development for Particle Physics at IHEP

The transition-edge sensor (TES) is a type of thermal equilibrium superconducting detectors that offers excellent energy resolution, a wide dynamic range, and high quantum efficiency. The Group of Low-Temperature Detectors at IHEP develops TES microcalorimeters for neutrino-less double beta decay (0$\nu\beta\beta$) experiments and high energy astrophysics missions.

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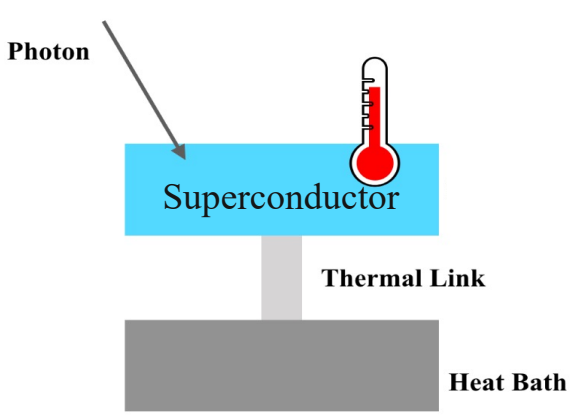
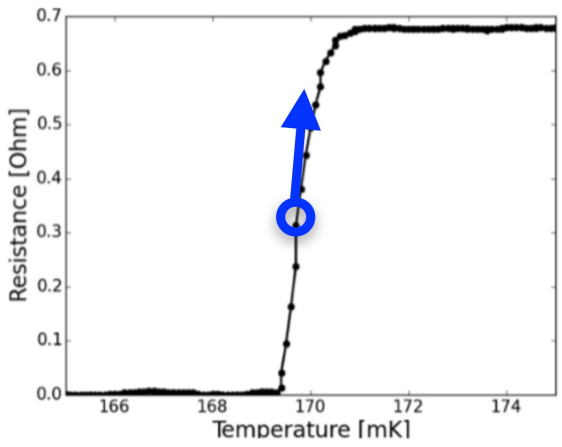
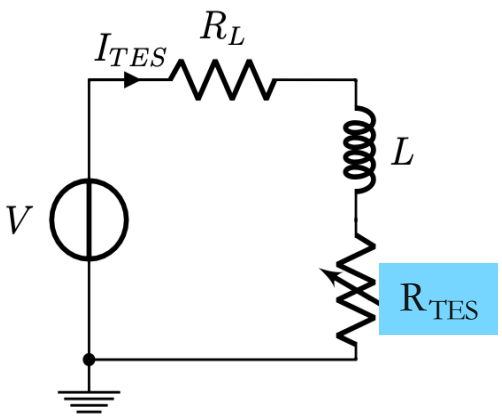
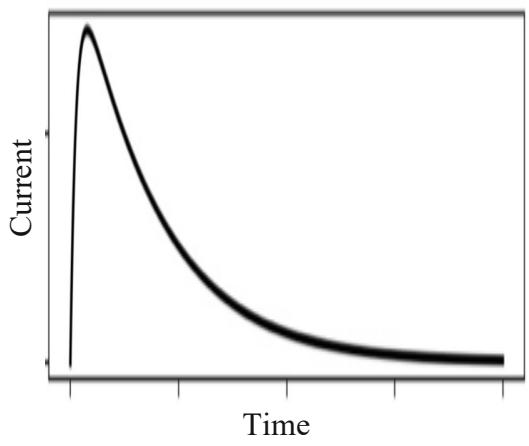
✉ yandk@ihep.ac.cn, zhangyf@ihep.ac.cn

Transition-edge sensor: towards better energy resolution

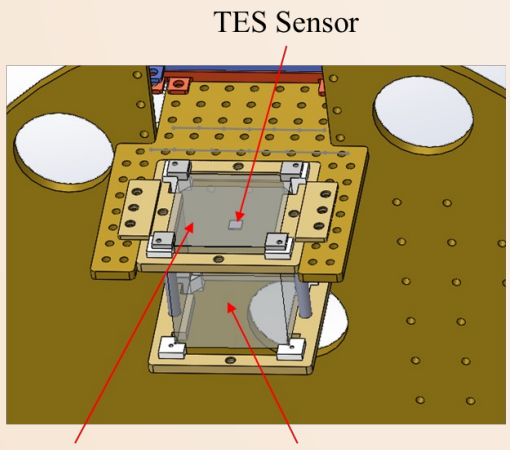


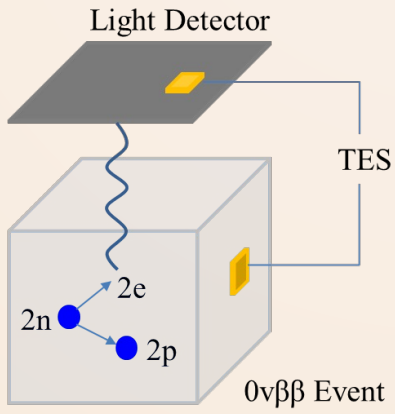






Neutrino-less double beta decay (0$\nu\beta\beta$): Majorana particle?

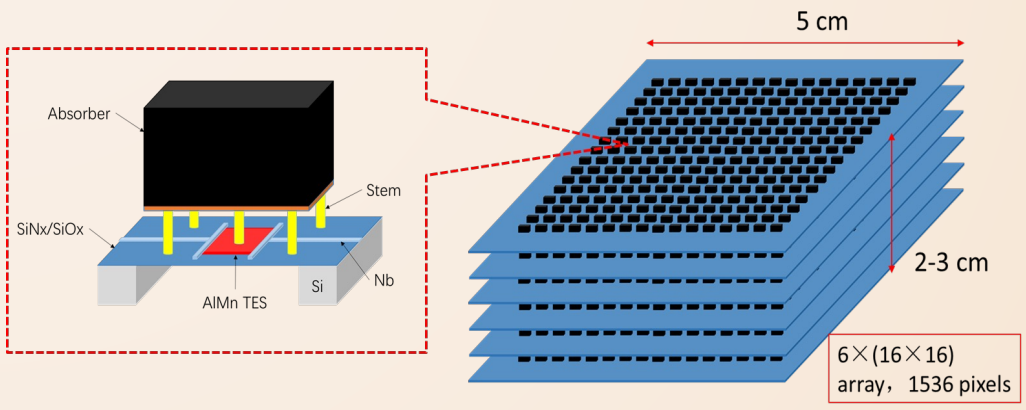




Science Goal:
- Validate the Majorana theory by detecting the 0vββ event of ^{100}Mo isotope
- Discover new physics beyond the standard model of particle physics.

Tech. Target:
- resolution: < 5 keV @ 3.034 MeV
- response time: 10-100 μs

511 keV space mission



Science Goal:
Origin of positron and its distribution in the center of the Milk Way.

Tech. Target:
- saturation: E > 511 keV
- resolution: E/ΔE > 1000
- focal plan detector area: >10 cm^2 (single layer)
- efficiency: 93% @ 511 keV

Future Work

1. TES energy resolution improvement
2. Large array fabrication and uniformity examination

Geometry implementation of CEPC Tracker in CEPCSW and full simulation validation

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on behalf of the CEPC ITK working group

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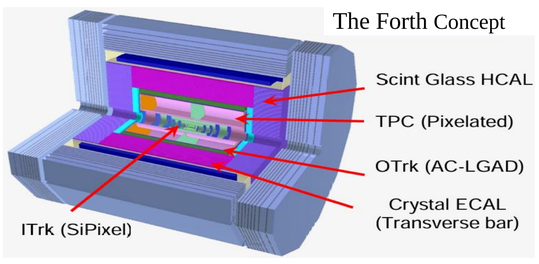
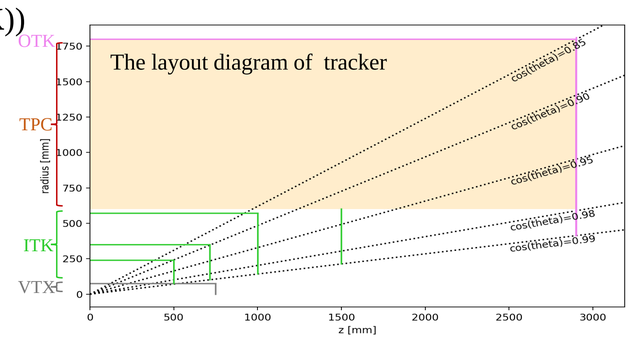
1.Abstract

The tracking system of CEPC plays an important role in **tracks reconstruction** and **PID**. The ITK working group reports a preliminary layout design of CEPC tracker based on the 4th CEPC conceptual detector. To verify its reliability and performance, it's necessary and urgent to study the momentum resolution and the PID capability of the tracker system using full simulation implemented in the CEPCSW framework. Meanwhile, a kind of staggered staves geometry of ITK Barrel (ITKB) was created in CEPCSW by DD4hep to better serve the simulation.

2.Introduction

- The tracking system of the fourth conceptual detector at CEPC consists of a silicon pixel vertex detector, a silicon tracker of HV-CMOS and LGAD, and a time projection chamber (This poster focus on **inner tracker** (**ITK**))

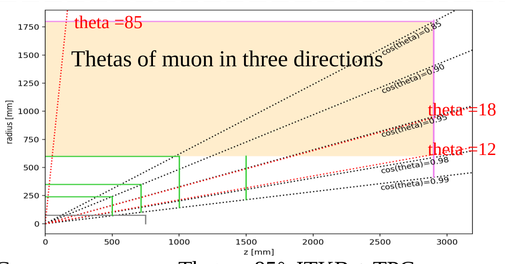




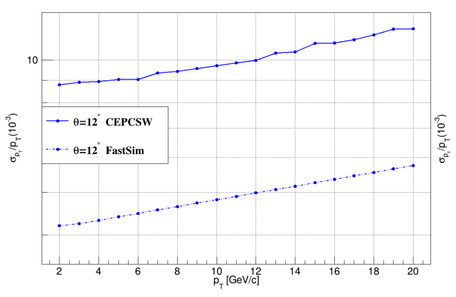
- ITK working group layout, compare with the initial
  - The third layer of ITK Barrel **closer** to TPC
  - The ITK Endcaps **cover more area**
  - **Finer** resolution of silicon sensor
- Tool: ILCSoft tracking MarlinTrk (full simulation), maintained , implemented in CEPCSW

3. ITK momentum resolution

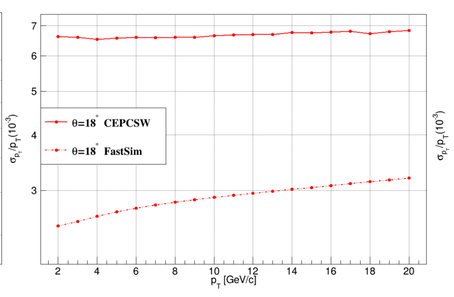
- Setting
  - Momentum resolution studied using muon events in range [2,20] GeV, for each momentum point 30k events are generated
- Three geometrical regions are studied separated



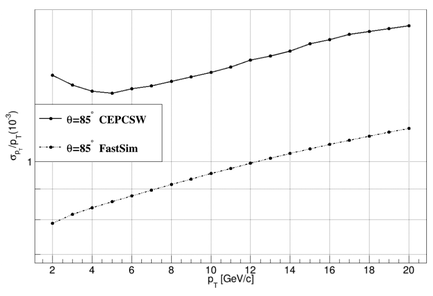
Theta = 12°, Only-ITKE



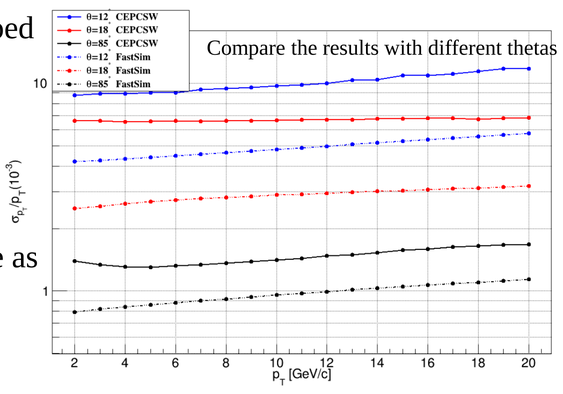
Theta = 18°, ITKE + part TPC



Theta = 85°, ITKB + TPC

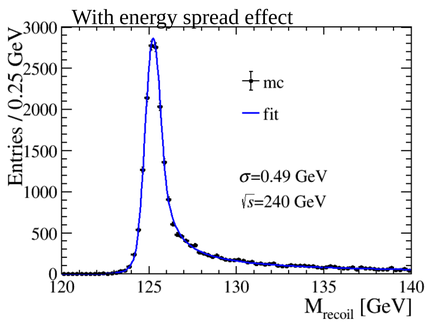


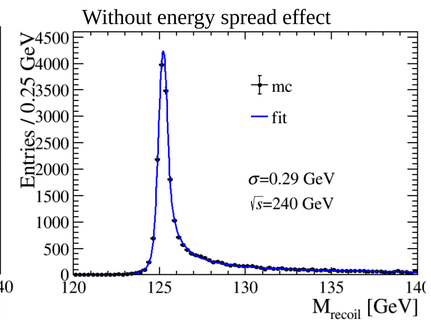
- FastSim : a matlab fast simulation package developed by Wiener group
  - Data provided by Qinglin Geng
  - A reference
- CEPCSW results have the **similar trends** with FatSim
- The pT resolution of full CEPCSW is about twice as bad as FastSim, but still meet CDR requirements
- Need further study: a strange lift at the low momentum end of full simulation

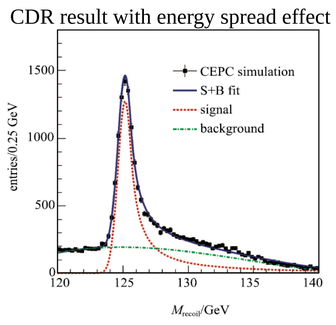


4. Recoiled Higgs reconstruction

- A validation of physics performance
  - Physics progress: e+e- -> ZH (μμγγ) with √s = 240 GeV
  - 30k events applied selection: nTrks == 2
  - Take the **energy spread** into considering, = 0.17% provided by accelerator TDR
    - Assume the beam energy is 120 GeV (same for e+ and e-), use the toyMC to sample with gauss shape
- Preliminary results



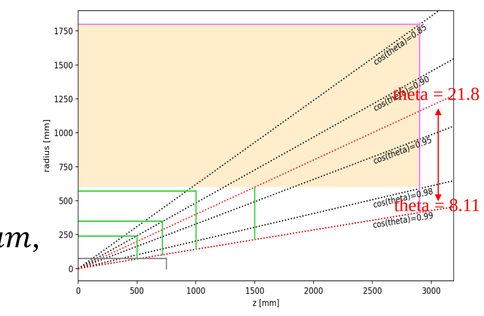




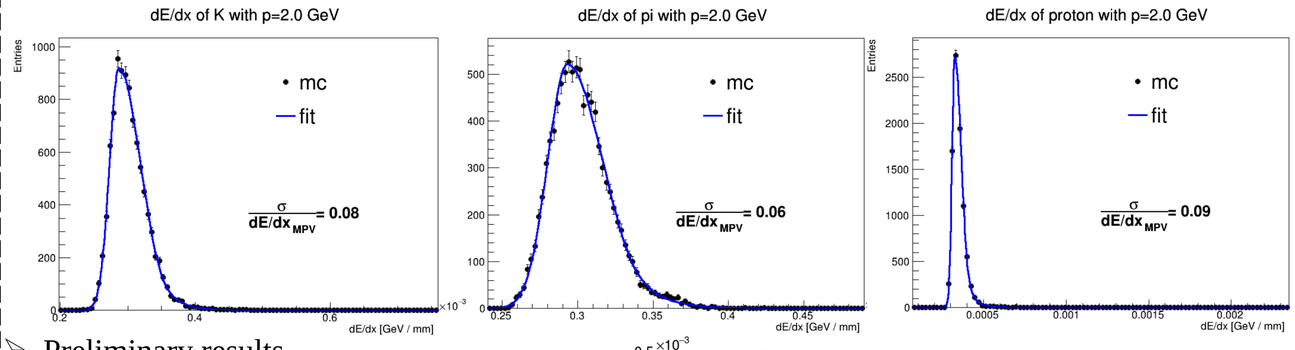
- The Higgs mass resolution: **0.39%** and **0.23%**
- The right tail caused by energy loss & beamstrahlung
- Has a **similar shape** with the previous CDR result

5. PID capacity of ITK endcap

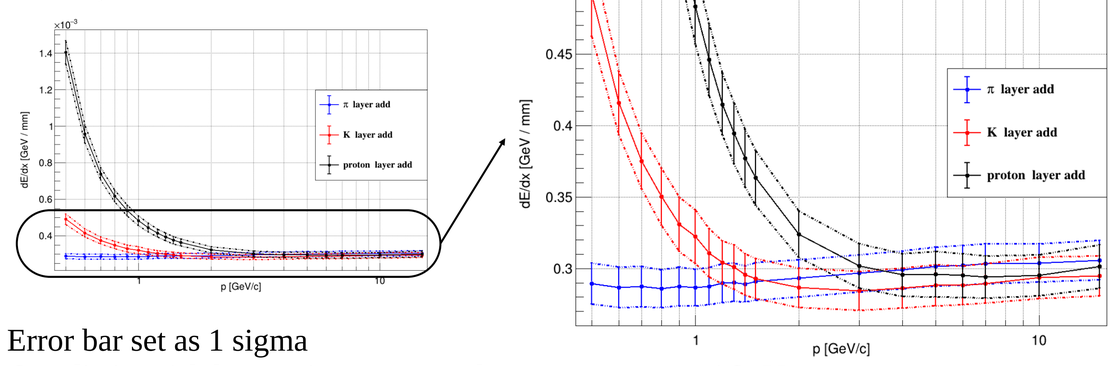
- Setting
  - 4 **double-layers** ITKE, **300μm** silicon per layer
  - Particles: e-, mu-, pi-, K-, proton, but not show e-, mu- results here
  - Momentum: 19 points in 0.5 - 15 GeV
  - Theta: 8.11° - 21.8°, to make sure only ITKE hit
  - 10k events to get Most Probable Values of $\sum \frac{dE}{dx}/hits\_num$, **removed the outlier** for every track



- Fitting
  - dE/dx distribution fitted by crystal ball PDF, examples @ p = 2 GeV



- Preliminary results

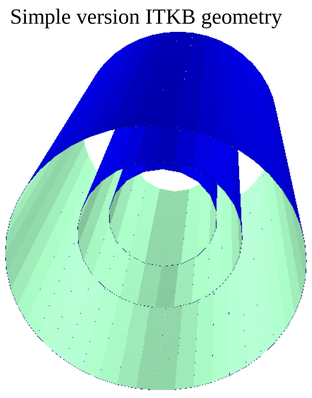


- Error bar set as 1 sigma
- Can distinguish kaon, pion, proton when momentum < 1GeV
- No distinguishing power for any particles with p > 2 GeV

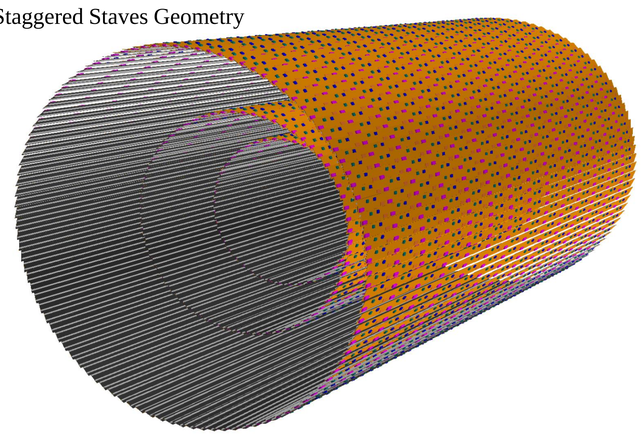
6. Staggered Staves Geometry Construction for CEPCSW

- Geometry of ITK Barrel
  - Need a finer geometry to get more precise simulation results
  - Based on the HVCOMS pixel design of ITKB, recreate with DD4hep

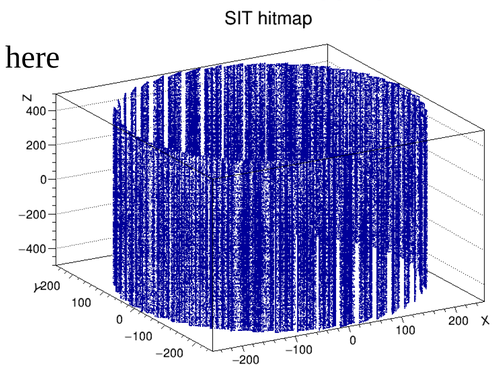
Simple version ITKB geometry

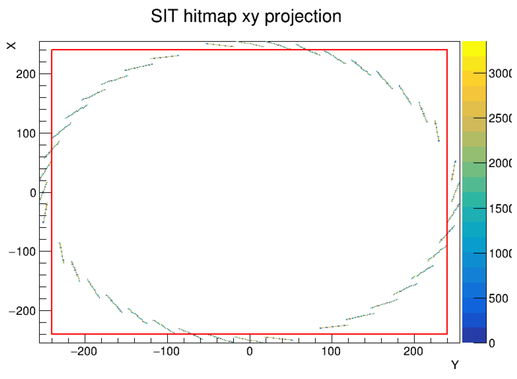


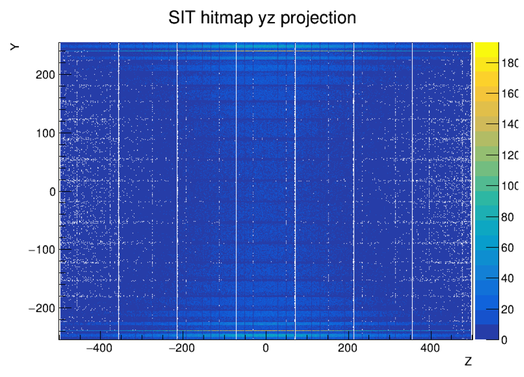
Staggered Staves Geometry



- 3 layers structure
  - With slices: Support + Ti tube + Flex + DCDC + Data link + Data aggregation + Optical connector
  - The sensor is under the flex but not visible here
- A very preliminary hitmap study
  - Using ~4M muon events only in 50GeV
  - Only hitmap of 1st layer showed here
  - Set offset for every stave to avoid overlap
  - The white lines in yz projection are gaps between silicon modules

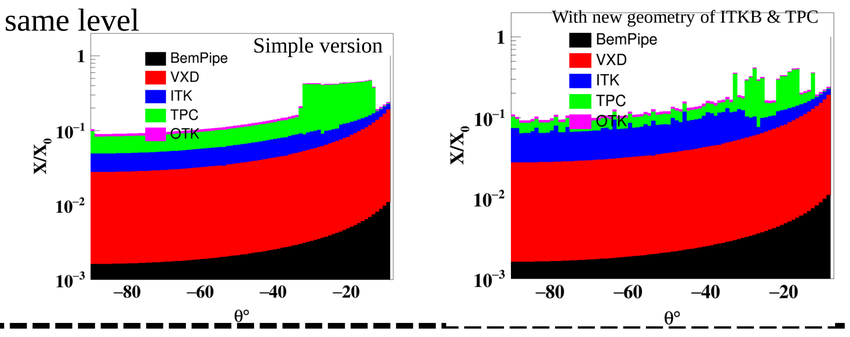






7. Material budget study

- New geometry of ITKB & TPC implemented in CEPCSW
- Compare the material budget with the simple version geometry
  - At the same level



8. Summary

- A series of simulation-related work has been performed for the latest CEPC ITK layout
  - Validate the tracker system's momentum resolution capability
  - Validate its physics performance of Higgs reconstruction
  - Check the PID capacity of ITK endcap
  - Create staggered staves geometry of ITKB
  - Calculate the material budget of tracking system

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Simulation result of CEPC OTK with CEPCSW

Dian Yu, on behalf of the ToF team

The 2024 international workshop on the high energy Circular Electron Positron Collider

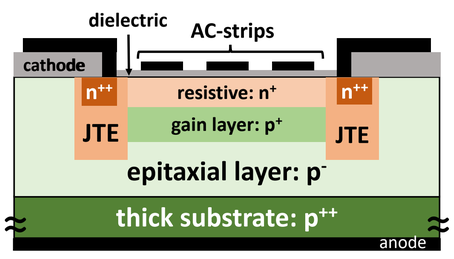
TSUNG-DAO LEE INSTITUTE

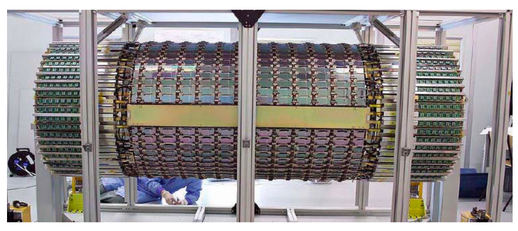
Physics Motivation

Event Disentangling ToF offers precise timing information to precisely distinguish k/p and k/pi in 0.5~2GeV and for more than 1.5GeV, respectively. The spatial and time resolution are nedded to reach 10μm and 30ps.

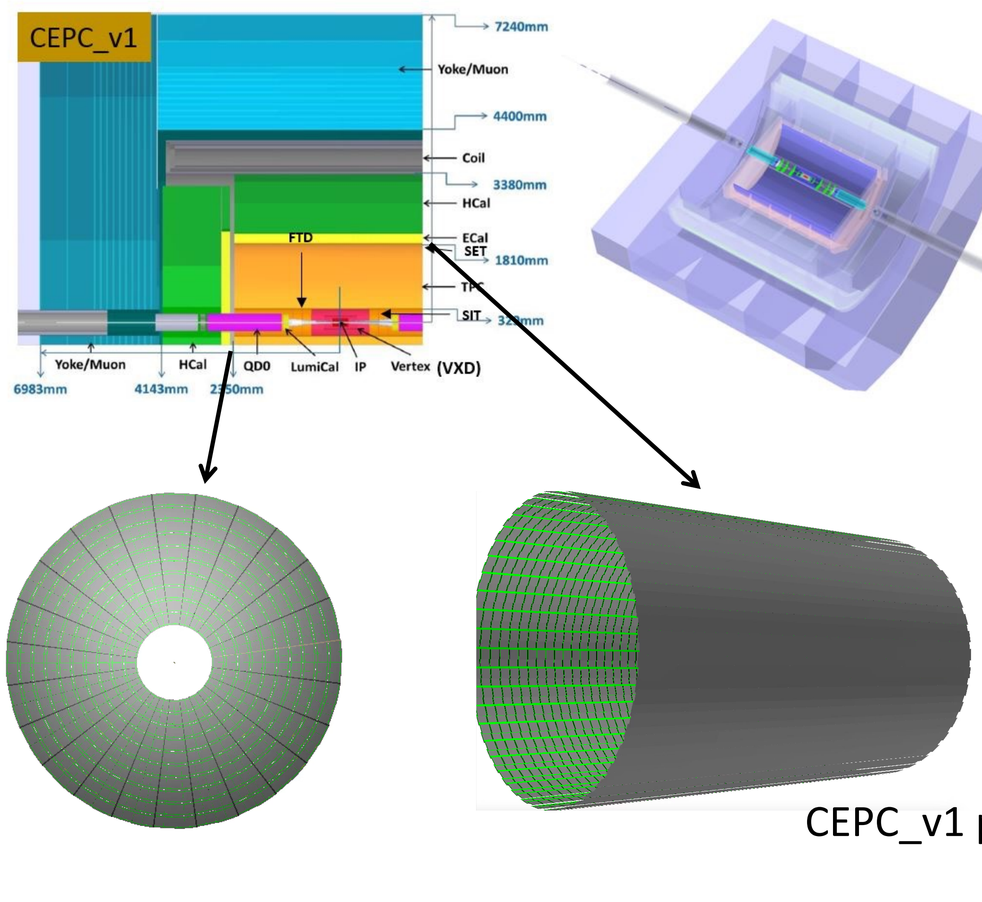
Detector

AC-LGAD (AC-coupled Low Gain Avalanche Detector) are mature detecors widly used like in ATLAS experiment, typically achieving fields of several hundred kV/cm in the gain layer. The spatial resolution can reach up to 10μm and resolution often less than 30 ps, making AC-LGADs crucial for applications like 4D particle tracking in future collider experiments.



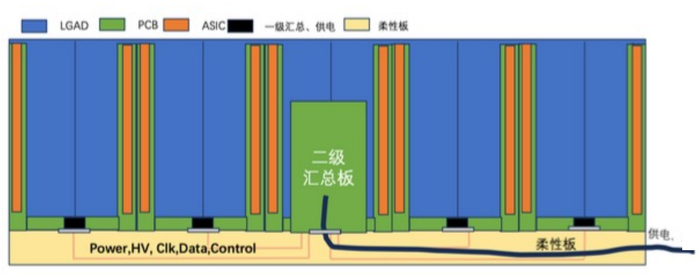


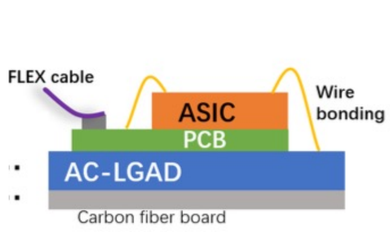
Geometric The AC-LGAD-based ToF and outer tracker will be positioned between the TPC and ECAL, covering an area of 90 m² with inner radius 400mm, outer radius 1800mm and length 5860mm.

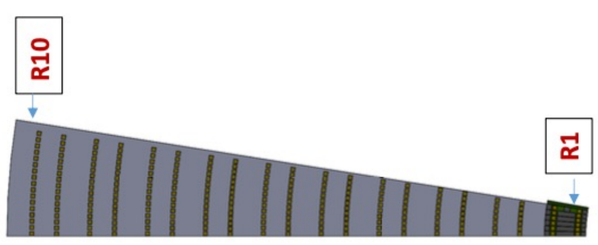


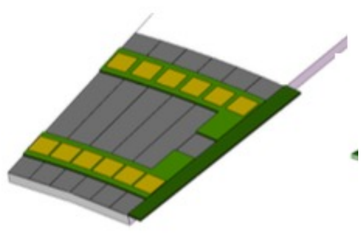
CEPC_v1 patch

Sub-structure The sub-structure consists of support, sensor, pcb boards, asic chips and electronics integration together with wires.





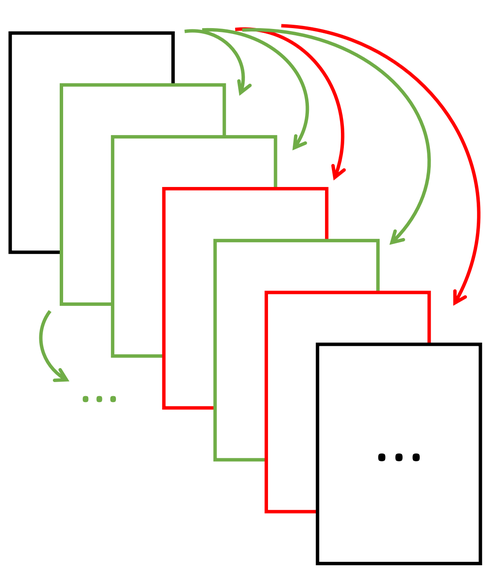


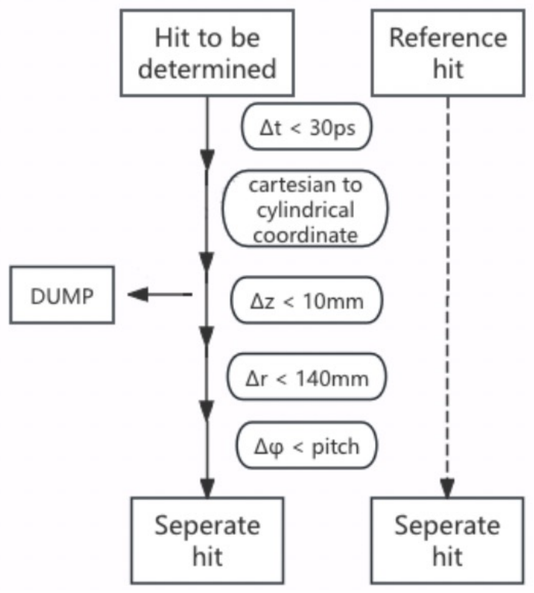


Simulation

CEPCSW The geometry design of OTK is added to /Detector/DetCRD/compact/CRD_common_v01/ and simulation truth details will be saved into OTKBarrelCollection and OTKEndcapCollection.

Hit Rate Utilizing new geomerty in CEPCSW, 10000 and 2000 hits are simulated for Higgs and Zpole background, respectively. Priliminary results are given with truth information with a algorithm as follows. Further developing in adding detailing structure to the detectors in the future will give out more precise result.

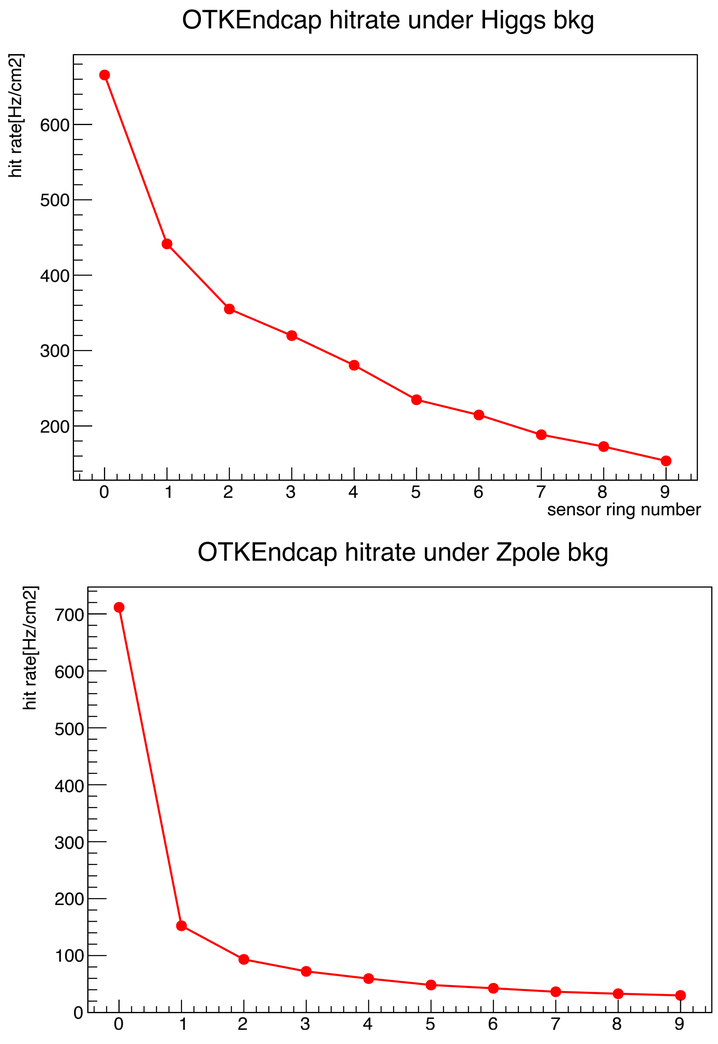




Results

Higgs By calculation, higgs bkg has maximum hit rate of 665.6Hz/cm², average hit rate of 253.7Hz/cm². The maximum electronic occupancy is 0.35%.

Zpole This bkg is still under optimization. Maximum hit rate is 711.594kHz/cm² and average 81.131kHz/cm².



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