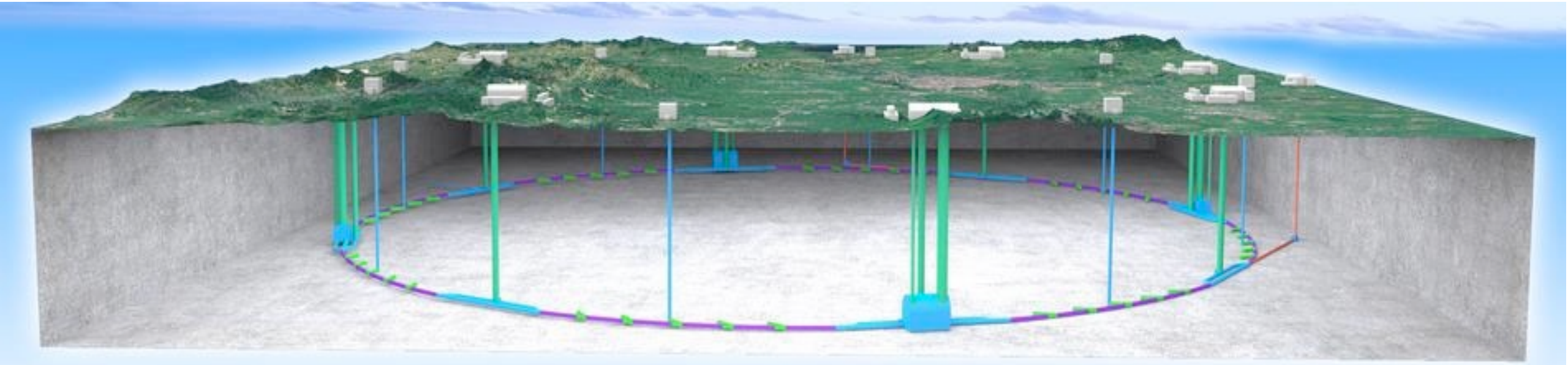
CEPC tracker R & D

Zhijun Liang

(On behalf of the CEPC physics and detector group)

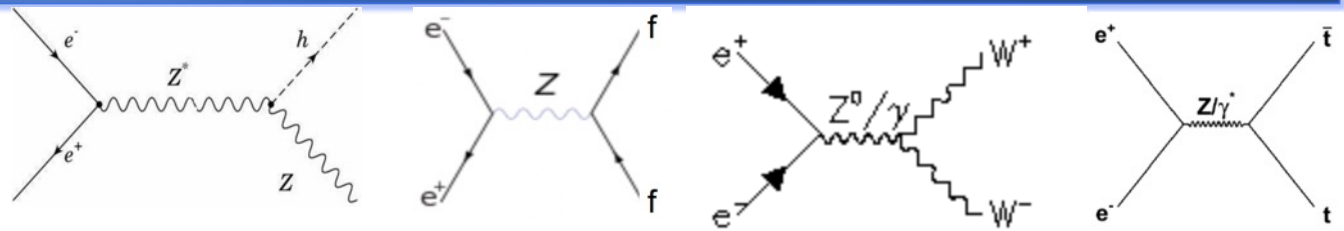
Institute of High energy physics, CAS



CEPC physics program

An extremely versatile machine with a broad spectrum of physics opportunities

→ Far beyond a Higgs factory



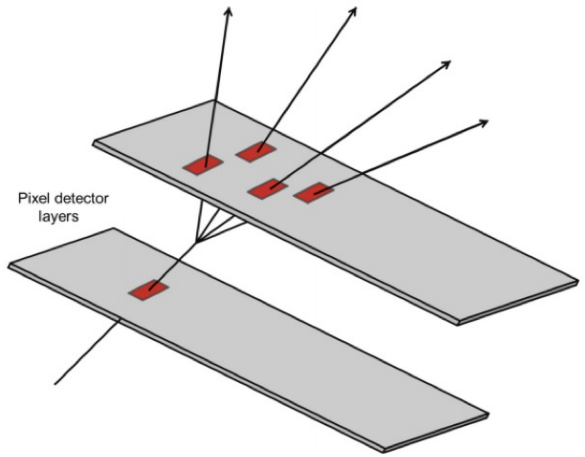
Operation mode		ZH	Z	W^+W^-	$t\bar{t}$
$\sqrt{s}$ [GeV]		~240	~91.2	~160	~360
Run time [years]		10	2	1	5
CDR (30 MW)	L / IP [$\times 10^{34}$ cm^{-2}s^{-1}]	**3**	**32**	**10**	-
	$\int L\,dt$ [ab^{-1}, 2 IPs]	5.6	16	2.6	-
	Event yields [2 IPs]	1×10^6	7×10^{11}	2×10^7	-
Run Time [years]		10	2	1	~5
Latest	**30 MW**	L / IP [$\times 10^{34}$ cm^{-2}s^{-1}]	**5.0**	**115**	**16**	**0.5**
	50 MW	L / IP [$\times 10^{34}$ cm^{-2}s^{-1}]	8.3	191.7	26.6	**0.8**
		$\int L\,dt$ [ab^{-1}, 2 IPs]	20	96	7	1
		Event yields [2 IPs]	4×10^6	4×10^{12}	5×10^7	5×10^5

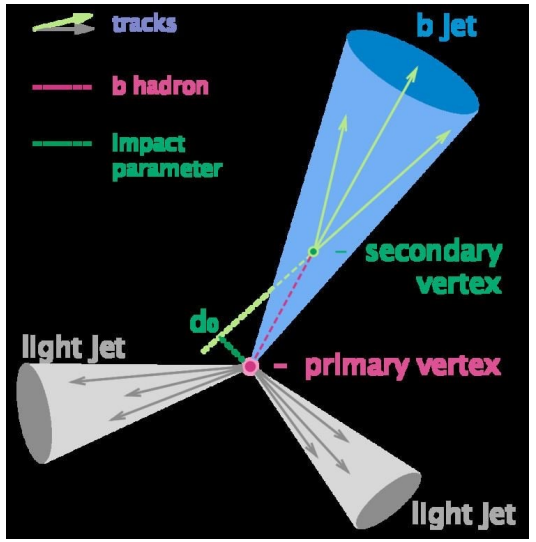
- **Huge measurement potential for precision tests of SM: Higgs, electroweak physics, flavor physics, QCD/Top**
- **Searching for exotic or rare decays of H, Z, B and τ, and new physics**
- **CEPC community joined ECFA Phy focus**
  - **Aiming towards next ESPPU Updates.**

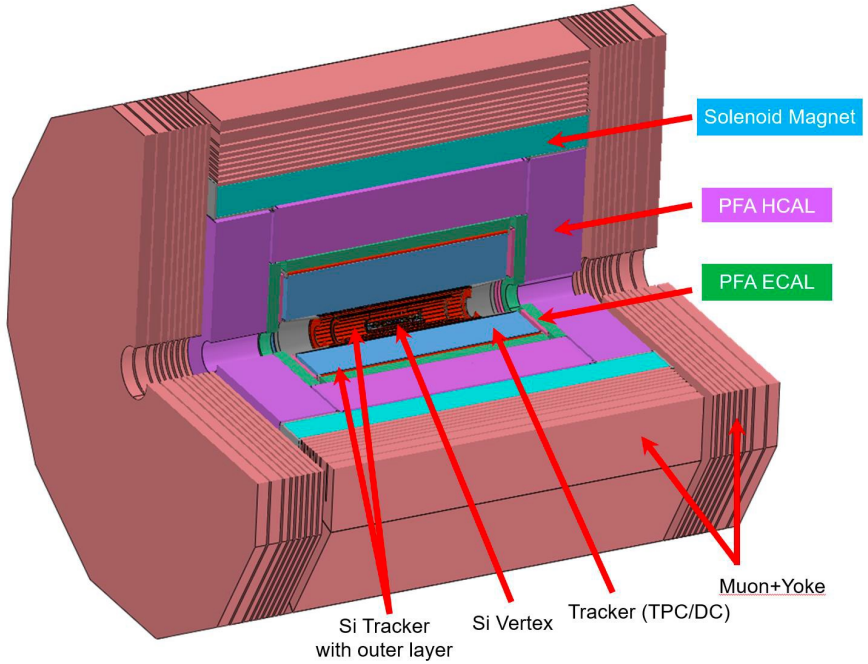
Both 50 MW and $t\bar{t}$ modes are currently considered as CEPC upgrades.

Vertexing and tracking detector and physics case

- **PID capability: 3 sigma K/pi separation power to 20GeV track**
  - TPC (or drift chamber) + Low Gain Avalanche Detector (LGAD) base time of flight detector
- **H→Zγ and H→ZZ∗ or H→Zγ ∗**
  - Key detector issue: Low energy tracks from Z*and γ∗ reconstruction, photon conversion
- **H→bb/cc/gg**
  - Vertexing and impact parameter measurement is the key

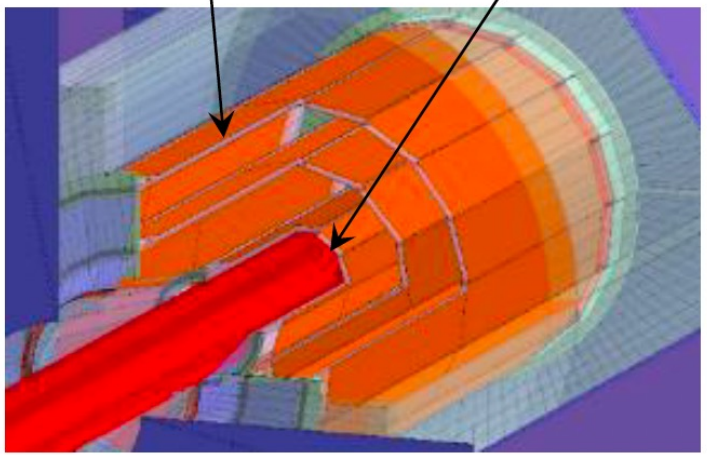






Silicon Pixel Chips for Vertex Detector

2 layers / ladder R_{in}~16 mm



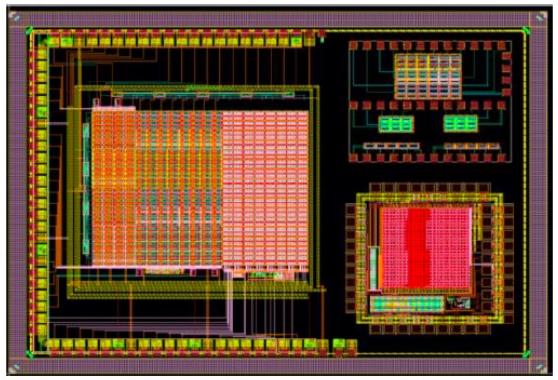
Goal: σ(IP) ~ 5 μm for high P track

CDR design specifications

- **Single point resolution ~ 3μm**
- **Low material (0.15% X_0 / layer)**
- **Low power (< 50 mW/cm²)**
- **Radiation hard (1 Mrad/year)**

Silicon pixel sensor develops in 5 series: JadePix, TaichuPix, CPV, Arcadia, COFFEE

Develop **COFFEE** for a CEPC tracker using SMIC 55nm HV-CMOS process

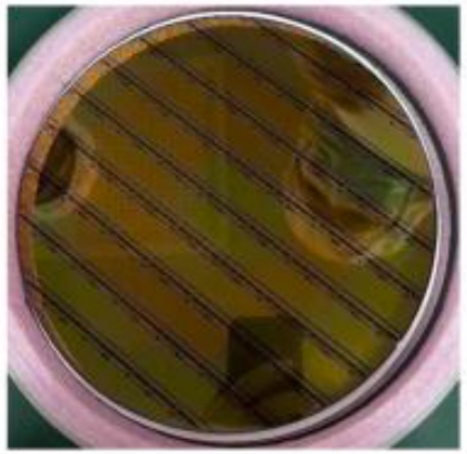


JadePix-3 Pixel size ~16×23 μm²

Tower-Jazz 180nm CiS process
Resolution 5 microns, 53mW/cm²

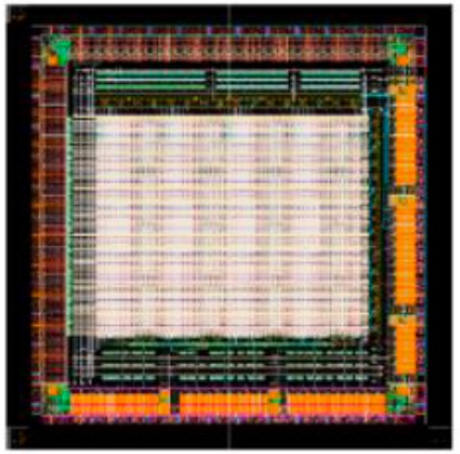
MOST 1

TaichuPix-3, FS 2.5x1.5 cm²
25×25 μm² pixel size

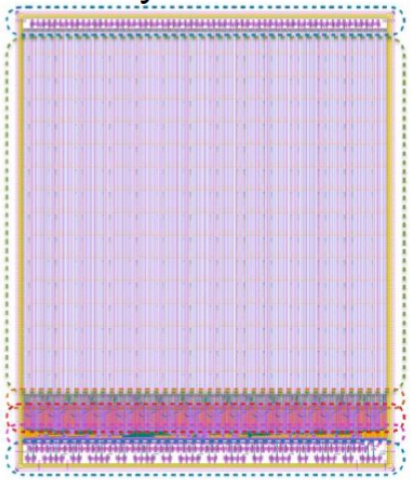


MOST 2

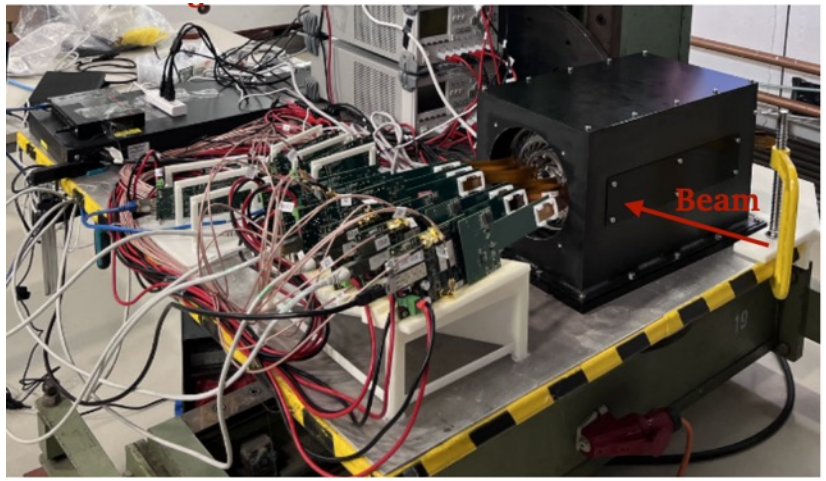
CPV4 (SOI-3D), 64×64 array
~21×17 μm² pixel size

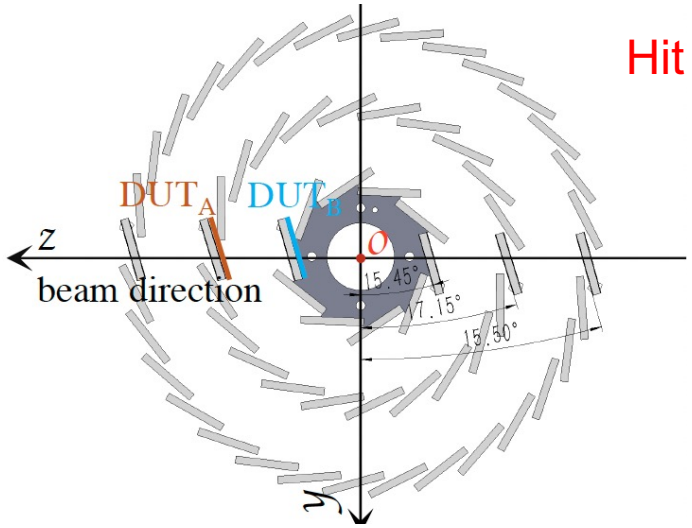


Arcadia by Italian groups for IDEA vertex detector
LFoundry 110 nm CMOS



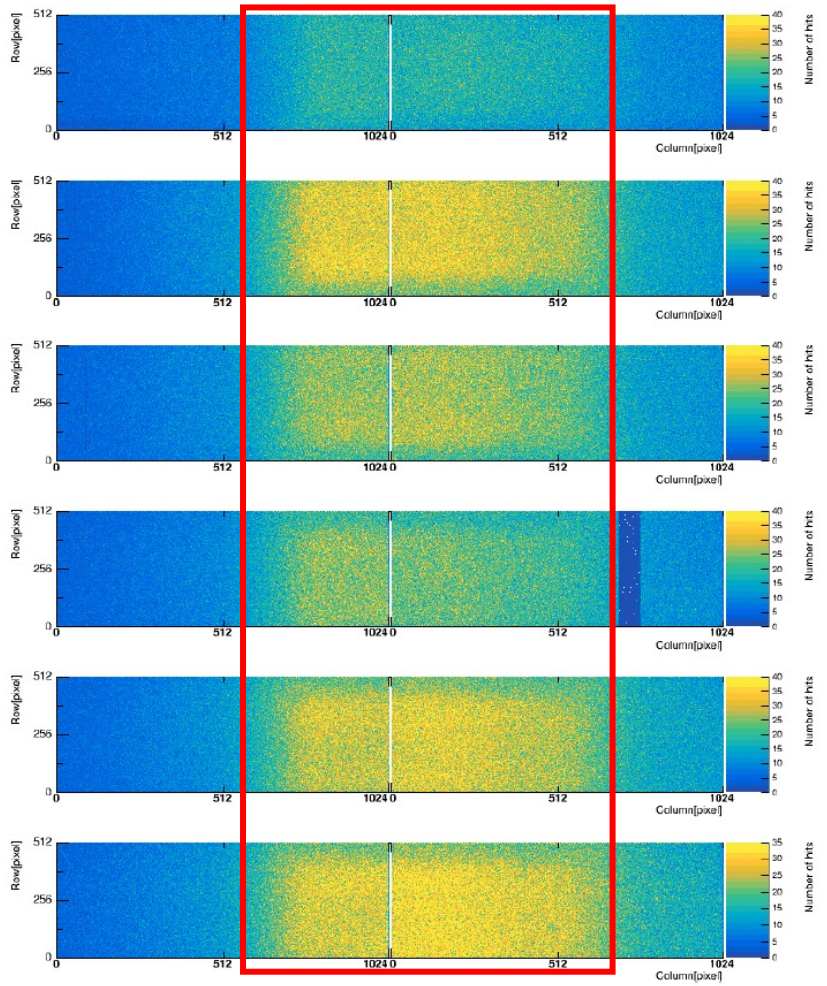
TaichuPix3 vertex detector prototype beam test @ DESY



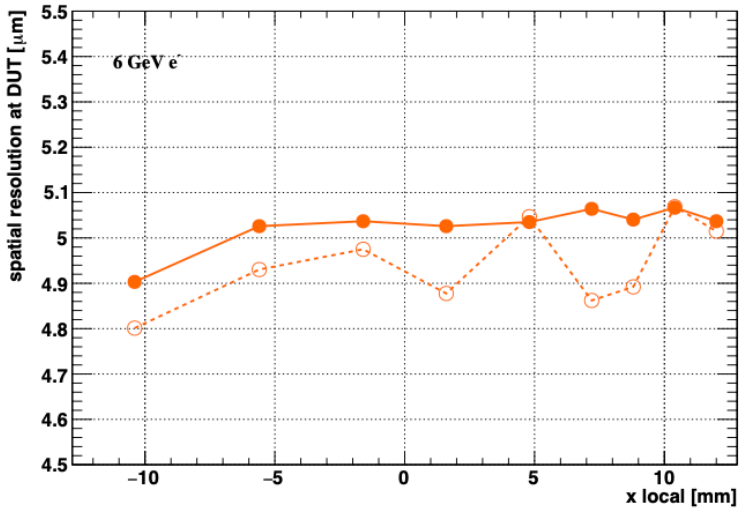


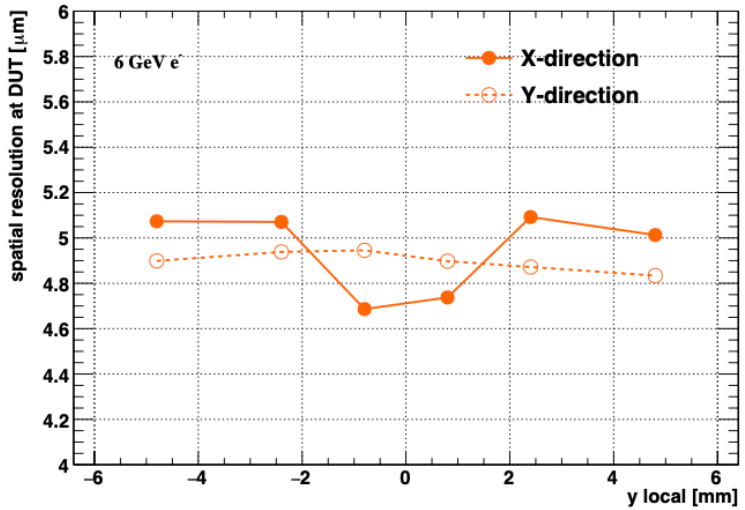
Hit maps of multiple layers of vertex detector

Beam spot



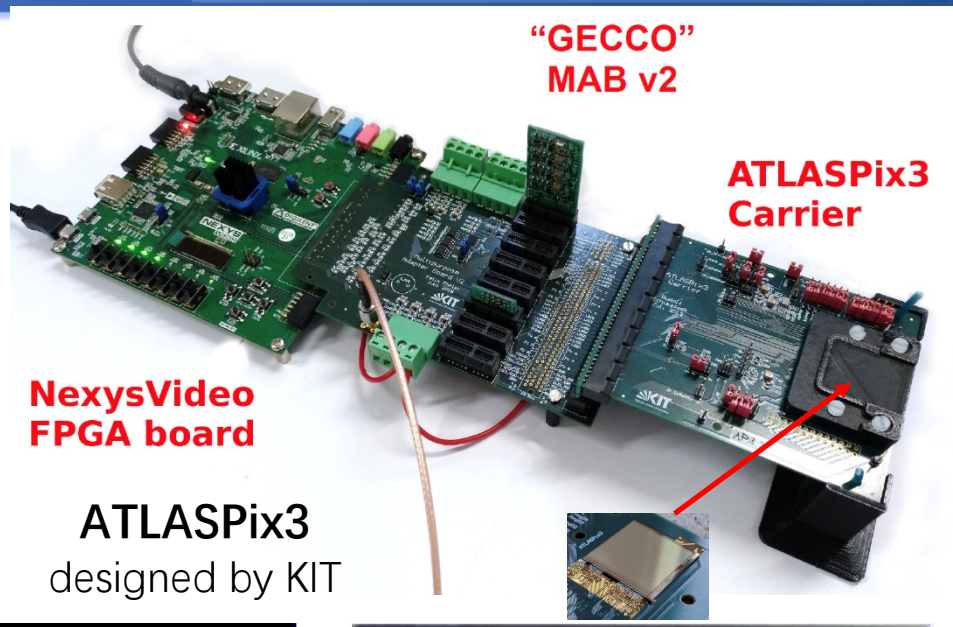
Spatial resolution ~ **5 μm**

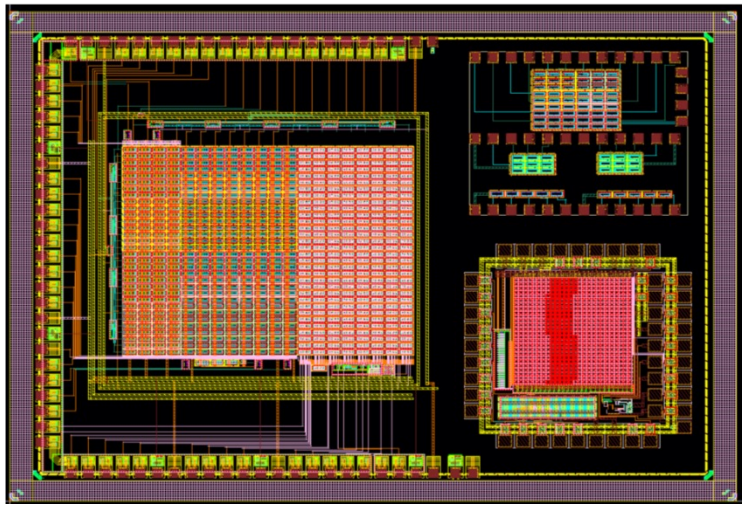




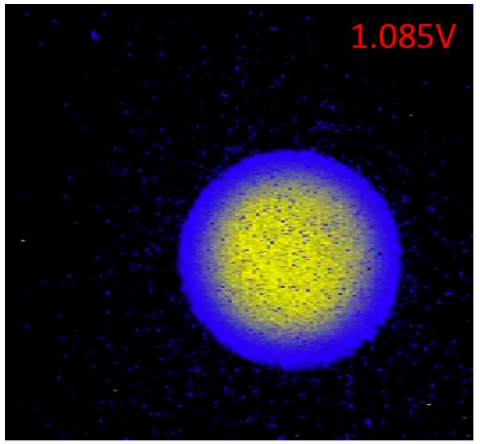
Silicon Tracker using HV-CMOS: ATLASPix → CEPCPix

- Large area: **~70 m²** in TPC+SiTrk ➔ Cost effectiveness
- Focus on MAPS pixel tracker, also started SSD for outer layers
- Joint efforts on an ATLASPix3 based demonstrator
- ATLASPix & MightyPix use TSI 180nm HV process
- Exploring SMIC 55 nm HV HR proces
  - ➔ Smaller feature size & alternative foundry
- Other possibilities, e.g. MALTA3, TPSCo-65nm

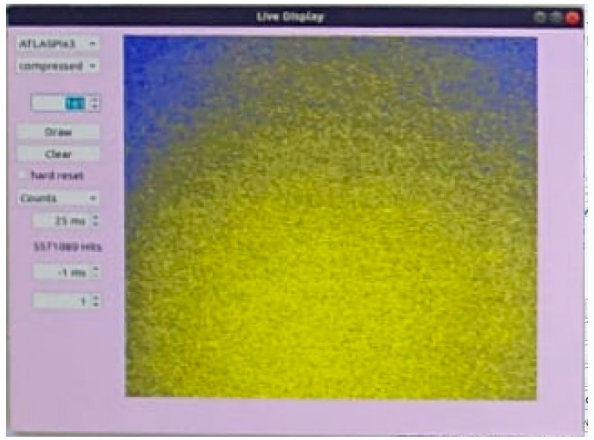




The 2nd design for SMIC 55nm HV HR process



Hitmap with Fe55 source



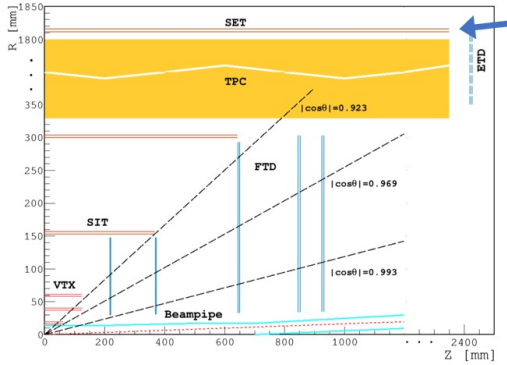
Hitmap with electron beam

Collaboration with UK/Germany/Italy colleague

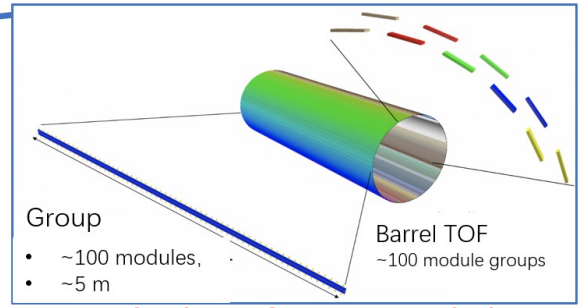
Time of flight detector

- **A new type of TOF detector for CEPC is under R & D**
  - Based on Low Gain Avalanche Detector (LGAD) technology
  - Synergy with ATLAS high granularity timing detector
  - Aim to have good time and spatial resolution(50ps and 10um)

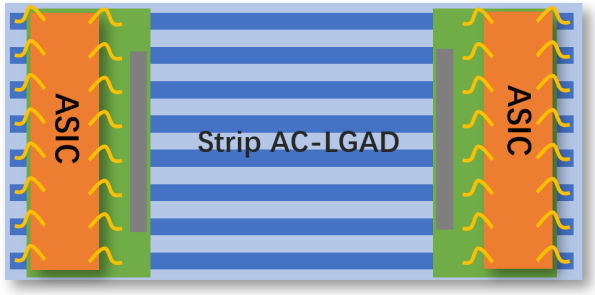
Baseline detector concept in CDR



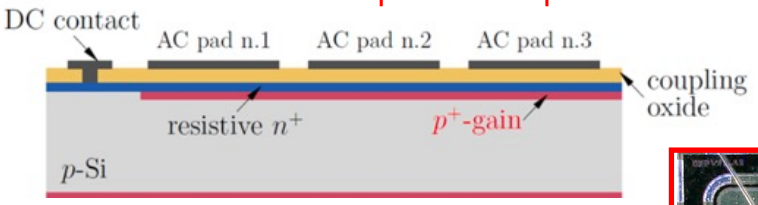
LGAD timing detector in Barrel region

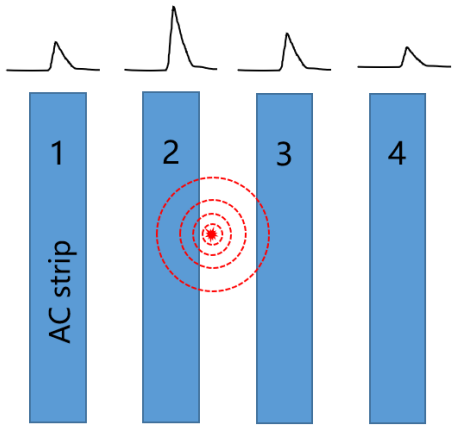


Strip LGAD module

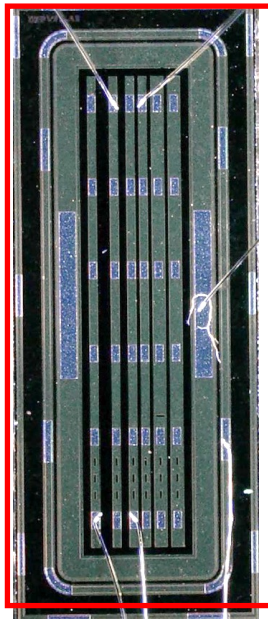


AC-coupled strip LGAD

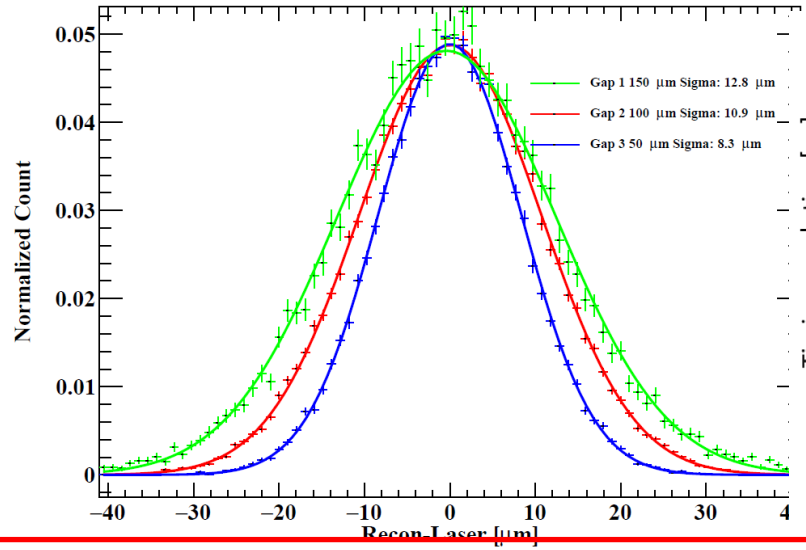




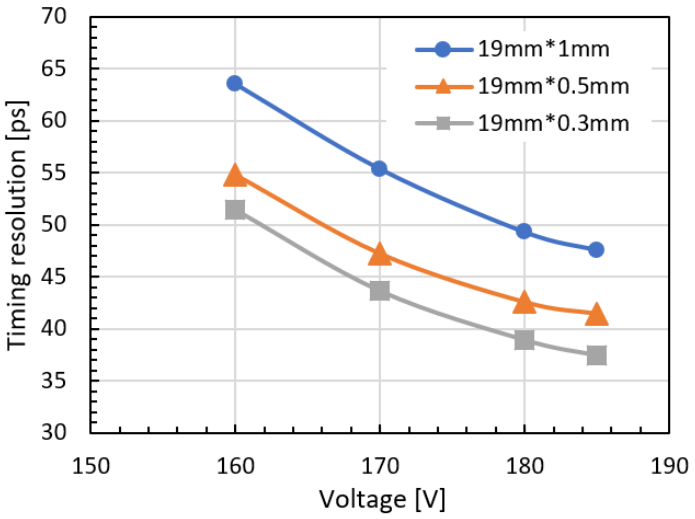
LGAD based strip silicon sensor prototype by IHEP



Spatial resolution (~10um)



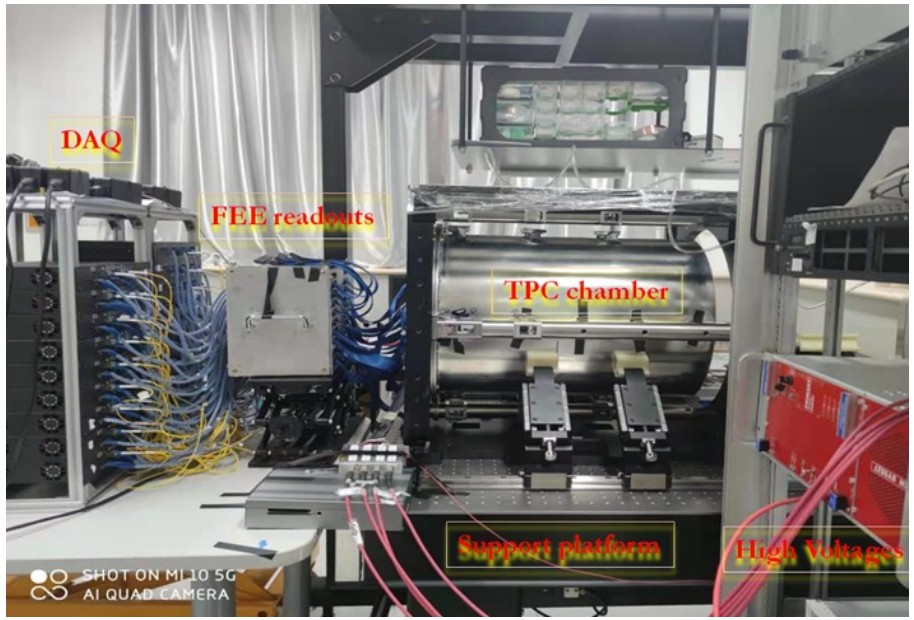
Time resolution (30-50ps)

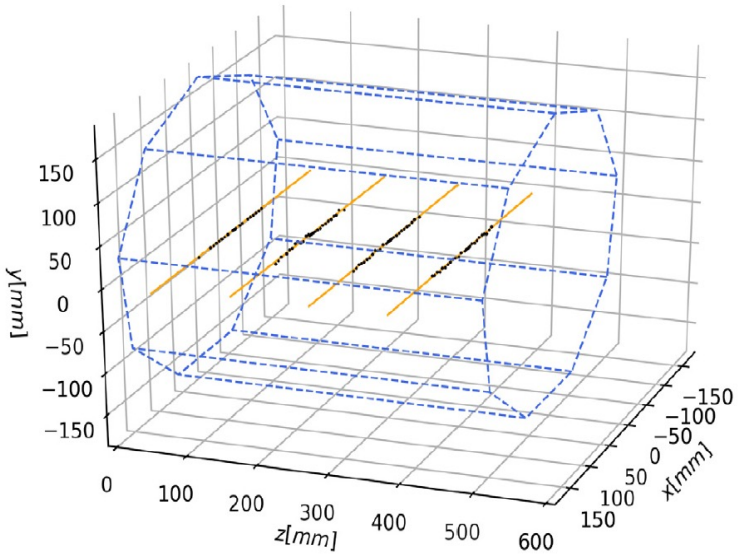


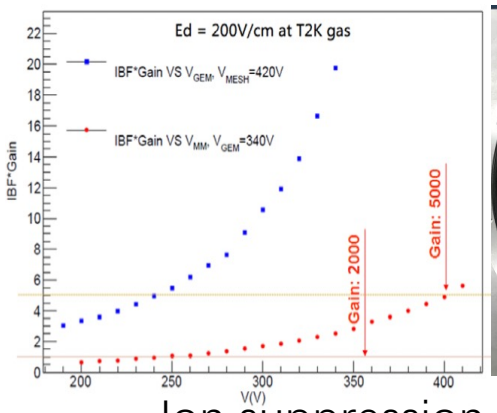
Roadmap of CEPC TPC detector R&D

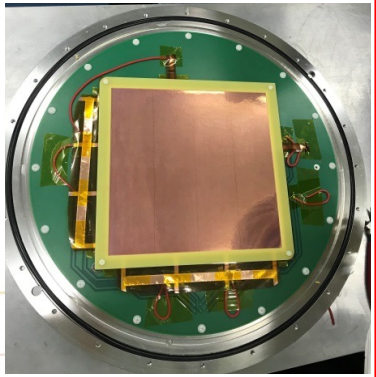
- **CEPC TPC detector prototyping roadmap:**
  - From TPC module to TPC prototype R&D for Higgs and Tera-Z
  - Easy-to-install modular design of **Pixelated readout TPC for CEPC TDR**
- **Achievement by far:**
  - Supression ions hybrid GEM+Micromegas module
    - IBF×Gain **~1 @ G=2000** validation with hybrid TPC module
  - Spatial resolution of **$\sigma_{r\varphi}$≤100 μm** and dE/dx resolution of 3.6%
  - FEE chip: reach **~3.0mW/ch** with ADC and the pixelated readout R&D

TPC prototype with integrated 266nm UV laser



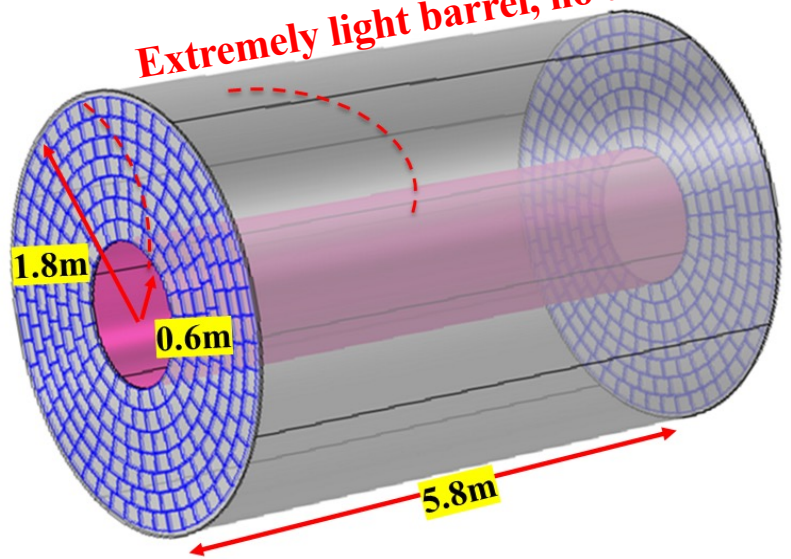






Ion suppression TPC module R&D

Extremely light barrel, no tension

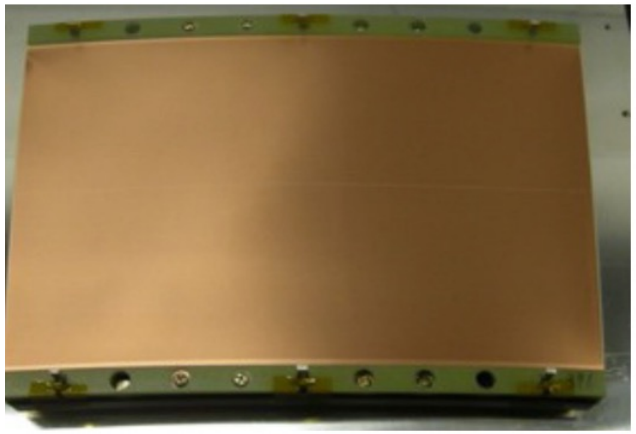


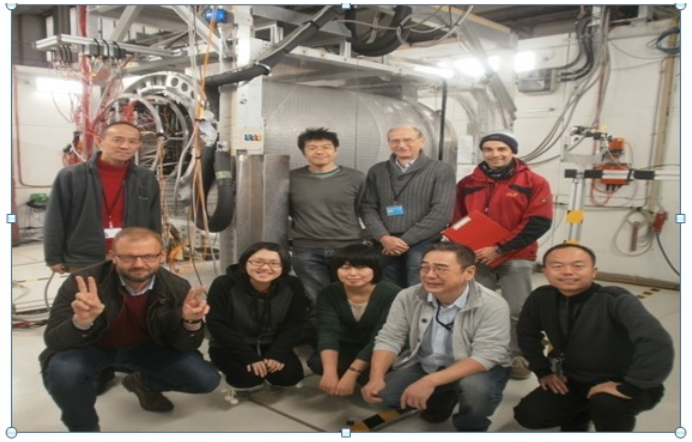
TPC for CEPC reference TDR

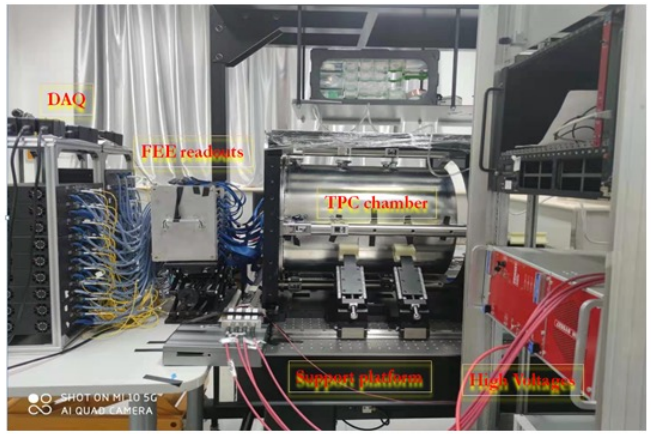
Activity international collaboration - TPC technology R&D

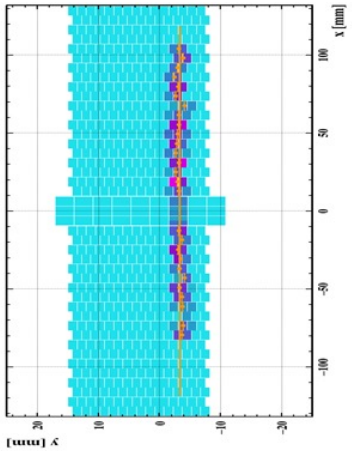
- Activity collaboration: Pixelated readout and Pad readout from IHEP and LCTPC collaboration
  - Large Prototype setup have been built to compare different detector readouts for Tera-Z
  - PCMAG: B < 1.0T, bore Ø: 85cm, Spatial resolution of $\sigma_{r\phi} \leq 100$ μm
  - Collaboration implement improvements in **a pixelated readout TPC for CEPC TDR**

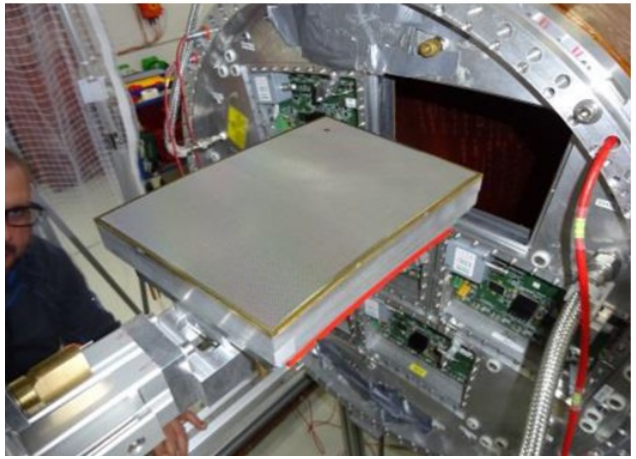
ArXiv. (2023)2006.08562
NIM A (2022) 167241
ArXiv (2022)2006.085
JINST 16 (2021) P10023
JINST 5 (2010) P10011
NIM A608 (2009) 390-396

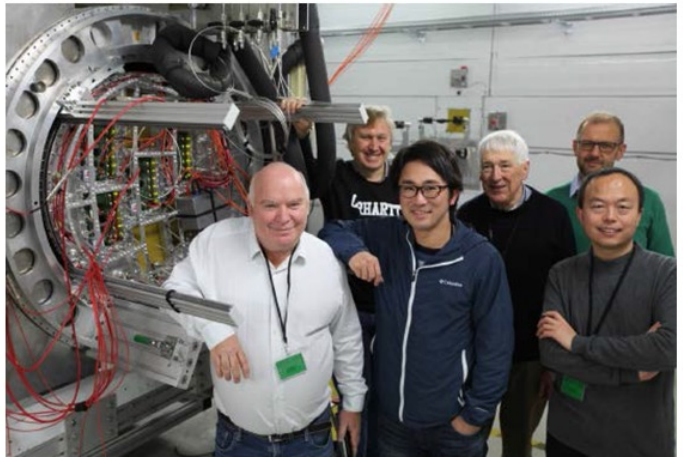


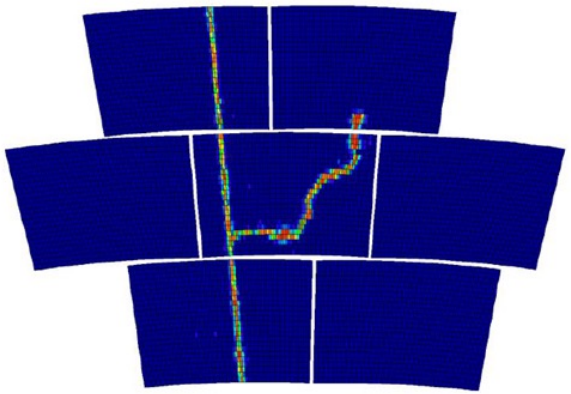




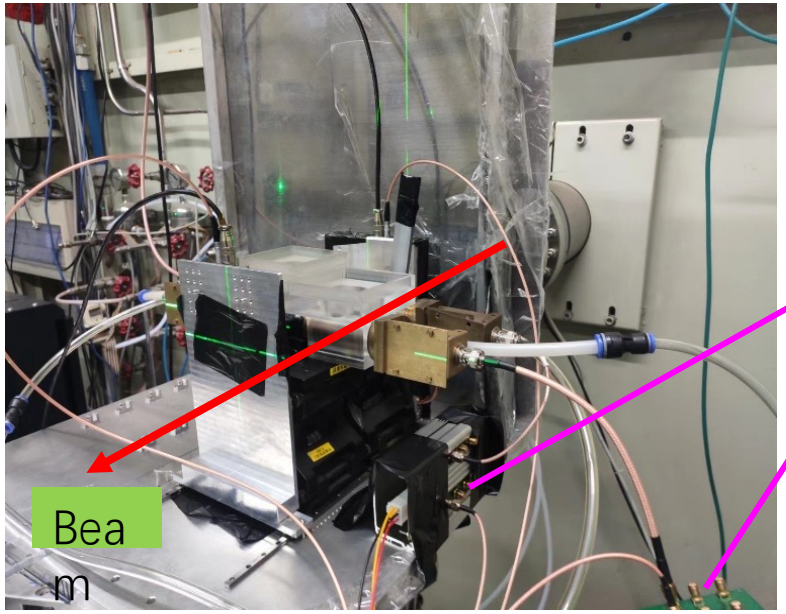


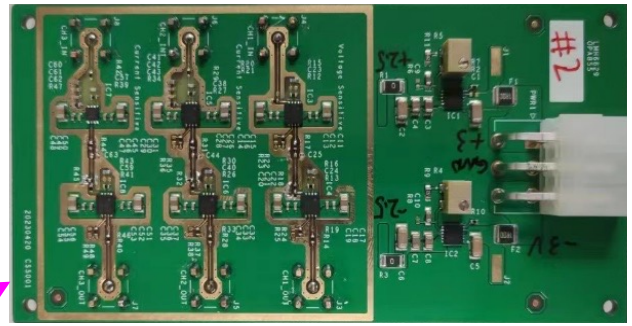


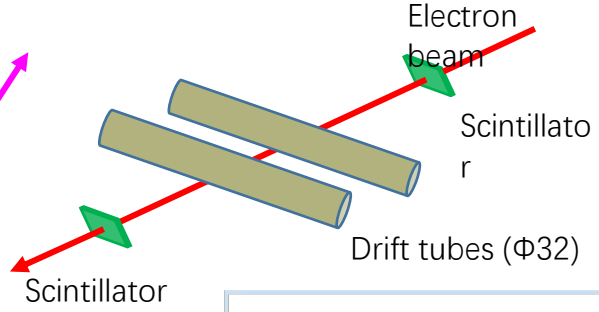


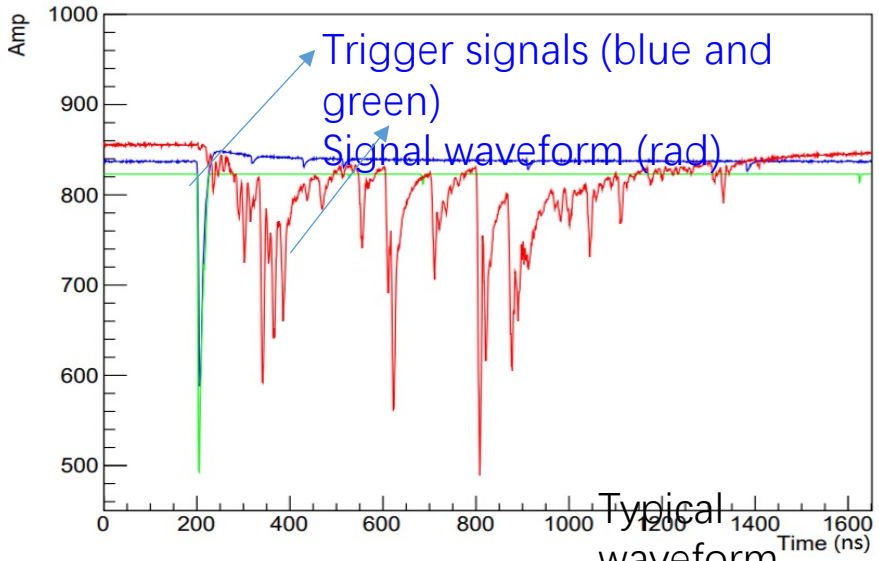


Drift chamber R&D and beam test



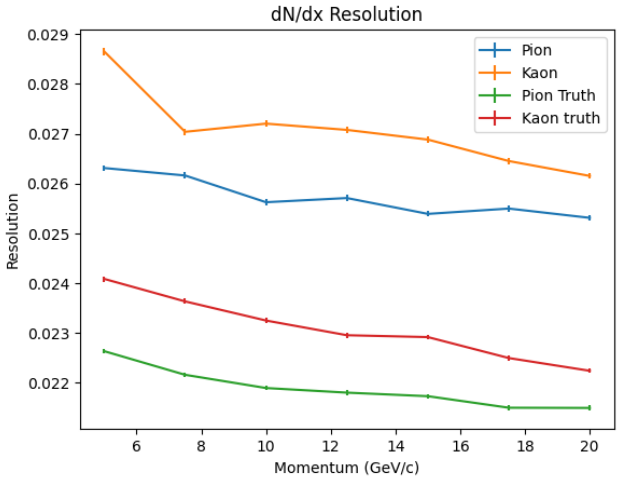




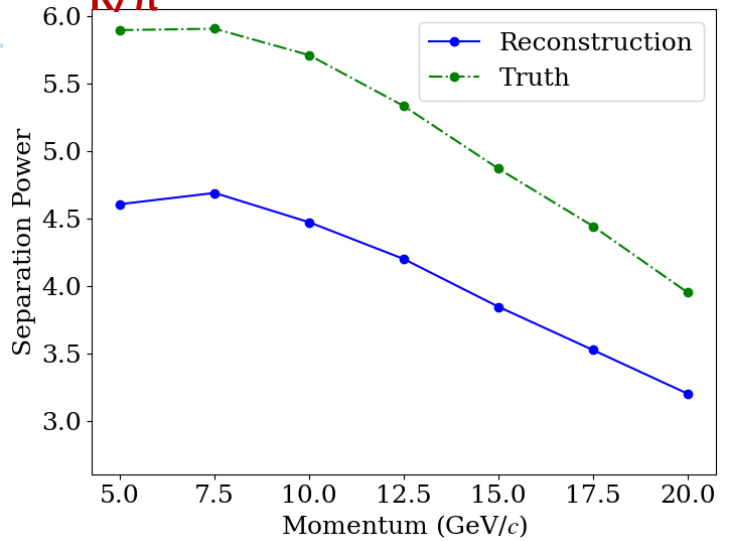


- Two drift tubes + preamps + ADC (1GHz)
- Two scintillators provide trigger signals
- Tested with electron beam at IHEP
- Clear peaks, low noise, ~ ns rise time

dN/dx resolution: ~2.5% for pion



Separation: 3.2σ for 20 GeV/c K/π



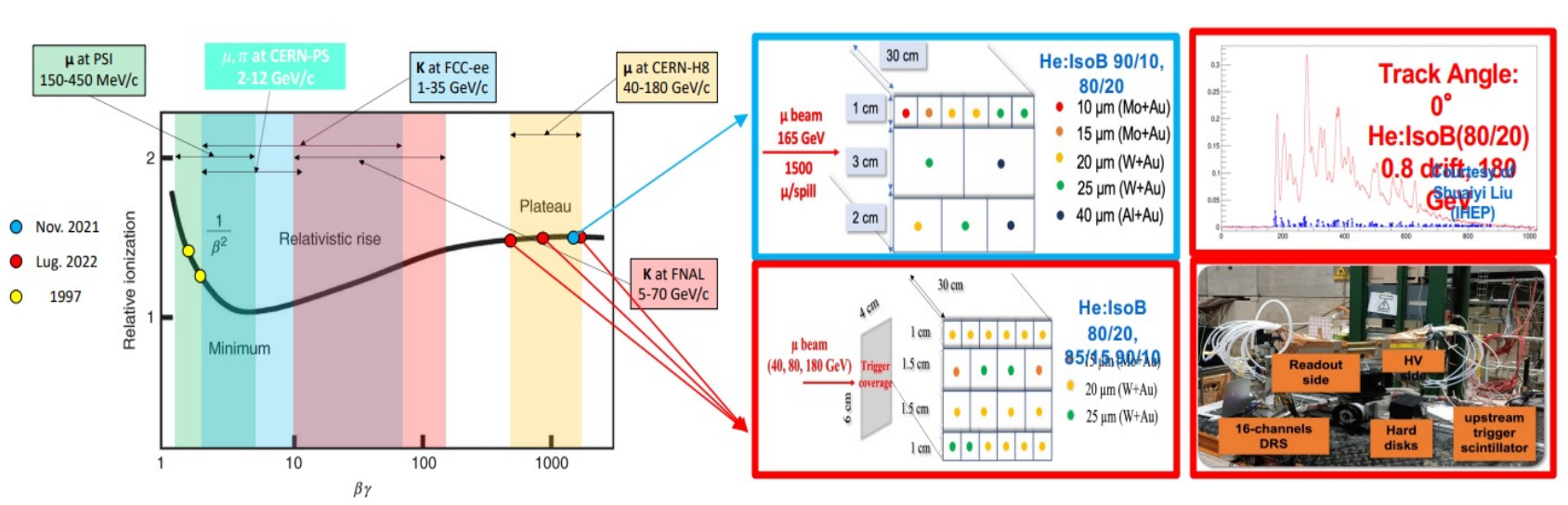
Drift chamber R&D, Synergy with IDEA

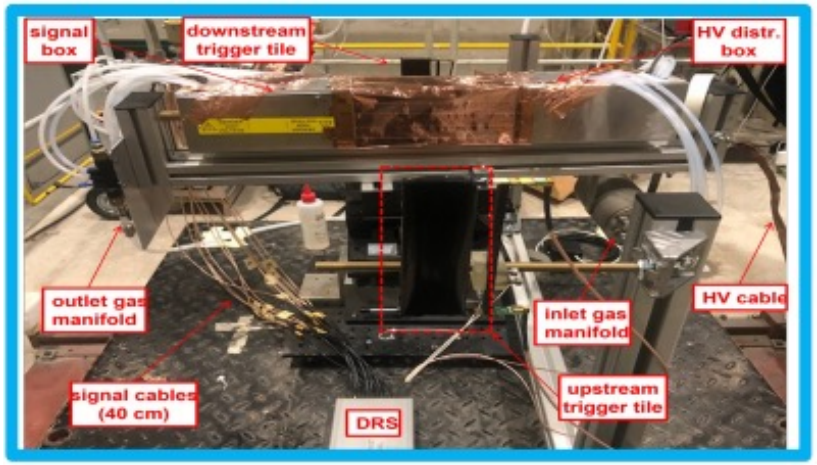
❖ Beam tests organized by INFN group:

- Two muon beam tests performed at CERN-H8 ($\beta\gamma > 400$) in Nov. 2021 and July 2022
- A muon beam test (from 4 to 12 GeV/c) in 2023 performed at CERN
- Ultimate test at FNAL-MT6 in 2024 with π and K (By = 10-140) to fully exploit the relativistic rise.

❖ Contributions from IHEP group:

- Participate data taking and collaboratively analyze the test beam data
- Develop the machine learning reconstruction algorithm



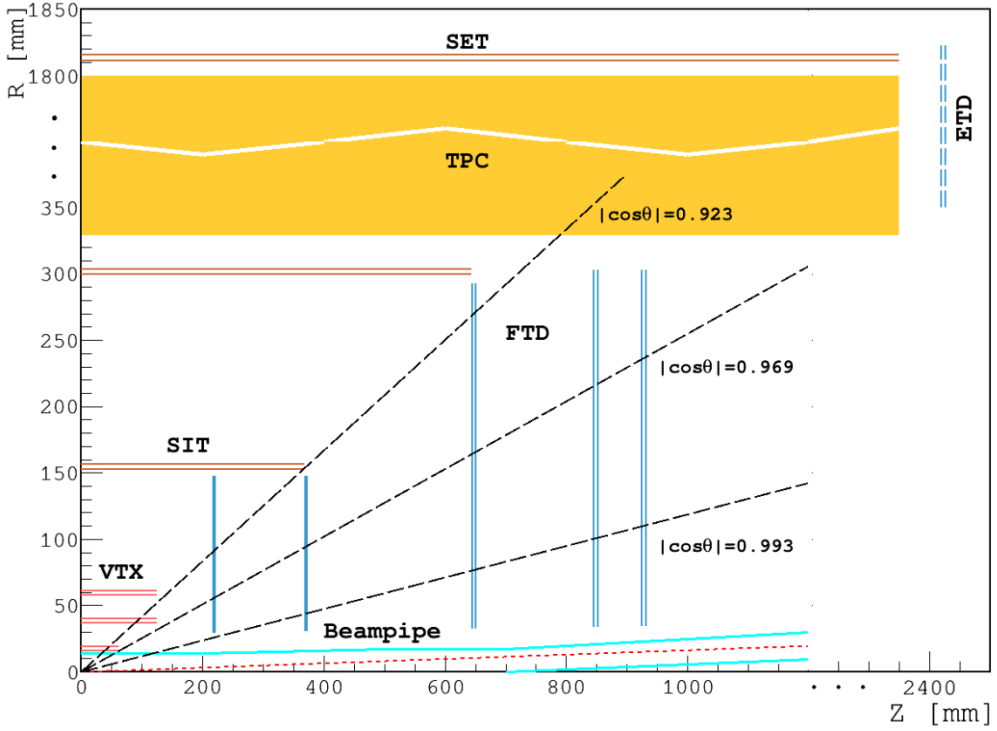


Summary

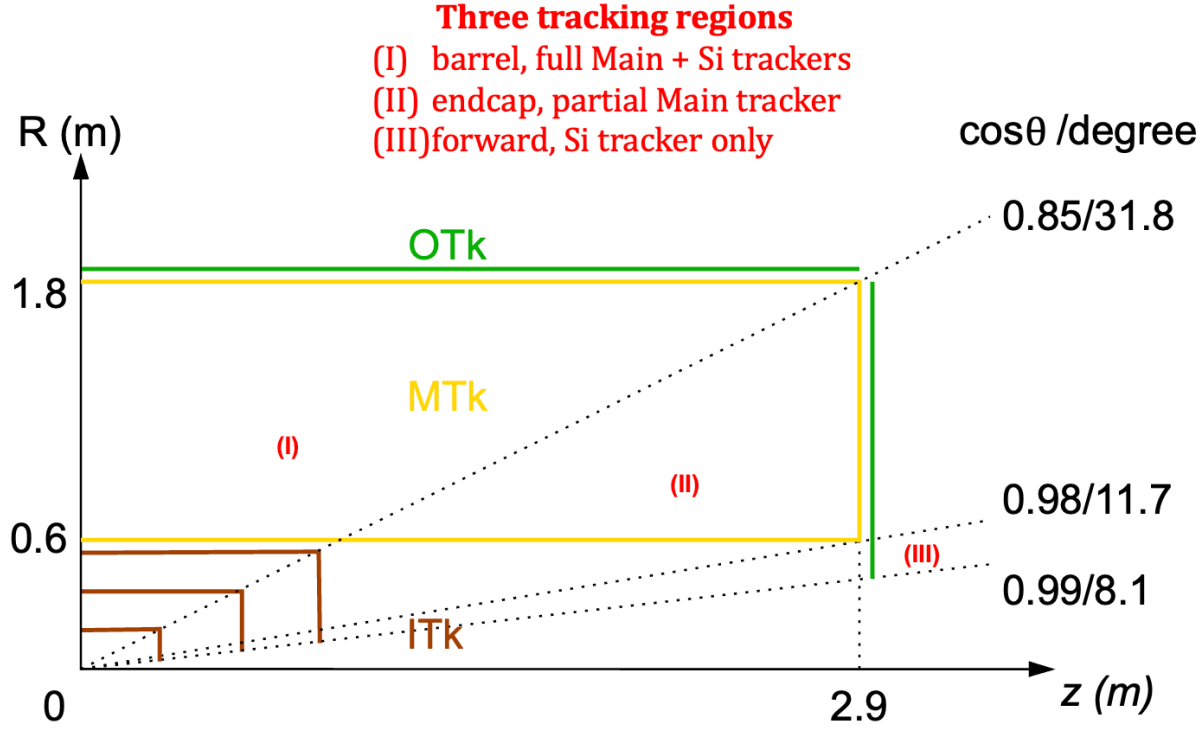
❖**Tracker key technology R & D and tracker optimization is on-going**

❖**PID system optimization and R & D**

CEPC Conceptual design report



Tracker optimization on-going toward reference TDR

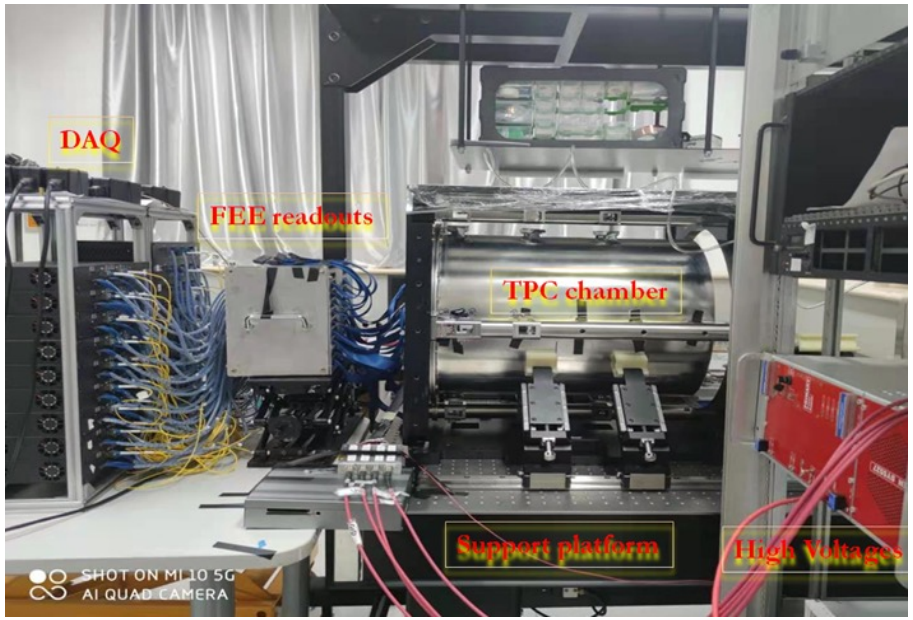


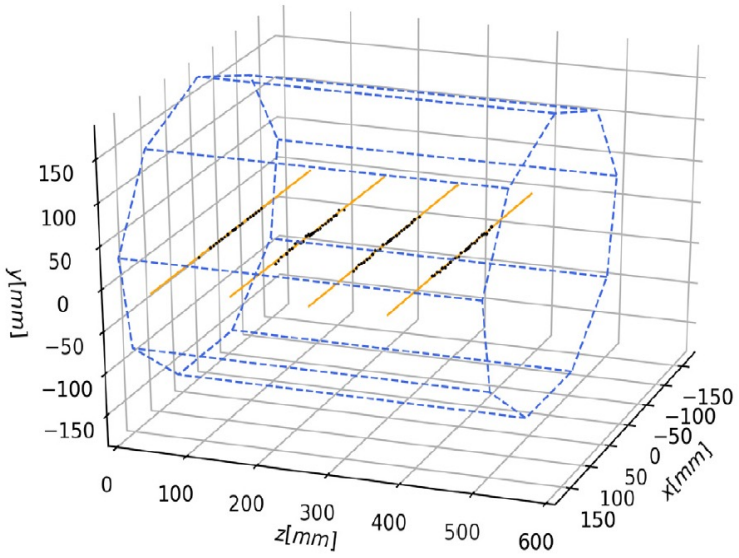
backup

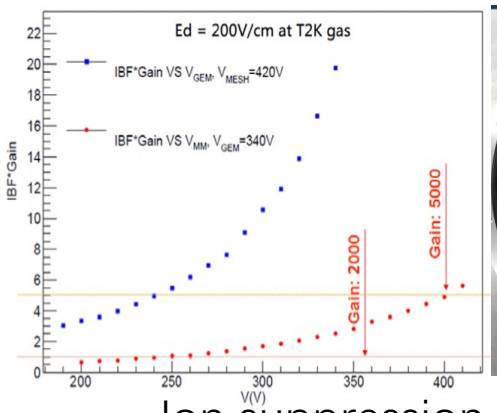
Roadmap of CEPC TPC detector R&D

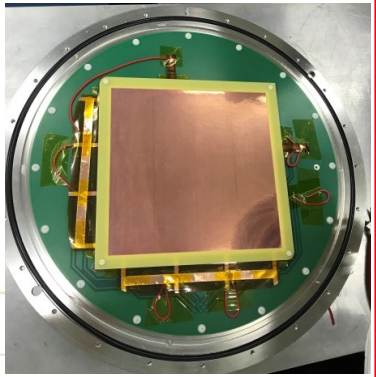
- **CEPC TPC detector prototyping roadmap:**
  - From TPC module to TPC prototype R&D for Higgs and Tera-Z
  - Easy-to-install modular design of **Pixelated readout TPC for CEPC TDR**
- **Achievement by far:**
  - Supression ions hybrid GEM+Micromegas module
    - IBF×Gain **~1 @ G=2000** validation with hybrid TPC module
  - Spatial resolution of **$\sigma_{r\varphi}$≤100 μm** and dE/dx resolution of 3.6%
  - FEE chip: reach **~3.0mW/ch** with ADC and the pixelated readout R&D

TPC prototype with integrated 266nm UV laser



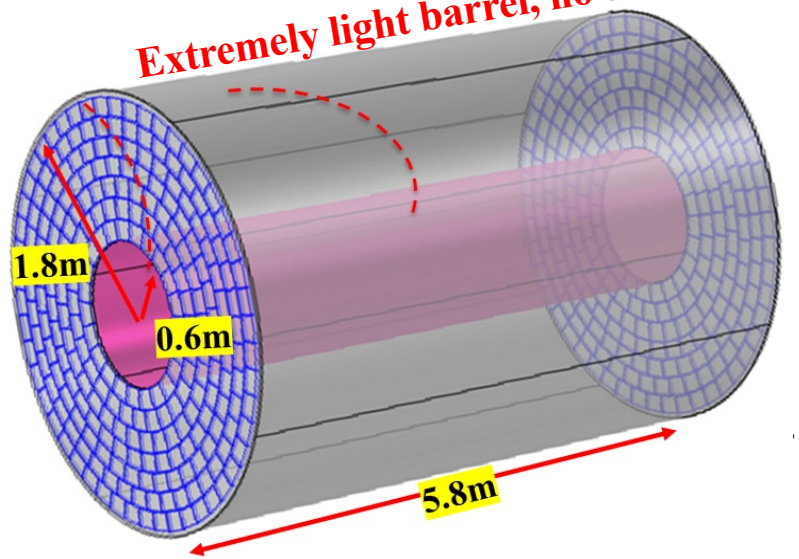






Ion suppression TPC module R&D

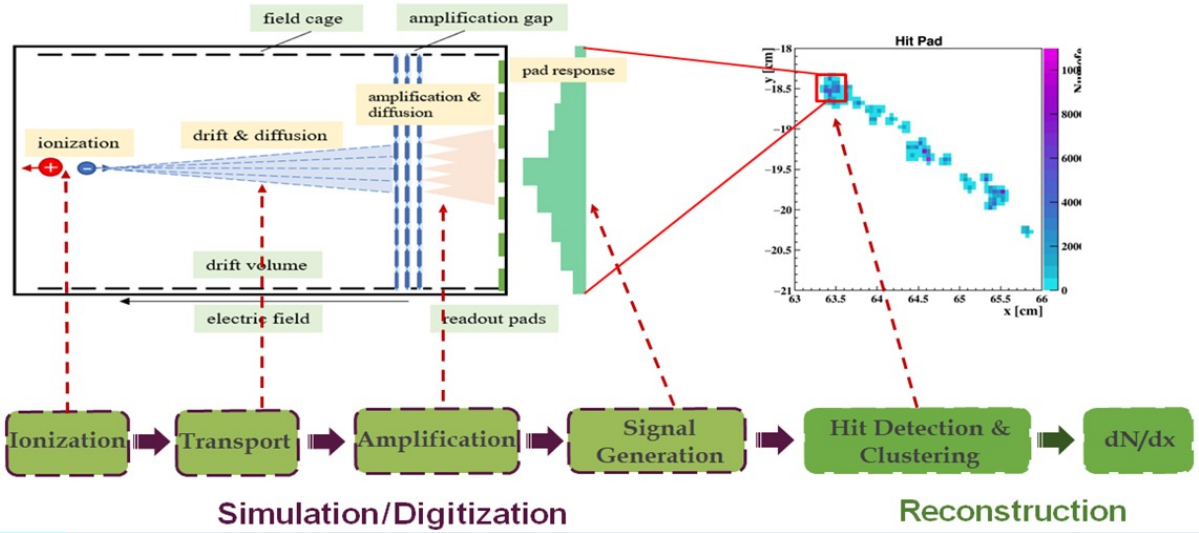
Extremely light barrel, no tension



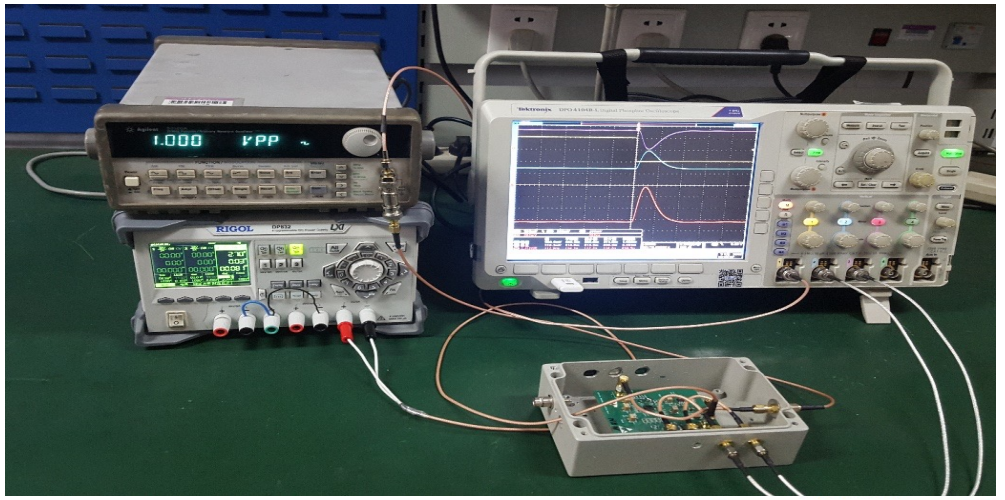
TPC for CEPC reference TDR

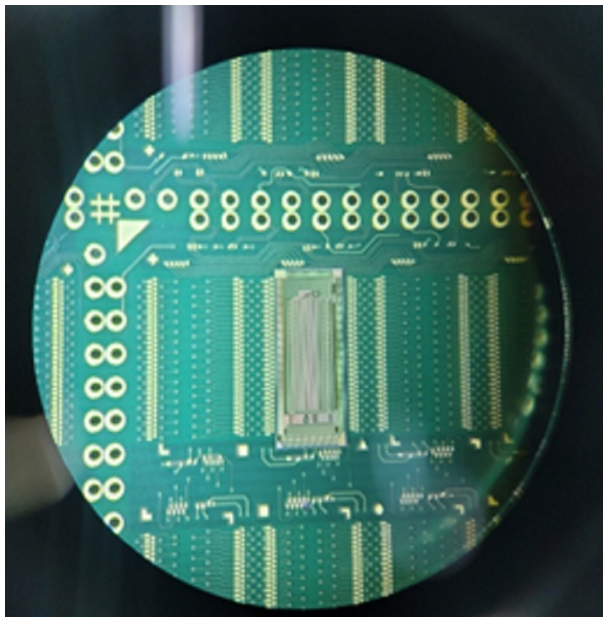
Status of Pixelated readout TPC for CEPC TDR

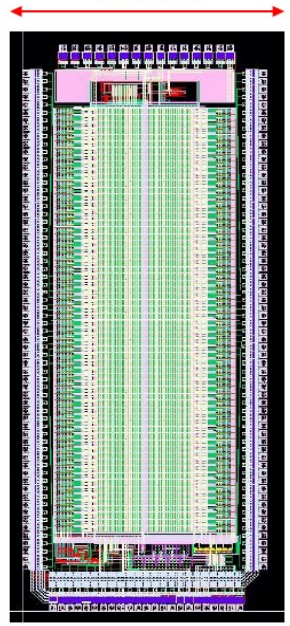
- **Simulation and R&D of Pixelated TPC readout for CEPC TDR**
  - Macro-Pixel TPC ASIC chip was started to developed and 2nd prototype wafer has done and tested
    - 500μm×500μm pixel readout designed
    - Noise of FEE: 100e
    - Time resolution: 14bit (5ns bin)
    - Power consumption: ~100mW/cm2 (2nd prototype)
- **Prototyping pixelated TPC detector at IHEP**
  - Principle of the prototype is no problem for testing
  - Developed prototype and aim for beam test @ DESY in 2024 with LCTPC collaboration



Framework of simulation at IHEP





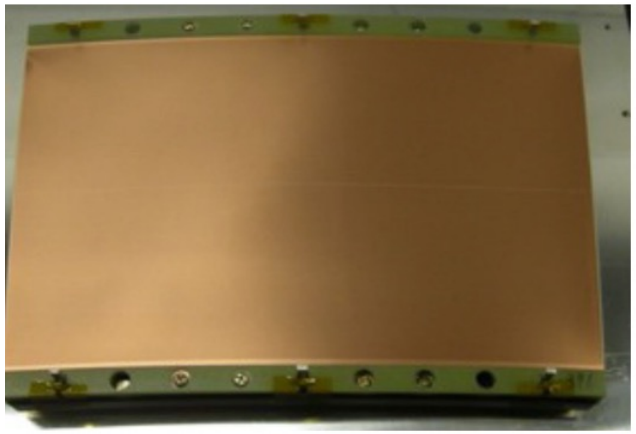


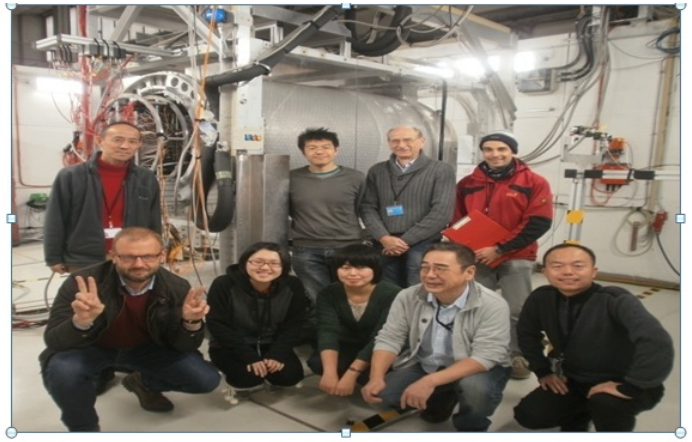
FEE ASIC chip R&D

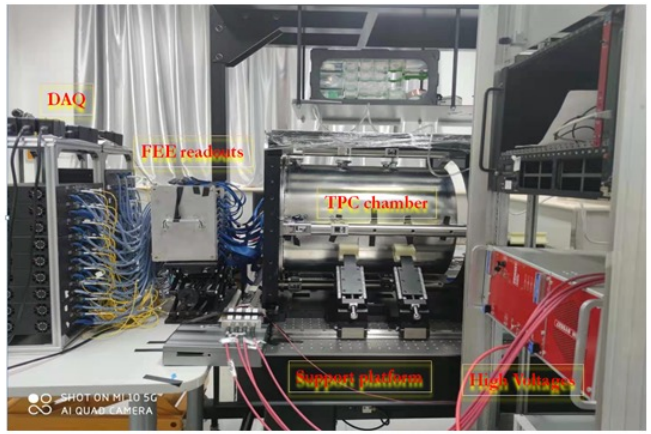
Activity international collaboration - TPC technology R&D

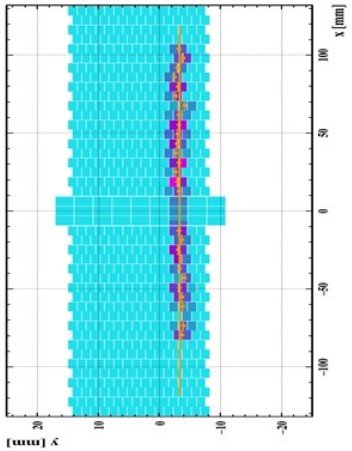
- Activity collaboration: Pixelated readout and Pad readout from IHEP and LCTPC collaboration
  - Large Prototype setup have been built to compare different detector readouts for Tera-Z
  - PCMAG: B < 1.0T, bore Ø: 85cm, Spatial resolution of $\sigma_{r\phi} \leq 100$ μm
  - Collaboration implement improvements in **a pixelated readout TPC for CEPC TDR**

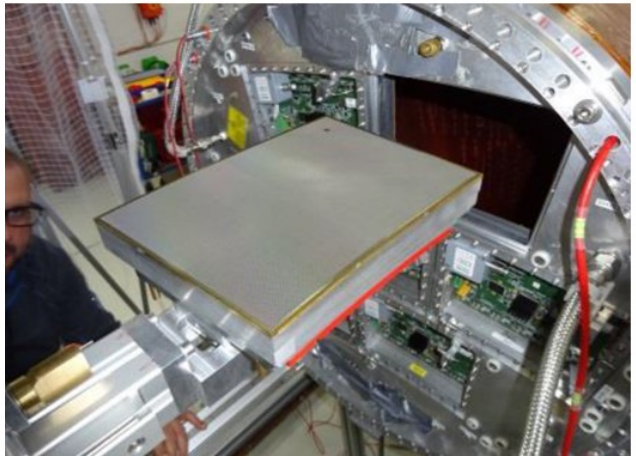
ArXiv. (2023)2006.08562
NIM A (2022) 167241
ArXiv (2022)2006.085
JINST 16 (2021) P10023
JINST 5 (2010) P10011
NIM A608 (2009) 390-396

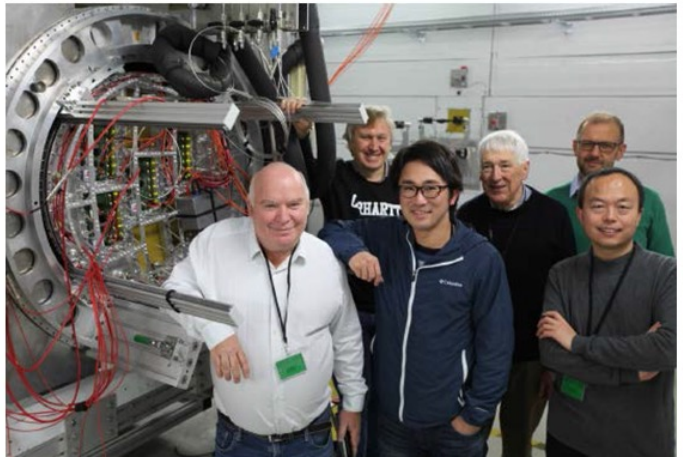


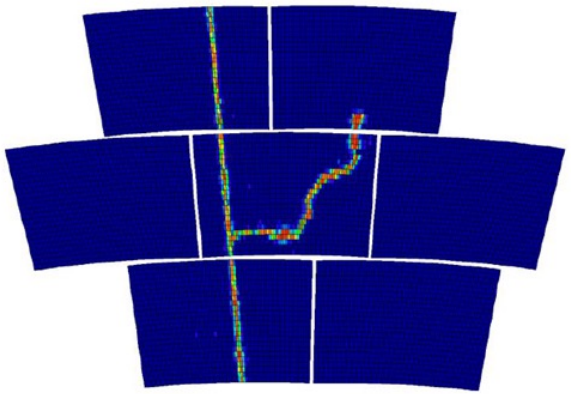




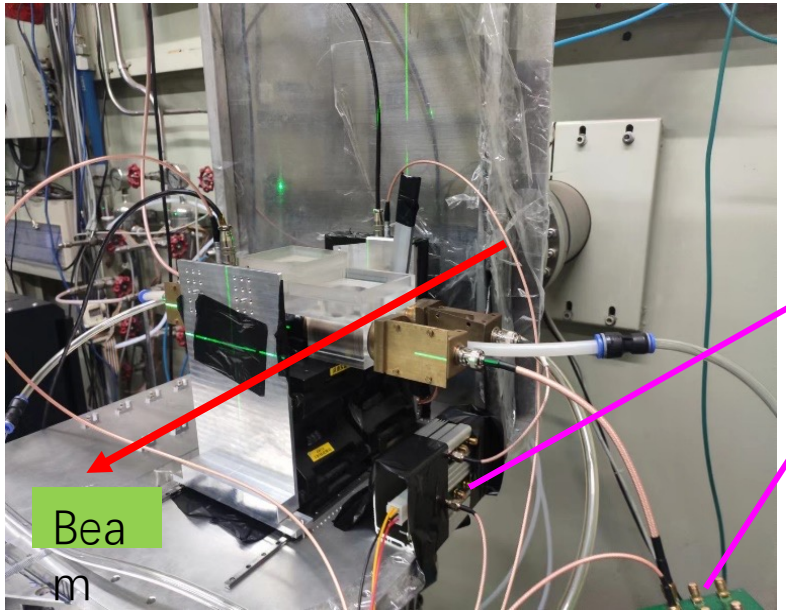


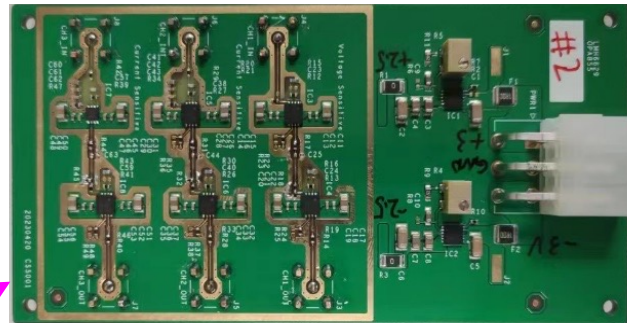


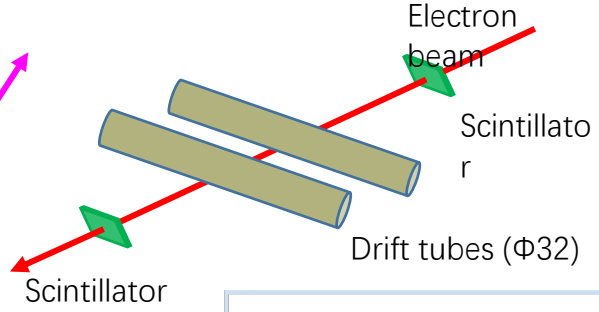


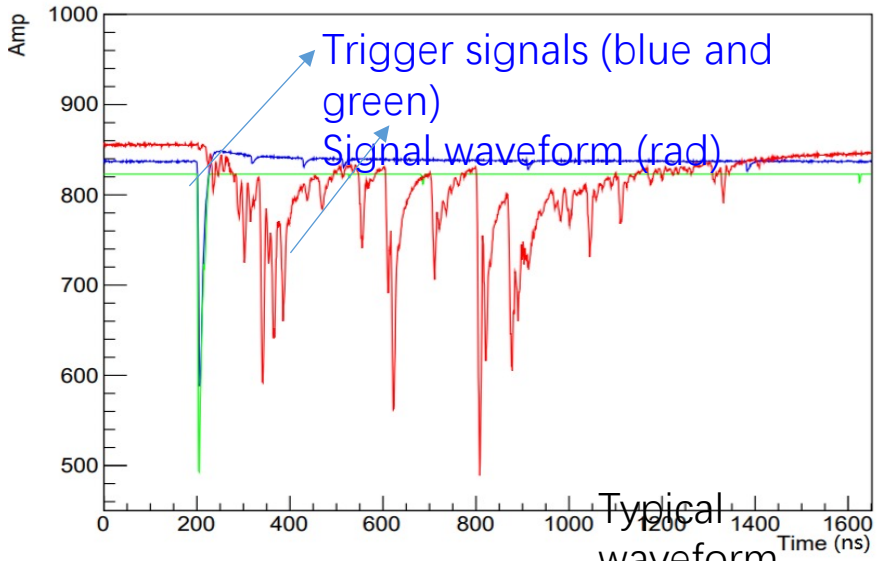


Drift chamber R&D and beam test



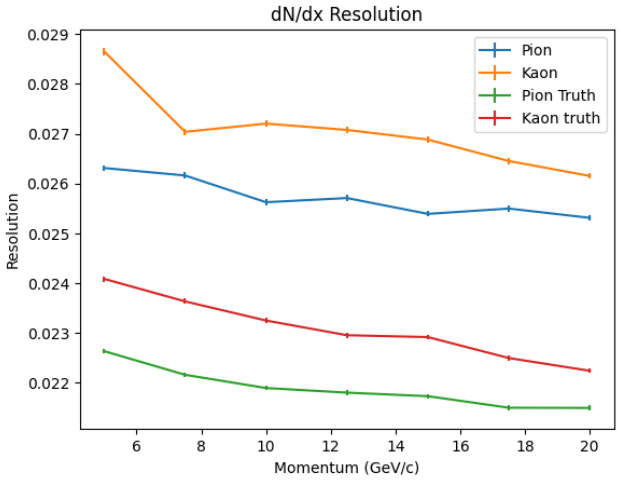




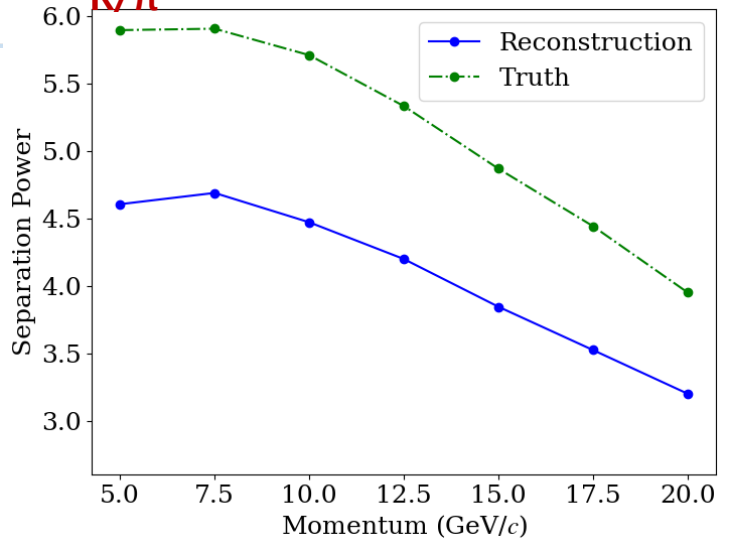


- Two drift tubes + preamps + ADC (1GHz)
- Two scintillators provide trigger signals
- Tested with electron beam at IHEP
- Clear peaks, low noise, ~ ns rise time

dN/dx resolution: ~2.5% for pion



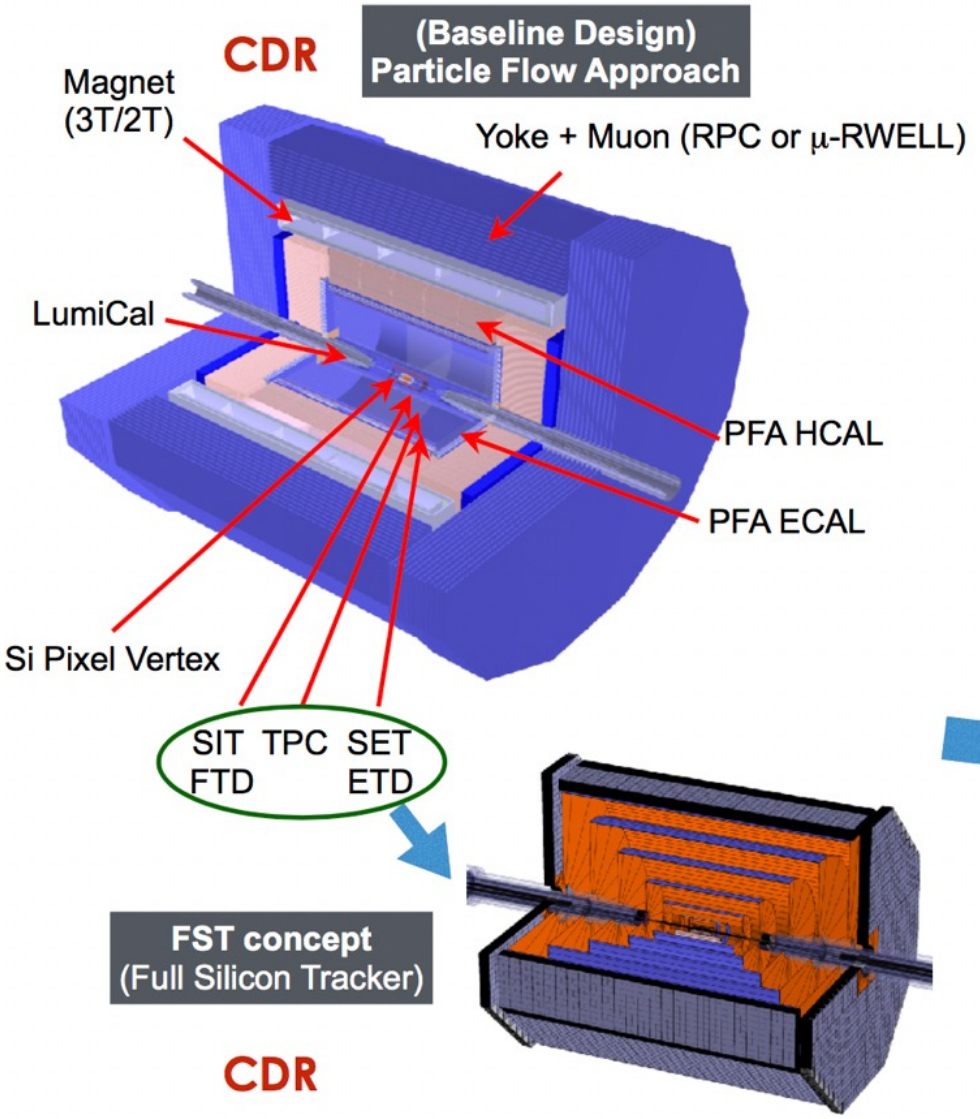
Separation: 3.2σ for 20 GeV/c K/π

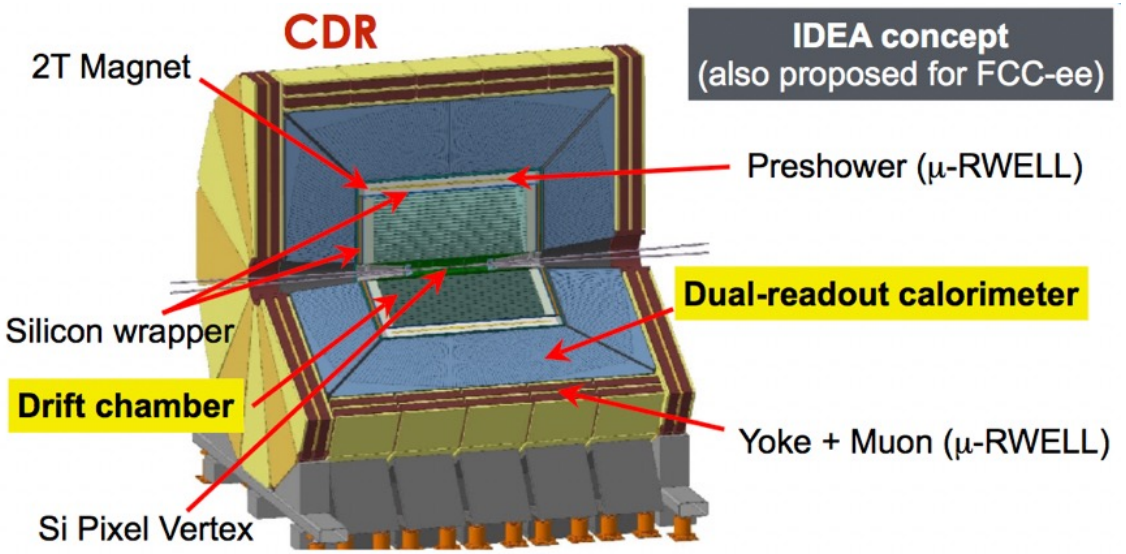


R&D for the baseline detector concept

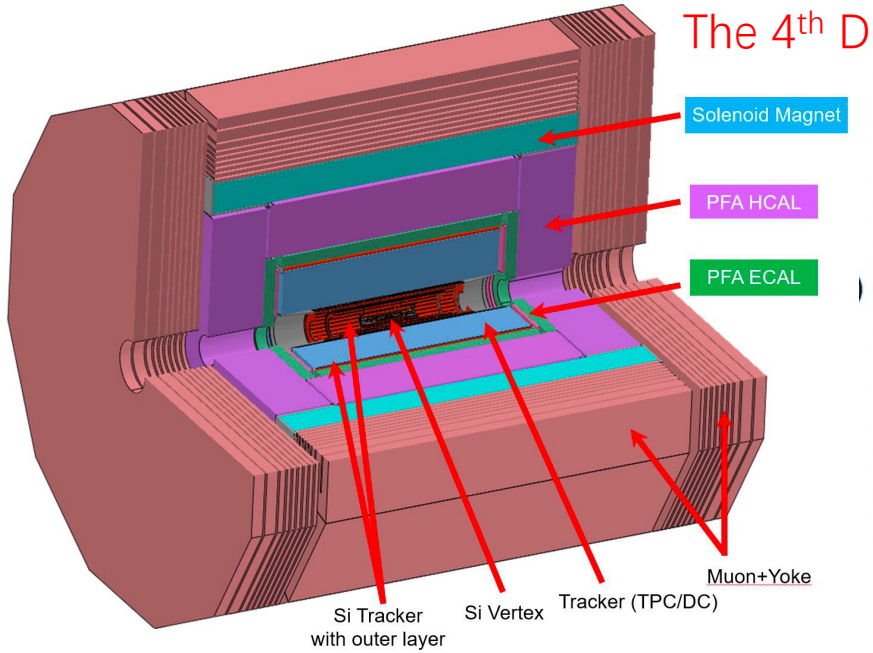
- ❖ Silicon detector R & D (vertex, silicon tracker, LGAD TOF detector)
- ❖Gas detector (TPC, Drift chamber)
- ❖PFA calorimetry : ECAL and HCAL
- ❖Solenoid Magnet

CEPC Detector Conceptual Designs



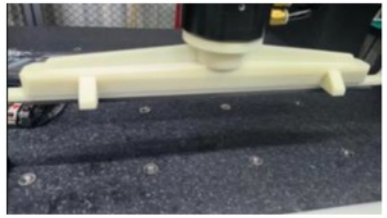


The 4th Detector Concept

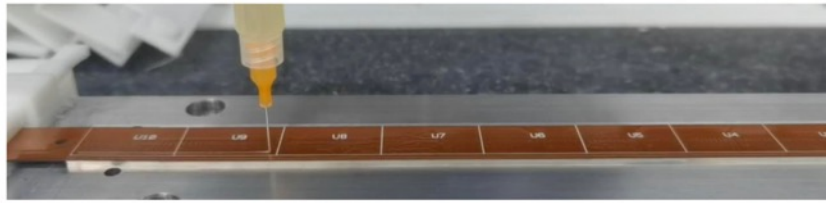


TaichuPix3 vertex detector prototype

New pickup tools

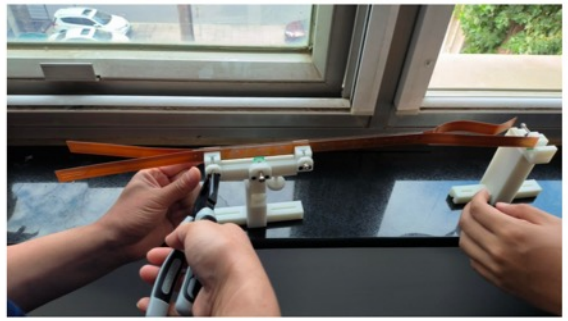


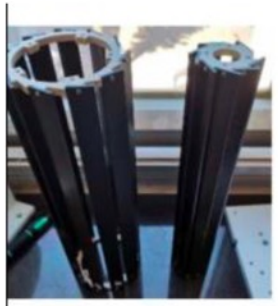
Dummy ladder glue automatic dispensing using gantry

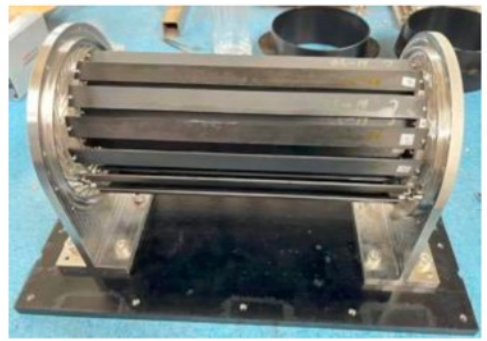


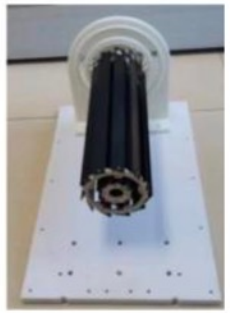
Ladder on wire bonding machine

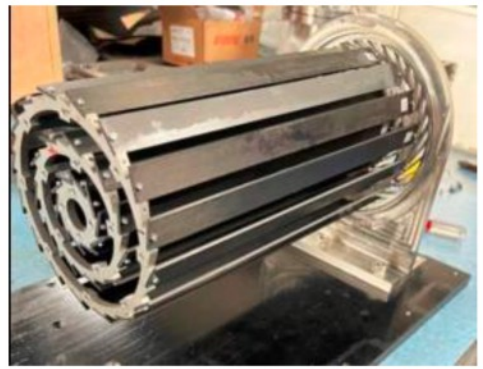
Dummy Ladder on holder









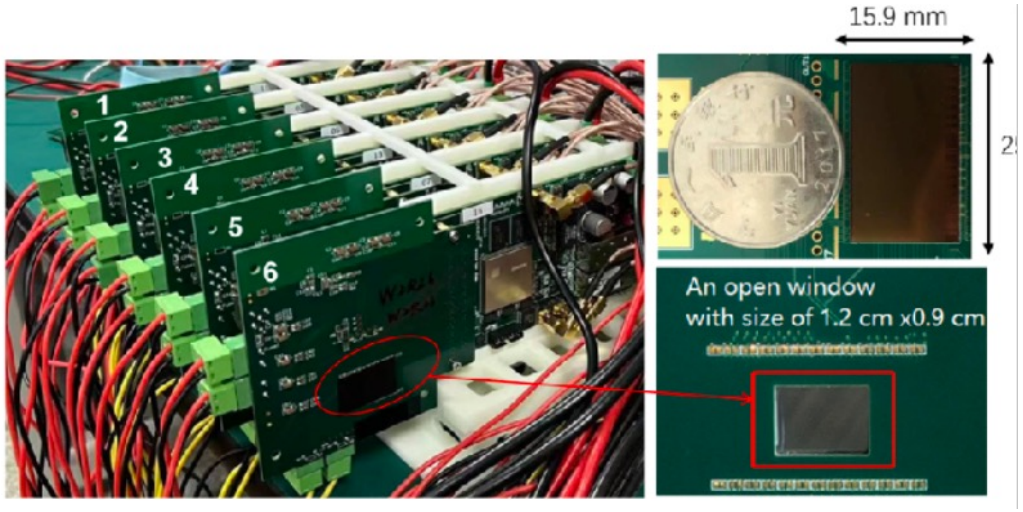


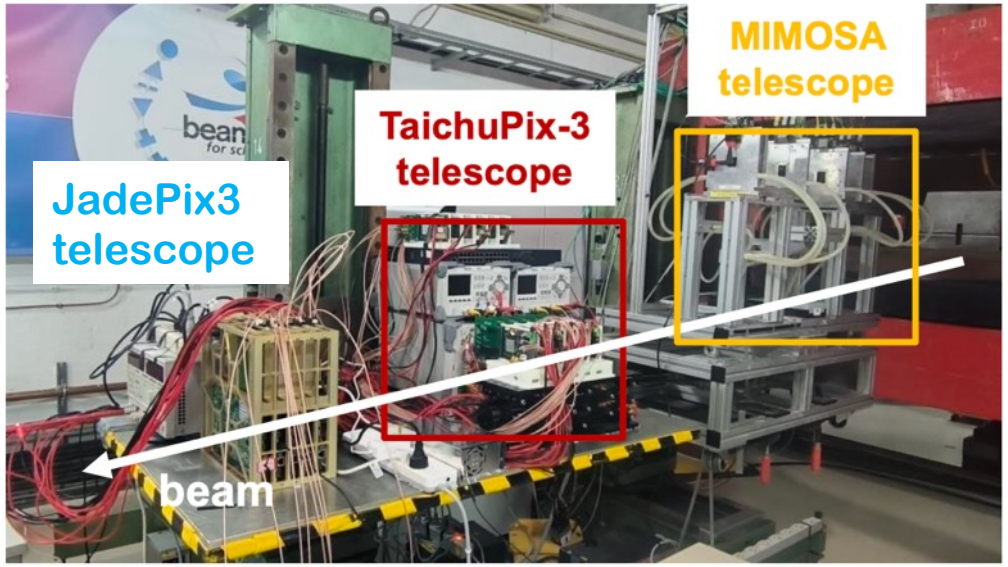
Ladder support tools

Ladder loaded on vertex detector

The first vertex detector (prototype) ever built in China

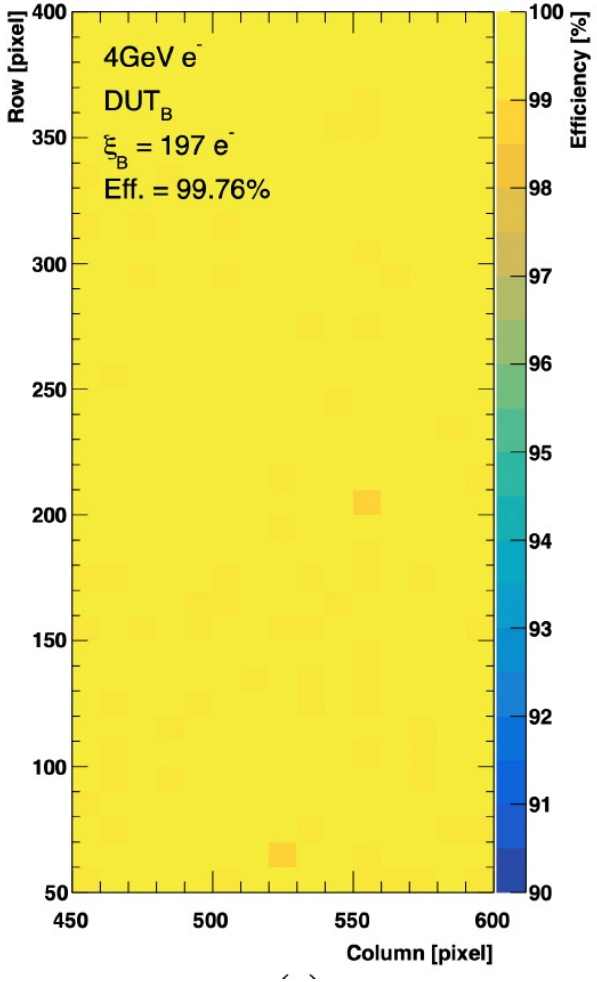
Jadepix3/TaichuPix3 beam test @ DESY



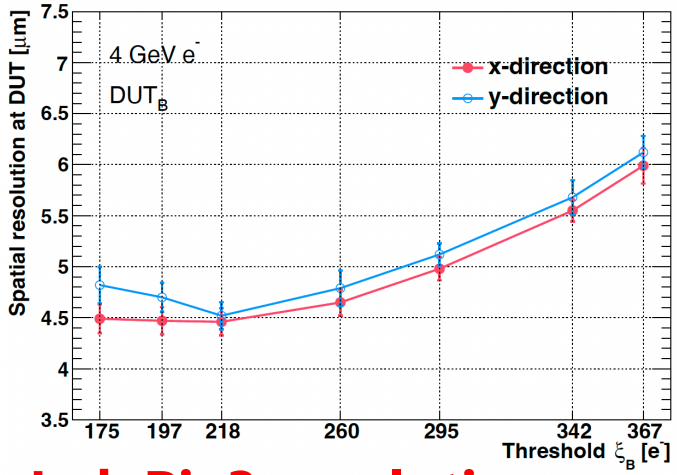


Spatial resolution 4~5um, Efficiency >99%

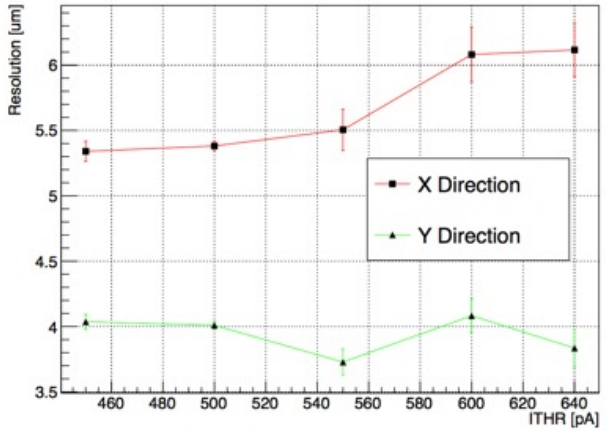
TaichuPix3 efficiency



TaichuPix3 resolution



JadePix3 resolution



Collaboration with CNRS and IFAE in Jadepix/TaichuPix R & D

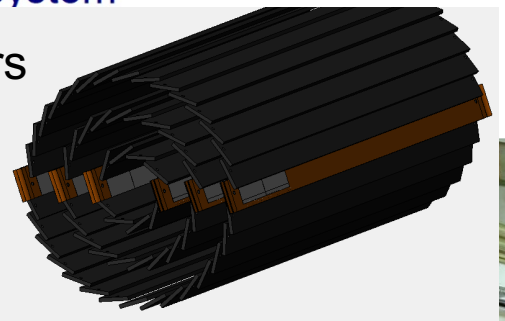
TaichuPix3 vertex detector prototype beam test @ DESY

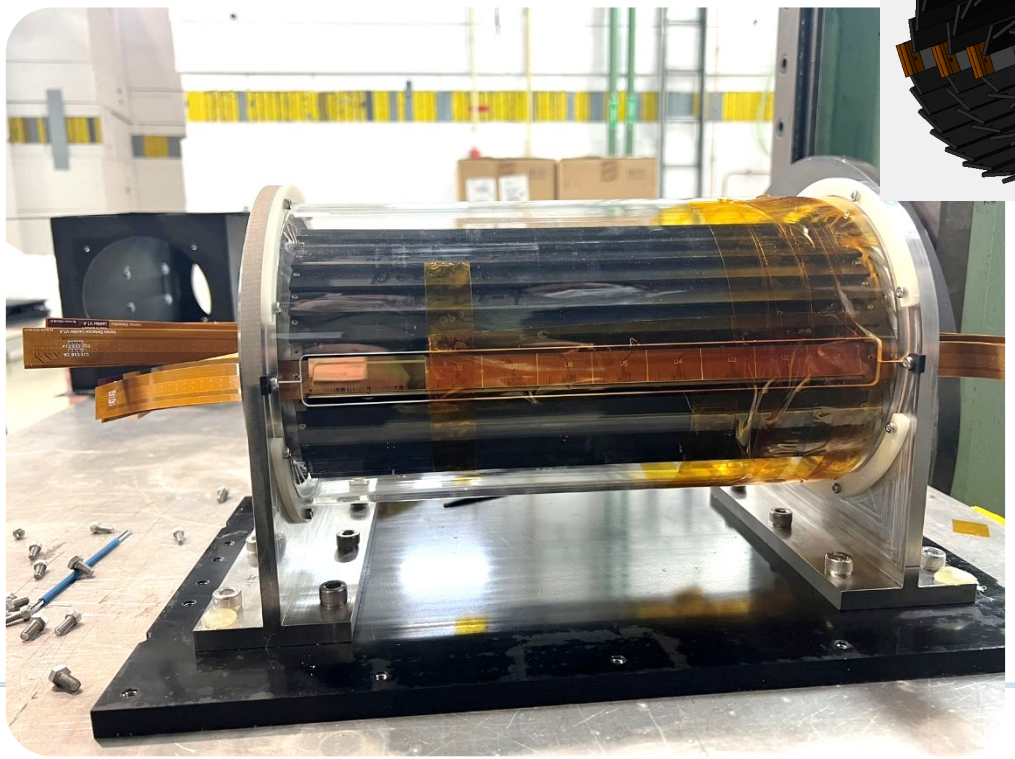
TaichuPix-based prototype detector tested at DESY in April 2023

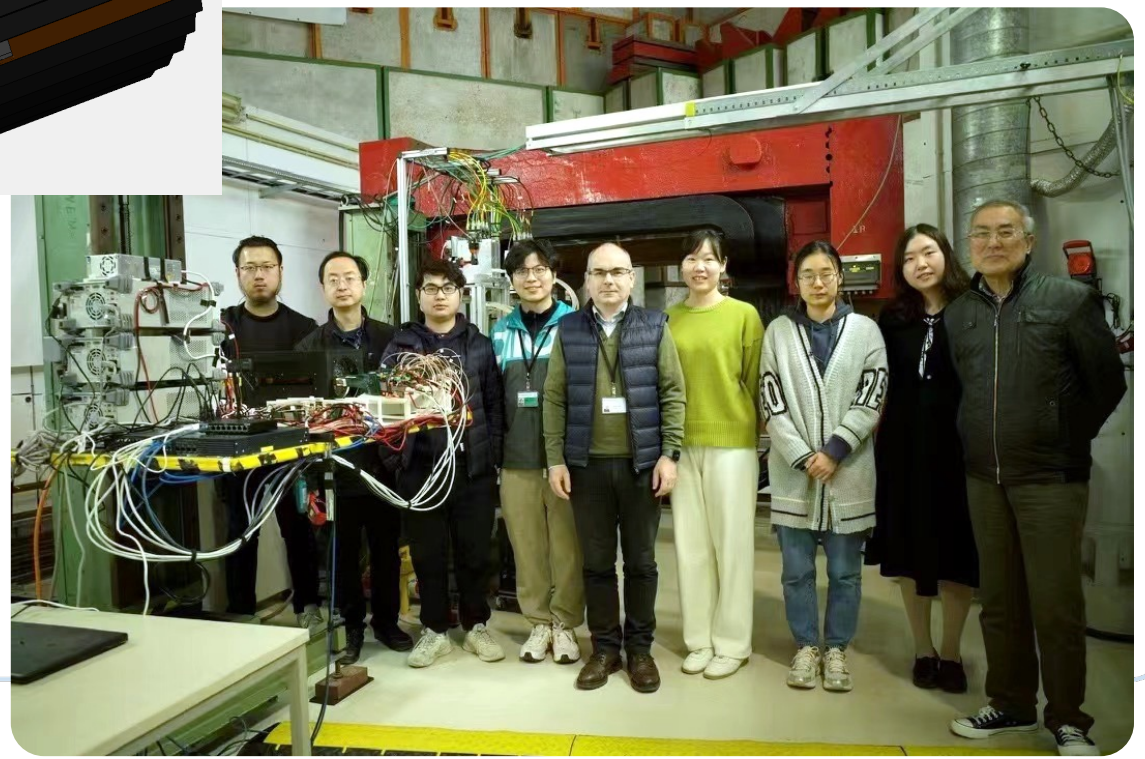
Spatial resolution ~ **4.9 μm**

Ladder readout system

6 double-sided ladders





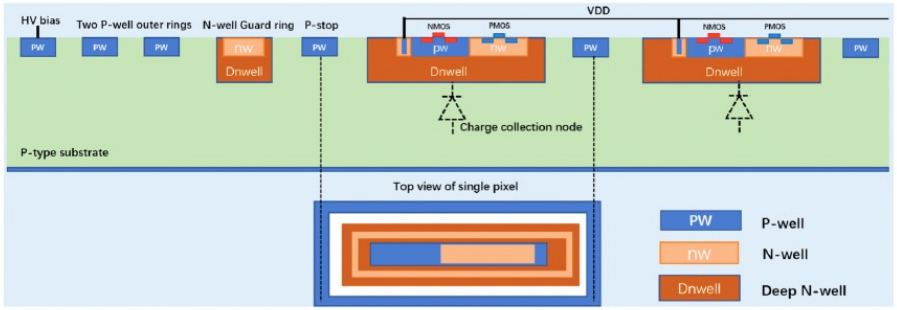


Silicon Tracker using HV-CMOS: the SMIC 55nm chips

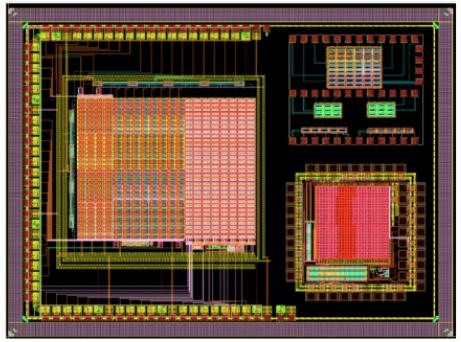
❖ MPW SMIC 55nm HVCMOS （COFFEE2 chip)

- CMOS SENOSR IN FIFTY-FIVE NM PROCESS (COFFEE)
- Submitted in Aug 2023, Received at the end of 2023.
- High-res wafer of 1k or 2k Ωcm available
- Breakdown voltage up to – 70V (enough depleted depth)

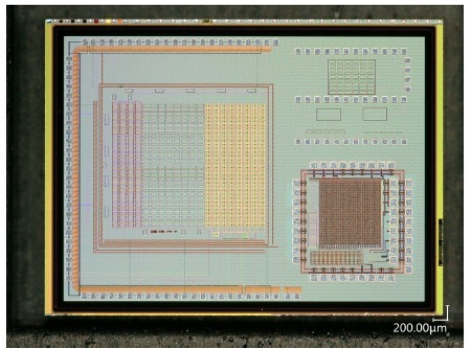
Cross-section of pixel strucure



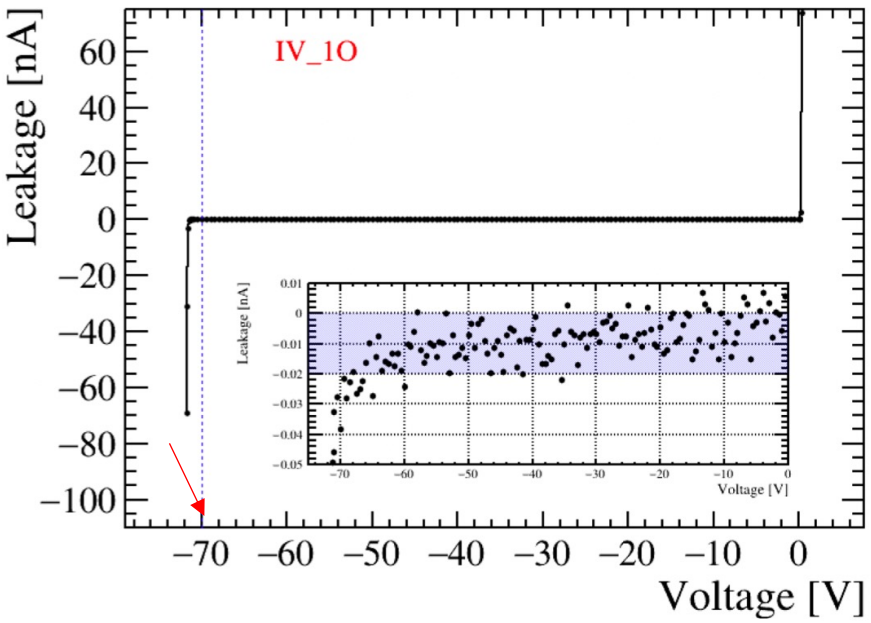
COFFEE2 floorplan



COFFEE2 photo



IV test



CV test
1 single Pixel