CMOS-based CEPC outer tracker option: a preliminary design and cost

Input:

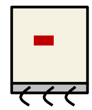
- CMOS tracker rate estimation @ rTDR tracker meeting, 15 Mar
- Outer tracker 方案和成本估算 @ rTDR tracker meeting, 15 Mar
- Elec-TDAQ framework @ CEPC workshop, 9 Apr
- LHCb Upgrade II FTDR
- Private discussion with Jianchun Wang, Meng Wang, Wei Wei, Xiongbo Yan, Jinyu Fu, Xuhao Yuan, Gang Li, Chengdong Fu, and many more
- All mistakes are mine (Yiming)

6 May 2024

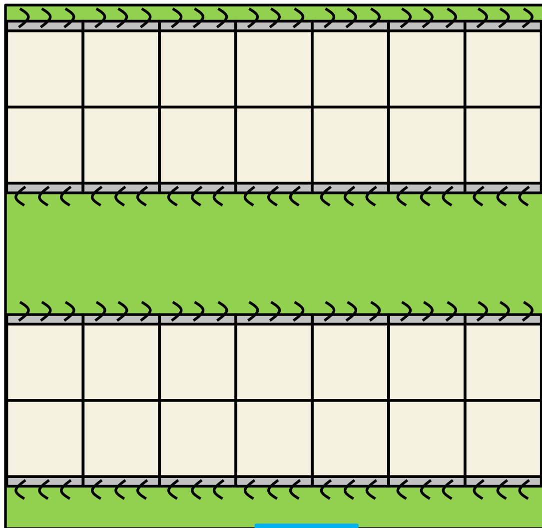
Event rate assumption

- Assuming:
  - Physics event rate 112 kHz => 1 MHz for all event including physics, bkg, noise
  - Track multiplicity: 100
  - Cluster size: 3
- CMOS sensor
  - Pixel size: 25×150 um^2.
  - Bits per hit: 48 bit.
- Outer tracker
  - Radius 1800 mm.
  - Length 5800 mm.

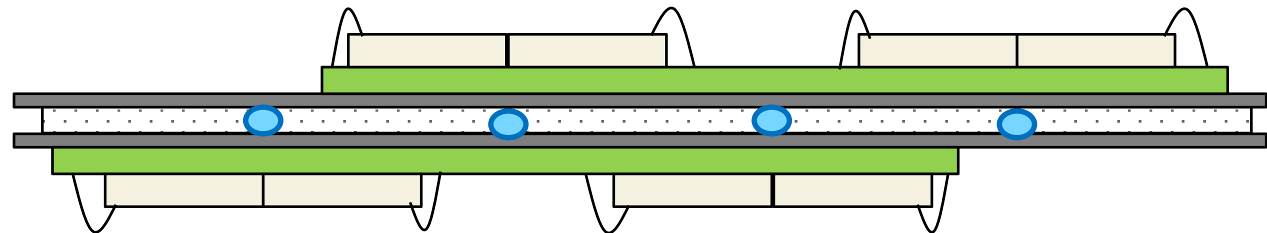
- Hit density: 0.74 kHz / cm^2.
- Data rate per chip: 140 kb/s



Sensor chip
20×20 mm^2

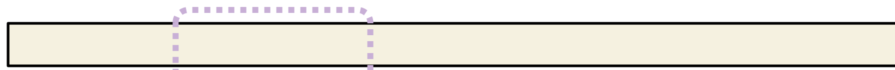


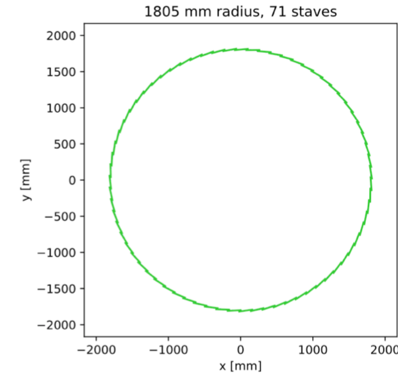
Module: 28 chips
* Rate per module: 4.0 Mb/s
* Note: lpGBT supports up to 28 e-links



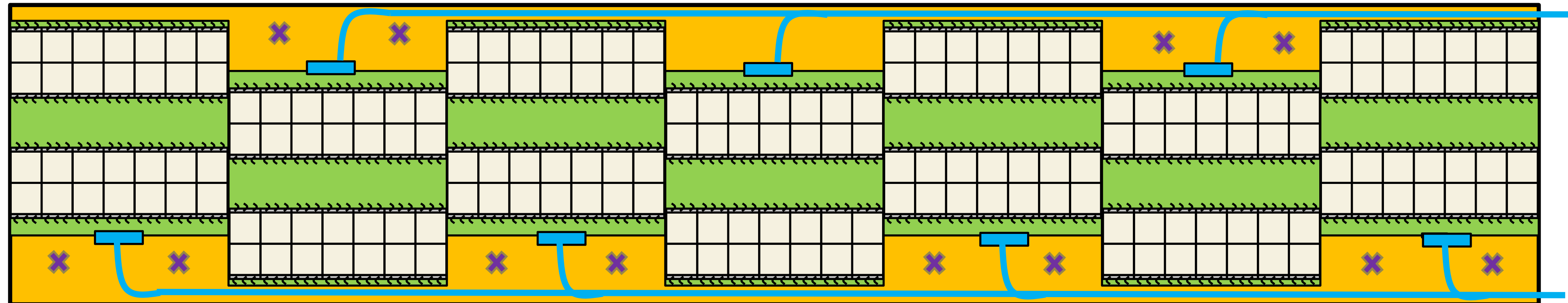
Modules mounted on both sides of staves to cover inefficient area
Cooling pipes embedded in stave/ladders

1 ladder (5880 mm) = 42 modules × 2 sides





71 staves
5964 modules
1.67 million chips



Sensor chip

Hybrid PCB

Optical convertor & fibre

Mechanical support (one side only)

Cost estimation

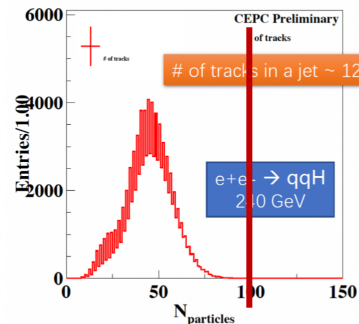
Category 类别	Item 名称	Total (10k CNY) 小计（万元）	Unit cost (CNY) 单价（元）	Unit 单位	Quantity 数量	Note 备注
Sensor chip	Sensor chip	3459	18,000	Wafer	1920	3.3 MCNY for NTO + 18k/wafer; assume 50% yield
Common electronics	Hybrid PCB	417	700	Piece	5964	
	Optical fibre	119	200	20m	5964	
	Optical connector	1193	2,000	Piece	5964	
	PCB connector	60	100	Piece	5964	
	Power cable	239	400	20m	5964	
Total		5487				

Note: cost on mechanical support and cooling not considered yet

BACKUP

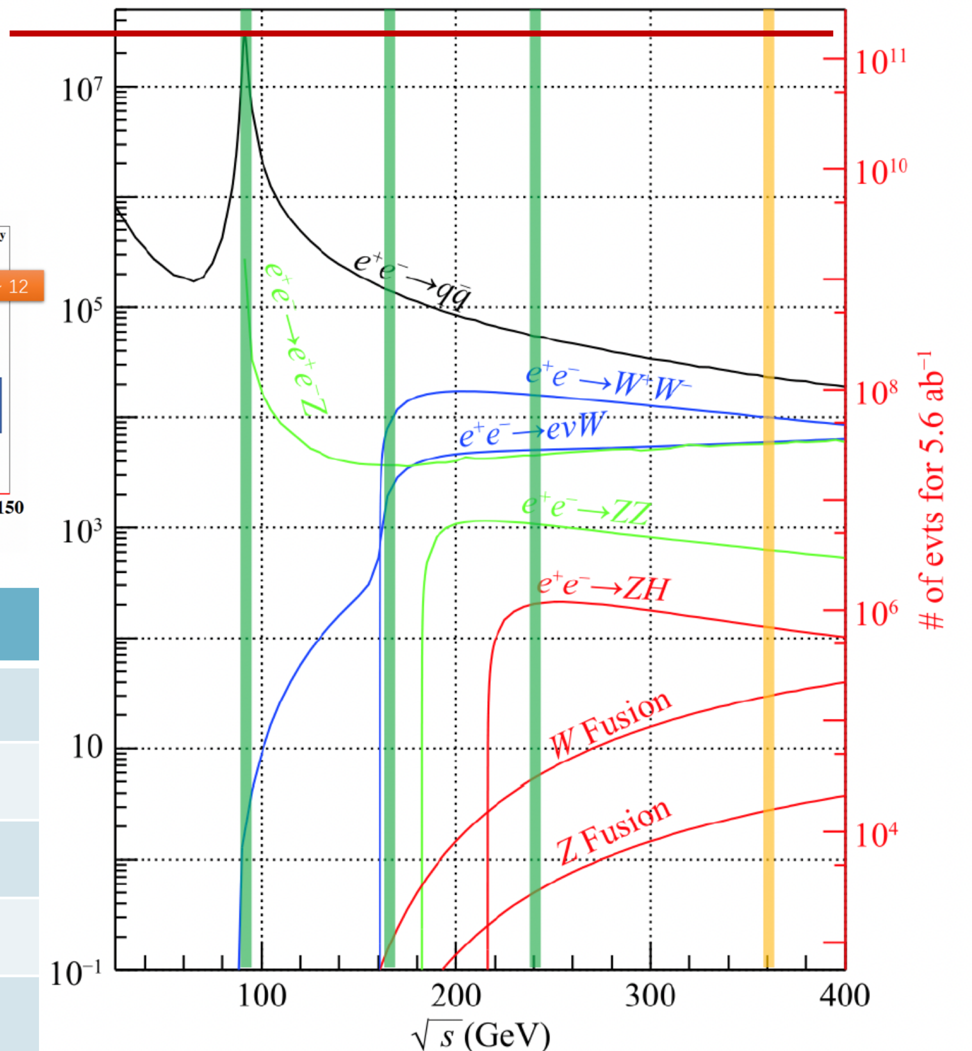
Assumption: Event rate

- Z pole: ee -> qqbar dominating.
  - $\sigma \sim 3\times10^{7}$fb
  - ×2 to account for other physics + background
  - $f = \sigma \cdot \mathcal{L} =$ 115 kHz
  - Note: Beam bkg can be significant!
  - Will update when MDI input available
- Track multiplicity: 100 (conservative)
- Cluster size: 3



L[e34cm-2s-1]	H	Z	W	Ttbar
Sqrt(s)[GeV]	240	91	160	360
L@30MW	5	115	16	0.6
L@50MW	8.3	192	26.7	0.8
years	10	2	1	5
#bunches	268	11934	1297	

CEPC Acc. TDR



Gang LI

FE design

- Bits per hit?
- ATLASPix3 as reference
  - Hit-driven mode (triggerless): 8/10b encoding, up to 96 bit/hit, target link speed 1.6 Gbps
  - Triggered mode: 64/66b encoding, up to 128 bit/hit, target link speed 1.28 Gbps
- CEPC HVCMOS hit size?
  - 14b timestamp (may be reduced)
  - 10b + 8b address (25um * 150 um => 800 col * 134 row)
  - 1b parity
  - 10b TOT (may be reduced)
  - 48 bit/hit should be enough
- Readout scheme?

Data rate estimation

Key assumptions: Event rate 112kHz, track multiplicity 100, cluster size 3, bits per hit 48; Beam bkg to be added

Layer	Hit density [kHz/cm^2]	Data rate /chip [Mbps]	Data rate / module [Mbps]	Data rate / layer [Gbps]
Barrel SIT 1	5.2	1.0	8.0	1.5
SIT 2	2.2	0.43	3.5	1.5
SIT 3	0.79	0.15	1.2	1.4
SET	0.08	0.02	0.13	1.4
Endcap SIT 1	1.3	0.24	2.0	0.17
SIT 2	0.57	0.11	0.87	0.17
SIT 3	0.26	0.05	0.41	0.22
SET	0.03	0.006	0.05	0.24

Total data rate: 6.6 Gbps for SIT+SET, or 5.0 Gbps for SIT only

Sensor chip cost

- # chips needed: 71 staves * 2 sides * 42 modules * 28 chips = 166,992 chips
- 12-inch wafer accommodates 174 chips => 960 wafers
- Assume 50% yield => 1920 wafers