



山东大学(青岛)

SHANDONG UNIVERSITY, QINGDAO

# 粒子物理实验硅像素探测器研究现状与发展趋势

张亮

第二十届全国科学计算与信息化会议，西宁，2023.7.9-14

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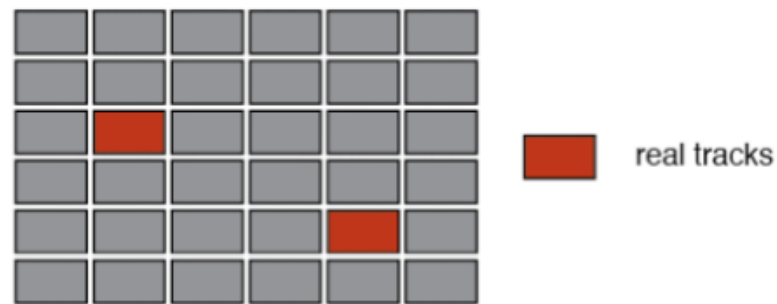
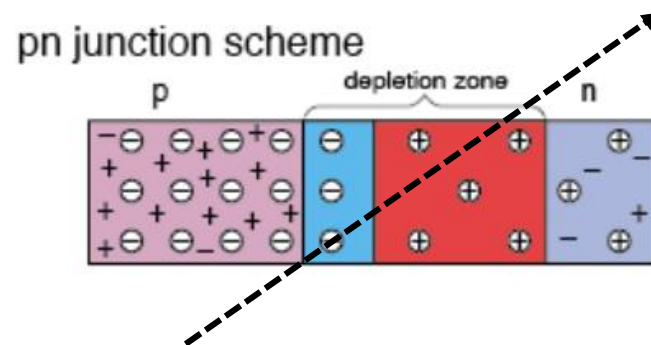
# 背景介绍

## □ 硅探测器

- ❖ 高能物理实验粒子径迹探测
- ❖ 粒子探测器重要参数：SNR
  - ✓ 大信号→低电离能→低带隙
  - ✓ 低噪声→较少本征载流子→高带隙
  - ✓ 理想材料： $E_g \approx 6\text{ eV}$ 
    - 金刚石，成本昂贵
- ❖ 硅探测器成本低、性能优异、技术成熟

## □ 类型

- ❖ 硅微条
- ❖ 硅像素
  - ✓ 混合式像素探测器（1980s）
  - ✓ 单片式像素探测器（2000）



硅像素结构

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  - ❖ SOI工艺
- 总结

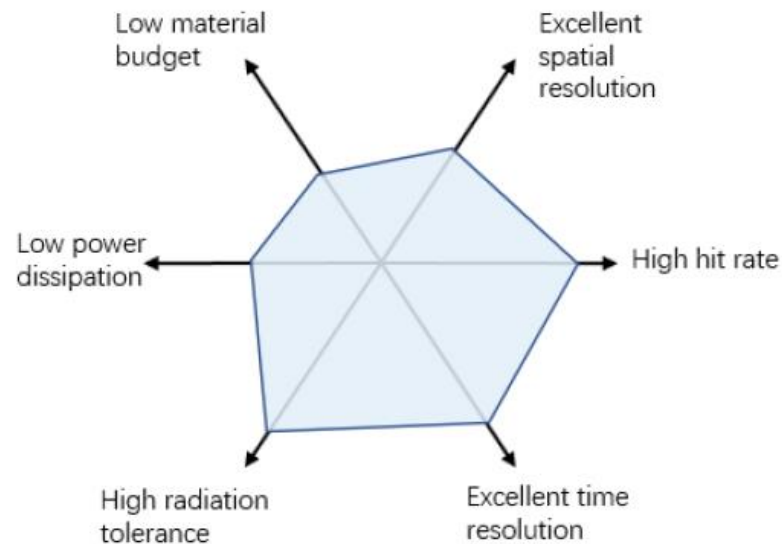
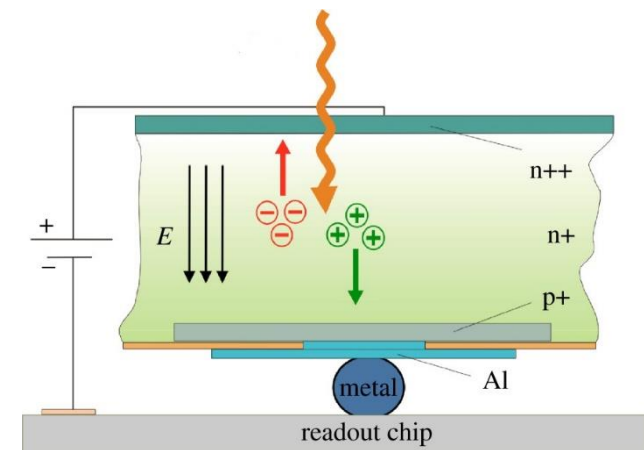
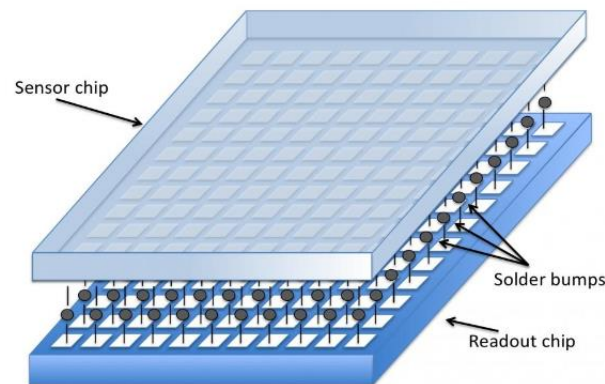
# 混合式像素探测器 (Hybrid Pixel Detector, HPD)

## □ 优点

- ❖ 灵敏度高
- ❖ 噪声低
- ❖ 抗辐照能力强
- ❖ 易于优化Sensor和ASIC芯片
  - ✓ ASIC不受工艺限制

## □ 缺点

- ❖ 功耗大
- ❖ 厚度大
  - ✓ 物质质量高
- ❖ Sensor和ASIC独立, 倒装焊
  - ✓ 成本高
  - ✓ 空间分辨率低



# 混合式像素探测器 (state-of-the-art)

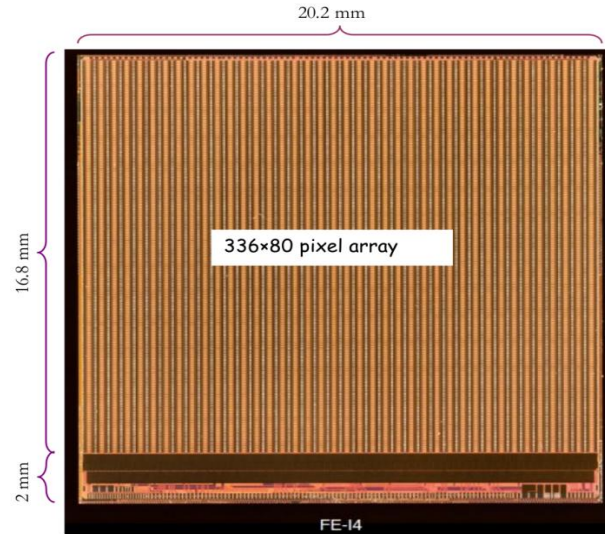
Chip	Process	Pixel array	Pixel size	Main Institute	Target	Comment
FE-I4	130 nm	80 × 336	50 × 250 $\mu\text{m}^2$	CERN	rad. hard	ATLAS Inner Tracker
PILATUS3	250 nm	60 × 97	172 × 172 $\mu\text{m}^2$	PSI	photo counting	X-ray
TimePix4	65 nm	512 × 448	55 × 55 $\mu\text{m}^2$	CERN	energy and time resolution	-
MediPix4	130 nm	320 × 320 160 × 160	75 × 75 $\mu\text{m}^2$ 150 × 150 $\mu\text{m}^2$	CERN	high granularity	X-ray
HEPS-BPIX4	130 nm	20 × 32	55 × 55 $\mu\text{m}^2$	IHEP	HEPS	HEPS

# 混合式像素探测器

## FE-I4 (CERN)

- ❑ 大型强子对撞机LHC ATLAS实验内径迹探测器
- ❑ 像素内集成CSA, 甄别器, DAC (阈值调节), SRAM
- ❑ 本地缓存, 四个像素共享数字逻辑

FE-I4	
Process	130 nm
Pixel size	$250 \times 50 \mu\text{m}^2$
Array size	$336 \times 80$
Chip size	$20.2 \times 18.8 \text{ mm}^2$
Power	$180 \text{ mW}/\text{cm}^2$
Active area	89%
TID	200 Mrad



Layout of the FE-I4

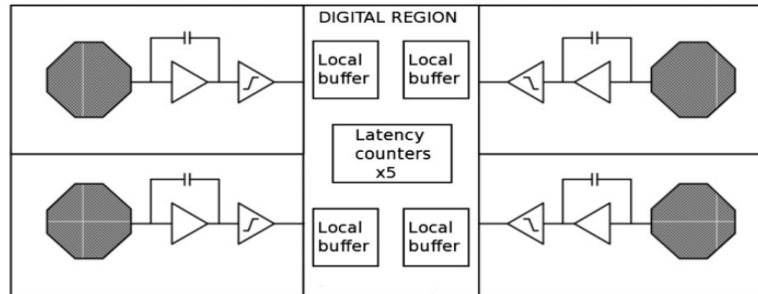
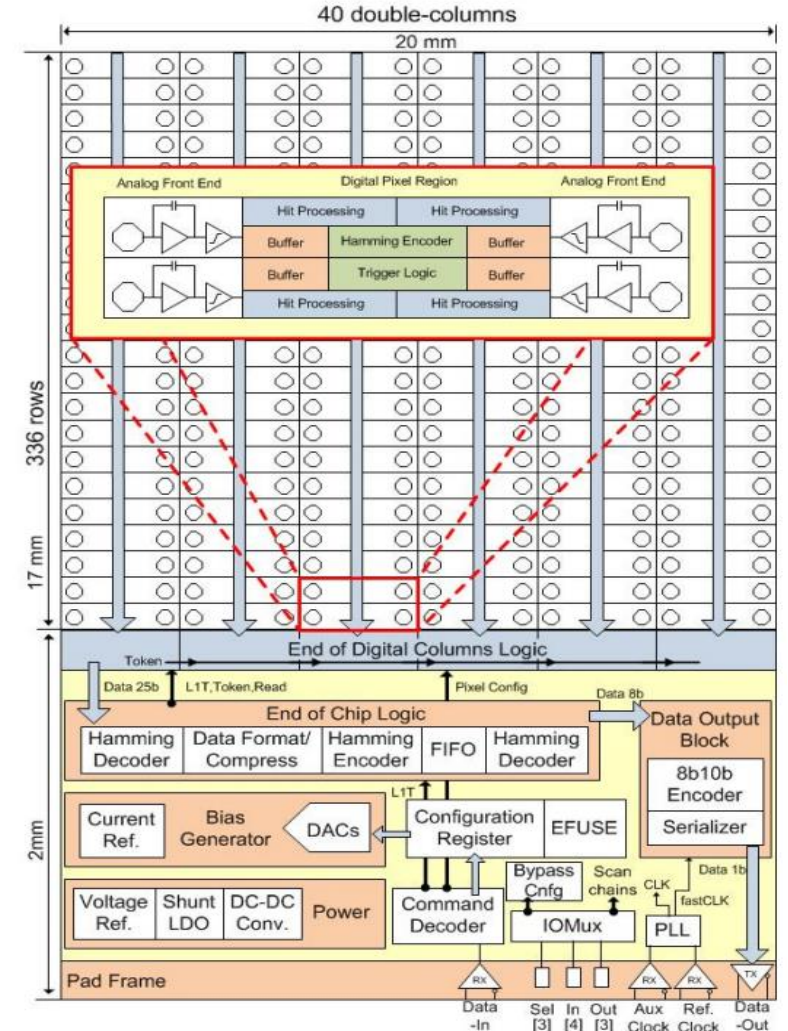


Diagram of 4-pixel region

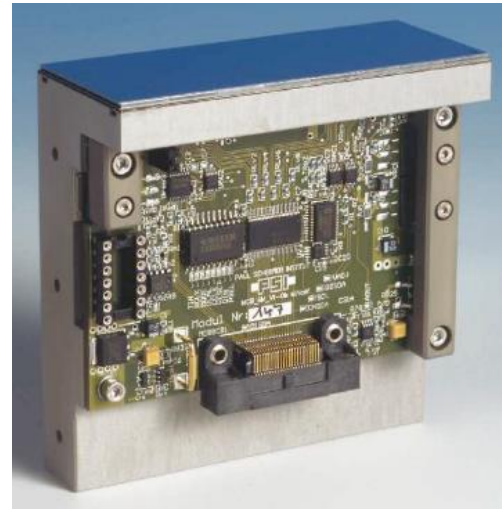
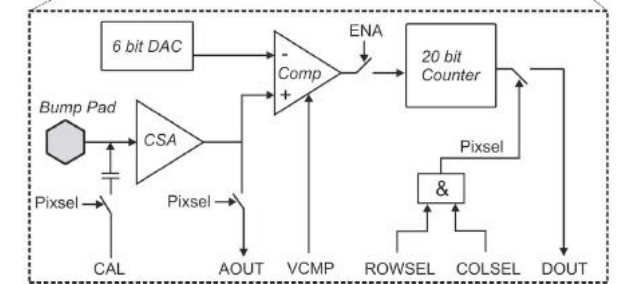
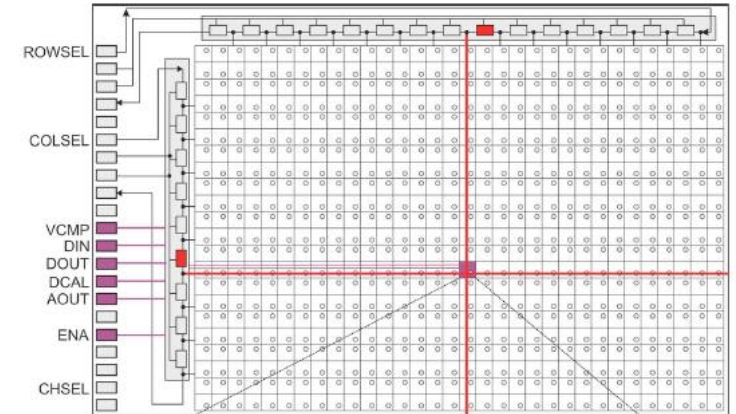
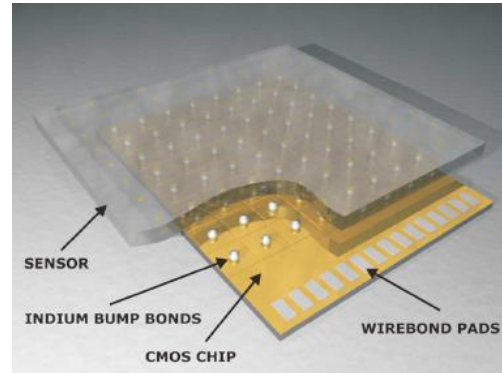


Schematic view of the FE-I4 architecture

# 混合式像素探测器

## PILATUS (PSI)

- ❑ 第一个商业化的X射线成像硅像素探测器
- ❑ 抗辐照版图设计：环形栅晶体管，保护环
- ❑ 像素内集成CSA, 甄别器， 阈值调节DAC
- ❑ ToT (time-over-threshold)



PILATUS3	
Process	UMC 250 nm
Pixel size	$172 \times 172 \mu\text{m}^2$
Array size	$60 \times 97$
Chip size	$10.5 \times 17.5 \text{mm}^2$
Power	80 mW (static) 90mW/MHz(dynamic)
photon rate	$>3 \times 10^8 \text{photons/s/mm}^2$
Energy range	3-21keV
Frame rate(max)	500 Hz

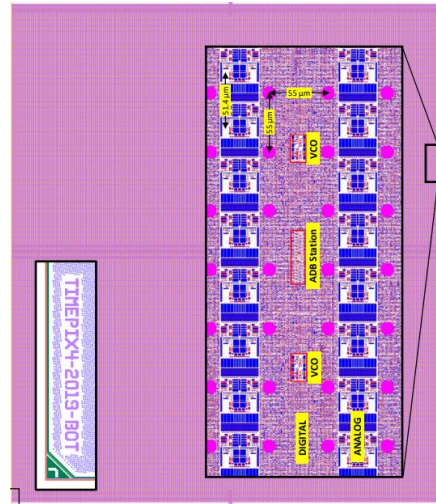


# 混合式像素探测器

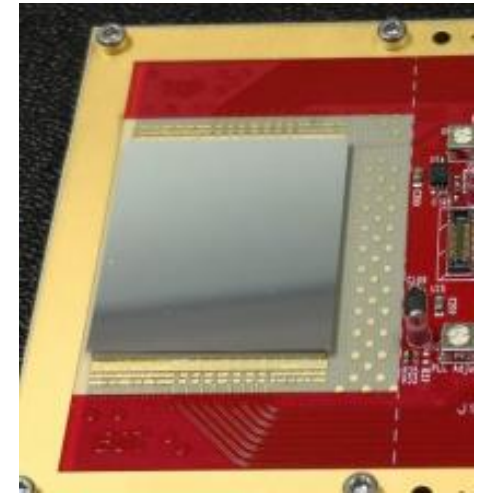
## Timepix-4 (CERN)

- ❑ 粒子径迹探测, X射线成像
- ❑ 200 ps 时间戳
- ❑ 像素内集成CSA, 甄别器, 阈值调节DAC
- ❑ ToA (time-of-arrival), ToT (time-over-threshold)
- ❑ 4边可拼接

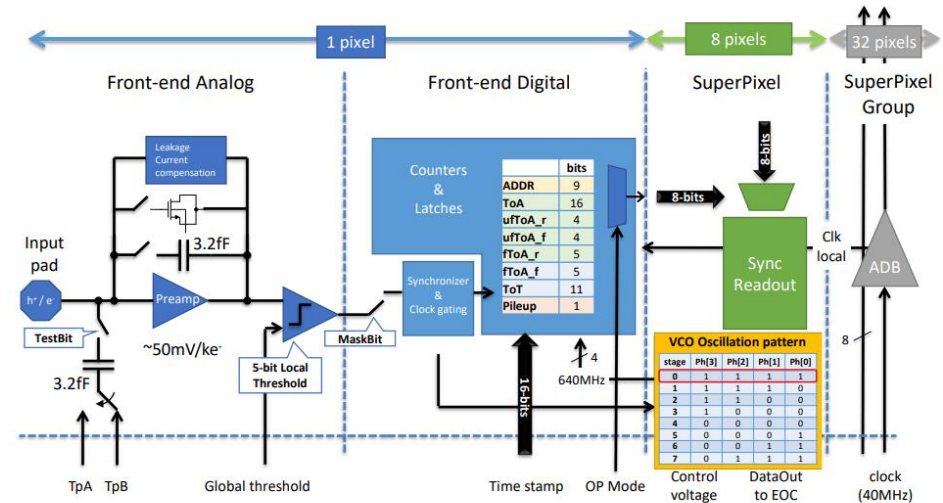
Timepix-4	
Process	65 nm-10 metal
Pixel size	$55 \times 55 \mu\text{m}^2$
Array size	$512 \times 448$
Chip size	$28.22 \times 24.7 \text{ mm}^2$
Power	$600 \text{ mW}/\text{cm}^2$
Active area	$6.94 \text{ cm}^2$
Time resolution	195.3125 ps
output rate	163.84 Gbps



Layout of the Timepix-4



Timepix-4 mounted on a PCB



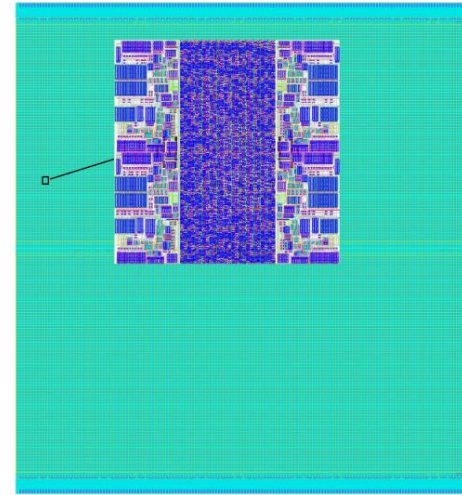
Functional description of the Timepix-4 architecture

# 混合式像素探测器

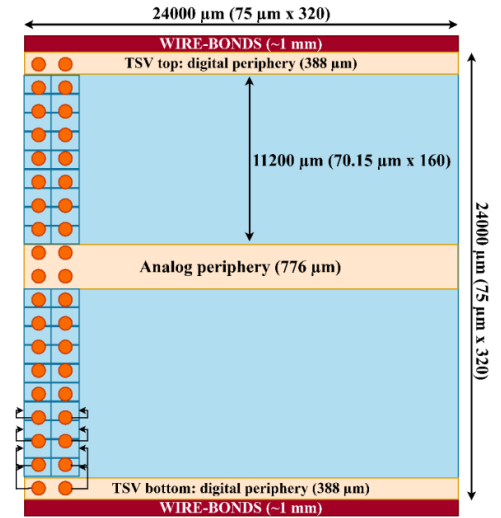
## Medipix-4 (CERN)

- ❑ X射线成像, 医学成像
- ❑ 多种像素尺寸
- ❑ 单像素模式和电荷累计模式
- ❑ 4边可拼接
- ❑ 全局读出模式

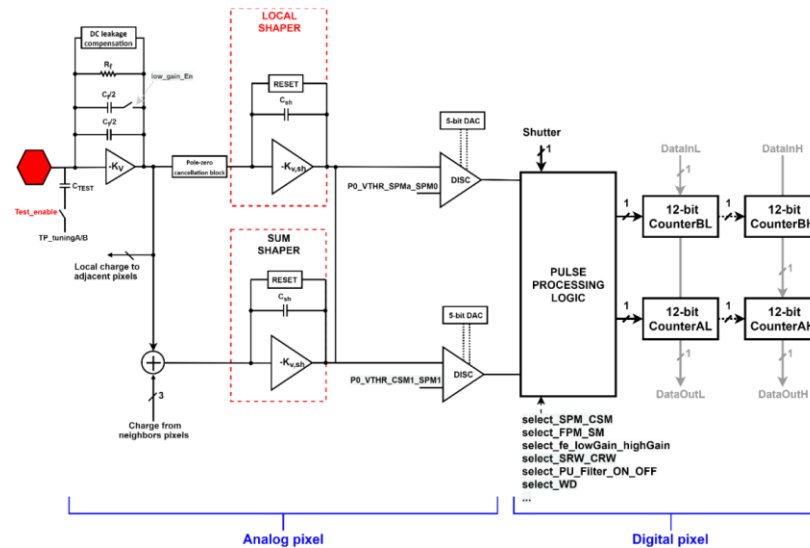
Medipix-4	
Process	130 nm
Pixel size	75 × 75 μm <sup>2</sup> 150 × 150 μm <sup>2</sup>
Array size	320 × 320 160 × 160
Chip size	24 × 24 mm <sup>2</sup>
Power	500 mW/cm <sup>2</sup>
Active area	99.37%
Energy resolution	2.2 keV FWHM
Output rate	4.8 Gbps



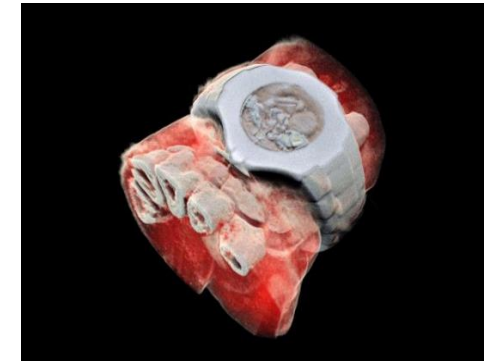
Layout of the Medipix4



Floorplan of the Medipix4



Block diagram of the pixel cell

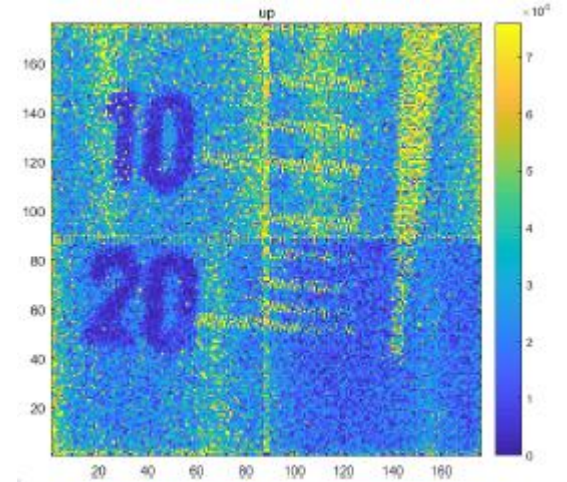
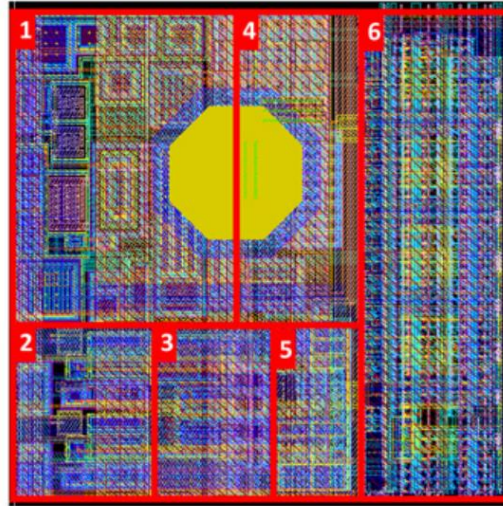


医学成像应用

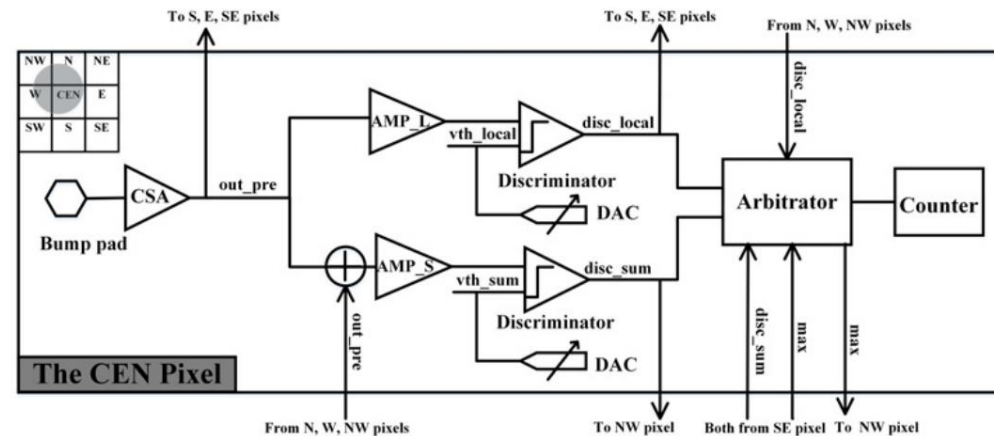
# 混合式像素探测器

## HEPS-BPIX (IHEP)

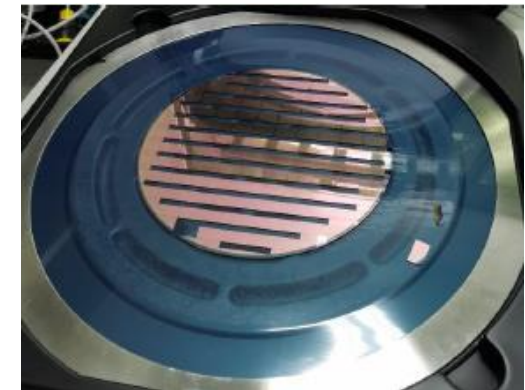
- ❑ 面向高能同步辐射光源自主研制
- ❑ 关键技术均实现国产化，包括传感器，ASIC芯片，DAQ，机械...
- ❑ 已列入高能光源HEPS工程序列
- ❑ 像素内集成CSA，放大器，甄别器，阈值调节DAC，计数器和控制逻辑
- ❑ 国内首个应用于工程的硅像素探测器，性能达到国际先进水平



HEPS-BPIX	
Process	130 nm
Pixel size	150 × 150 μm <sup>2</sup> 55 × 55 μm <sup>2</sup> BPIX4
Array size	208 × 288
Energy range	8-20keV
Frame rate	1KHz



Block diagram of the HEPS-BPIX pixel cell



工程批晶圆

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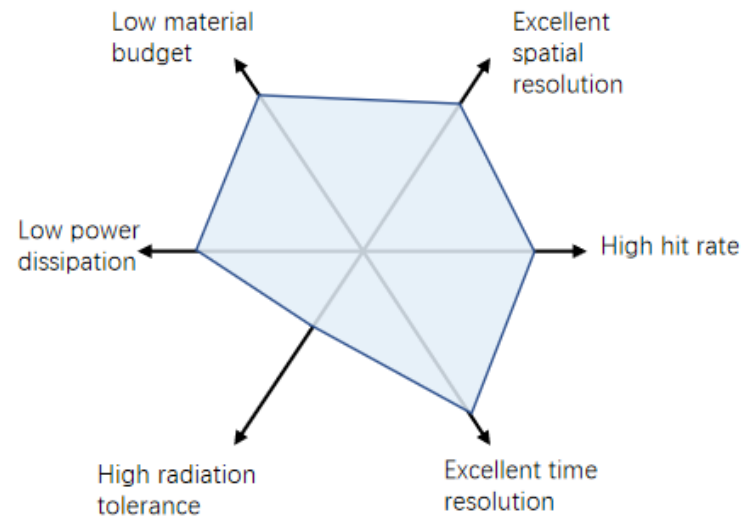
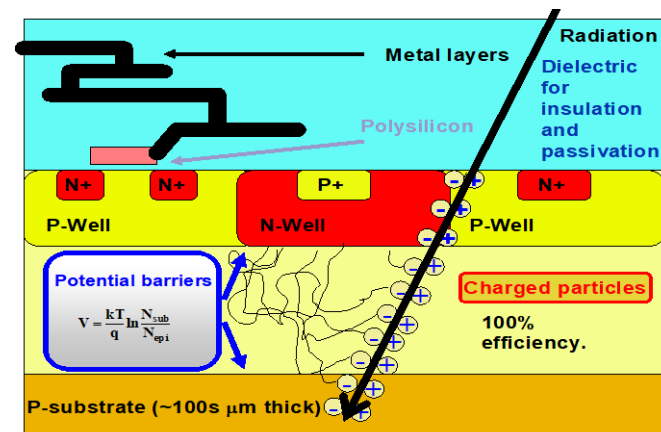
# 单片式像素探测器 (Monolithic Active Pixel Sensor, MAPS)

## □ 最初想法: Sensor和ASIC集成在同一块衬底上

- ❖ 电荷在外延层 (Epitaxial layer) 产生, 低掺杂, 厚度10~15  $\mu\text{m}$
- ❖ 电荷通过热扩散被N-well/P-epi二极管收集

## □ 优点

- ❖ 高空间分辨
  - ✓ 像素尺寸小,  $\sim 10 \mu\text{m} \times 10 \mu\text{m}$
- ❖ 低物质质量
  - ✓ 可减薄至50  $\mu\text{m}$
  - ✓ 功耗低
- ❖ 高计数率
- ❖ 较好的抗辐照能力
- ❖ 采用商业化CMOS工艺
  - ✓ 集成度高、成本低、室温下工作、研发周期短



# 单片式像素探测器 (state-of-the-art)

Chip	Process	Pixel array	Pixel size	Main Institute	Target	Comment
MIMOSA28	350 nm OPTO	928 × 960	20.7 × 20.7 $\mu\text{m}^2$	IPHC	rad. hard	STAR
WCPS	350 nm OPTO	644 × 3600	30 × 120/160/200 $\mu\text{m}^2$	SDU/IHEP/HIT	low material budget	Stitching
ALPIDE	TJ 180 nm	512 × 1024	28 × 28 $\mu\text{m}^2$	CERN	high granularity	ALICE ITS
MIMOSIS	TJ 180 nm	504 × 1024	30.24 × 26.88 $\mu\text{m}^2$	IPHC	rad. hard high granularity	CBM Micro-Vertex
MALTA	TJ 180 nm	224 × 512	36.4 × 36.4 $\mu\text{m}^2$	CERN	high granularity	HL-LHC
TJ-Monopix2	TJ 180 nm	512 × 512	33.04 × 33.04 $\mu\text{m}^2$	CERN/Bonn	rad. hard	HL-LHC
TaichuPix	TJ 180 nm	512 × 1024	25 × 25 $\mu\text{m}^2$	IHEP/IFAE/CCNU/SDU/NWPU/NJU	High granularity, rad. hard, fast readout	CEPC
MIC4	TJ 180 nm	128 × 64	25 × 25 $\mu\text{m}^2$	CCNU	Fast readout	CEPC
JadePix3	TJ 180 nm	192 × 512	16 × 26 $\mu\text{m}^2$ 16 × 23.11 $\mu\text{m}^2$	IHEP/CCNU/SDU	position resolution and low power	CEPC
Nupix-A1	130 nm	128 × 64	30 × 30 $\mu\text{m}^2$	IMP SLIMP	heavy-ion experiments	HIRFL & HIAF
ATLASpix3	AMS/TSI 180 nm	372 × 132	150 × 50 $\mu\text{m}^2$	KIT/CPPM	rad. hard	ATLAS
RD50-MPW3	150 nm HVCOMS	64 × 64	62 × 62 $\mu\text{m}^2$	RD50	rad. hard high granularity	HL-LHC FCC
MuPix10	TSI 180 nm	250 × 256	80 × 80 $\mu\text{m}^2$	University of Heidelberg	rad. hard	Mu3e
LF-Monopix2	LF 150 nm	340 × 56	50 × 150 $\mu\text{m}^2$	Bonn	rad. hard	HL-LHC
MightyPix1	TSI 180 nm	320 × 29	165 × 55 $\mu\text{m}^2$	University of Liverpool	rad. hard	LHCb upgrade
SOFIST	SOI 200 nm	128 × 128	36 × 36 $\mu\text{m}^2$	KEK	high granularity, fast readout	ILC
CPV-4	SOI 180 nm	128 × 128	21.04 × 17.24 $\mu\text{m}^2$	IHEP	high granularity	CEPC

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双阱工艺

四阱工艺

高压工艺

SOI工艺

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# 单片式像素探测器

## 双阱CIS工艺 (350 nm)

### □ 高阻外延层

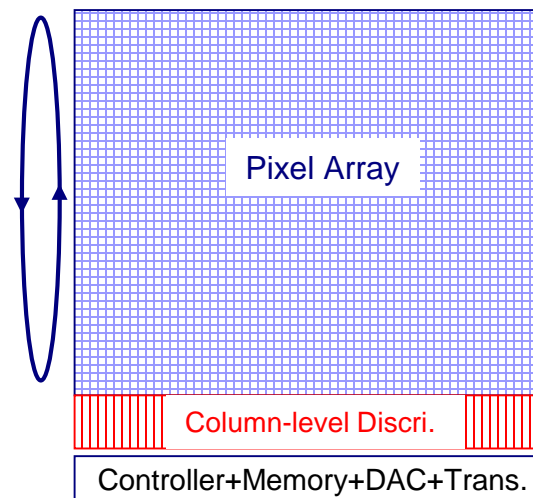
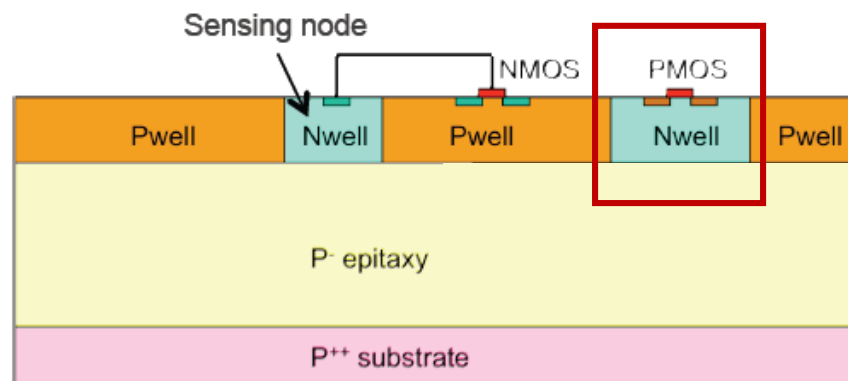
### □ Nwell和Pwell

- ❖ 由于电荷竞争，像素内不能使用PMOS晶体管
- ❖ 像素内不能使用数字逻辑
  - ✓ 不能使用数据驱动(data driven)等高速读出模式，读出速度受限
  - ✓ 一般采用逐行扫描读出模式

### □ 4层金属

- ❖ 版图布局受限，电路面积较大

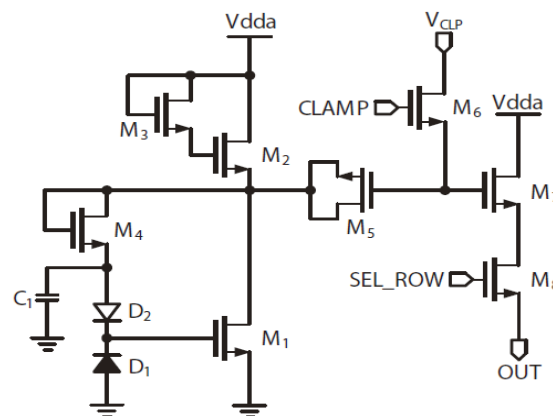
### □ 研发成本低



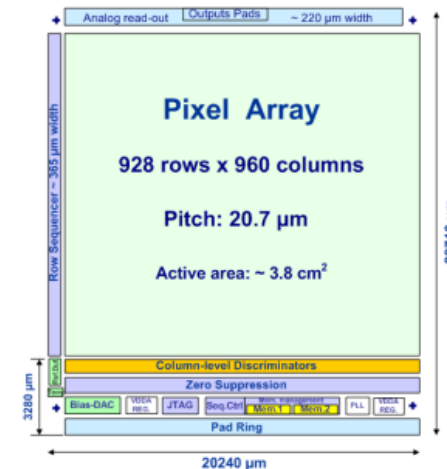
# 单片式像素探测器

## MIMOSA-28 (IPHC)

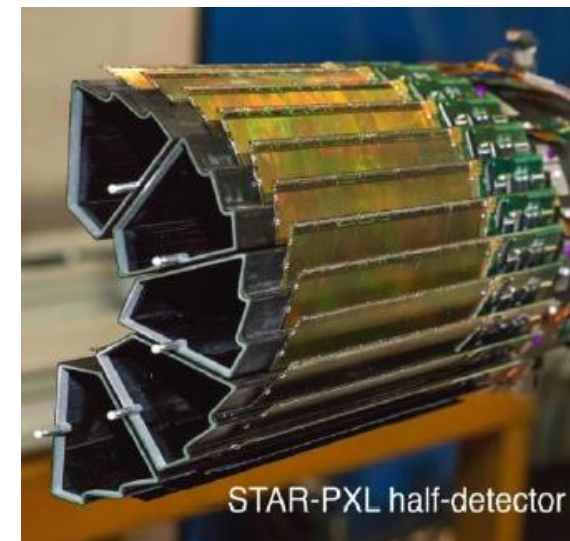
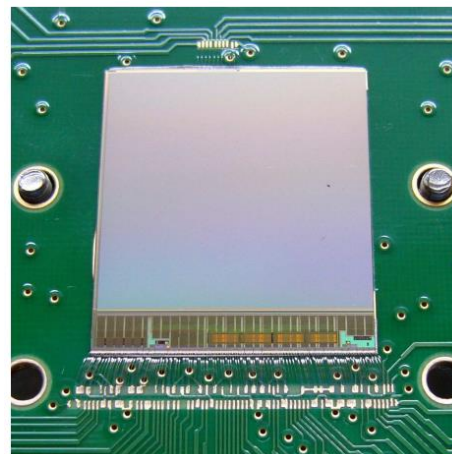
- 应用于相对论重离子对撞机STAR实验PXL
- 逐行扫描读出模式，像素内集成放大器、CDS
- 片上集成列级甄别、消零逻辑、DAC偏置、I2C、PLL、LDO...
- 第一个应用于粒子物理实验的单片式像素探测器



像素电路



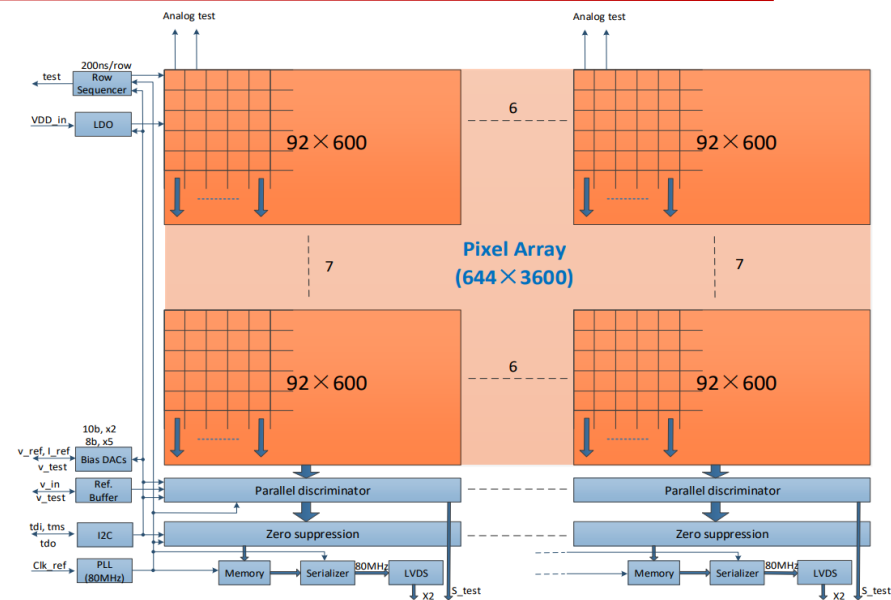
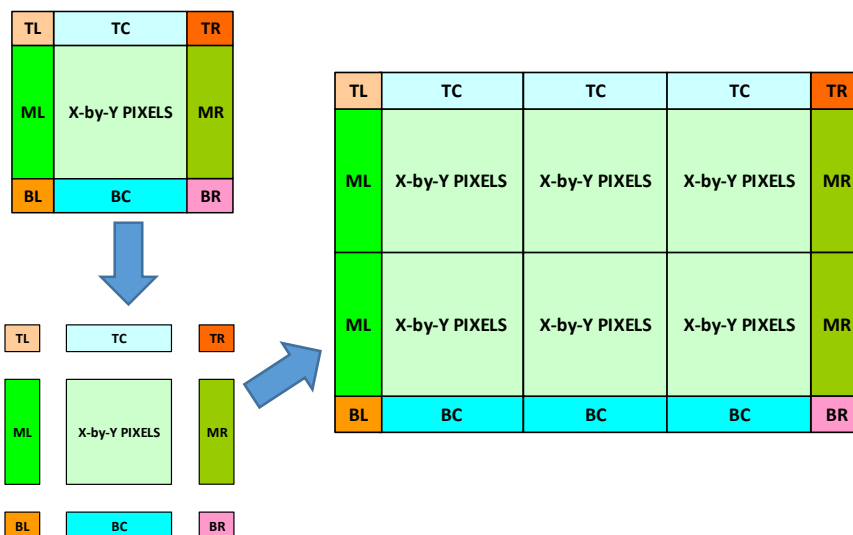
MIMOSA-28	
Process	350 nm OPTO
Pixel size	$20.7 \times 20.7 \mu m^2$
Array size	928 × 960
Chip size	$20.2 \times 22.7 mm^2$
Power	$150 mW/cm^2$
Active area	$19.9 \times 19.2 mm^2$
Spatial resolution	$10 \mu m$
Readout time	$186.5 \mu s$



# 单片式像素探测器

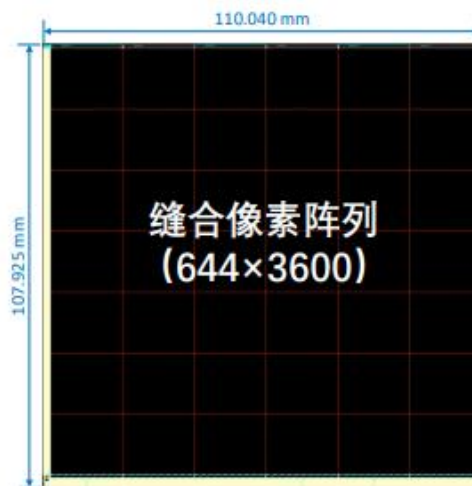
## WCPS (SDU/IHEP/HIT)

- ❑ 晶圆级芯片、减薄后自卷曲，极低物质质量
- ❑ 逐行扫描读出结构
- ❑ 全功能芯片，像素内集成放大器和CDS，片内集成列级甄别、消零逻辑、DAC偏置、I2C、PLL、LDO...

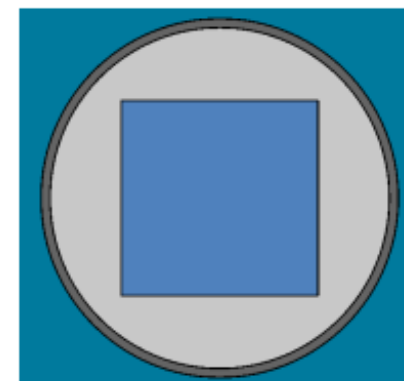


Block diagram of the Stitching architecture

MuPix10	
Process	350 nm OPTO
Pixel size	$30 \times 120/160/200 \mu m^2$
Array size	$644 \times 3600$
Integration time	129 $\mu s$
Chip size	$11 \times 11 cm^2$



Pixel array



Chip on a 8-inch wafer



# 目录

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- 背景介绍
- 混合式像素探测器
- 单片式像素探测器
  - ❖ 双阱CIS工艺
  - ❖ 四阱CIS工艺
  - ❖ 高压CMOS工艺
  - ❖ SOI工艺
- 总结

# 单片式像素探测器

## 四阱CIS工艺 (TJ 180/65 nm; 华力55 nm)

### □ Nwell, Pwell, deep-Nwell, deep-Pwell

- ❖ 像素内能使用PMOS晶体管，实现复杂CMOS电路
- ❖ 像素内能使用数字逻辑，实现数据驱动等高速读出模式

### □ 6层金属

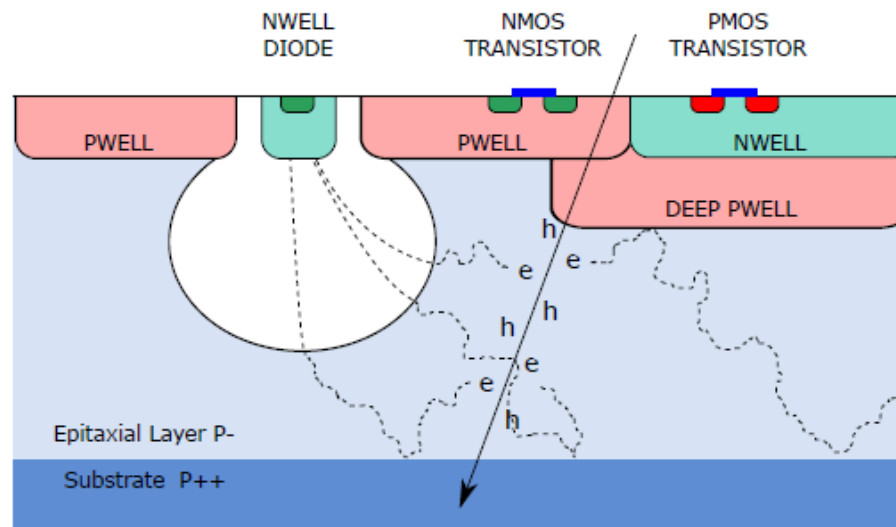
- ❖ 面积较小，减小死区

### □ 供电电压更小

- ❖ 功耗低

### □ 栅氧化层更薄

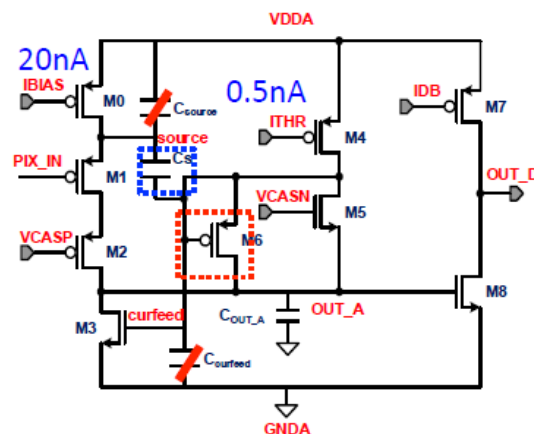
- ❖ 提高抗辐照能力



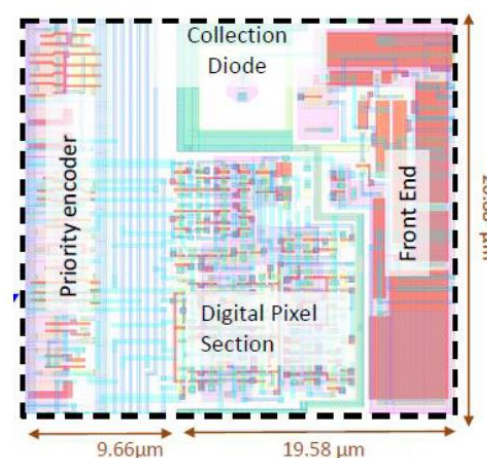
# 单片式像素探测器

## ALPIDE (CERN)

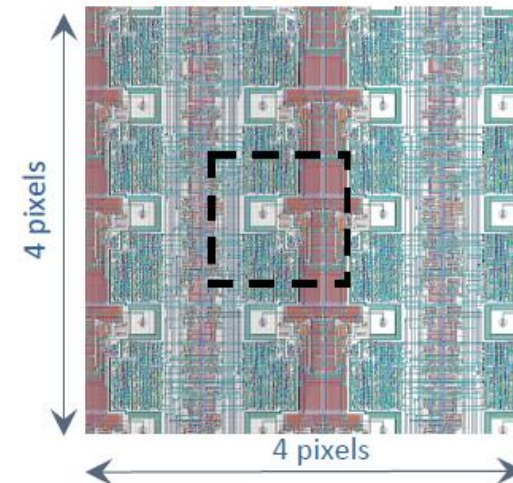
- ❑ LHC ALICE实验升级 (ITS2)
- ❑ 像素内集成模拟前端、AERD优先编码逻辑、数字控制单元
- ❑ 模拟前端完成放大和甄别, 静态功耗40 nW
- ❑ 第一个采用全局读出模式的MAPS



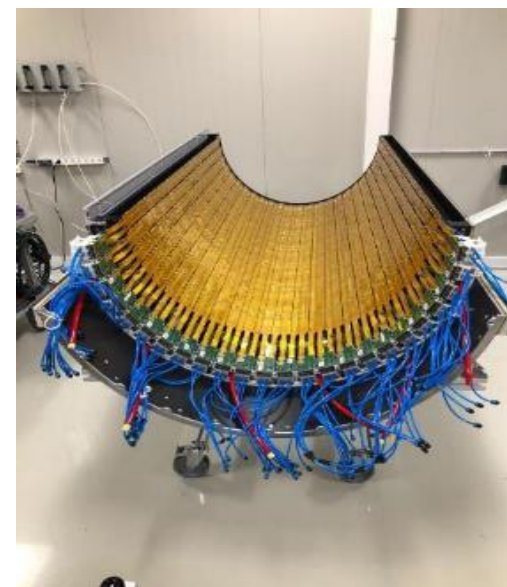
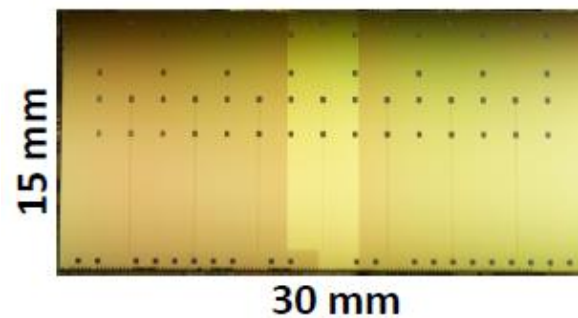
Pixel Layout



Matrix layout



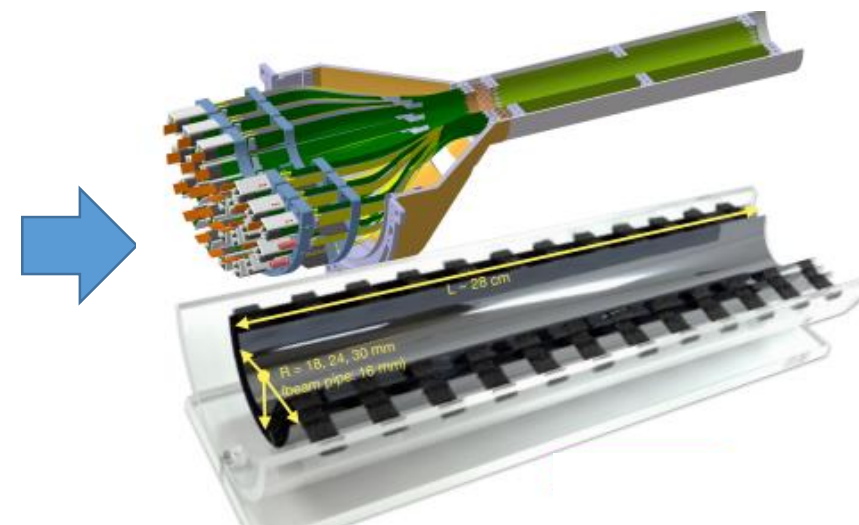
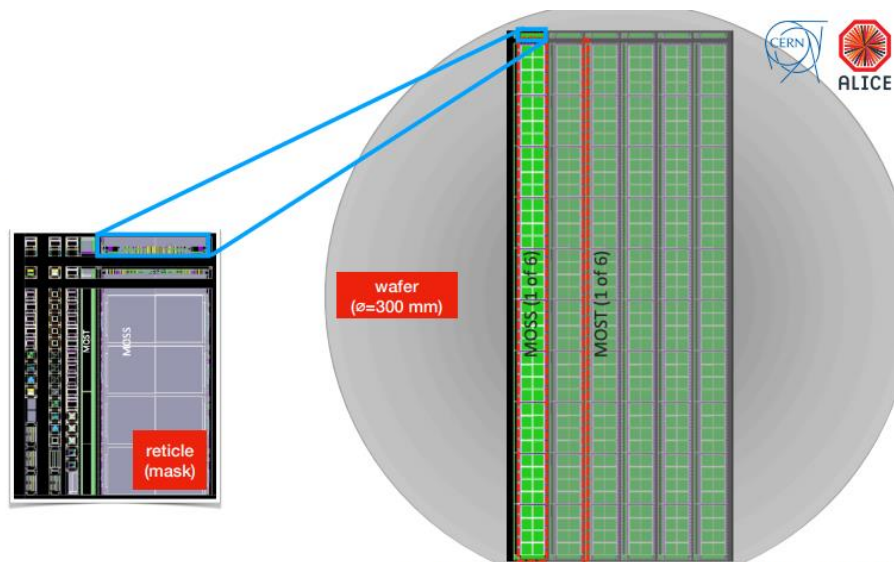
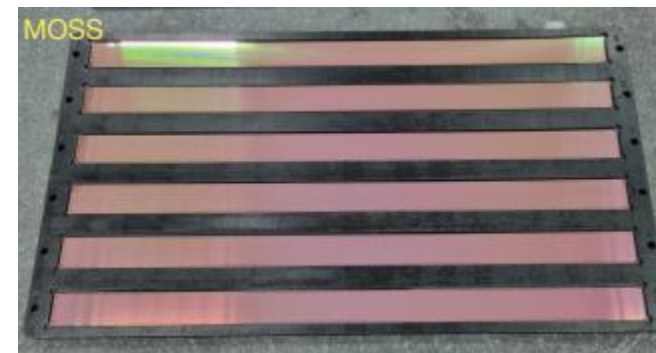
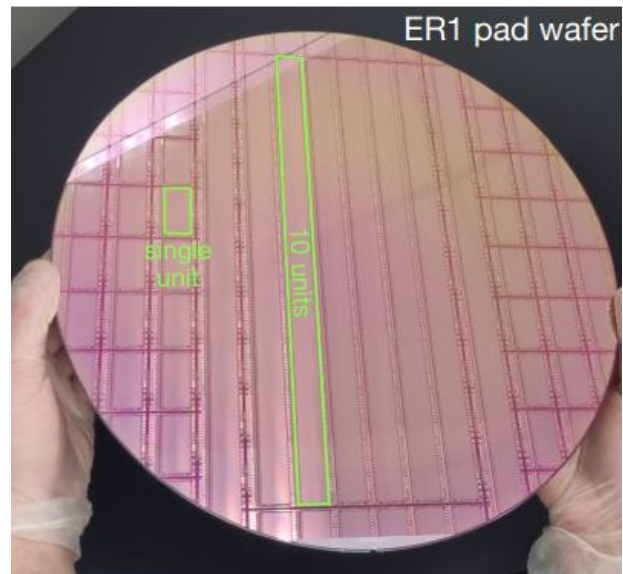
ALPIDE	
Process	TJ 180 nm
Pixel size	$28 \times 28 \mu m^2$
Array size	$512 \times 1024$
Spatial resolution	$5 \mu m$
Power	$< 40 mW/cm^2$
TID	$> 2.7 Mrad$
Hit rate	$100 MHz/cm^2$



# 单片式像素探测器

## ER1 (Engineering run, CERN)

- ❑ 65 nm stitching technology
- ❑ “MOSS”: 14 x 259 mm, 6.72 Mpixel (22.5 x 22.5 and 18 x 18  $\mu\text{m}^2$ )
  - ❖ conservative design, different pitches
- ❑ “MOST”: 2.5 x 259 mm, 0.9 Mpixel (18 x 18  $\mu\text{m}^2$ )
  - ❖ more dense design



# 单片式像素探测器

## MIMOSIS-1 (IPHC)

- ❑ 面向CBM-MVD
- ❑ 像素甄别电路基于ALPIDE结构
- ❑ 高阻外延层
- ❑ 像素内集成数据驱动和缓存

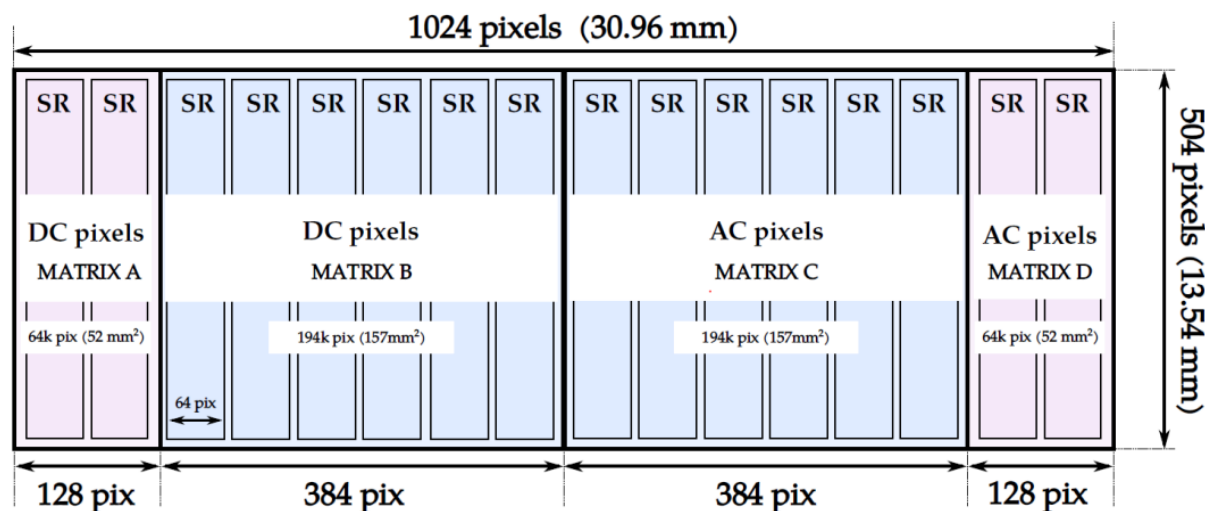


Layout of the MIMOSIS-1



MIMOSIS-1

MIMOSIS-1	
Process	TJ 180 nm
Pixel size	$30.24 \times 26.88 \mu\text{m}^2$
Array size	$504 \times 1024$
Chip size	$3.1 \times 1.7 \text{ cm}^2$
Power	$50 \text{ mW/cm}^2$
Active area	$4.2 \text{ cm}^2$
Frame time	$5 \mu\text{s}$



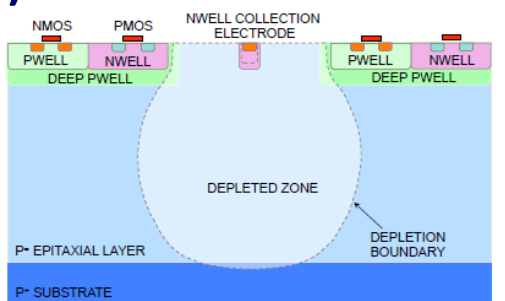
Functional description of the pixel array



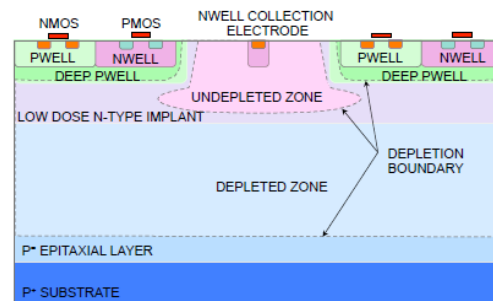
# 单片式像素探测器

## MALTA2 (CERN)

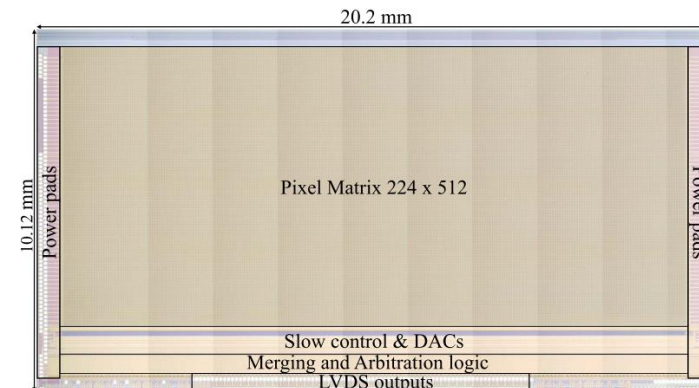
- ❑ LHC ATLAS内径迹室
- ❑ 优化前端电路设计
- ❑ 有效降低了1/f 噪声
- ❑ 更好的时间精度
- ❑ 异步读出结构 (速度更快)



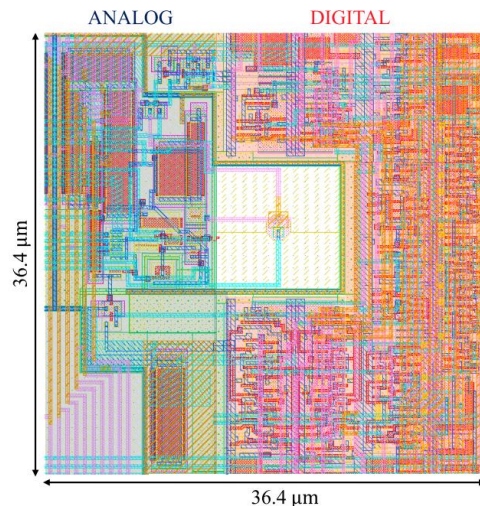
Standard, not fully depleted (ALPIDE)



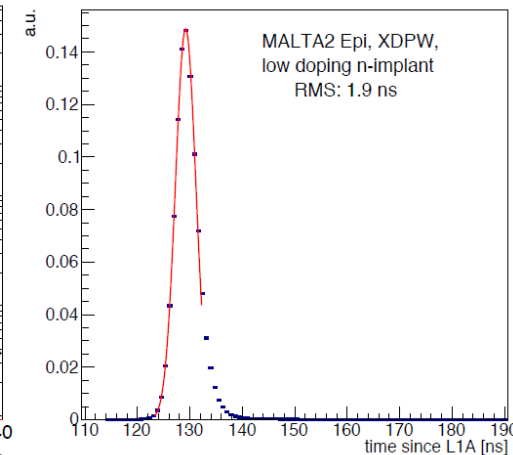
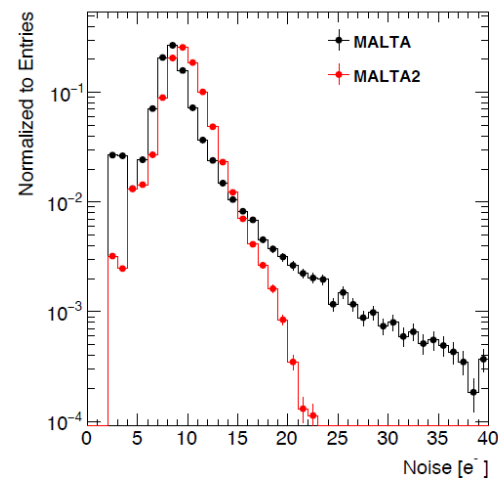
Not fully depleted at low reverse bias



MALTA2	
Process	Modified TJ 180 nm
Pixel size	$36.4 \times 36.4 \mu\text{m}^2$
Array size	$224 \times 512$
Chip size	$20.2 \times 10.12 \text{mm}^2$
Power	$75 \text{mW}/\text{cm}^2$
TID	100 Mrad
charge collection efficiency	97.5%



Layout of the pixel

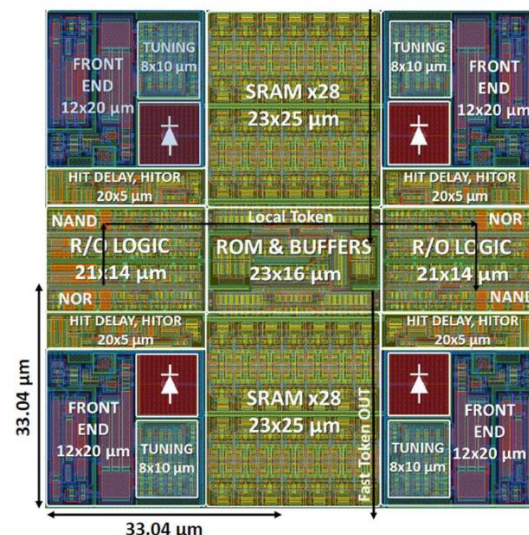


# 单片式像素探测器

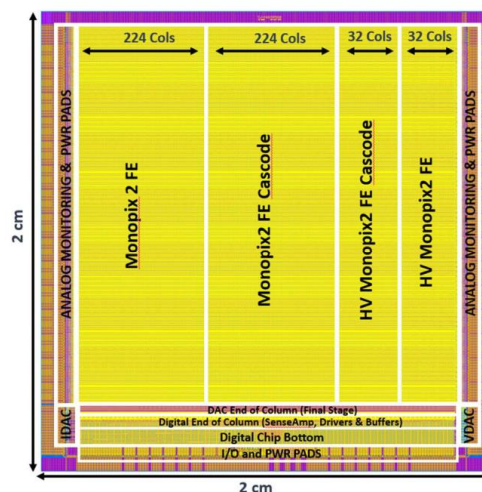
## TJ-Monopix2 (CERN/Bonn)

- ❑ 面向HL-LHC ATLAS 径迹室外层
- ❑ 采用修改的CIS工艺
- ❑ 优化了前端模拟电路：更高增益，更低噪声
- ❑ 列端同步读出结构，类似FE-I4读出结构

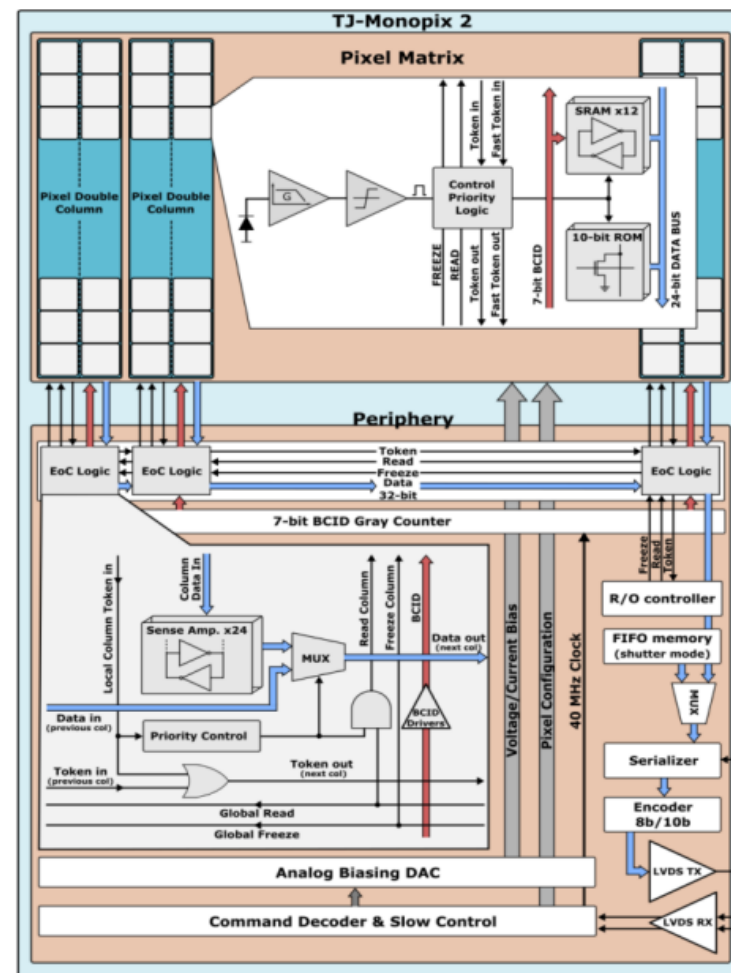
TJ-Monopix2	
Process	Modified TJ 180 nm
Pixel size	$33.04 \times 33.04 \mu\text{m}^2$
Array size	$512 \times 512$
Chip size	$20 \times 20 \text{mm}^2$
Noise	$< 10 \text{e}^-$
Time stamp	7-bit
Power	$170 \text{mW}/\text{cm}^2$



Layout of pixels



Layout of the TJ-Monopix



Block diagram of the TJ-Monopix-2 chip

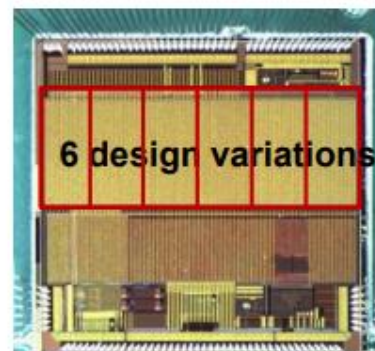
# 单片式像素探测器

## TaichuPix (IHEP/IFAE/CCNU/SDU/NWPU/NJU)

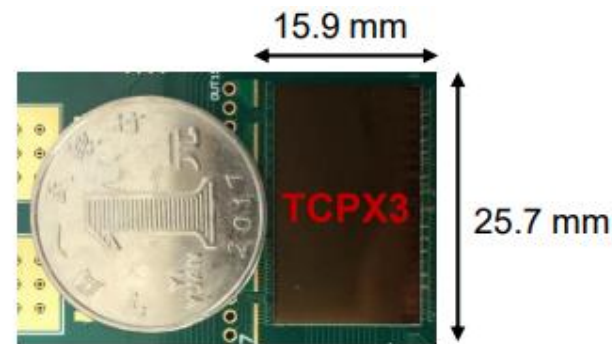
- 环形正负电子对撞机（CEPC）顶点探测器
- 像素阵列采用列读出方式：数据驱动读出，每列加入时间戳，读出时间50 ns
- 2级FIFO结构
- Trigger-less (3.84 Gbps) & Trigger mode



TaichuPix-1

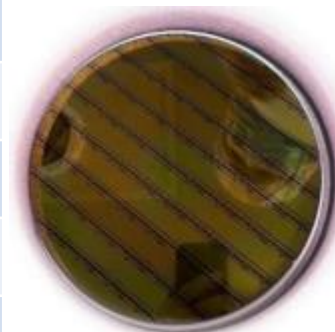


TaichuPix-2

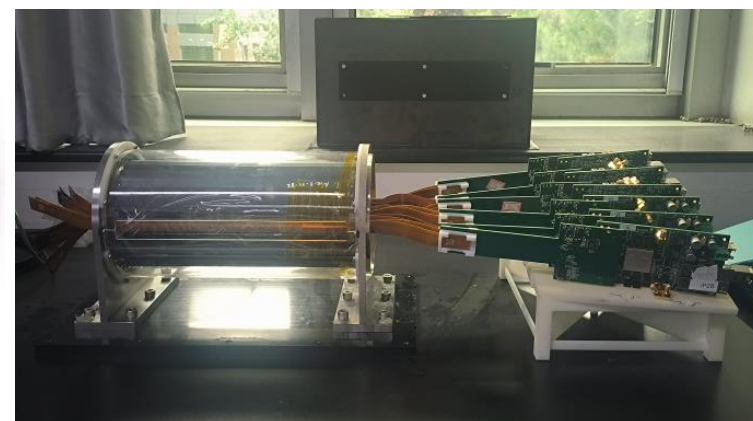


TaichuPix-3  
Pixel size:  $25\ \mu\text{m} \times 25\ \mu\text{m}$

	TaichuPix-1	TaichuPix-2	TaichuPix-3
Process	TJ 180 nm CIS	TJ 180 nm CIS	TJ 180 nm CIS
Pixel size	$52 \times 25\ \mu\text{m}^2$	$25 \times 25/24\ \mu\text{m}^2$	$25 \times 25\ \mu\text{m}^2$
Array size	$64 \times 192$	$64 \times 192$	$512 \times 1024$
Chip size	$5 \times 5\ \text{mm}^2$	$5 \times 5\ \text{mm}^2$	$2.6 \times 1.6\ \text{cm}^2$
Power	$130\ \text{mW}/\text{cm}^2$	$50\text{-}140\ \text{mW}/\text{cm}^2$	$89\text{--}164\ \text{mW}/\text{cm}^2$
TID		$> 3\ \text{Mrad}$	
Spatial resolution		$< 5\ \mu\text{m}$	



8-inch wafer

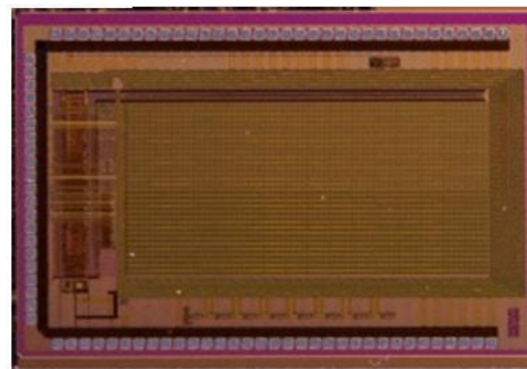
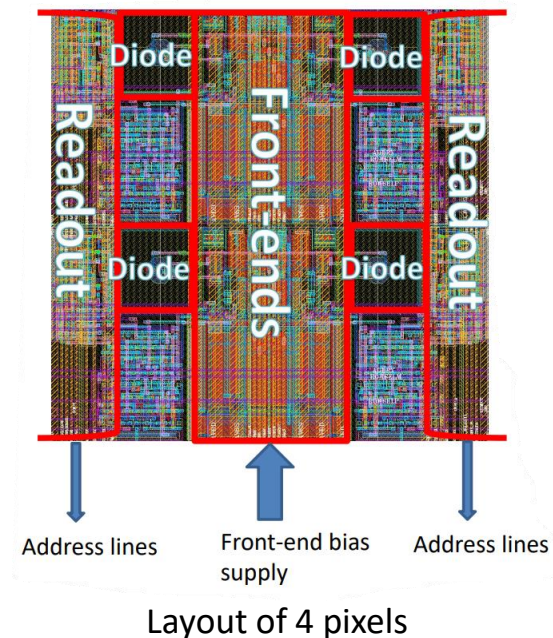


# 单片式像素探测器

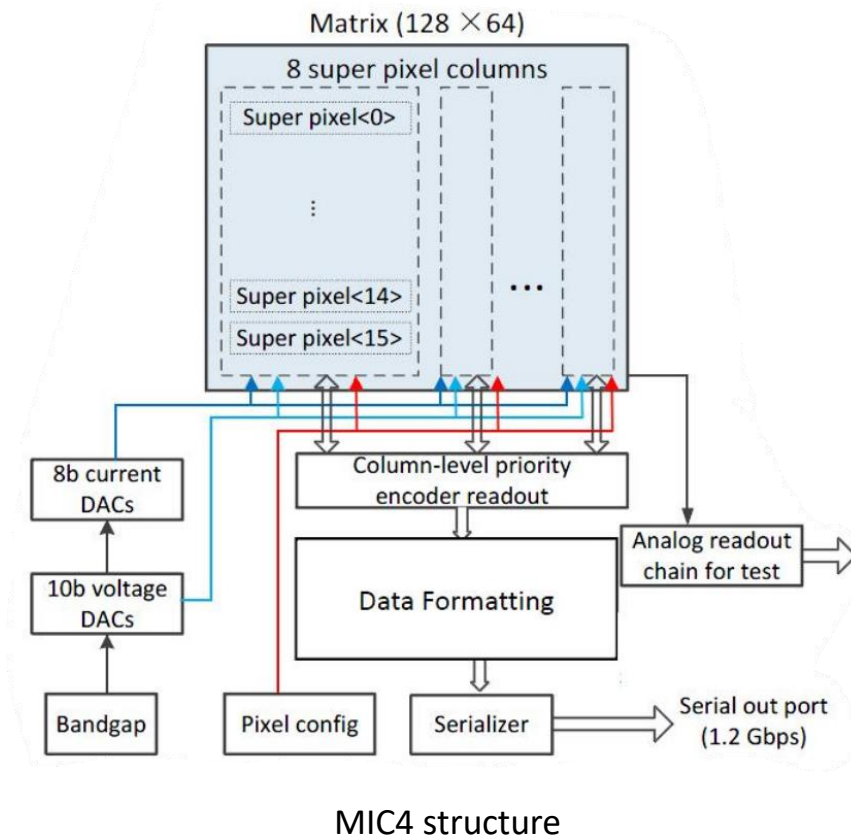
## MIC4 (CCNU/IHEP)

- ❑ CEPC顶点探测器
- ❑ 前端电路基于ALPIDE, 优化了数据驱动结构
- ❑ 测试ENC  $\sim 32 e^-$ , 模拟功耗 $\sim 0.11 \mu W/\text{pixel}$
- ❑ 快速读出( $\sim 3 \mu s$ )
- ❑ 小像素尺寸

MIC4	
Process	TJ 180nm
Pixel size	$25 \times 25 \mu m^2$
Array size	$128 \times 64$
Chip size	$3.2 \times 3.7 mm^2$
Power	$150 mW/cm^2$
Output rate	1.2Gbps



Layout of MIC4



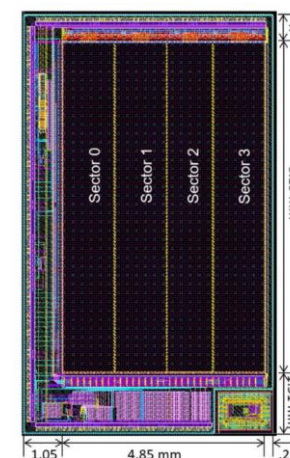
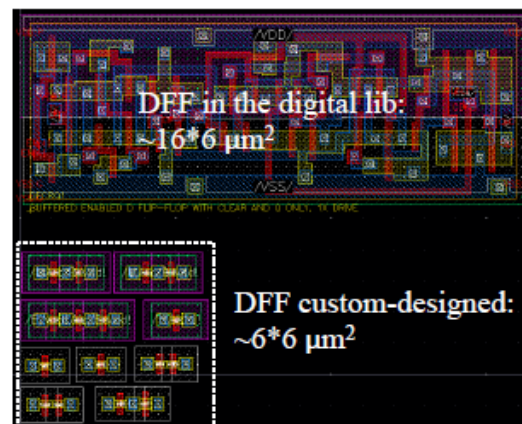
# 单片式像素探测器

## JadePix3 (IHEP/CCNU/SDU)

- ❑ CEPC顶点探测器
- ❑ 小像素尺寸、高空间分辨率、低功耗
- ❑ 基于MIC4的低功耗前端电路
- ❑ 逐行扫描读出方式
- ❑ 定制设计DFF，版图面积降低60%
- ❑ JadePix4/MIC5：快读出、低功耗

JadePix3	
Process	TJ 180nm CIS
Pixel size	$16 \times 26/23.11 \mu\text{m}^2$
Array size	$192 \times 512$
Chip size	$6.1 \times 10.4 \text{mm}^2$
Power	$87 \text{mW}/\text{cm}^2$
Active area	$4.85 \times 8.19 \text{mm}^2$
Spatial resol.	$3 \mu\text{m}$
Time resol.	$98.3 \mu\text{s}$

	JadePix1 2015	JadePix2 2017	MIC4	JadePix3 2019
Architecture	Roll. Shutter + Analog output	Roll. Shutter + In pixel discri.	Data-driven r.o. + In pixel discri.	Roll. shutter + end of col. priority encoder
Pitch ( $\mu\text{m}^2$ )	$33 \times 33 / 16 \times 16$	$22 \times 22$	$25 \times 25$	$16 \times 26 / 16 \times 23.11$
Power con. ( $\text{mW}/\text{cm}^2$ )	--	--	150	$\sim 55^*$
Integration time ( $\mu\text{s}$ )*	--	40-50	$\sim 3$	$\sim 100$
Prototype size ( $\text{mm}^2$ )	$3.9 \times 7.9$ (36 individual r.o)	$3 \times 3.3$	$3.1 \times 4.6$	$10.4 \times 6.1$
Main goals	Sensor optimization	Small binary pixel	Small pixel + Fast readout+ nearly full functional	Smaller pixel + Low power + fully functional



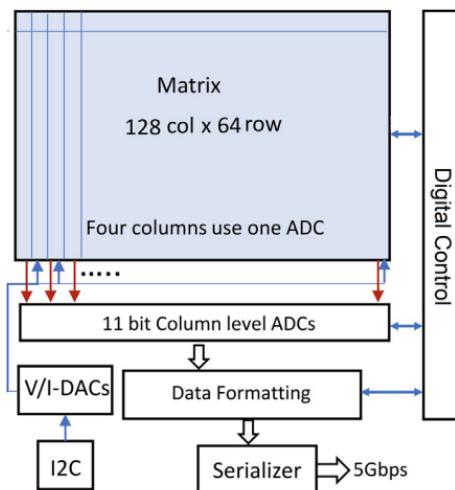
Layout of the JadePix-3

# 单片式像素探测器

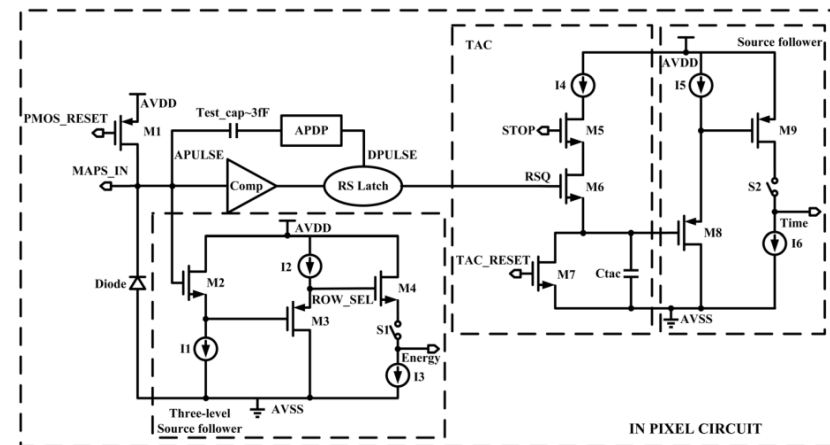
## Nupix-A1 (IMP/CCNU)

- ❑ 面向电子离子对撞机探测器 (EIC)
- ❑ 位置、时间和能量测量
- ❑ 像素内集成放大、甄别器
- ❑ 芯片集成高精度列级ADC、DAC偏置
- ❑ 高速数据传输

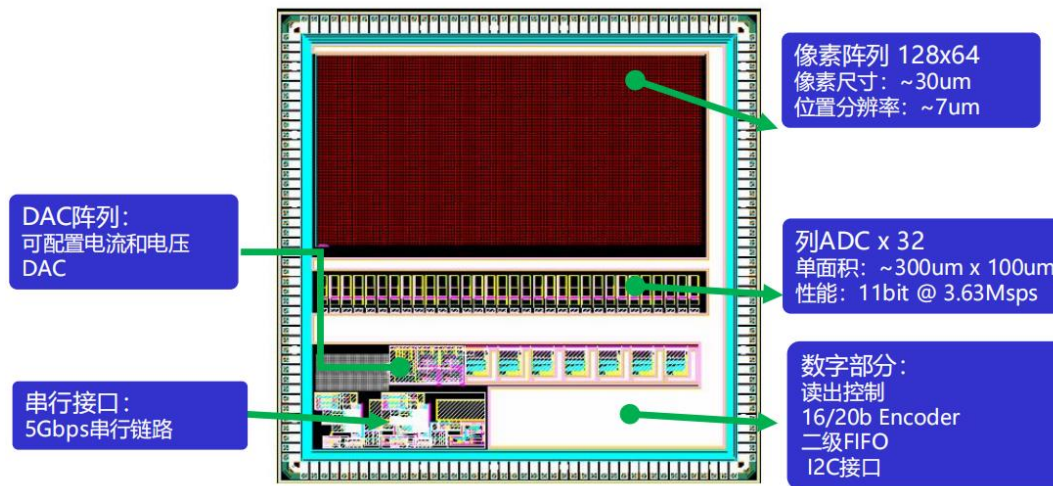
Nupix-A1	
Process	130 nm
Pixel size	$30 \times 30 \mu m^2$
Array size	$64 \times 128$
Speed	$8 \mu s/row$
Power	$300 mW/cm^2$
Output rate	5Gbps



Structure of the Nupix-A1



Structure of the in-pixel circuit



Layout of the Nupix-A1

- 背景介绍
- 混合式像素探测器
- **单片式像素探测器**
  - ❖ 双阱CIS工艺
  - ❖ 四阱CIS工艺
  - ❖ **高压CMOS工艺**
  - ❖ SOI工艺
- 总结

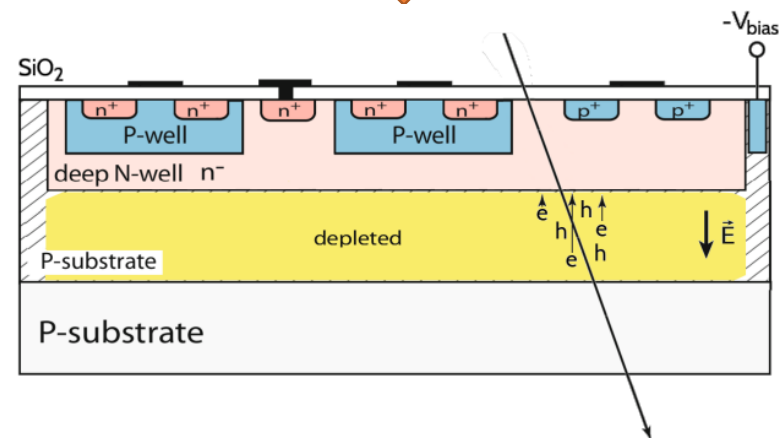
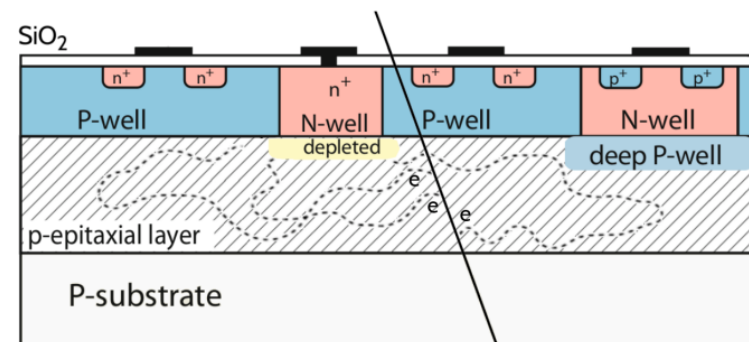
# 单片式像素探测器

## 标准CIS工艺

- ❑ 电荷收集采用热扩散方式，收集时间较长
- ❑ 抗辐照能力弱

## 高压CMOS工艺

- ❑ 全耗尽，电荷收集采用漂移方式，收集时间短
- ❑ 抗辐照能力强
- ❑ 像素尺寸大，减小像素阵列，降低功耗
- ❑ 具有CMOS工艺的优点

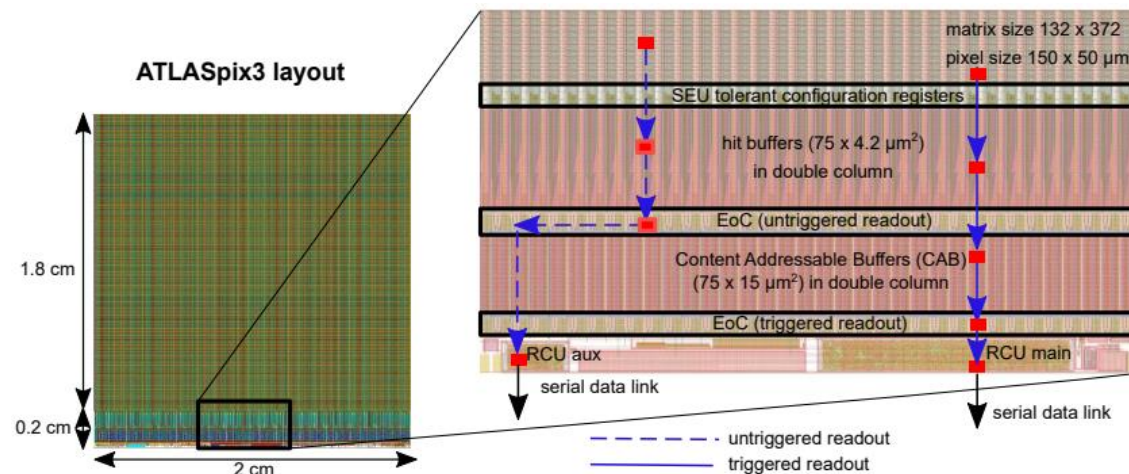




# 单片式像素探测器

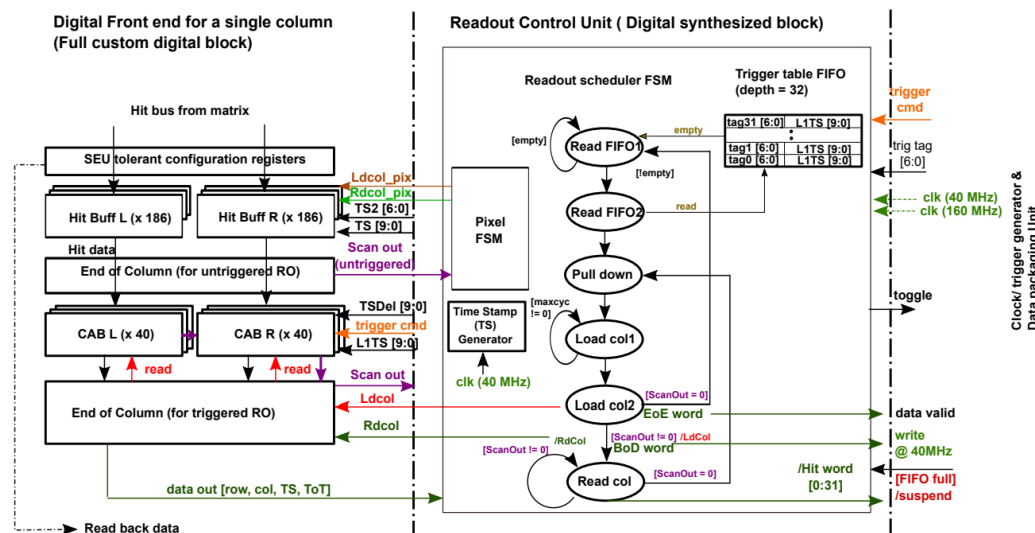
## ATLASpix3 (KIT/CERN)

- ❑ 面向ATLAS Inner Tracker
- ❑ 像素阵列采用列读出结构
- ❑ 存储单元采用抗辐照设计



Layout of the ATLASpix3

ATLASpix3	
Process	AMS/TSI 180nm
Pixel size	150 × 50μm <sup>2</sup>
Array size	132 × 372
Chip size	2.02 × 2.1cm <sup>2</sup>
Power	160 mW/cm <sup>2</sup>
Active area	90%

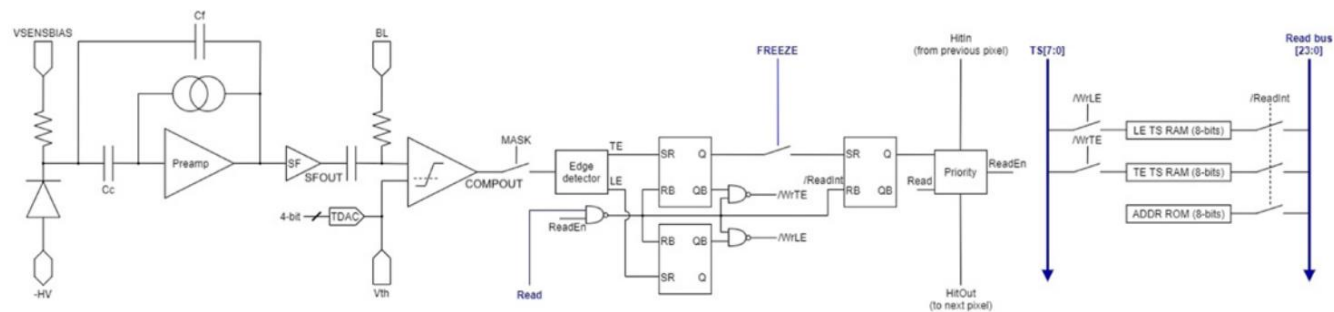


Block diagram of the readout periphery

# 单片式像素探测器

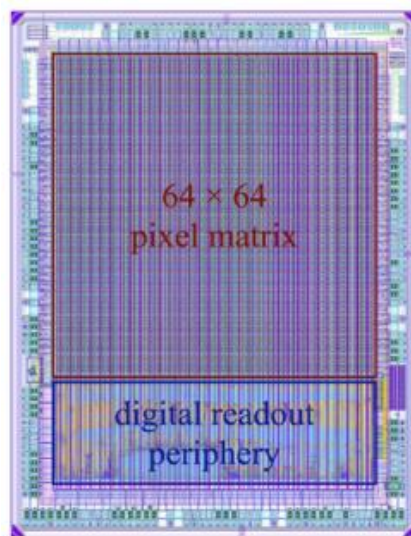
## RD50-MPW3

- 面向LHC、FCC相关实验
- 逐行扫描读出方式
- 采用双列读出架构
- 像素内电荷灵敏前置放大器，可调阈值比较器、锁存器

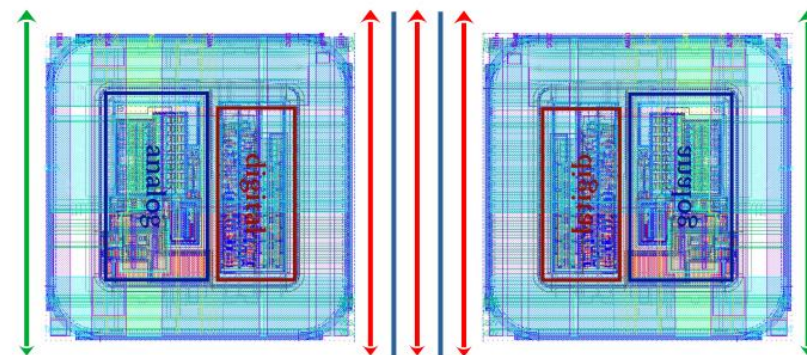


Block diagram of in-pixel electronics

RD50-MPW3	
Process	150 nm HVCMOS
Pixel size	$62 \times 62 \mu\text{m}^2$
Array size	$64 \times 64$
Chip size	$5.1 \times 6.0 \text{mm}^2$
Power	$23.4 \mu\text{W}/\text{pixel}$ $300 \text{mW}/\text{Digital periphery}$



Layout of RD50-MPW3



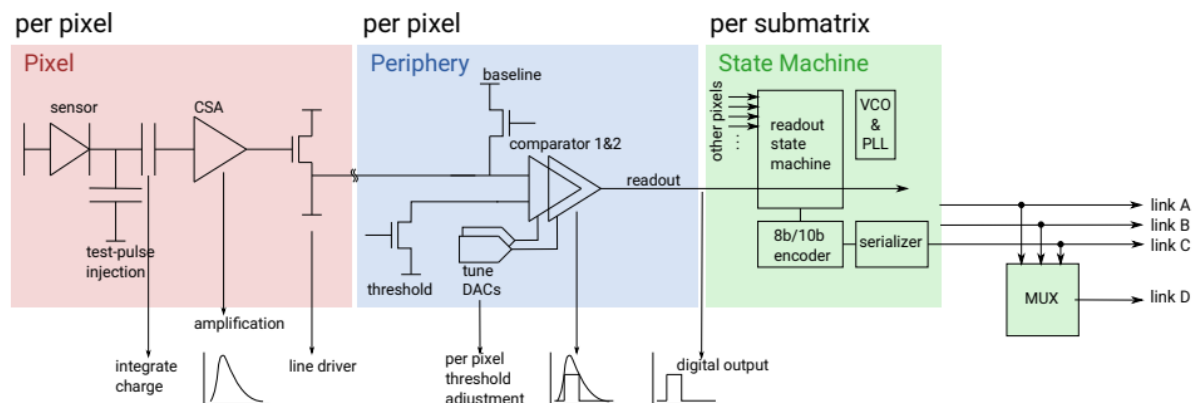
- ↔ Analog signal line
- ↔ Digital signal line
- Shielding line

Two pixels in a double column

# 单片式像素探测器

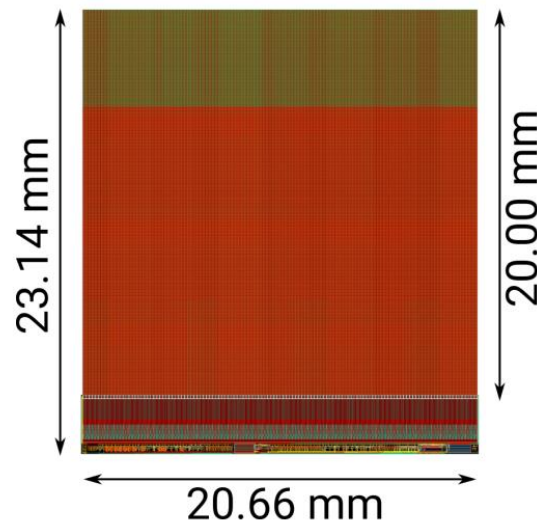
## MuPix10 (University of Heidelberg)

- 面向缪子衰变实验 ( Mu3e )
- 像素内集成CSA, 甄别器
- ToT技术

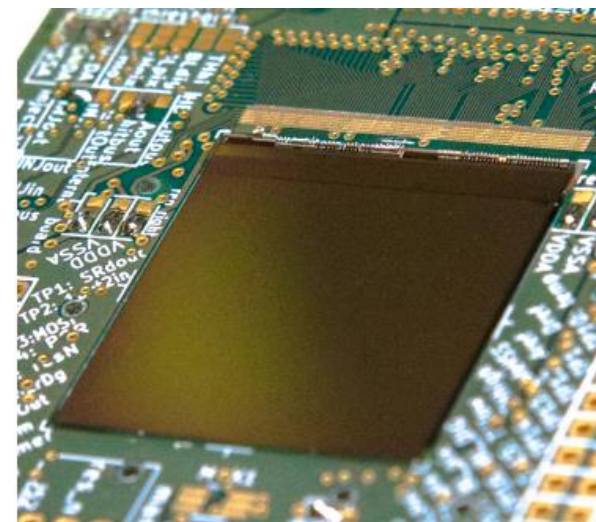


Block diagram of the MuPix10 architecture

MuPix10	
Process	180nm HVCMOS
Pixel size	$80 \times 80 \mu m^2$
Array size	$256 \times 250$
Chip size	$20.66 \times 23.14 mm^2$
Power	$190 mW/cm^2$
Active area	$20.48 \times 20 mm^2$
output rate	$1.6 Gbps \times 4$



Layout of MuPix10

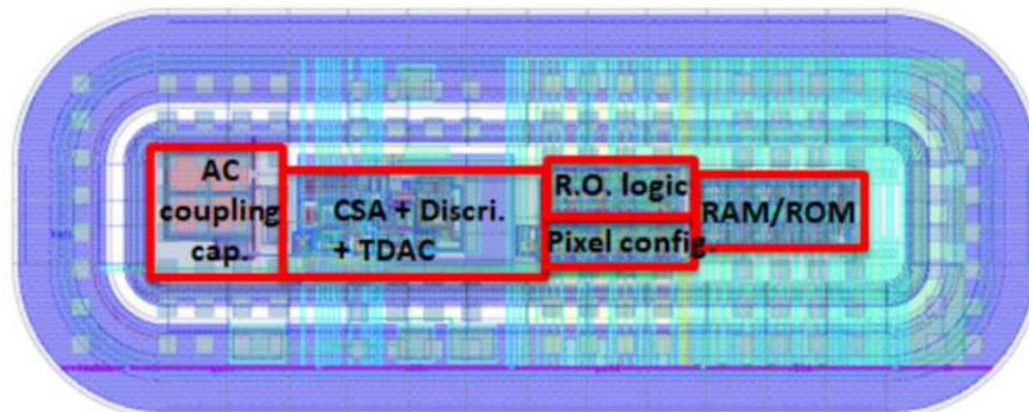


MuPix10 mounted on a PCB

# 单片式像素探测器

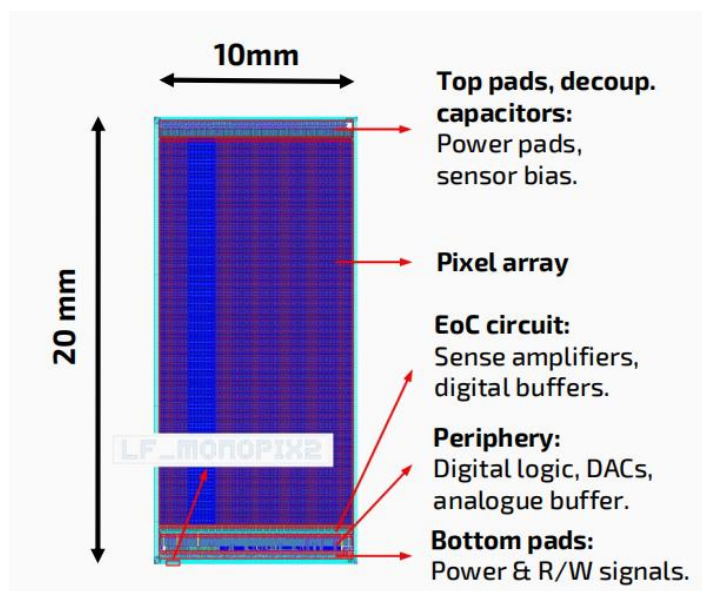
## LF-Monopix2

- ❑ 面向ATLAS实验
- ❑ 大面积(~cm<sup>2</sup>)，大收集电极（相比TJ-Monopix2）
- ❑ 像素阵列采用列读出结构
- ❑ 像素内集成CSA，甄别器，阈值调节DAC，数字逻辑，存储单元
- ❑ >2k Ohm 高阻衬底

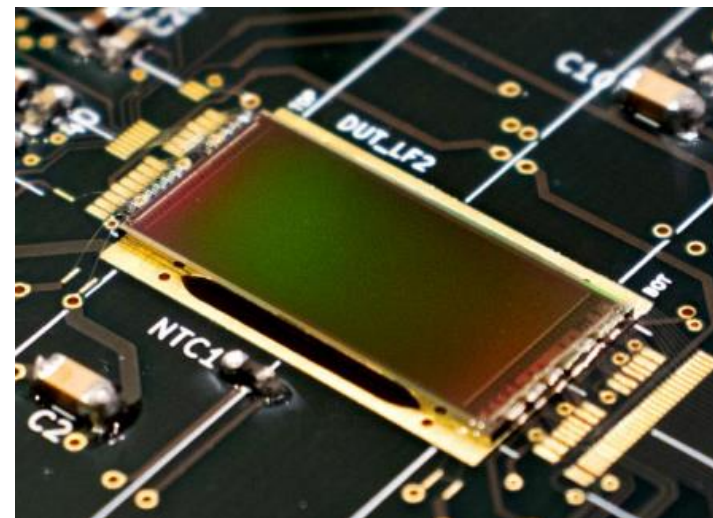


Layout of a pixel

LF-Monopix2	
Process	LF 150nm
Pixel size	150 × 50μm <sup>2</sup>
Array size	340 × 56
Chip size	10 × 20mm <sup>2</sup>
Power	30 μW/pixel
CMOS or LVDS serial output	40 MHz/160MHz



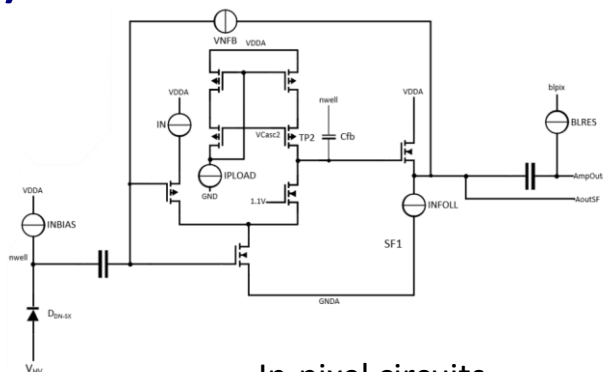
Layout of LF-Monopix2



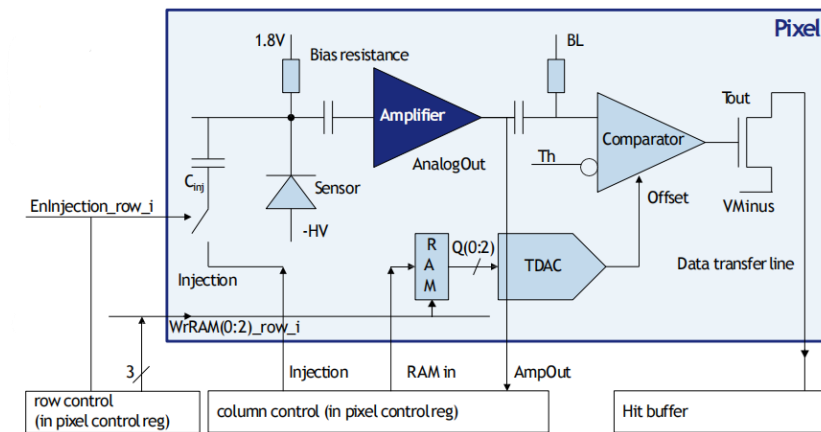
# 单片式像素探测器

## MightyPix1 (University of Liverpool)

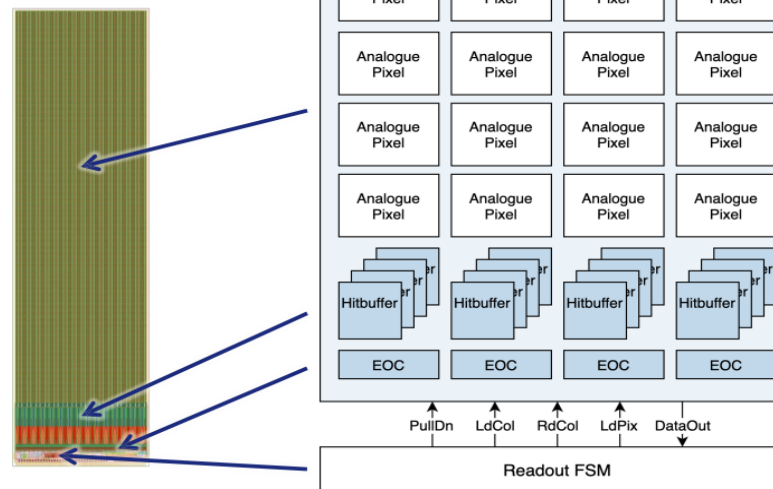
- 面向LHCb升级
- 芯片尺寸:  $\sim 2\text{ cm} \times 0.5\text{ cm}$   $\rightarrow$  全尺寸长,  $\frac{1}{4}$  宽
- 像素内集成CSA, 甄别器, 阈值调节DAC, 数字逻辑, 存储单元



In-pixel circuits



MightyPix1	
Process	TSI 180 nm HV-CMOS
Pixel size	$165 \times 55\mu\text{m}^2$
Array size	$320 \times 29$
Chip size	$5 \times 20\text{mm}^2$
Time walk	2.5 ns(2500 e- and 25000 e-)
Output rate	1.28 Gbps



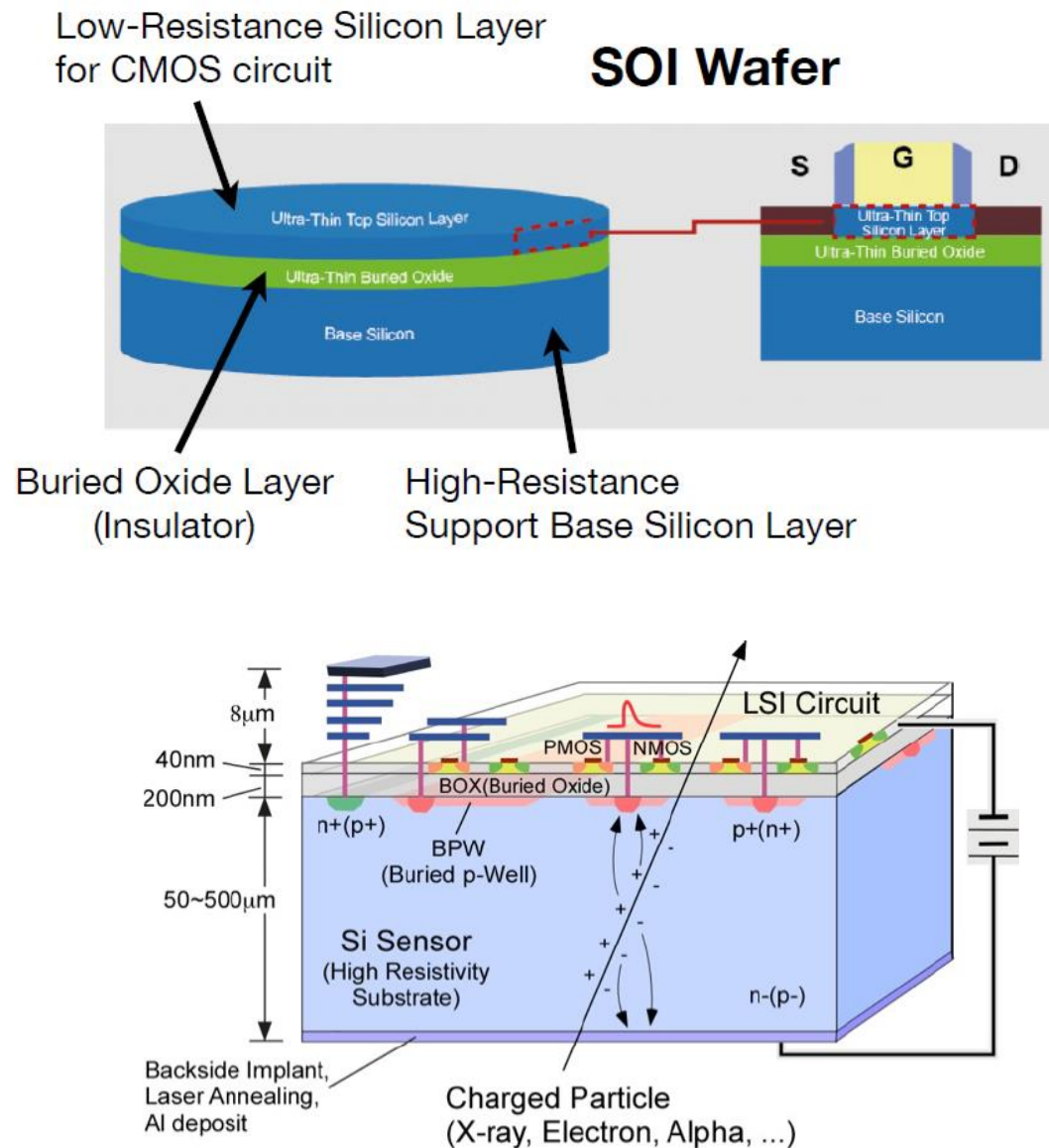
Block diagram of the MightyPix1

- 背景介绍
- 混合式像素探测器
- 单片式像素探测器
  - ❖ 双阱CIS工艺
  - ❖ 四阱CIS工艺
  - ❖ 高压CMOS工艺
  - ❖ **SOI工艺**
- 总结

# 单片式像素探测器

## SOI工艺

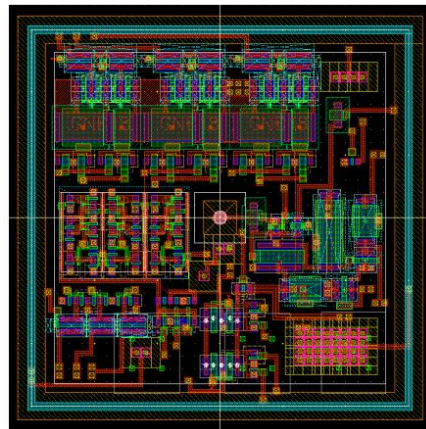
- ❑ Silicon-on-Insulator technology
- ❑ Utilize 0.2  $\mu\text{m}$  FD-SOI CMOS process by Lapis Semiconductor Co. Ltd.
- ❑ 单片式，能使用较小像素尺寸
- ❑ 极低的漏电流：低噪声、低功耗
- ❑ 全耗尽 (high basing voltage)
- ❑ 抗单粒子效应强
- ❑ Sensor thickness: 50 - 500  $\mu\text{m}$
- ❑ Sensor Resistivity: > 1  $\text{k}\Omega\cdot\text{cm}$
- ❑ 易于3D集成



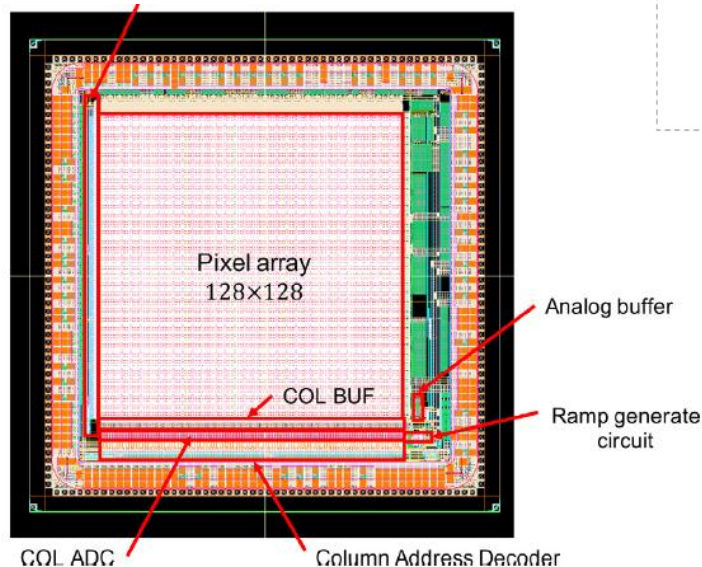
# 单片式像素探测器

## SOFIST3 (KEK)

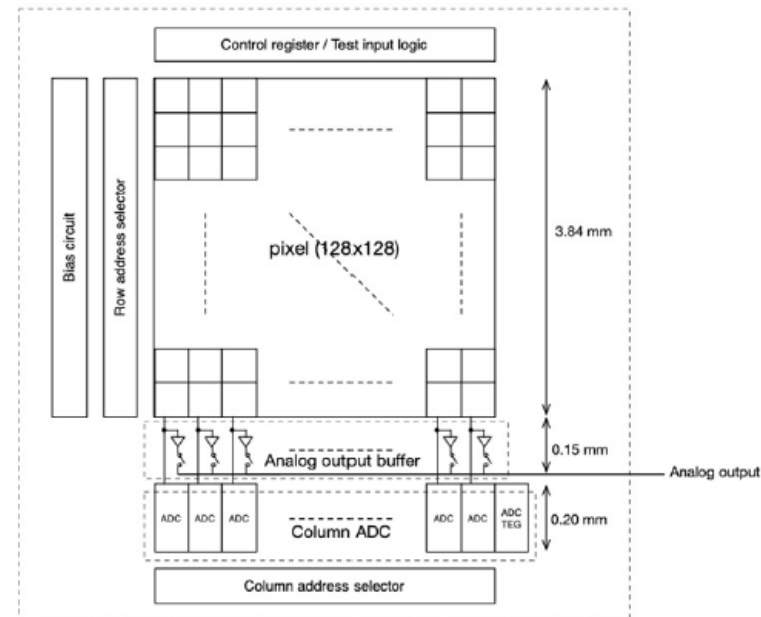
- 面向ILC顶点探测器
- 像素内集成CSA、甄别器、移位寄存器、模拟存储单元、时间戳
- 8-bit 列级ADC实现位置分辨



Pixel layout



Layout of SOFIST3



Block diagram of the circuits

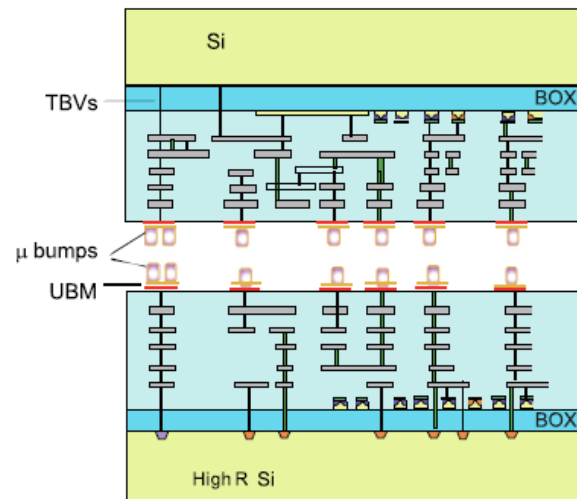
SOFIST3	
Process	SOI 200 nm
Pixel size	$30 \times 30 \mu\text{m}^2$
Array size	$128 \times 128$
Chip size	$6 \times 6 \text{mm}^2$
Time resolution	$1.92 \mu\text{s}$



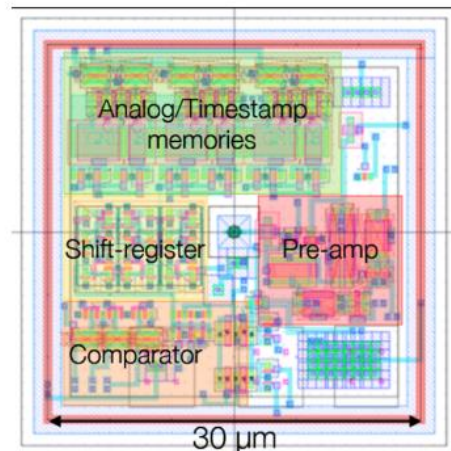
# 单片式像素探测器

## SOFIST4 (KEK)

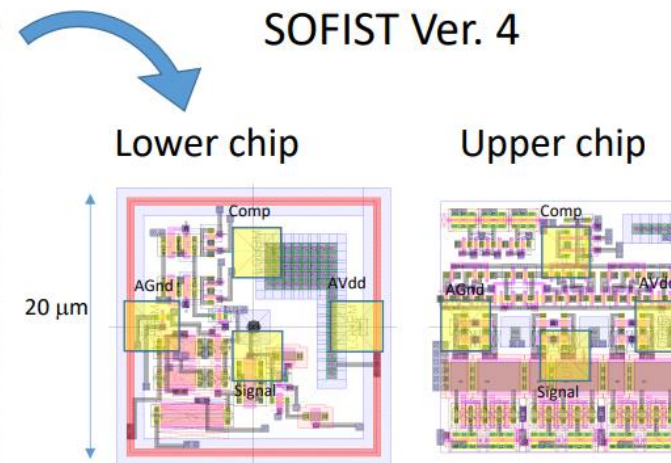
- ❑ 3D集成
- ❑ Micro bumps by T-Micro: 直径 $3\ \mu\text{m}$
- ❑ 像素尺寸更小
- ❑ 模拟电路和数字电路分开
- ❑ 同时获得时间分辨和位置分辨



## SOFIST Ver. 3

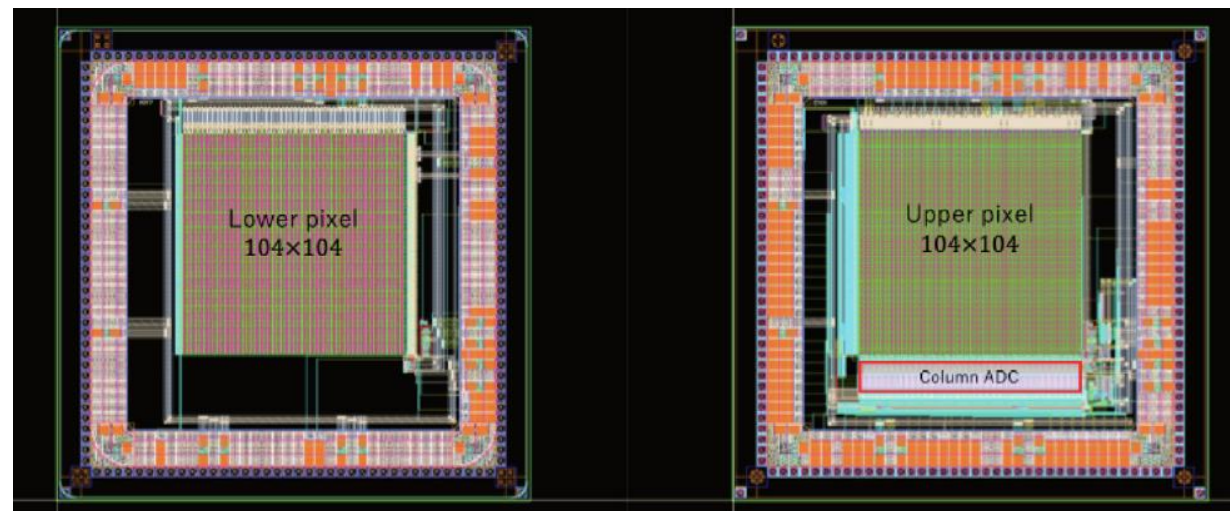


## SOFIST Ver. 4



## SOFIST4

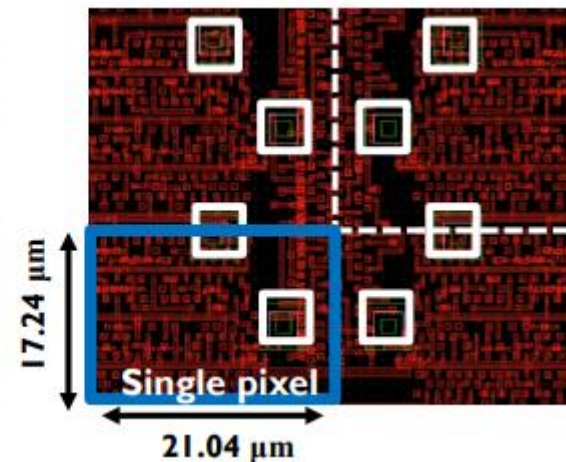
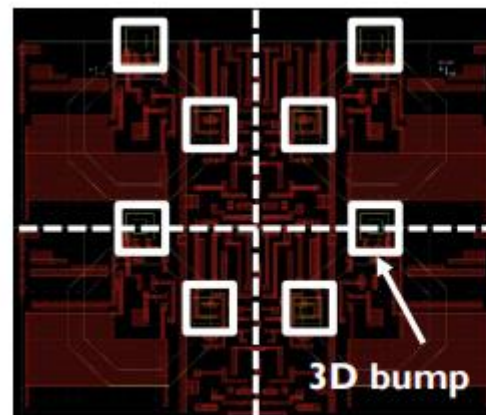
Process	SOI 200 nm
Pixel size	$20 \times 20\ \mu\text{m}^2$
Array size	$104 \times 104$
Chip size	$4.5 \times 4.5\ \text{mm}^2$
Bump connection yield	99.9%



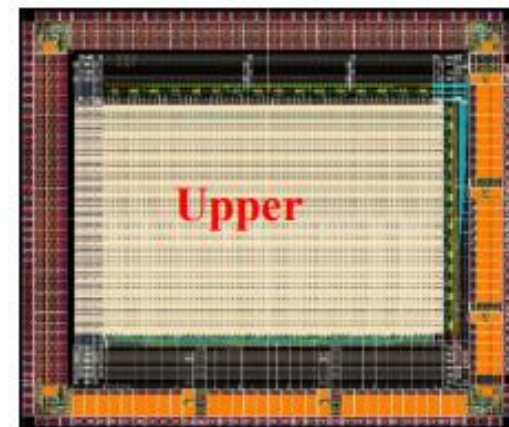
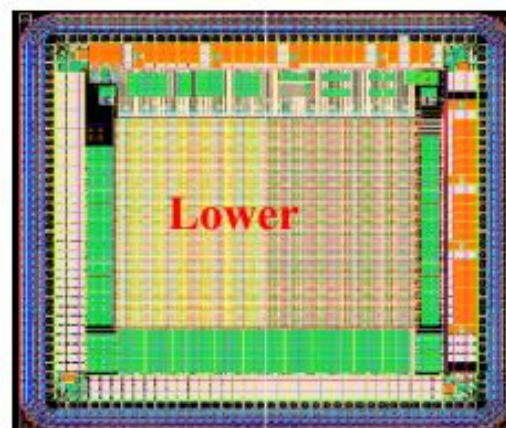
# 单片式像素探测器

## CPV4 (IHEP)

- ❑ 面向CEPC 顶点探测器
- ❑ 基于ALPIDE芯片的模拟前端设计和读出构架
- ❑ 比较器输出前沿定分辨率 $\sim 1\mu\text{s}$
- ❑ 下层模拟像素: 粒子击中信息转换为数字信号
- ❑ 上层数字像素: 击中触发器 + 控制寄存器
- ❑ 数据驱动读出结构, 异步优先级编码 AERD



CPV-4	
Process	200 nm
Pixel size	$21.04 \times 17.24\mu\text{m}^2$
Array size	$128 \times 128$
Chip size	$4.5 \times 4.5\text{mm}^2$
Time resolution	$\sim 1\mu\text{s}$ or $\sim 3\mu\text{s}$
Bias voltage	-200V



# 总结与展望

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- 在粒子物理实验中，硅像素探测器展现出的优异性能使其成为重要探测技术。
- 随着高能物理实验升级，对硅像素探测器提出了更高要求，高空间分辨、高速、抗辐照、低物质质量....
- 国外开展硅像素探测器的研究较早，大型粒子物理实验需求驱动，技术较成熟，已有应用于大型实验的芯片。
- 近十年来，国内已开展多种硅像素探测器的开发，掌握了研制关键技术，为应用于国内大型实验奠定基础。
- 硅像素探测器将呈现快速发展趋势，其不仅能用于粒子物理实验，而且能广泛应用于天体物理、X射线和中子成像、核物理等领域。

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# 谢谢!