环形正负电子对撞机
Circular Electron Positron Collider

# CEPC电子学机械接口需求及考虑


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**On behalf of the Elec-TDAQ system of the CEPC Ref-TDR team**

**IHEP, CAS**


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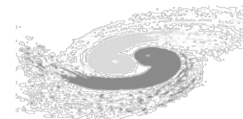
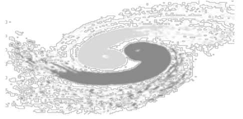
# Outline



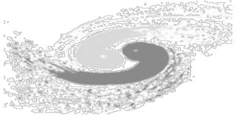
- 电子学触发系统总体框架
- 需求输入-MDI接口及考虑
- 子探测器读出接口-读出框架及关键器件尺寸、功耗
- 整体及基建接口-电子学间初步调研
- 新方案需求-无线传输方案与机械接口

# Requirement from Sub-Detector



| | Vertex | Pix(ITKB) | Strip (ITKE) | TOF (OTK) | TPC | ECAL | HCAL |
|---|---|---|---|---|---|---|---|
| Channels per chip | 512*1024 Pixelized | 512*128 (2cm*2cm@34um*150um) | 512 | 128 | 128 | 8~16 | 8~16 |
| Ref. Signal processing | XY addr + BX ID | XY addr + timing | Hit + TOT + timing | ADC+TDC/TOT+TOA | ADC + BX ID | TOT + TOA/ ADC + TDC | TOT + TOA/ ADC + TDC |
| Data Width /hit | 32bit (10b X+ 9b Y + 8b BX + 5b chip ID) | 48bit （9b X+7b Y +14b BX + 6b TOT + 5TOA + 4b chip ID） | 32bit (10b chn ID + 8b BX + 6b TOT + 5b chip ID) | 40~48bit （7b chn ID + 8b BX + 9b TOT + 7b TOA+5b chip ID ) | 48bit (7b chn ID + 8b BX + 11b chip ID + 12b ADC + 10b TOA) | 48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID) | 48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID) |
| Data rate / chip | 1Gbps/chip@ Triggerless@ Low LumiZ Innermost | 640Mbps/chip Innermost | Avg. 1.01MHz/chip Max. 100MHz/chip | Avg：26kHz/chip @ z pole Max：210kHz/chip @z pole | ~70Mbps/module Inmost | <4.8Gbps/module | <4.8Gbps/module |
| Data aggregation | 10~20:1, @1Gbps | 1. 1-2:1 @Gbps；2. 10:1@O(10Gbps) | 1. 10:1 @Gbps 2. 10:1 @O(10Gbps) | 1. 10:1 @1Mbps 2. 10:1 @O(10Mbps) | 1. 279:1 FEE-0 2. 4:1 Module | 1. 4~5:1 side brd 2. 7*4 / 14*4 back brd @ O(10Mbps) | < 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC) |
| Detector Channel/module | 2218 chips @long barrel | 30,856 chips 2204 modules | 22720 chips 1696 modules | 41580 chips 1890 modules | 258 Module | 1.1M chn | 6.7M chn |
| Data Volume before trigger | 2.2Tbps | 2Tbps | 22.4Gbps | 1Gbps | 18Gbps | 164.8Gbps | 14.4Gbps |

# CEPC电子学触发整体框架



FEE(Customize) Rad-tol

Det-ASIC
Det-ASIC
Det-ASIC
Det-ASIC

Data Aggregation & Data Buffering & Event Building （TaoTie）

Data Interface （ChiTu）

Optical Module （KinWoo）

DC-DC - LV 1.2/2.5V （BaSha-LV）

DC-DC - MV 12/48 V (BaSha-MV）

Power Cable

Fiber (Only)

Trigger Comm-Brd

Most Trg

DAQ

BEE Comm-Brd

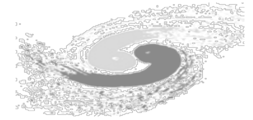
Slow Ctrl

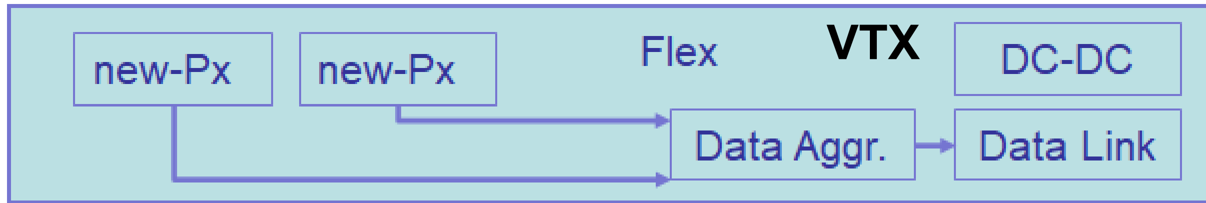
Non Rad-tol

Common platform

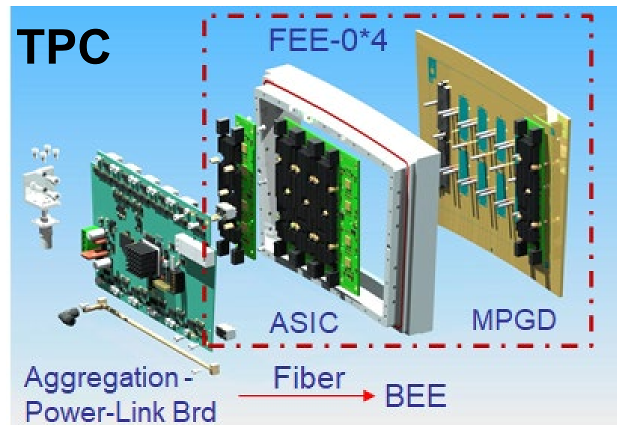
- **Common subsystems (data buffering, aggregation, transmission; powering)**
- **Det. specific ASICs waiting for detector final choices.**
- **A common BEE hardware, configurable for individual subsystems.**
- **TDAQ interface is (probably) only on BEE**

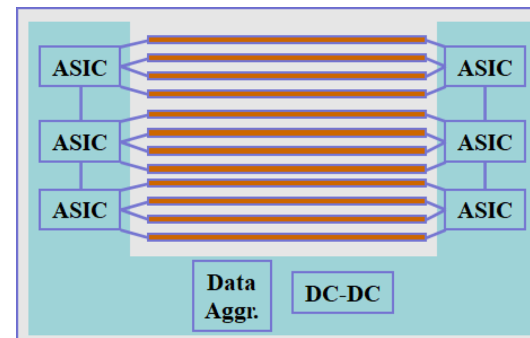
# An overview of the Sub-Det readout electronics

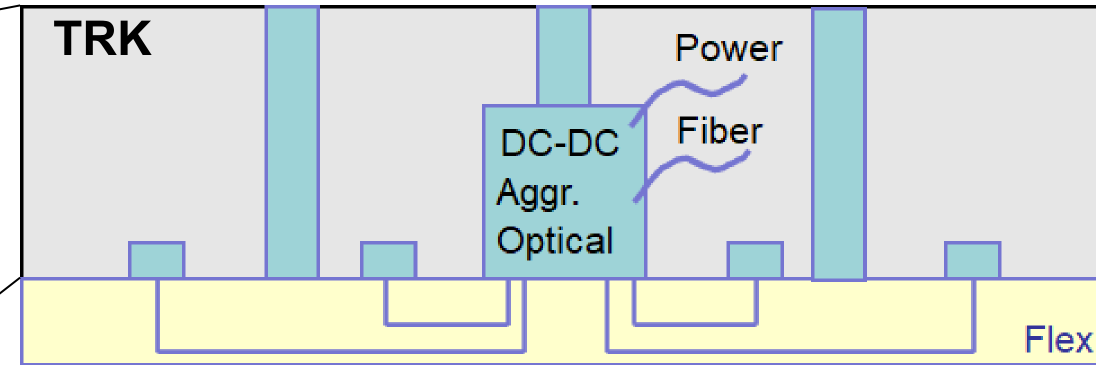


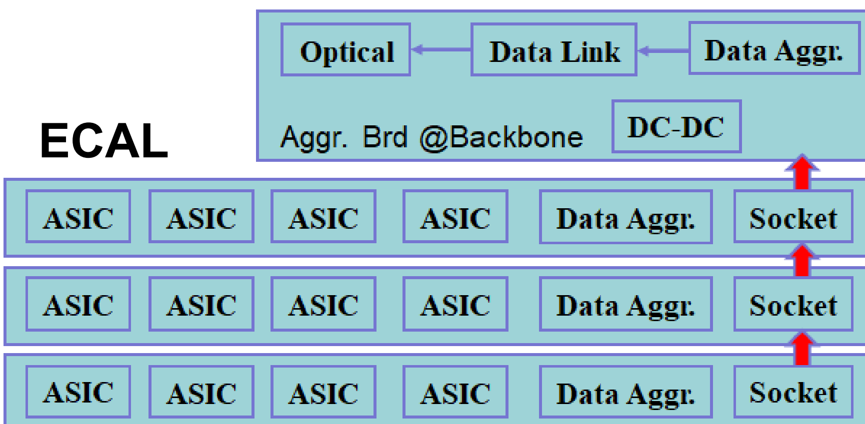


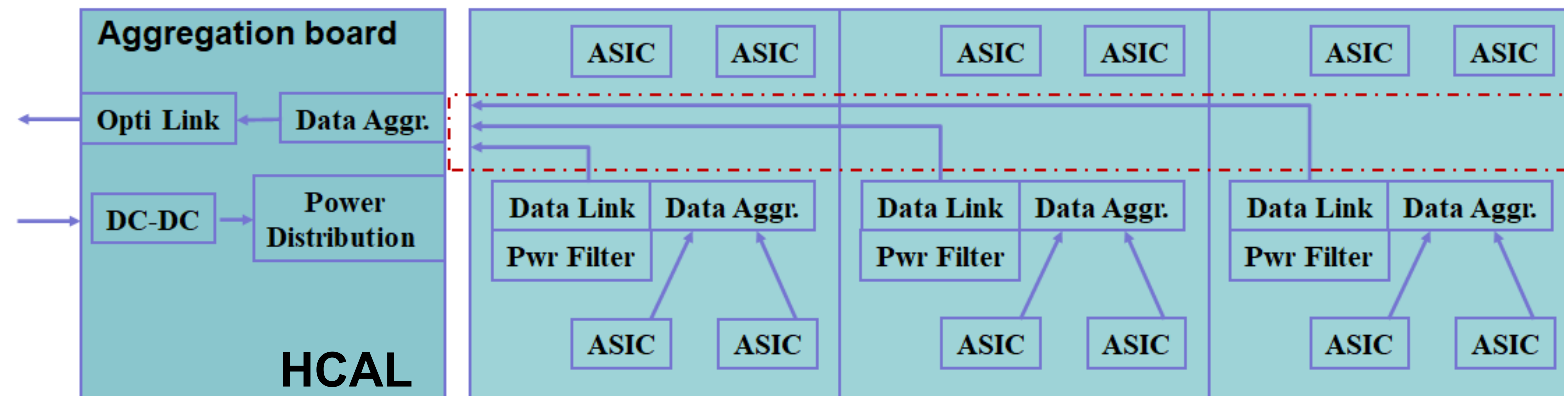

- **All sub-det readout electronics were proposed based on this unified framework, maximizing possibility of common design usage.**



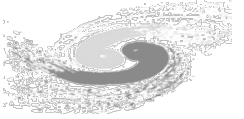



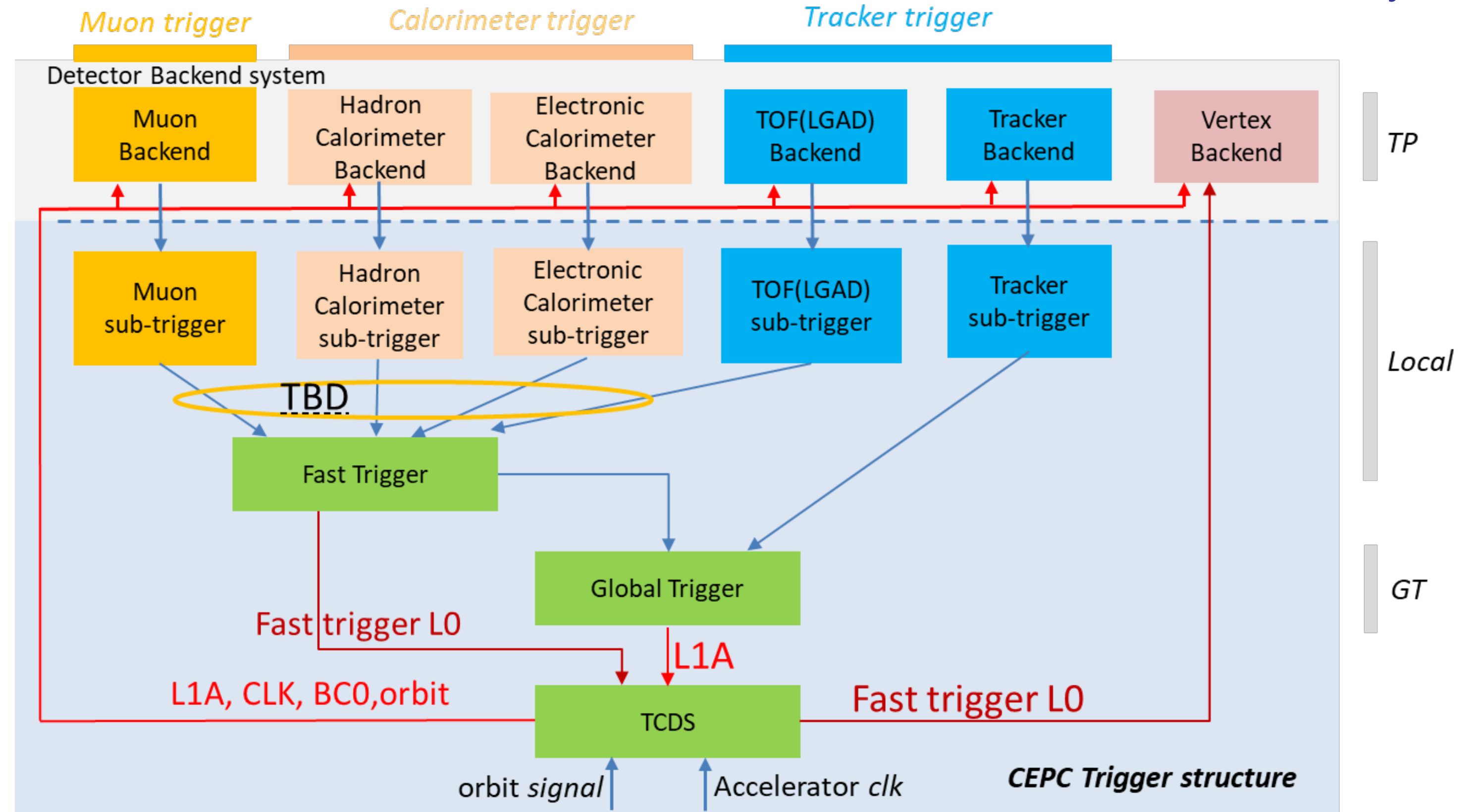
# 本底率vs电子学触发框架



- The proposed framework was based on the estimated background rate of all sub-det.
- In case of under-estimation or unexpected condition:

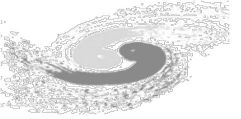
1. Additional optical links can be allocated to the hottest module.
2. In case the background rate is too high for FEE-ASIC to process, Intelligent Data Compression algorithm can be integrated on-chip, for the initial data rate reduction.

Ref: TDAQ talk by Fei Li



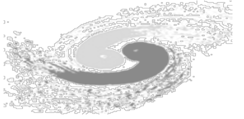

The conventional trigger scheme can always serve as a backup plan, with sufficient on-detector data buffering and reasonable trigger latency, the overall data transmission rate can be controlled.

# 当前关键探测器本底与读出方案的一些近期更新



- **顶点**
  - 按前十年Low LumiZ，单芯片数据率~1Gbps （@30MW，Higgs Bunch Spacing@592ns）
  - 如果运行在50MW（ Higgs Bunch Spacing@355ns），Hit Density不变时数据率将接近单芯片~2Gbps – 更高的挑战
- **ECAL**
  - 不考虑阈值时，单bar事例率~700kHz
  - 添加阈值后，单bar事例率~100kHz
  - Q：高堆积vs能量分辨，高事例率是否导致电子学读出方案需要调整？
  - 当前功耗@15mW/chn （与方案及应用目标接近的最好芯片HGCROC相一致），目前没有进一步功耗优化的目标（计划）
- **OTK / AC-LGAD TOF**
  - 当前功耗@20mW/chn for 30ps
  - 基于多通道TDC共享方案，可进一步优化功耗
- **端盖最内层**
  - 目前均缺少具体数值评估（计数率约高十倍），可能将对读出方案产生较大冲击

# 通用数据读出框架



By Di Guo@CCNU

GBTx-like ASIC
Clock Phase Control
PLL
Clock
D-Link
D-Link
Data
D-Link
D-Link
D-Link
D-Link
...
D-Link
Phase Aligner
Downlink Direction
Decode
De-serializer
CDR
Uplink Direction
Encode Scramble
Serializer
I2C Configuration

Front-end
Pre-Aggregation ASIC
Data
Data

TIA ASIC
Back-end
Fiber
Array Laser Driver ASIC
Optical Module(Array form)

Different data rate and channels from different detectors

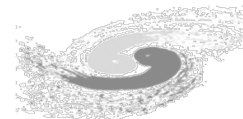
Fixed data rate
Fixed data channels
(may vary in limited options)

...
More GBTx ASIC

饕餮-TaoTie　　赤兔-ChiTu　　金乌-KinWoo

- **Pre-Aggregation ASIC (TaoTie): Intend to fit with different front-end detector (different data rates/channels)**
- **GBTx-like ASIC (ChiTu): Bidirectional serdes ASIC including ser/des, PLL, CDR, code/decode …**
- **Array Laser Driver ASIC + TIA ASIC + Customized Optical module (KinWoo)**

# 阵列式的多通道光模块



- 阵列式光模块：4Tx + 1Rx, 4Tx + 4Rx, …

- 使用阵列式的激光器芯片、阵列式PD光电二极管
- 使用阵列式的光路耦合器件（图中黄色“盖子”）

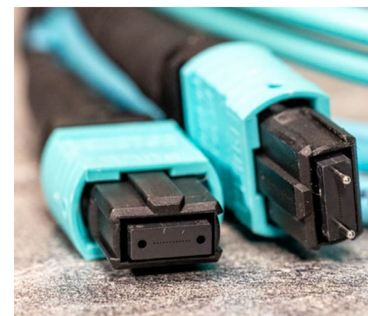
- 不再使用LC光纤接头，使用MTP接头
- 通道数可定制
- CERN的第二代VTRx+ 即升级为了阵列式光模块（采用了4Tx + 1Rx）

- 目前阵列式光模块的组装生产已非常成熟

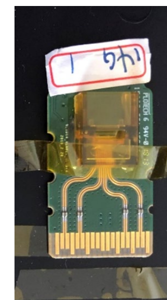
- 模块高度最小可缩减至 3mm左右

- 在数据通量巨大的单板上，使用阵列式光模块可减少光模块使用数量
  例如：　使用一个 4Tx + 1Rx光模块
  　　　　上行速率 4 x 10.24 Gbps/ch
  　　　　一个光模块可对应 4颗 GBTx芯片，
  　　　　解决 4 x 前端通道数据传输

商用光模块QSFP (4Tx+4Rx)



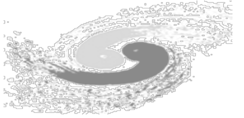
光纤MTP接头

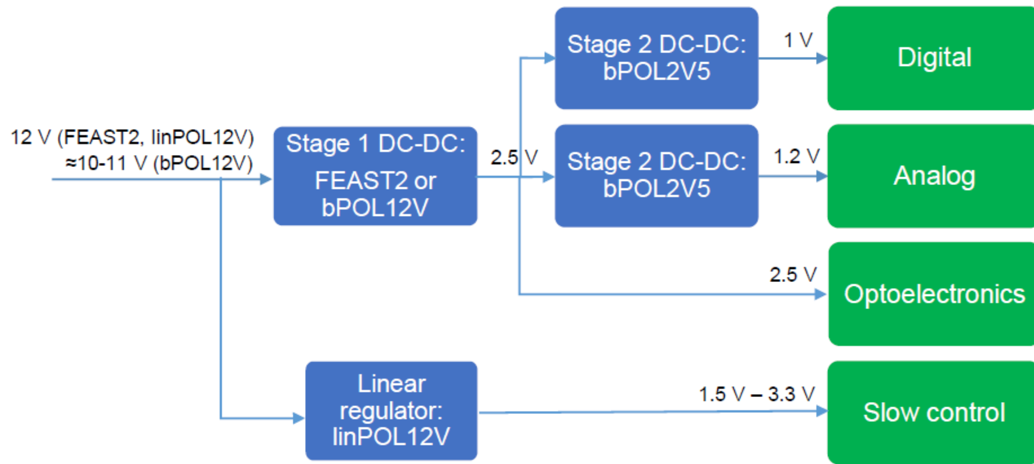


自研的阵列式光模块 4Tx

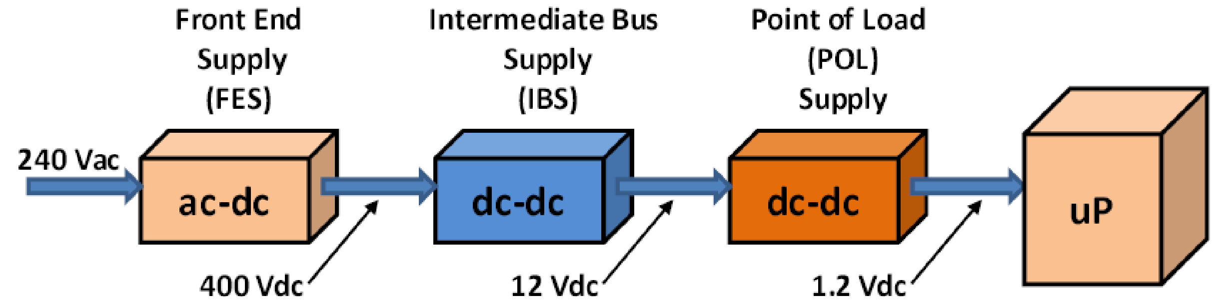
CERN VTRx+光模块 (4Tx+1Rx)

# 通用电源框架

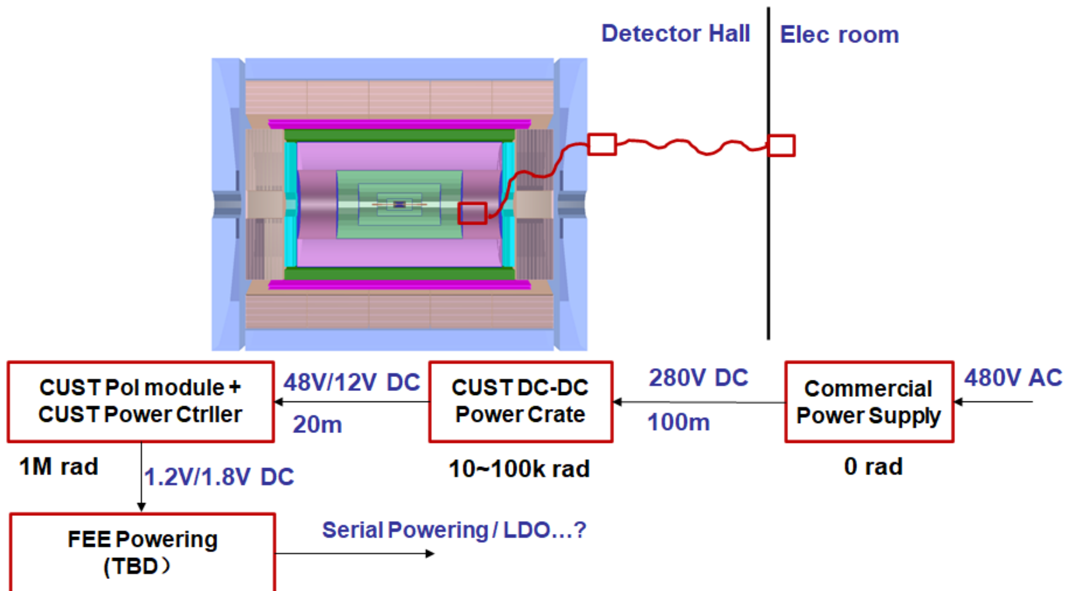





Ref. F. Faccio, FEAST and bPOL status and plans, 2020

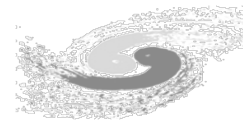


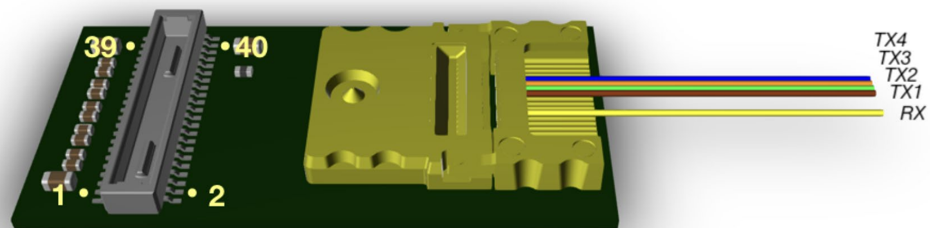

A 400V to 1.2V chain, lower power loss on cable

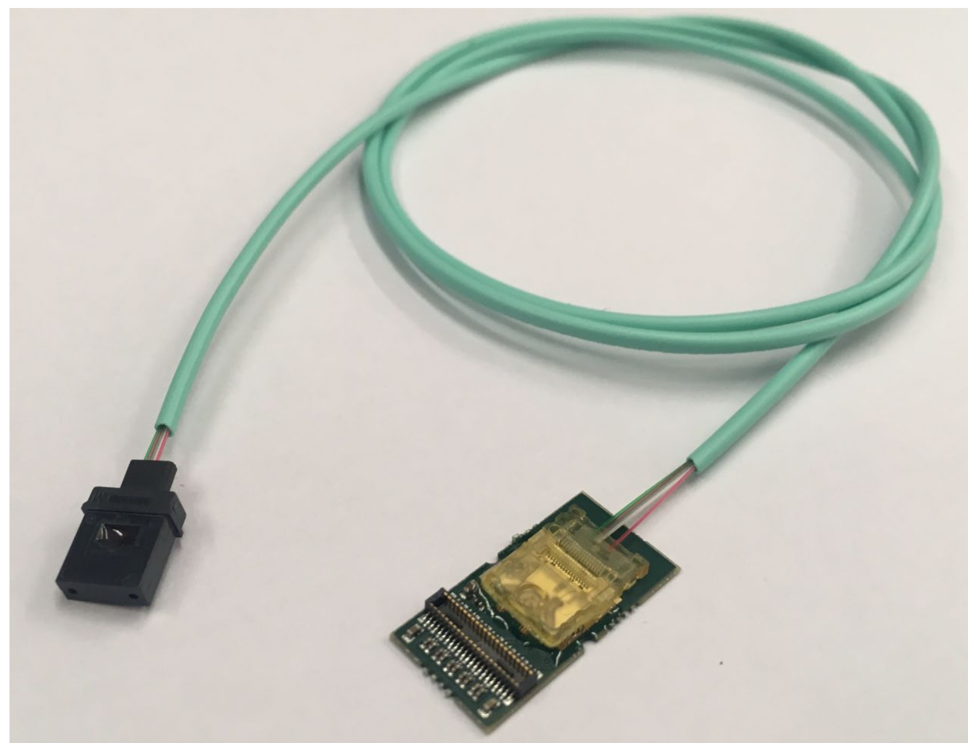



- **The GaN transistor has been a game changer in recent years, enabling DC-DC converters to achieve ultra-high efficiency, high radiation tolerance, and noise performance comparable to LDO.**
- **also enables high voltage power distribution, for low cable material and low power loss**

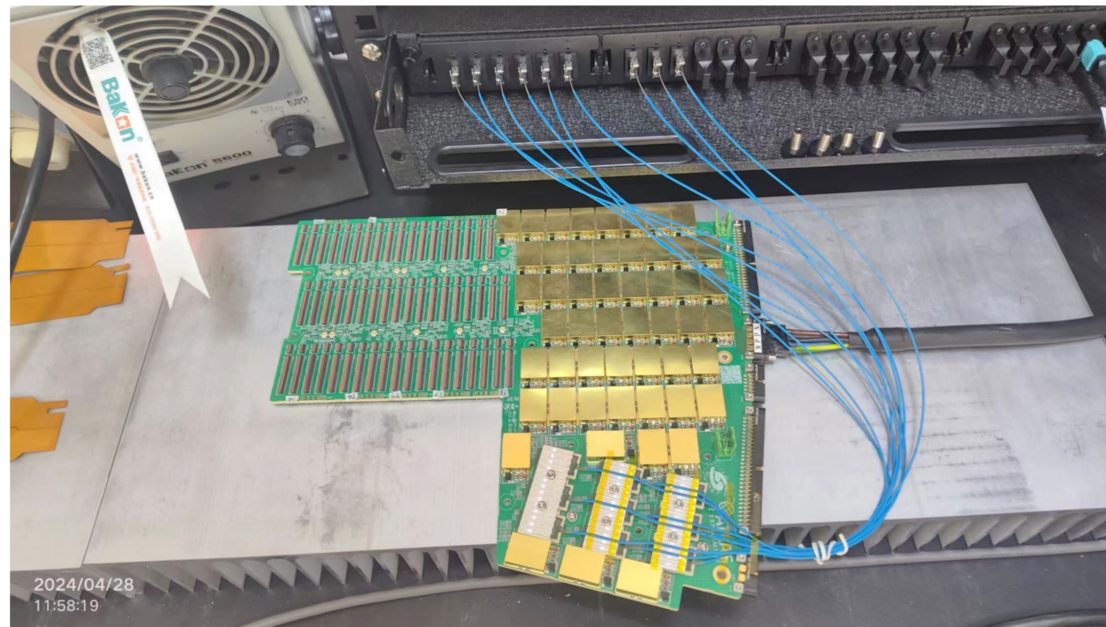
# 子探测器机械接口-模块尺寸

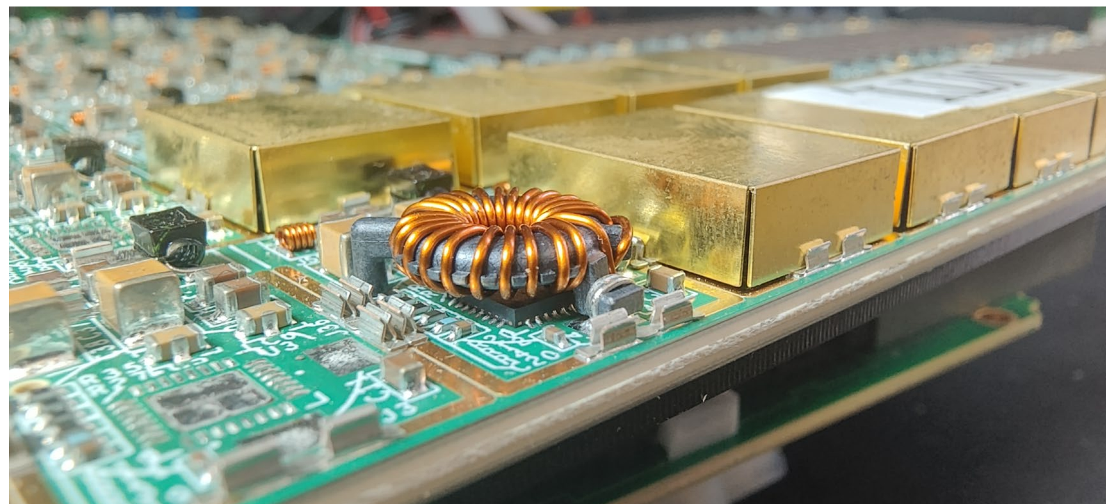




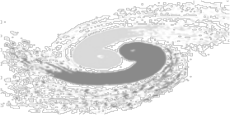
光模块尺寸及光纤



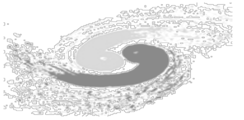
电源模块、电感及屏蔽壳

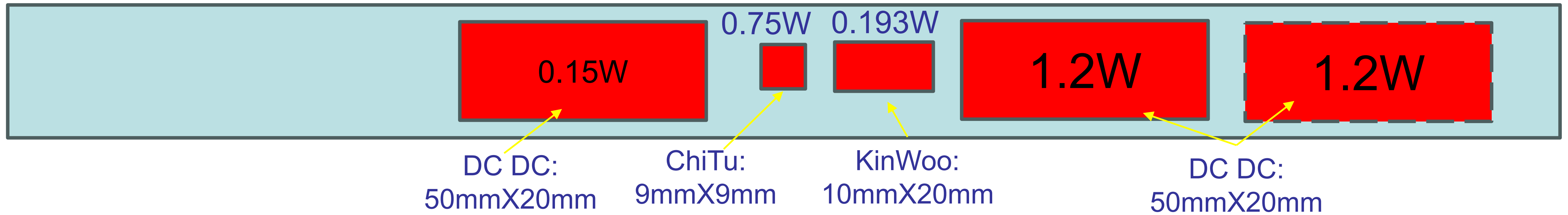
# 子探测器机械接口



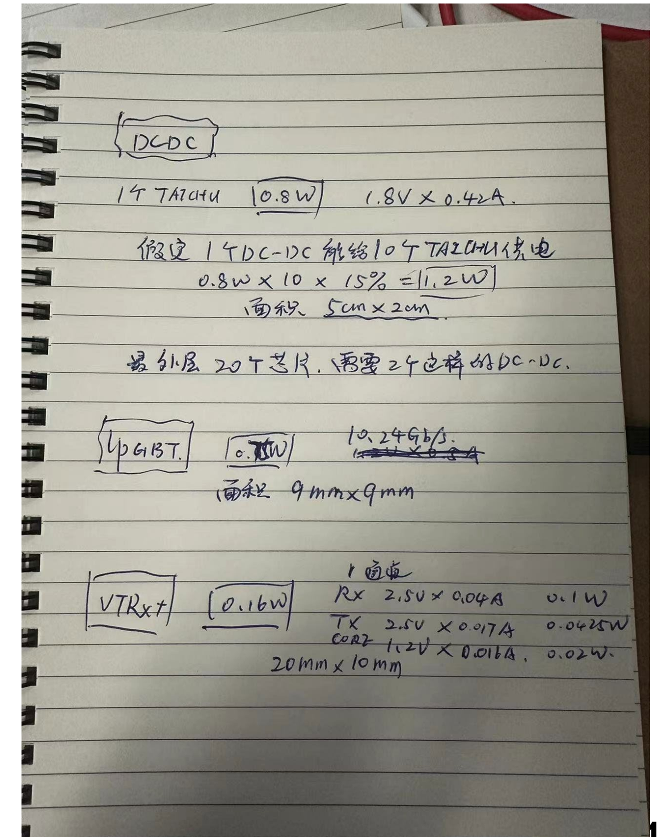
- 电子学高度（Major Constraint）
  - KinWoo光模块：~3mm
  - BaSha电源模块：~6.7mm （电感高度限制）
  - 薄型纯PCB：~3.2mm（1.2mmPCB + 2mm单面表贴器件）
  - 电缆尺寸：
    - ➢ 薄型PCB：<2mm，基于双绞线实现信号传输
    - ➢ （VTX等空间紧张的Sub-D）光电复合缆：~5mm，光纤+电源电缆合一
    - ➢ 普通探测器：采用DC-DC高压供电方案，减少电源电缆线径，取决于探测器组织及模块功耗
- 关键器件尺寸
  - 数据接口：ChiTu 9mm×9mm + KinWoo 10mm×20mm
  - 电源模块：BaSha 50mm×20mm
- 关键器件功耗
  - 数据接口：ChiTu 0.75W + KinWoo 0.2W
  - 电源模块：
    - ➢ BaSha – 低压：0.15W
    - ➢ BaSha – 中压：1.2W

# 子探测器机械接口-以顶点探测器为例

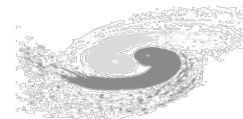





- **DC-DC BaSha：电源管理芯片**
  - TAICHU功耗0.8W（1.8V*0.42A）
  - 单个DC-DC最多为10个TAICHU提供电源，效率按85%计算
  - DCDC功耗为0.8*10*15% = 1.2W
  - 如果最外层需要20个芯片则需要2个DCDC
  - lpGBT和VTRX+需要其他种类电源（1.2V，2.5V），总体功耗不高，~1W，则DCDC功耗为0.15W
- **ChiTu：数据汇总芯片**
  - 0.75W@10.24Gb/s
- **KinWoo：光电转化芯片**
  - 1发1收：0.193W（RX：2.5V*0.05A，TX：2.5V*0.02A，core：1.2V*0.015A）
- **说明：1：图中仅展示ladder一端一面，底面及ladder另一端有同样的配置**
- **2：lpGBT及VTRX+的参数为CERN对应芯片手册得到，CEPC最终参数可能有所不同。**
- **Ladder长度及端部器件位置，需结合机械及安装设计来调整**



# 电子学间需求初步调研



## 以CERN的CMS为参考，分为地面大厅和地下控制间两部分

CMS地面建筑

1，SX5（surface assembly building）

为地面装配建筑，约1000平米。内部包括各系统的测试组装房间及洁净间，还有一个控制室。

2，UPS系统也在地面，是独立的一个建筑，停电为主要系统提供临时备份电力

3，USC55（Underground Service Cavern）

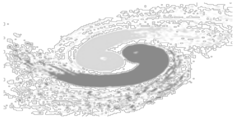
为地下主要的机房，包括高低压电源机柜等各种设备，电子学大部分设备所在地

4，UXC55(Underground experimental Cavern)

真正的地下实验大厅，谱仪所在地，周围也有相对少量的前端读出电子学设备及机柜

By Lei Fan@IHEP

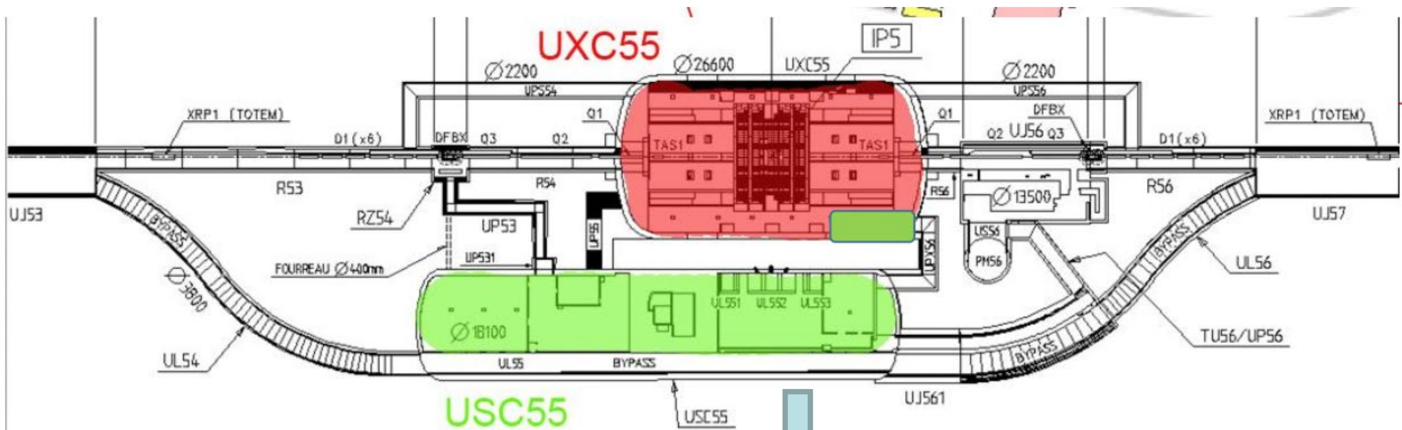
# 电子学间需求初步调研



**SX5地面大厅：**

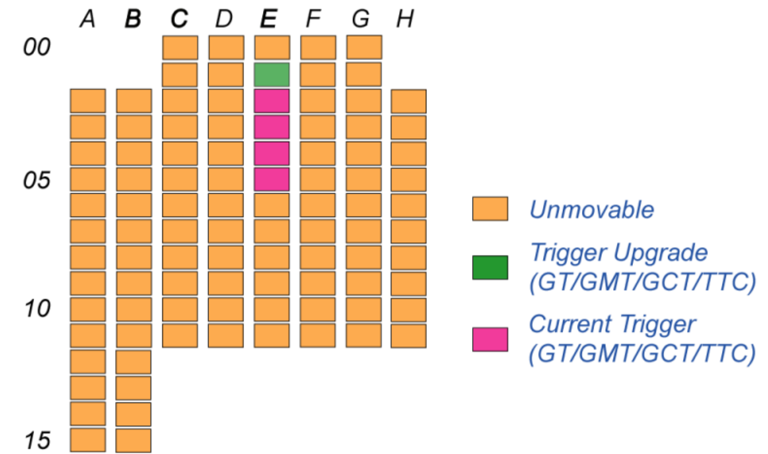
**包括了磁铁组装测试间，像素探测器的洁净间，地面控制间，测试间等，大概1000平米，可能还分层。**

By Lei Fan@IHEP



CMS机房CSC55的结构图

## Potential Trigger Upgrade Racks in S1 (USC55)




某报告中触发机柜的数量

- 从图纸上粗算**USC55**的面积：直径**18**米，长**108**米的洞室
- 洞室内部用钢结构建成了一个**4**层的机房
- 机柜数量规模**>1000**台

By Lei Fan@IHEP

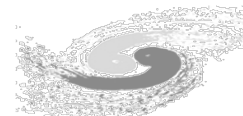
# 电子学空间需求

根据CMS的情况作为参考依据，初步预估电子学空间的需求：

- 地面至少300~400平米的组装，测试及缓存的空间；100平米的洁净间。（不包括库房）
  - 仅指纯电子学组装测试空间需求，不含VTX、TRK等联合组装的空间
- 地面要有独立的UPS机房，估计至少200平米（取决于功率需求）
- 地下谱仪周围要预留空间存放前端电子学设备。
- 地下主机房洞室横切面直径18米，长100米，根据系统划分多层结构，机柜数量>1000台。还需要配套大量的电缆槽，电缆架，防静电地板。

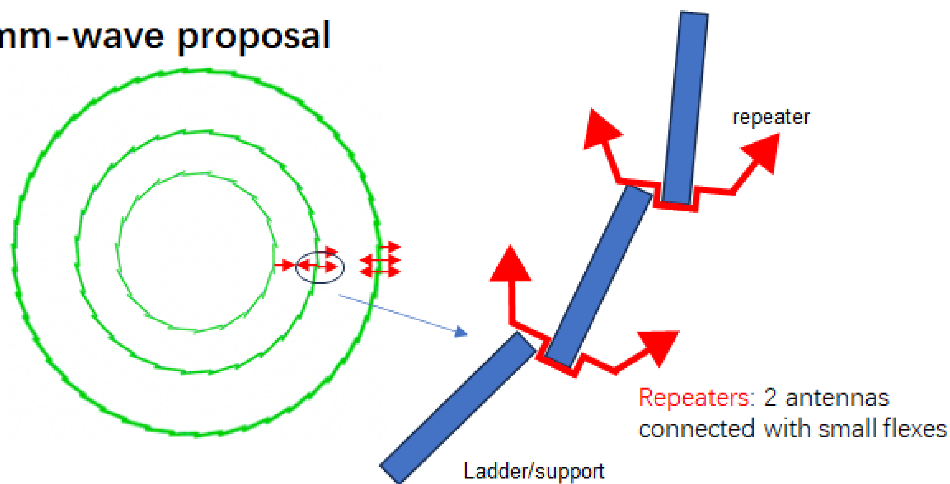
➢ 准确的需求要统计各系统的详细数据，目前只能初步估计整体规模

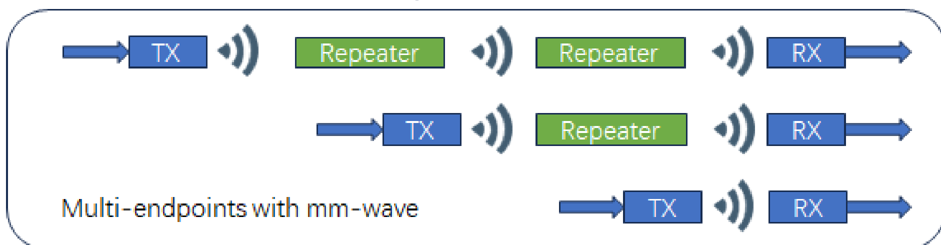
# 基于无线传输的数据读出及时钟同步方案

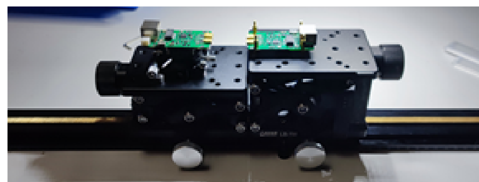


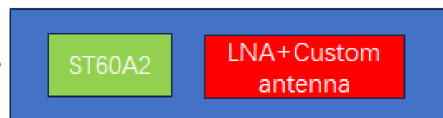
By Jun Hu@IHEP

## mm-wave proposal



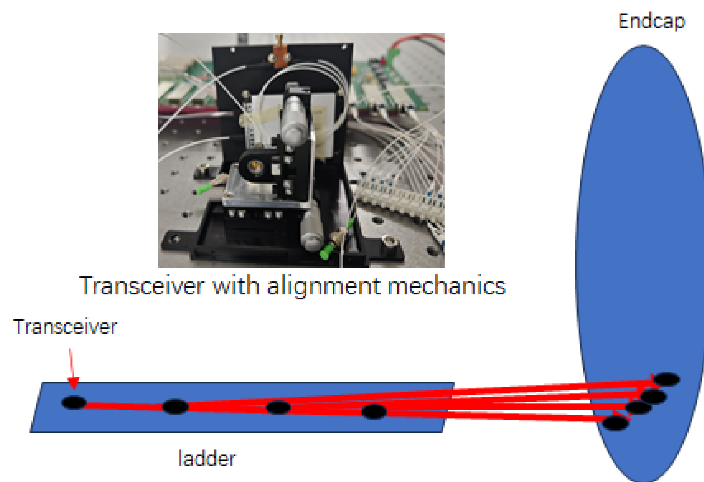


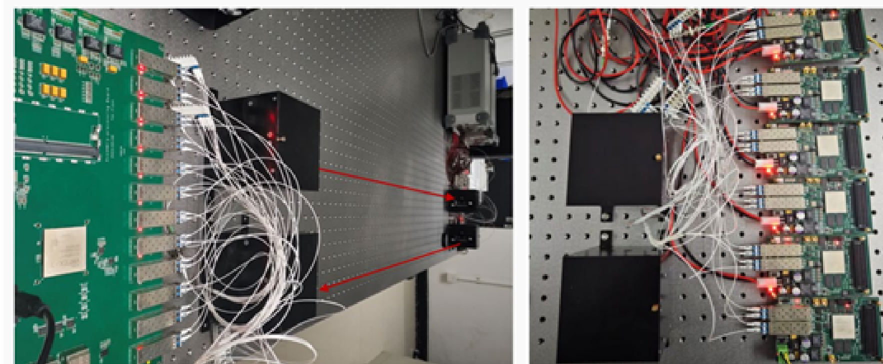

Test with evaluation boards – SK202

- Based on the commercial 60GHz RF chip ST60A2 transceiver from ST Microelectronics company.
- The transmission speed can exceed 900Mbps when the distance is less than 6 cm.

- Design a small PCB module with ST60A2. LNA and custom antenna.
- Higher bandwidth and longer distance
- Evaluate the interference with detector
- Under design, cheap and easy
- → custom transceiver + antenna +AIP

## Optical wireless proposal

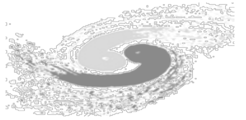


DWDM transceivers +AWG + lens

- Up to 6-meter free space optical transmission distance
- 10Gbps X 12 channels bandwidth
- PRBS 31bits error rate < BER-15 @ 10Gbps under 1.6m distance

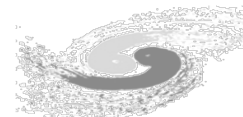
# 无线传输vs机械接口新需求



| Technology | Single channel speed | Channel integration | Technical maturity | Distance | Power consumption | Possible application scenarios | Key Technology need to be development |
|---|---|---|---|---|---|---|---|
| WiFi | <1Gbps | ~2m | Very High | ~10-100m | ~2W | DCS information | |
| mmWave | ~5-6Gbps | ~10cm | Medium | <10cm | ~100mW | Used for data/trigger transfer between layers inside Tracker | Radiation-hard transceiver and antenna chip design |
| FSO | >10Gbps | ~1cm | High | ~10m | ~2W | Used for calorimeter data transfer to outside | Mechanical alignment constrains design |

- 基于无线传输的读出方案要求探测器机械设计提供更高的对准精度
  - 水平面对准精度
  - 安装高度对准
- 基于毫米波的层间传输方案要求子探测器考虑增加特殊的穿层及中继器件
  - 子探测器读出方案需要整体调整

# 总结

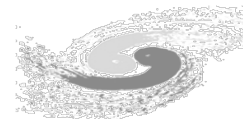


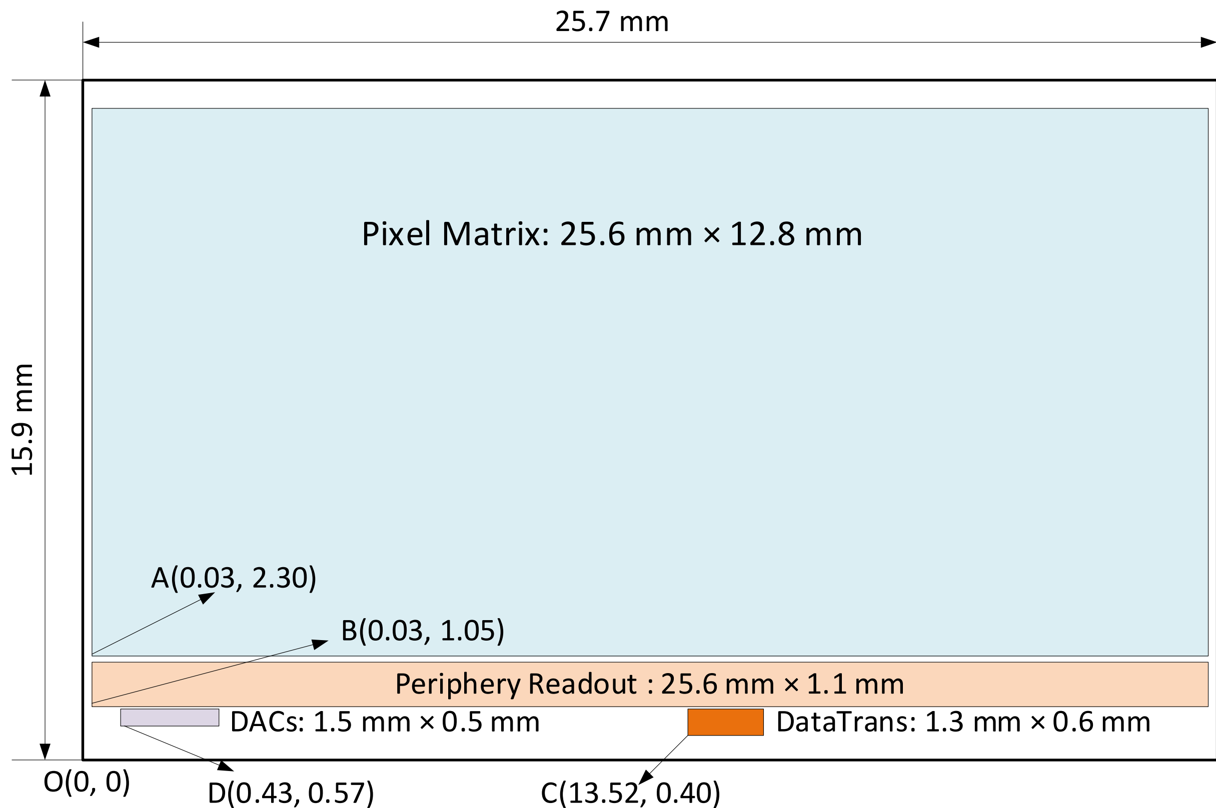
- 电子学触发框架基本确定
- 与机械系统接口主要通过光模块和DC-DC模块
  - 模块尺寸、功耗参考CERN已有芯片
- 物理本底仍将可能对读出方案产生巨大影响
  - 机器本底目前未考虑，若无法优化，则数据率将显著提升
  - 各子探测器本底事例率统一计算中
  - 端盖最内层也是一个关键hot点
- 电子学间需求目前很难估计
  - 初步根据CMS情况进行了调研，可作为讨论起点
- 无线数据传输方案对机械系统还有更高的对准的要求
- 需进一步同子探测器、机械系统联合设计
  - 优化模块排布
  - 细化电缆走线
  - 优化功耗和散热设计

Thank you!

# Backup

# VTX像素芯片功耗分布估算



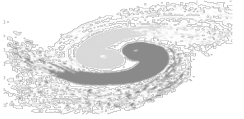



## 估算说明：

- 太初芯片：180 nm工艺，电源1.8 V;
- 65 nm芯片：电源1.2 V;
- Data rate @Triggless-CDR: 4.48 Gbps /chip
  bunch spacing (min.): 25 ns需要快前沿前端
- Data rate @Triggless-TDR (Low Lumi):
  1 Gbps/chip
- Low Lumi@TDR: bunch spacing ~几百ns，像素前端不需要快前沿，Matrix功耗可降低
- 图中芯片坐下角标为坐标原点，标注4个功耗模块的左下角坐标(X,Y)，单位为毫米

| | Matrix | Periphery | DataTrans. | DACs | Total Power |
|---|---|---|---|---|---|
| 太初芯片<br>@ triggerless (CDR) | 304 mW | 135 mW | 206 mW | 10 mW | 655 mW |
| 65nm 芯片<br>@ 1 Gbps/chip<br>(TDR LowLumi) | 60 mW | 80 mW | 36 mW | 10 mW | 186 mW |

# Flex厚度和物质分布



叠层

**Stack Up**

| Layer | Thickness | Unit | Material | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 12.5 | um | Coverlay (yellow) | | | | | |
| | 20 | um | Coverlay Adhesive | | Soldmask (green) | | | |
| Layer 1 | 24 | um | ED Base Copper | 12 um | um + | Plated | 18 | um . |
| | 13 | um | Polyimide (Adhesiveless) | | | | | |
| | 12.5 | um | Adhesive | | | | | |
| Layer 2 | 12 | um | ED Base Copper | 12 um | | | | |
| | 25 | um | Polyimide (Adhesiveless) | | Flex Thickness | | 绕折区 | |
| Layer 3 | 12 | um | ED Base Copper | 12 um | | | | 补强区 |
| | 12.5 | um | Adhesive | | | | | |
| | 13 | um | Polyimide (Adhesiveless) | | | | | |
| Layer 4 | 24 | um | ED Base Copper | 12 um | um + | Plated | 18 | um . |
| | 20 | um | Coverlay Adhesive | | | | | |
| | 12.5 | um | Coverlay (yellow) | | | | | |

FPC厚度: 213 um    Spec: 210 um  +/- 50 um

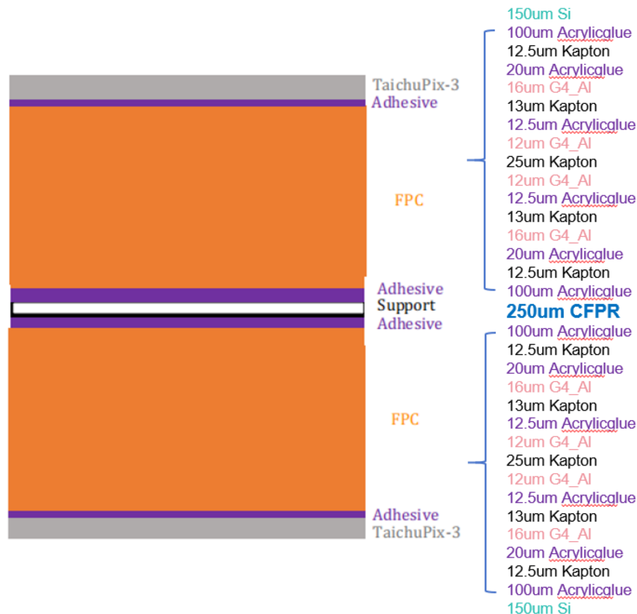
Created By: HLJ

Date:

4层柔性板基于国内Cu工艺（当前阶段）

| | | | |
|---|---|---|---|
| | 12.5 | um | Coverlay |
| | 20 | um | Coverlay adhesive |
| layer1 | 24 | um | ED Base Copper |
| | 13 | um | Polymide(Adhesiveless) |
| | 12.5 | um | Adhesive |
| layer2 | 12 | um | ED Base Copper |
| | 13 | um | Polymide(Adhesiveless) |
| | 12.5 | um | Adhesive |
| layer3 | 12 | um | ED Base Copper |
| | 25 | um | Polymide(Adhesiveless) |
| layer4 | 12 | um | ED Base Copper |
| | 12.5 | um | Adhesive |
| | 13 | um | Polymide(Adhesiveless) |
| layer5 | 12 | um | ED Base Copper |
| | 12.5 | um | Adhesive |
| | 13 | um | Polymide(Adhesiveless) |
| layer6 | 24 | um | ED Base Copper |
| | 20 | um | Coverlay adhesive |
| | 12.5 | um | Coverlay |
| | | | |
| 厚度 | 288 | um | |

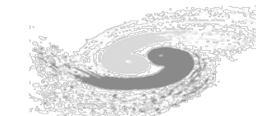
6层柔性板基于国内Cu工艺（当前阶段）




Proposed Double-sided ladder based on 铝

- 国内工艺当前只能实现基于铜的PCB，如需采用铝材料，需要委托CERN进行加工（accessibility？）
- Long barrel方案，同ladder芯片更多，需要更多层的PCB
  - For Innermost：4层Flex（now：Cu based，proposed：Al based）
  - For Middle & Outer：6层Flex（now：Cu based，proposed：Al based）

# Backup



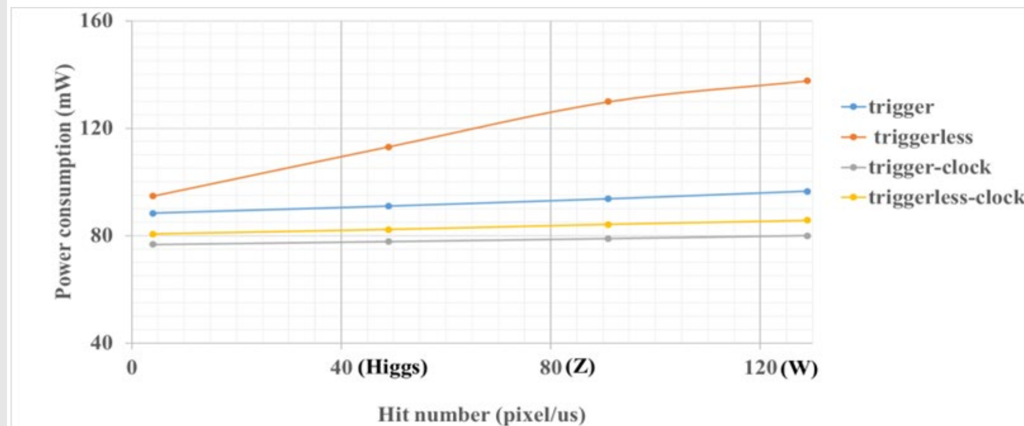
## Specification calculation- from hit density

| | | Hit density ($Hits/cm^2/BX$) | Bunch spacing (ns) | Hit rate (M $Hits/cm^2$) | Hit Pix rate (M $Px/cm^2$) | Hit rate/chip (MHz) | Data rate@triggerless (Gbps) | Pixel/bunch | FIFO Depth @3us rg latency | Data rate@trigger (Mbps) |
|---|---|---|---|---|---|---|---|---|---|---|
| CDR | Higgs | 2.4 | 680 | 3.53 | 10.59 | 34.62 | 1.1 | 23.5 | 103.9 | 105.28 |
| | W | 2.3 | 210 | 10.95 | 32.86 | 107.44 | 3.4 | 22.6 | 322.3 | 101.248 |
| | Z | 0.25 | 25 | 10 | 30 | 98.1 | 3.1 | 2.4 | 294.3 | 53.76 |
| | | | | | | | | | | |
| TDR | Higgs | 0.81 | 591 | 1.37 | 4.11 | 13.44 | 0.43 | 7.96 | 40.4 | 213.9? |
| | W | 0.81 | 257 | 3.16 | 9.45 | 30.90 | 0.98 | 7.96 | 92.8 | 213.9? |
| | Z | 0.45 | 23 | 19.6 | 58.7 | 191.9 | 5.9 | 4.4 | 575 | 118 |

- **TDR raw hit density: Higgs 0.54， Z 0.3; Safety factor: TDR 1.5, CDR 10;**
- **Cluster size: 3pixels/hit (@Twjz 180nm, EPI 18~25um)**
- **Area: 1.28cm*2.56cm=3.27cm² (@pixel size 25um*25um)**
- **Word length: 32bit/event (@Taichu's scale, 512*1024 array)**
- **Trigger rate： 20kHz@CDR， 120kHz@TDR estimated**
  - **Trigger latency: 3us(very likely not enough), Error window: 7 bins**
  - **FIFO depth: @3us * hit rate/chip**
  - **Data rate=pixel/bunch*trigger rate*32bit*error window**

2

Rate for Low LumiZ still missing




仅外围电路功耗vs计数率

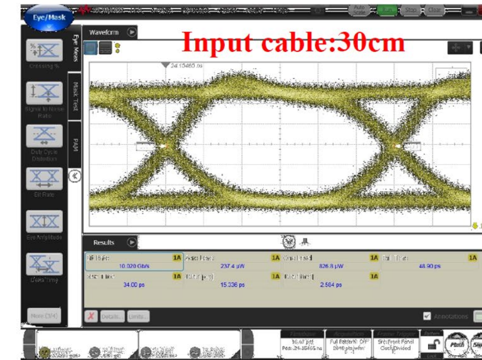
| | 160Mbps | 2.56Gbps | 4.48Gbps |
|---|---|---|---|
| PLL | 20 | 34 | 34 |
| MUX | 8 | 27.8 | 44.2 |
| CMLdriver | | 36.5 | 36.5 |
| LVDS_TX | 5 | 7.5 | 10 |
| | 33 | 98.3 | 114.7 |

数据接口功耗vs数据率

# R&D efforts and results on Data Link

By Di Guo@CCNU

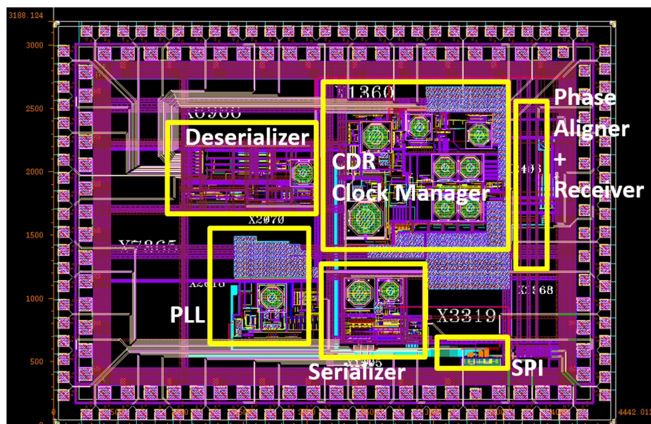
- Self-developed GBT-like prototypes verified:
  - 5.12 GHz PLL + 10.24 Gbps Serializer verified√
  - 2.56 Gbps CDR + 2.56 Gbps Deserializer verified√
  - Phase aligner under test
- 10 Gbps Laser Driver Verified √
- Customized optical module prototype Done √
- The rad-tol fiber will be investigated together with the accelerator clocking system



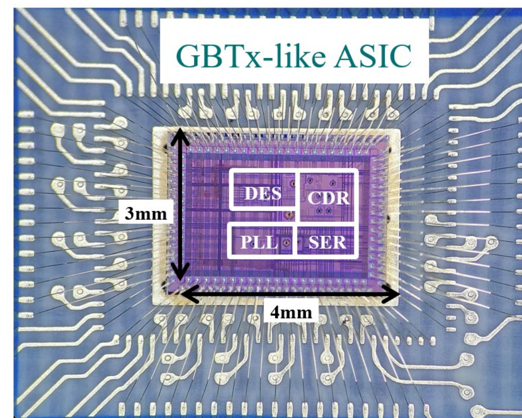

10 Gbps optical eye

| Bit Rate | 10Gbps | RMSJ | 2.6ps |
|---|---|---|---|
| Rise Time | 34.0ps | PPJ | 15.3ps |
| Fall Time | 48.9ps | Amp | 589.4μW |

10 Gbps optical eye diagram

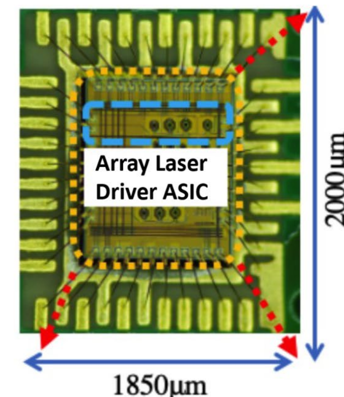


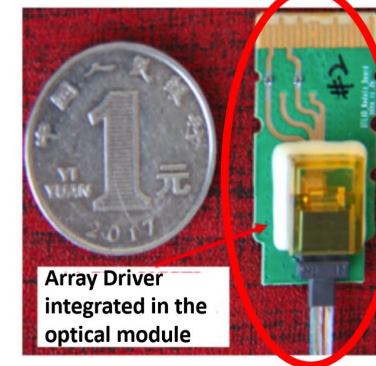

GBT-like ASIC prototype layout

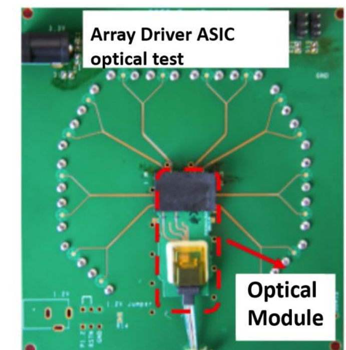



GBT-like ASIC wire-bonding picture

Customized Optical module

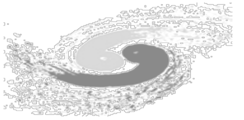


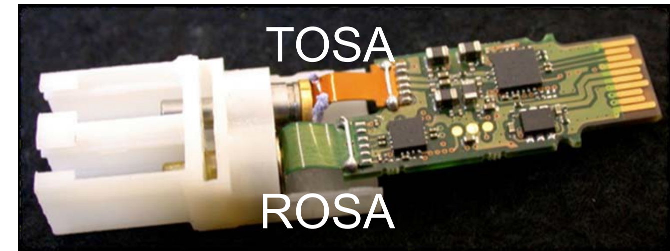



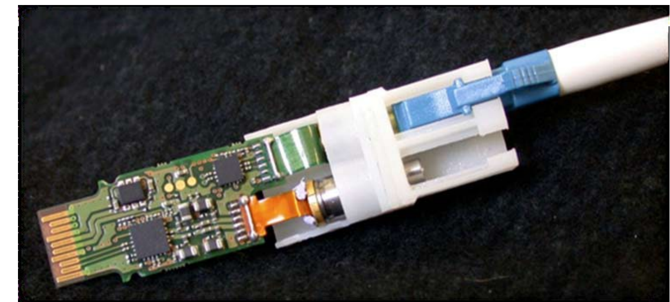

4 x 10 Gbps/ch VCSEL Array Driver with customized optical module

# 单通道式的光模块

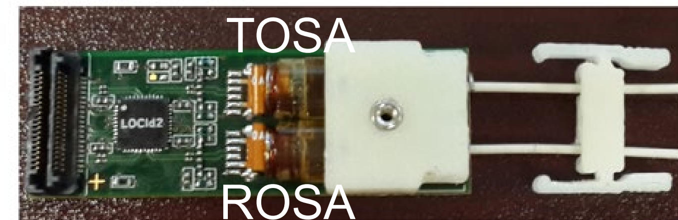


- 单通道式光模块：1Tx + 1Rx
  - 商用的SFP光模块即为此类型
- 基于成熟的TOSA 和 ROSA光组件
  - 把激光器、PD封装在里面
    并提供了LC接口
- Tx/Rx方向均使用LC光纤接口（2根多模LC接口的光纤）
- 定制化“相对简单”，主要为设计高速高密度基板、LC光纤的“固定”装置（图中白色）
- 模块高度最小可缩减至 6mm左右 （由TOSA/ROSA组件所限制）
- CERN “非常关注”光模块的高度问题
  以Inner Tracker为例，其读出板“缝隙”很小



CERN的第一代VTRx光模块 (1Tx+1Rx)




另一款 (1Tx+1Rx)定制化光模块MTx