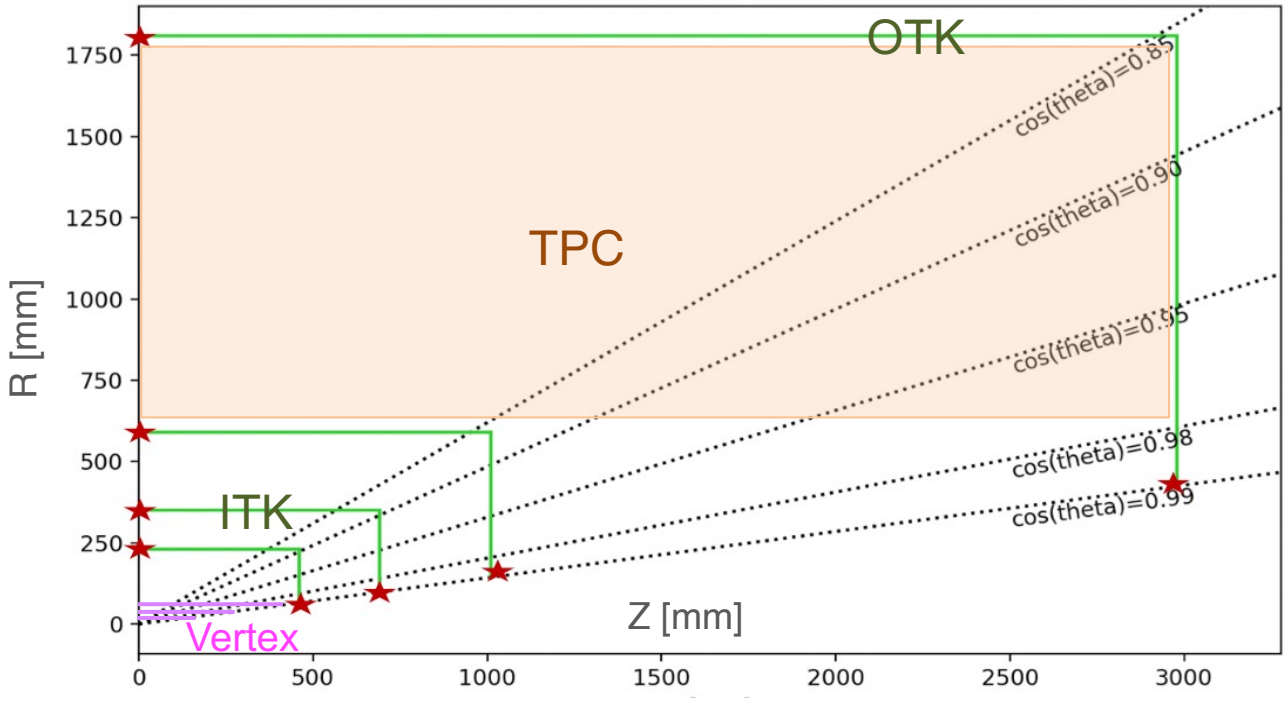
Towards CEPC Silicon Tracker TDR

Qi Yan *on behalf of the ITK+OTK Group*

July 9, 2024, IHEP

Overall Status of the CEPC Tracker TDR

The CEPC Tracker includes detectors of the Vertex, Inner Silicon Tracker (ITK), Time Projection Chamber (TPC), and Outer Silicon Tracker (OTK). The Technical Design Reports (TRDs) for all these components must be completed simultaneously within a short time frame. The task is urgent, and each subsystem needs to produce high-quality oral and written reports promptly to meet the stringent international review standards.



Currently, the development progress of each subsystem of the tracker is uneven. The design and development maturity of the Vertex, TPC, OTK detectors are far ahead of the ITK. The ITK lacks a baseline for the overall detector design scheme.

CEPC TDR Requirement

CEPC

Conceptual Design Report

Volume II - Physics & Detector

4	**Tracking System**		**139**
4.1	Vertex Detector		139
	4.1.1	Performance requirements and detector challenges	141
	4.1.2	Baseline design	141
	4.1.3	Detector performance studies	142
	4.1.4	Beam-induced background in the vertex detector	145
	4.1.5	Sensor technology options	146
	4.1.6	Mechanics and integration	147
	4.1.7	Critical R&D	149
	4.1.8	Summary	150
4.2	Time Projection Chamber and Silicon Tracker		150
	4.2.1	Time Projection Chamber	150
	4.2.2	Silicon Tracker	165
	4.2.3	TPC and silicon tracker performance	169
4.3	Full Silicon Tracker		170
	4.3.1	Full silicon tracker layout	170
	4.3.2	Detector simulation and reconstruction	173
	4.3.3	Tracking performance	174
	4.3.4	Conclusion	175
4.4	Drift Chamber Tracker		175
	4.4.1	Introduction	177
	4.4.2	Expected performance	180
	4.4.3	Tracking system simulation results	181
	4.4.4	Backgrounds in the tracking system	182
	4.4.5	Constraints on the readout system	184

Compared with the CDR (Conceptual Design Report), the TRD should at least demonstrate the level of “Technical Design Report”,

- Especially, following aspects for each subsystem:

  1: Beseline detector

  2: Readout electronics

  3: Mechanics and cooling

  4: Detector performance

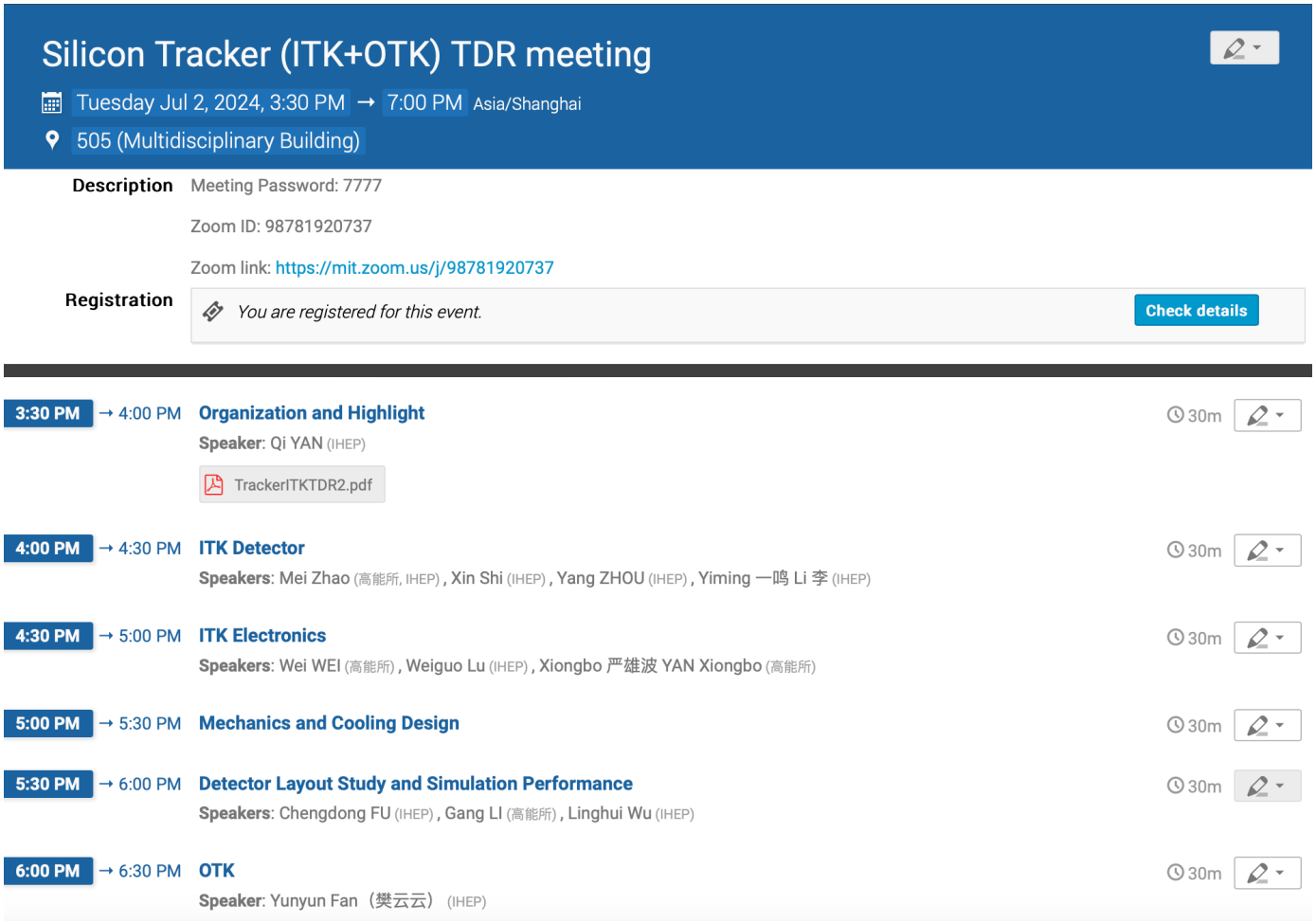
  5: Costs

  …

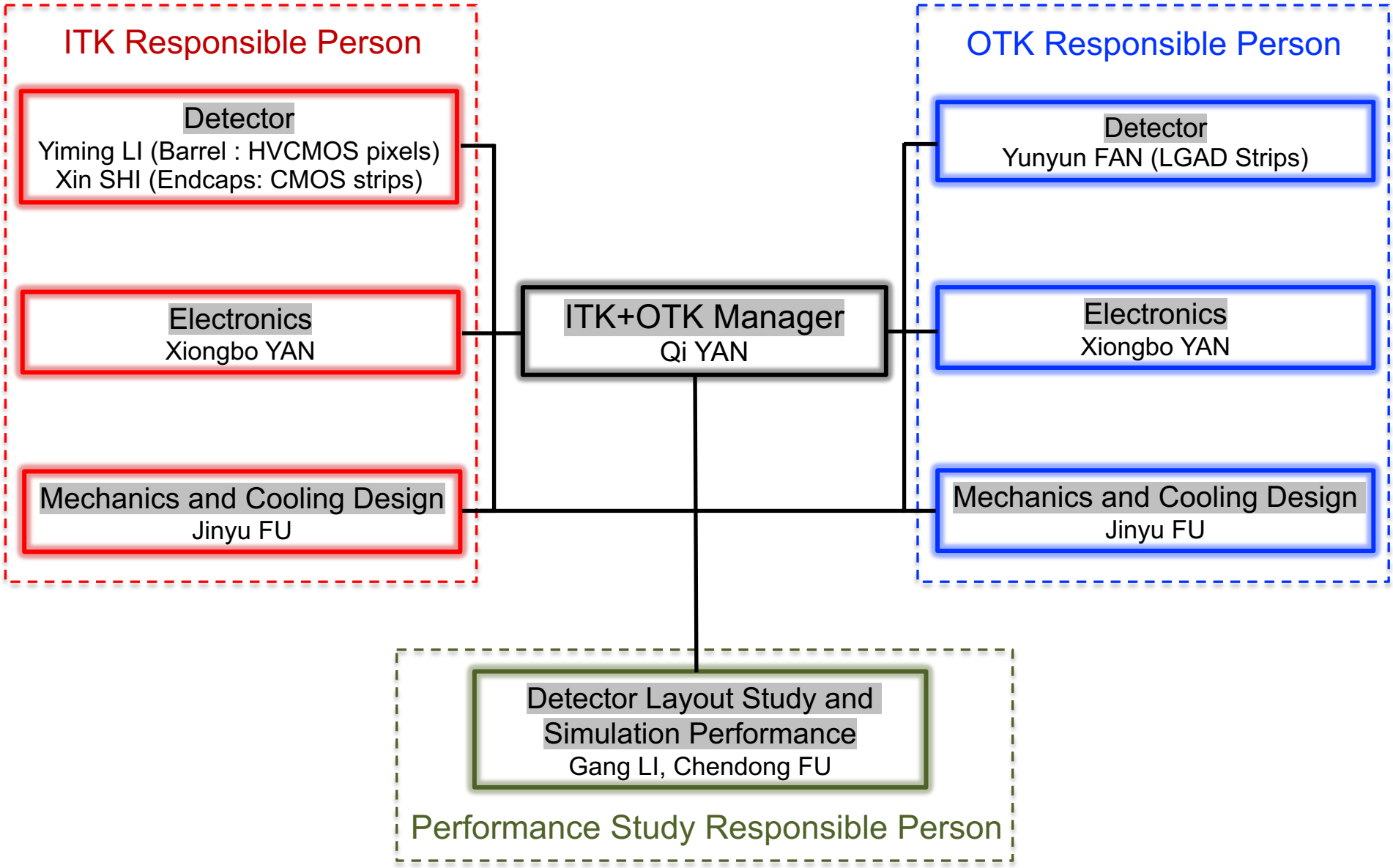
- Simulation and performance of the whole tracker system

Silicon Tracker TDR Meeting

In addition to the general tracker meeting on Friday, I organized our first specific meeting last Tuesday on Silicon Tracker TRD, primarily focusing on the ITK-related issues. We will continue this meeting at least weekly, along with other regular discussions. My office has been rearranged into a meeting room to facilitate these discussions.



New ITK+OTK Personal Assignment and Task Arrangement



Baseline of ITK Detector and Readout Electronics and Responsibilities

- Barrel detector, HVCMOS COFFEE 55nm process pixels:
  Task: Overall detector design, counting rate, power consumption, and cost estimation
  Responsible: Yiming LI
- Endcap detector, double-side monolithic CMOS silicon strips:
  Task: Overall detector design, counting rate, power consumption, and cost estimation
  Responsible: Xin SHI
- CMOS chip electronics development:
  There will be regular exchanges involving Yang ZHOU/HVCMOS-pixels, Weiguo LU/CMOS-strips, Xiongbo YAN, and others to promote the development of CMOS chip electronics.
- Readout electronics design:
  Task: Design of chip PCB and readout system, managed by Xiongbo YAN
- Readout system chain:
  1: Detector design (including quad or ladder module) and counting rate estimation: Yiming LI, Xin SHI, Qi YAN
  2: Chip readout: Yang ZHOU (Weiguo LU), Xiongbo YAN
  3: Chip PCB and readout system design: Xiongbo YAN

Responsibilities for Layout and Simulation Performance Study, and Mechanical and Cooling Design

- Layout optimization and performance study (including Barrel and Endcaps):

  1: The overall design of the detector will adhere to the current layout scheme and will not be changed at this time.

  2: The layout optimization study is independent of current detector baseline design until it has been finalized.

  Responsible: Gang LI

- Simulation software interface and reconstruction for the silicon tracker:
  Responsible: Chengdong FU

- Mechanical and cooling system design for the silicon tracker:
  Responsible: Jingyu FU

ITK TDR Chapter: Introduction and Sections

6.5 Silicon inner tracker

The baseline desgin of the CEPC inner tracker comprises 3 layers of barrel detectors and 3 layers of endcap detectors, as shown in Figure XXX. To optimize both readout rate and detector peformance, different detector technologies are utilized in the barrel and endcap parts. The barrel part is optimized using HV-CMOS pixels detectors, while the endcap part employs double-side CMOS silicon strips detectors. The pitch size and wire routing scheme for the silicon strip sensors in the endcaps are specifically designed to minimize track multiplicity ambigurity, achieving a performance level comparable to that of pixel detectors. This section will cover the detector based on advanced sensor technology and its research and development (R&D), sensor layout, readout electronics, as well as the mechanical design and cooling systems for the baseline inner tracker of the CEPC.

Responsible person: Qi YAN

6.5.1 Inner tracker barrel . . . . . .
6.5.1.1 HV-CMOS sensor and R&D . . . . . .
6.5.1.2 Quad sensor module and layout in barrel . . .
6.5.2 Inner tracker endcaps . . . . . .
6.5.2.1 Double-side CMOS silicon strip and R&D . .
6.5.2.2 Sensor ladder and layout in endcaps . . . . .
6.5.3 Readout electronics . . . . . .
6.5.4 Mechanical and cooling design . . . . . .
6.5.5 Costs . . . . . .
6.5.6 Prospects and backup plan . . . . . .

ITK TDR Sections and Responsible Persons

6.5.1 Inner tracker barrel

Overall introduction and review of pixel detector technology.

Responsible person: Qi YAN, Yiming LI

6.5.1.1 HV-CMOS sensor and R&D

Pixel size: 150×25 μm^2

Responsible person: Yang ZHOU, Mei ZHAO

6.5.1.2 Quad sensor module and layout in barrel

Responsible person: Yiming LI, Qi YAN

6.5.2 Inner tracker endcaps

Overall introduction and review of strip detector technology.

Responsible person: Qi YAN, Xin SHI

6.5.2.1 Double-side CMOS silicon strip and R&D

p-side implantation (readout) strip pitch: 20 (60) μm

n-side implantation (readout) strip pitch: 100 (200) μm

Responsible person: Xin SHI, Weiguo LU, Mei ZHAO

6.5.2.2 Sensor ladder and layout in endcaps

Responsible person: Xin SHI, Qi YAN

6.5.3 Readout electronics

Responsible person: Xiongbo YAN

6.5.4 Mechanical and cooling design

Responsible person:

6.5.5 Costs

Responsible person: Yiming LI, Xin SHI, Xiongbo YAN, ...

6.5.6 Prospects and backup plan

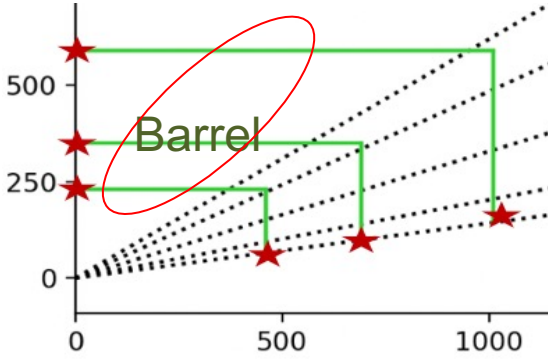
Prospects: HV-CMOS pixel and CMOS silicon strip detector

Backup plan: Hybrid double-side strip detector

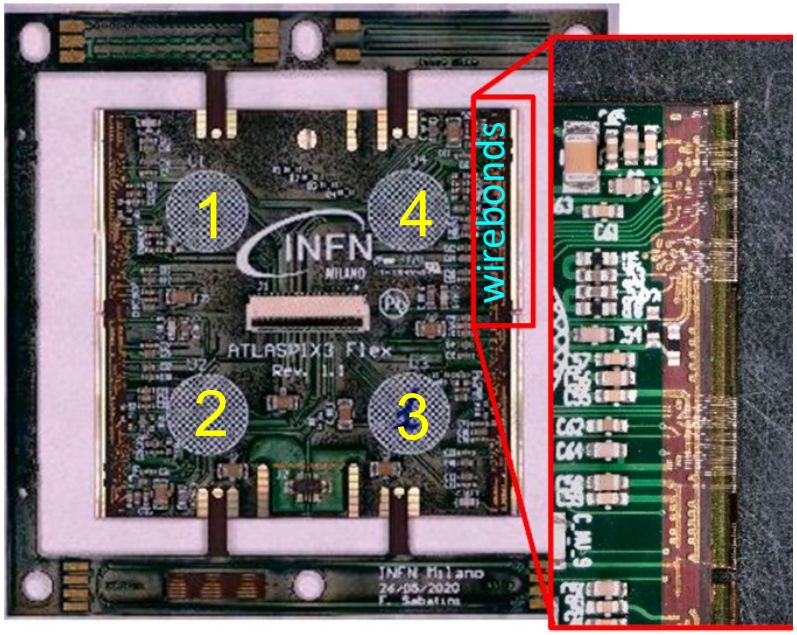
Responsible person: Qi YAN, Yiming LI, and Xin SHI

Proposed HVCMOS Pixels for ITK Barrel Baseline

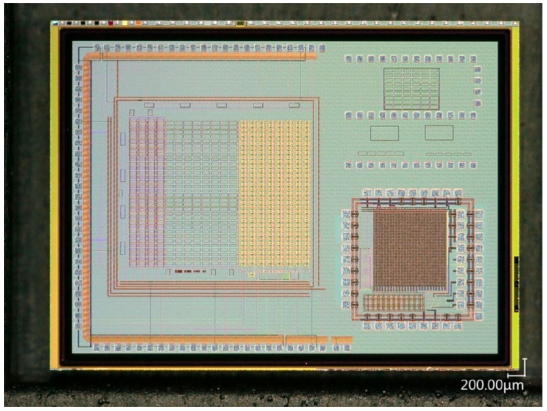
- COFFEE (HVCMOS) based on sensor technology ATLASPix3:
  - 55nm HVCMOS process
  - Pixel size: 150 µm × 25 µm
  - Resistivity of wafer: 1k-2k Ohm cm



- Quad modules consist of an array of 2 × 2 sensors:



Quad module of 4 ATLASPix3 chips

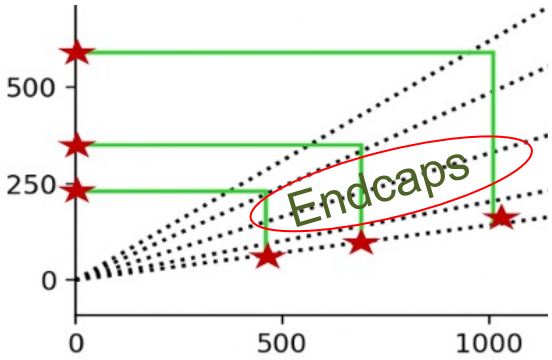


COFFEE2 test chip

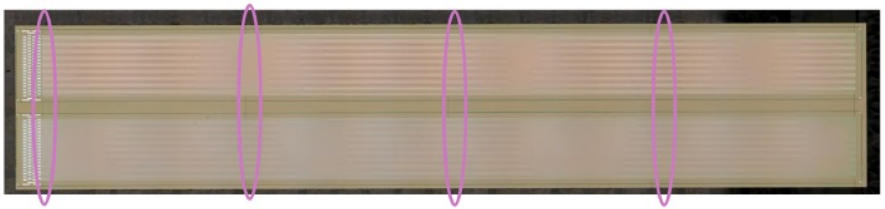
Yang ZHOU, Mei ZHAO, Weiguo LU, Yiming LI, and … contribute to the development.

Proposed CMOS Silicon Strips for ITK Endcap Baseline

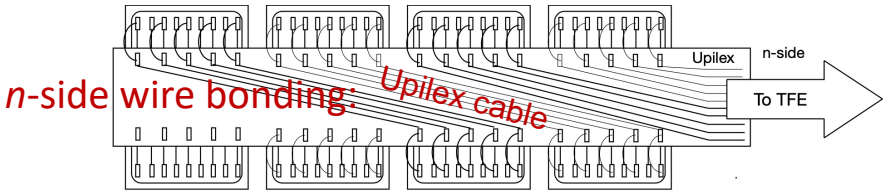
- Based on sensor design for ATLAS ITk strips. First CMOS stitched strip sensor has been produced on 8” wafer by commercial foundry:
  - L-Foundry 150 nm process (deep N-well/P-well), float-zone processing
  - Up to 7 metal layers
  - Resistivity of wafer: > 2k Ohm cm



- Frontside process: Reticle stitching for large sensors



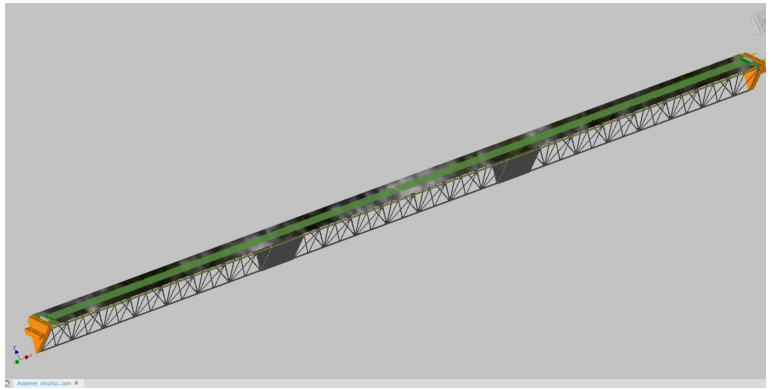
- Double-side strip detector:
  - *p*-side implantation (readout) pitch: 20 µm (60 µm)
  - *n*-side implantation (readout) pitch: 100 µm (200 µm)

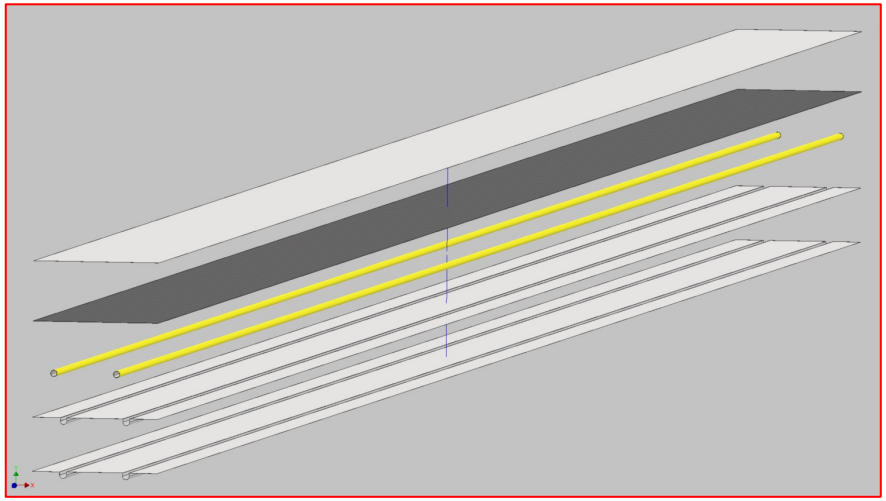


Xin SHI, Mei ZHAO, Weiguo LU, and … have launched the development.

ITK Mechanics Design

- The mechanics design of ITK is not yet complete, especially the endcap section. This part is urgent and essential as it is integrated with the detectors, electronics, and cooling design. Jingyu FU and I reached an initial agreement on the design yesterday. We will continue our discussion at next ITK meeting.





OTK TDR Chapter: Sections and Responsible Persons

4.6 Silicon ToF and outer tracker

Responsible person: Yunyun FAN

4.6.1 Performance requirement

Responsible person: Yunyun FAN, Gang LI...

4.6.2 Overall review - Barrel and endcap design

Responsible person: Yunyun FAN

4.6.3 Sensor

Responsible person: Mei Zhao

4.6.4 Readout electronics

Responsible person: Xiongbo YAN

4.6.5 Module and assembly

Responsible person: Yunyun FAN

4.6.6 Mechanical and cooling design

Responsible person: Jinyu Fu

4.6.7 Cost

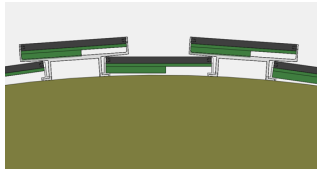
Responsible person: Yunyun FAN

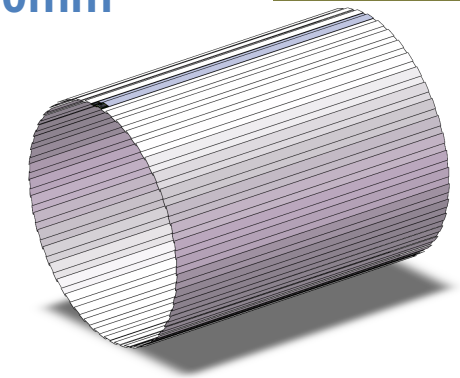
Mechanics and Module of OTK Barrel

- One layer: 3780 modules

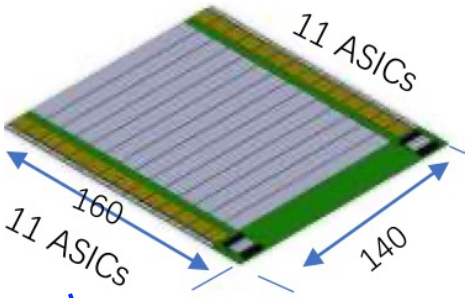
  90 ladders, 45 ladders each side
  - ✓ 42 modules/ladder,
  - ✓ 22 ASIC/module, 128 Channel/ASIC
- The cooling issue should be considered
  - ✓ Simulation on going

One layer ToF
R= 1800 mm
H～5800mm

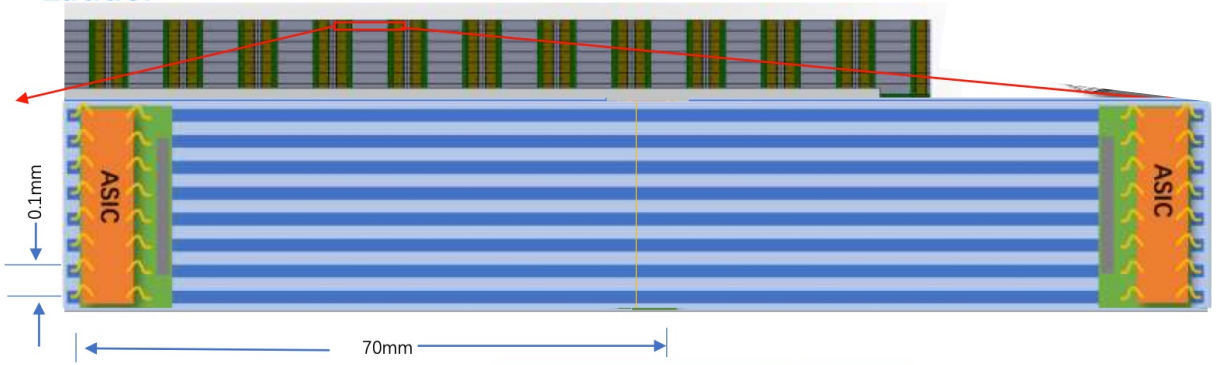


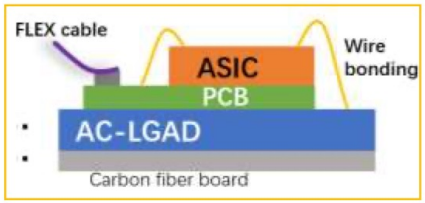


Module
140mm x 160mm



Ladder





Provided by Yunyun FAN

Outline of the Entire Tracker TDR

The CEPC is designed as a next-generation particle accelerator to explore the frontiers of high-energy physics. A crucial detector component of the CEPC is the tracker system, which provides highly precise position measurements for accurate reconstruction of charged particle trajectories, determining particle momentum, and reconstructing interaction vertices with high accuracy.

The CEPC tracker system incorporates advanced silicon sensor technology for precise position measurements. Its mechanical design is optimized to minimize material traversal, and in conjunction with the gaseous detector, enhances the quality of track measurements at low momentum. Additionaly, the system integrates precision time measurement of charged particles with advanced semiconductor detectors and detects primary ionizations in gaseous detector to enhance particle identification (PID) capabilities. The electronics and cooling system of the tracker system are designed to efficiently process massive amounts of data, ensuring reliable data acquisition.

Responsible person: Qi YAN, ...

Chapter 1 Tracker

1.1 Requirements . . . . .
1.2 Tracker system overview . . . . .
1.3 Vertex . . . . .
1.4 Time Projection Chamber tracker . . . . .
1.5 Silicon inner tracker . . . . .
1.6 Silicon outer tracker with TOF . . . . .
1.7 Performance of the whole tracker system . . . . .
1.8 Summary . . . . .

王萌

革命尚未成功，同志仍需努力😁