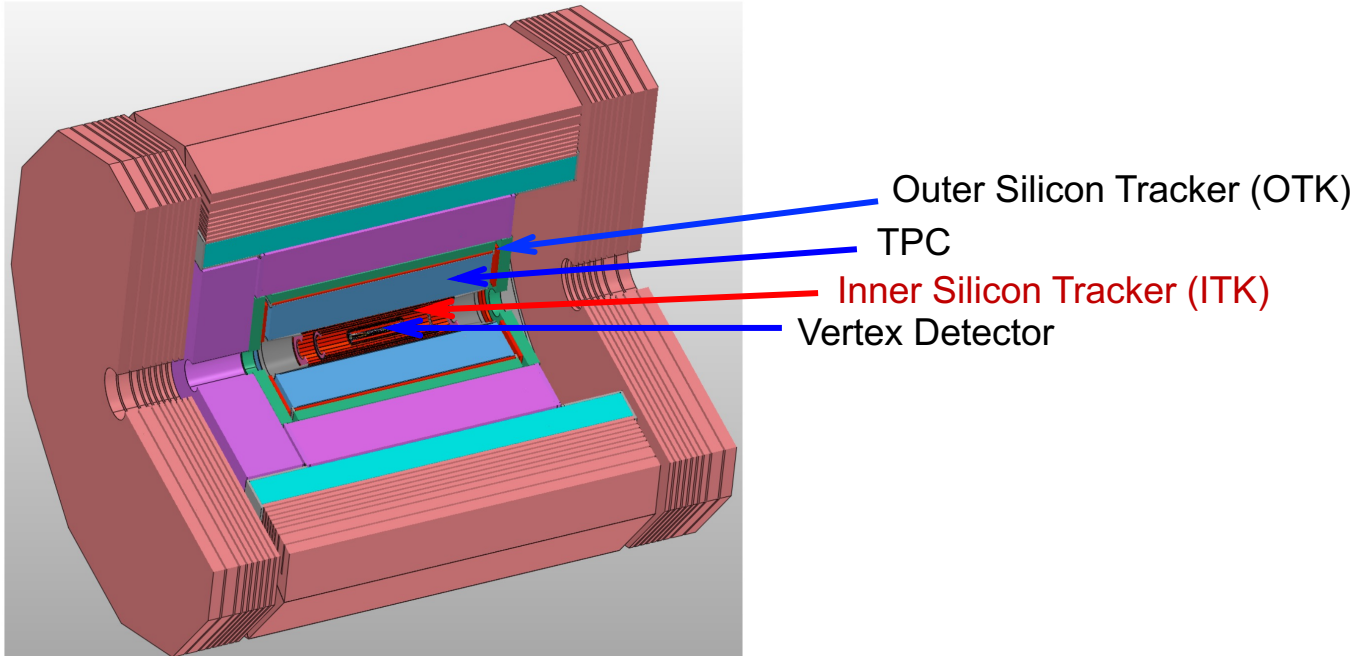
Towards CEPC Silicon Tracker TDR

Qi Yan *on behalf of the Silicon Tracker Group*

CEPC Day, Aug 5, 2024, IHEP

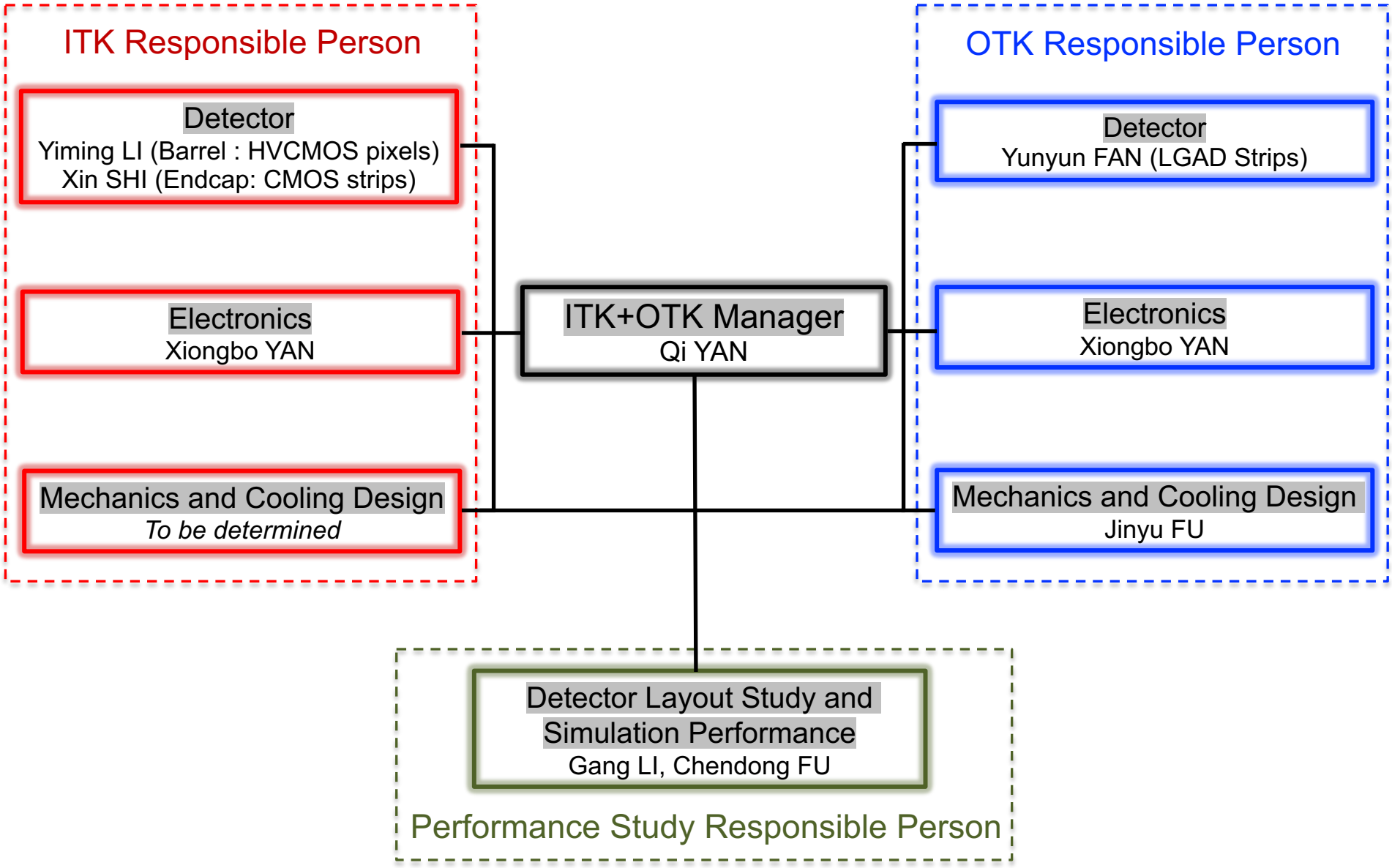
Overview of CEPC Tracker TDR Progress

The CEPC Tracker includes detectors of the Vertex, Inner Silicon Tracker (ITK), Time Projection Chamber (TPC), and Outer Silicon Tracker (OTK). I have been responsible for the Silicon Tracker since June 28, 2024. Over the past month, my primary focus has been on the ITK, as it's the most urgent and lacks a baseline design for the overall detector scheme.



Through extensive efforts with our colleagues in the ITK group, we have developed the first complete baseline version of the ITK. Although time constraints prevented us from achieving a a perfect detector baseline, this initial version still includes several unique design features compared to existing experiments.

New ITK+OTK Personal Assignment and Task Arrangement



ITK Baseline Tasks

1) Sensor and module design (ladder/stave):
   Parameters and readout of sensor and module (Yang ZHOU, Yiming LI, Xin SHI, Xiongbo YAN, Weiguo LU)
2) Barrel design (HVCMOS pixels)
   2D and 3D layout of the barrel detector (Yiming LI, Qi YAN, Yihan ZHANG)
3) Endcap design (CMOS strips)
   2D and 3D layout of the endcap detector (Xin SHI, Qi YAN, Shoudong LUO)
4) Barrel and endcap counting rate (Li ZHAN, Qi YAN, Xin SHI)
5) Readout electronics design (Xiongbo YAN)
6) Power consumption and costs (Yiming LI, Xin SHI)
7) Mechanics and cooling design (Qi YAN, Yihan ZHANG, Shoudong LUO)
8) Layout optimization and performance study (Gang LI, Qi YAN)
9) Implementation in MC simulation (Chengdong FU)
10) Others

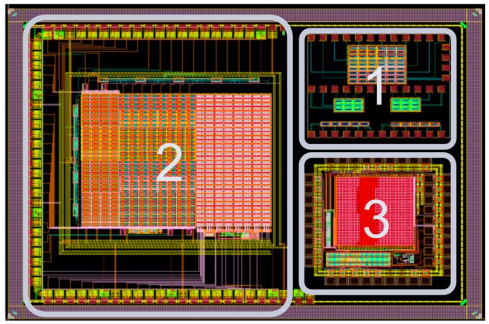
Considerations of HVCMOS Pixels VS CMOS Strips

CMOS sensor technology represents the future direction for silicon tracker:

- Cost-effective due to widespread use in the semiconductor industry
- Combine the active detection layer and the readout electronics into a single device

CMOS SENSOR IN FIFTY-FIVE NM PROCESS

In China, CMOS sensor technology for HEP has not yet been realized. HVCMOS pixels, developed under COFFEE project, have undergone two rounds of R&Ds: COFFEE1 (no HV process, received in April 2023) and COFFEE2 (received in Dec 2023). This development is still in its early stages, and no functional chip has been produced yet.



COFFEE2 test chip:
no performance result yet

HVCMOS pixel technology development in China may face unresolved technical barriers due to interference between the detection layer and chip readout electronics (domestic industry limitation). Both HVCMOS pixels and CMOS strips can, in principle, meet the requirement of CEPC ITK.

Since CEPC presents a unique opportunity to advance HEP semiconductor technology in China, it's wise to also provide opportunity to develop independent CMOS strip sensor technology, which may encounter few barriers and be easier to achieve. Additionally, CMOS strips should offer practical advantages in terms of power consumption and cost.

At current stage of development, it's beneficial to have competition between the two technologies to promote progress.

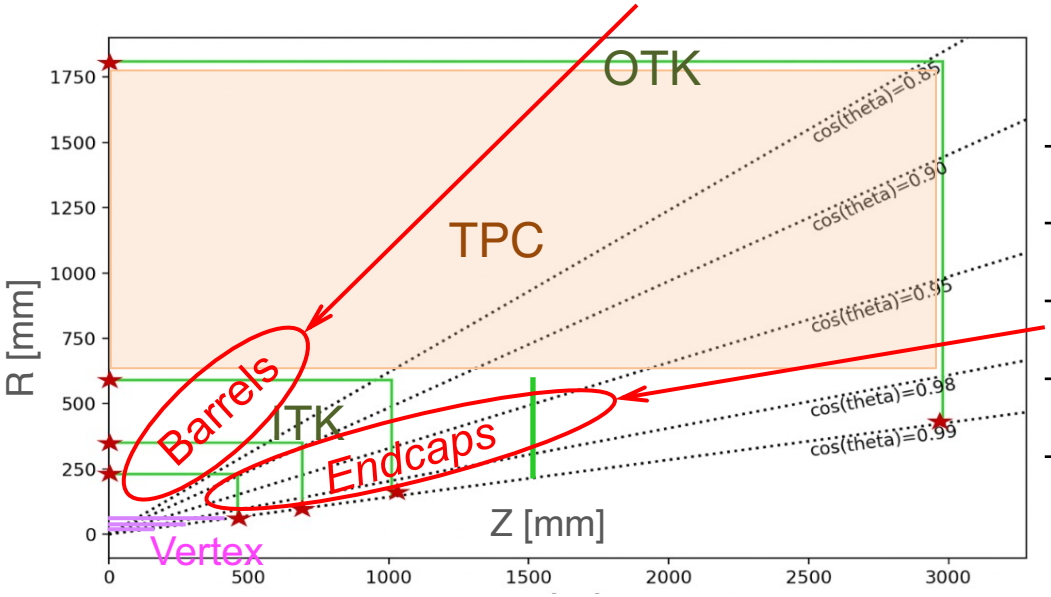
In the short term, within the ITK group, dividing the barrel to use HVCMOS pixels and the endcap to use CMOS strip could help organize and accomplish the ITK baseline most efficiently.

In the future, if both technologies are realized, the final CEPC ITK baseline could integrate HVCMOS pixels and CMOS strips for both the endcaps and barrels.

The first tape-out of the CMOS strip test chip (CSC1) is expected to be submitted before the end of this year.

Barrel and Endcap Layout for the ITK Baseline

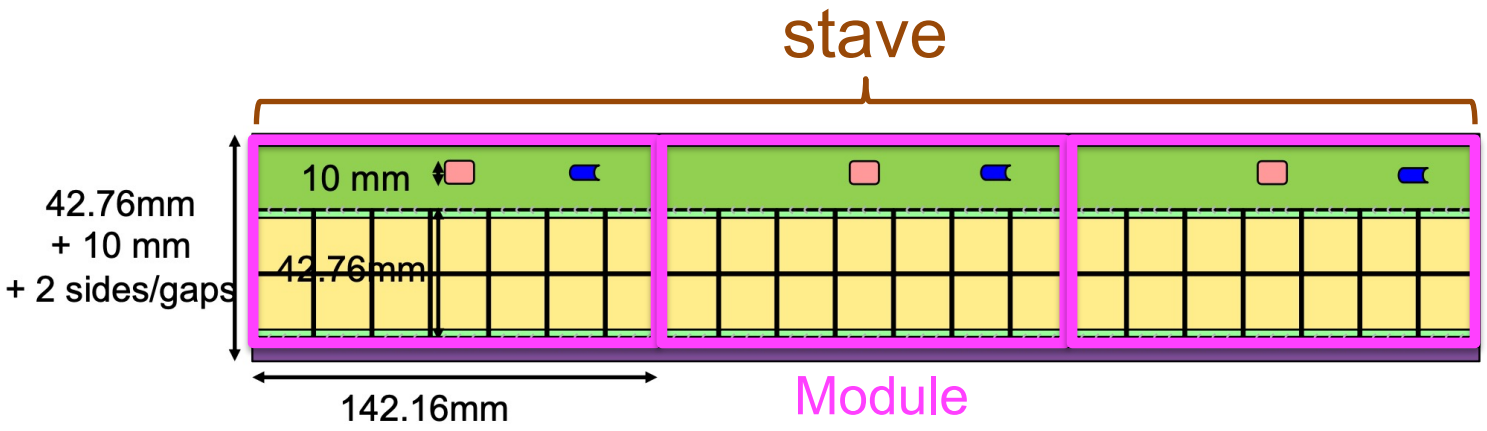
Barrel	ITKB1	ITKB2	ITKB3
R [mm]	240	350	600
Half-Z [mm]	500.5	715	1001



Gang LI *and* Qi YAN

Endcap	ITKE1	ITKE2	ITKE3	ITKE4
|Z|[mm]	500.5	715	1001	1500
R-I [mm]	75	101.9	142.6	214
R-O[mm]	240	350	600	600

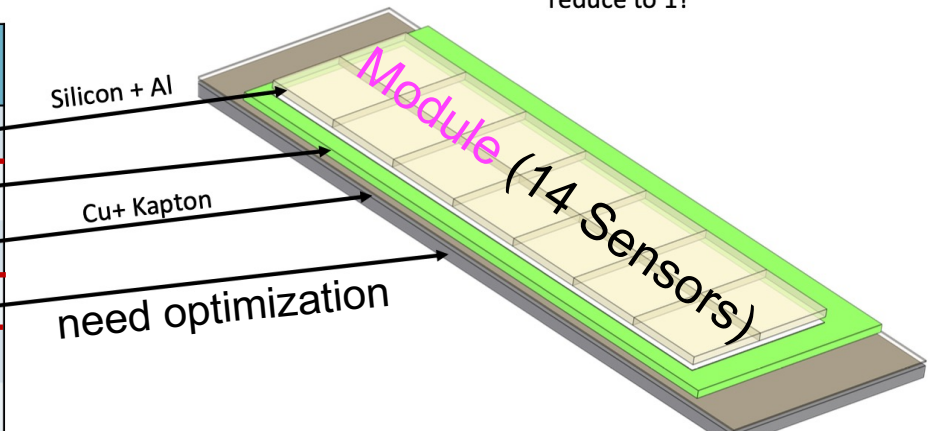
Progress Iteration 1： ITK Barrel Sensor, Module, and Stave



lpGBTx: W=9, L=9
Optical connector: W=10, L=20

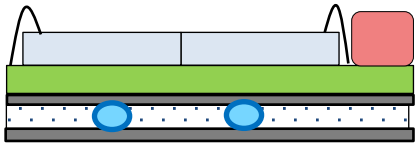
1 lpGBT provides 28×0.32, 14×0.64, or 7×1.28 Gbps **DATA** links
=> 2 lpGBT needed for current bkg rate; may reduce to 1?

	Thickness (mm)	Radiation Length [%X0]
Pixel Sensor	0.150	0.18
HybridFlex	0.200	0.28
Kapton Tape	0.100	0.14
BareStave	4.000	0.21
Optical connector	1.250	0.13
lpGBTx	4.000	0.07

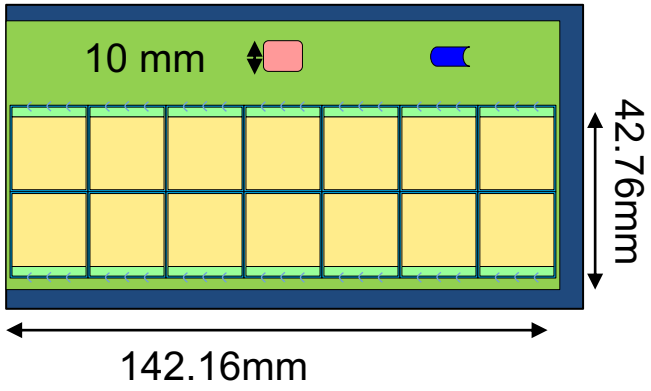


Yiming LI @ ITK+OTK meeting (July 10, 2024)

Latest Progress Iteration 2: New Design of the Barrel Module

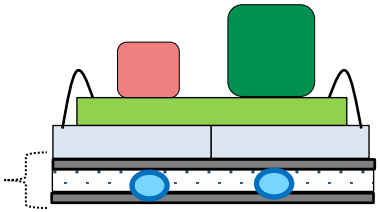


42.76mm
+ 10 mm
+ 2 sides/gaps



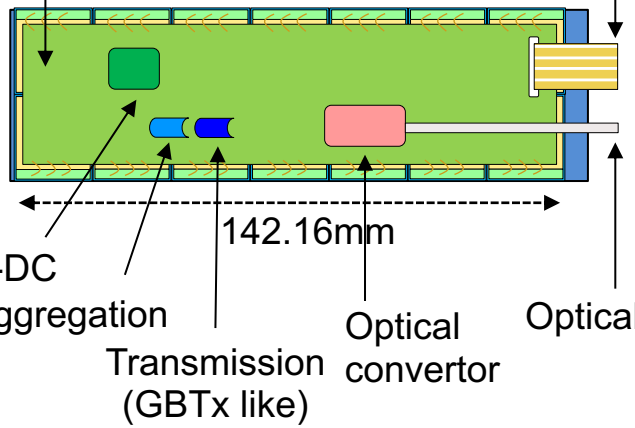
Iteration 1

Yiming LI *et al.* @ ITK+OTK meeting
(July 24, 2024)



Supporting & cooling to
be optimized seperately

42.76mm
~~+ 10 mm~~
~~+ 2 sides/gaps~~

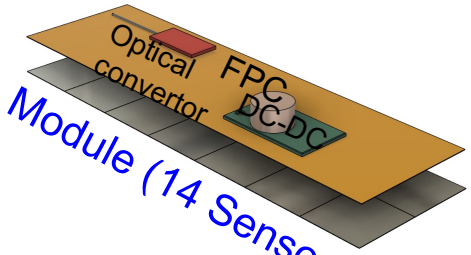


Iteration 2

The new design of the barrel module reduces the inactive area and facilitates the design of the supporting and cooling structure.

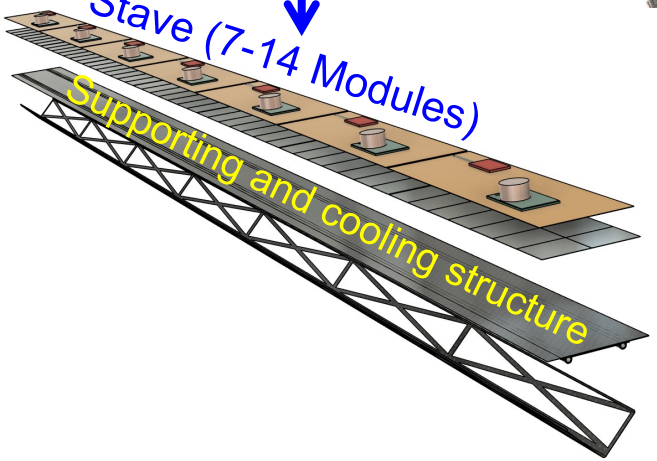
Latest Progress： ITK Barrel Design (3 Barrels)

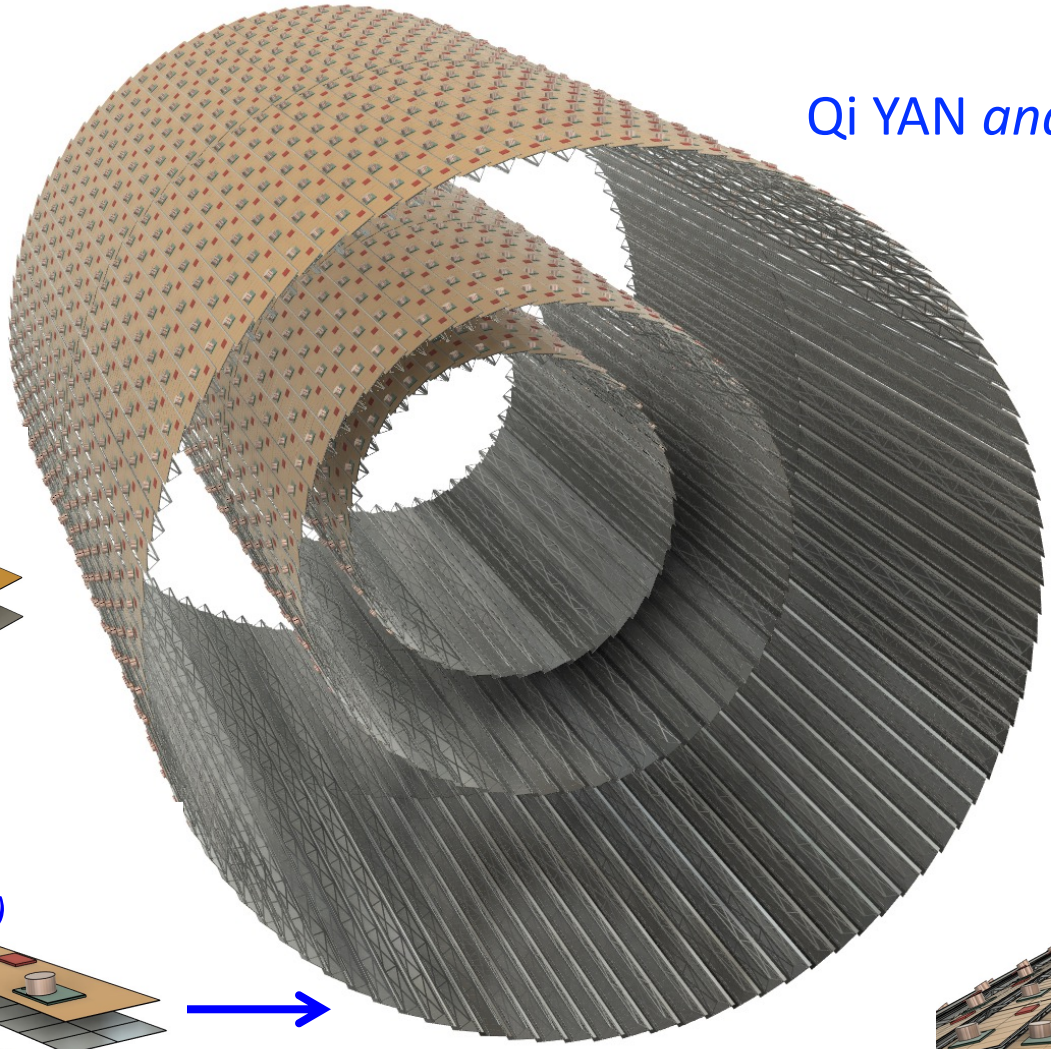
Qi YAN *and* Yihan ZHANG



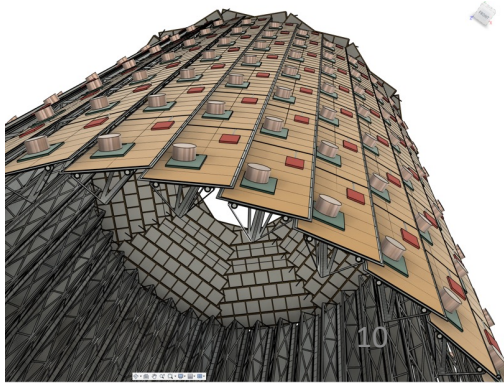
Module (14 Sensors)

Stave (7-14 Modules)



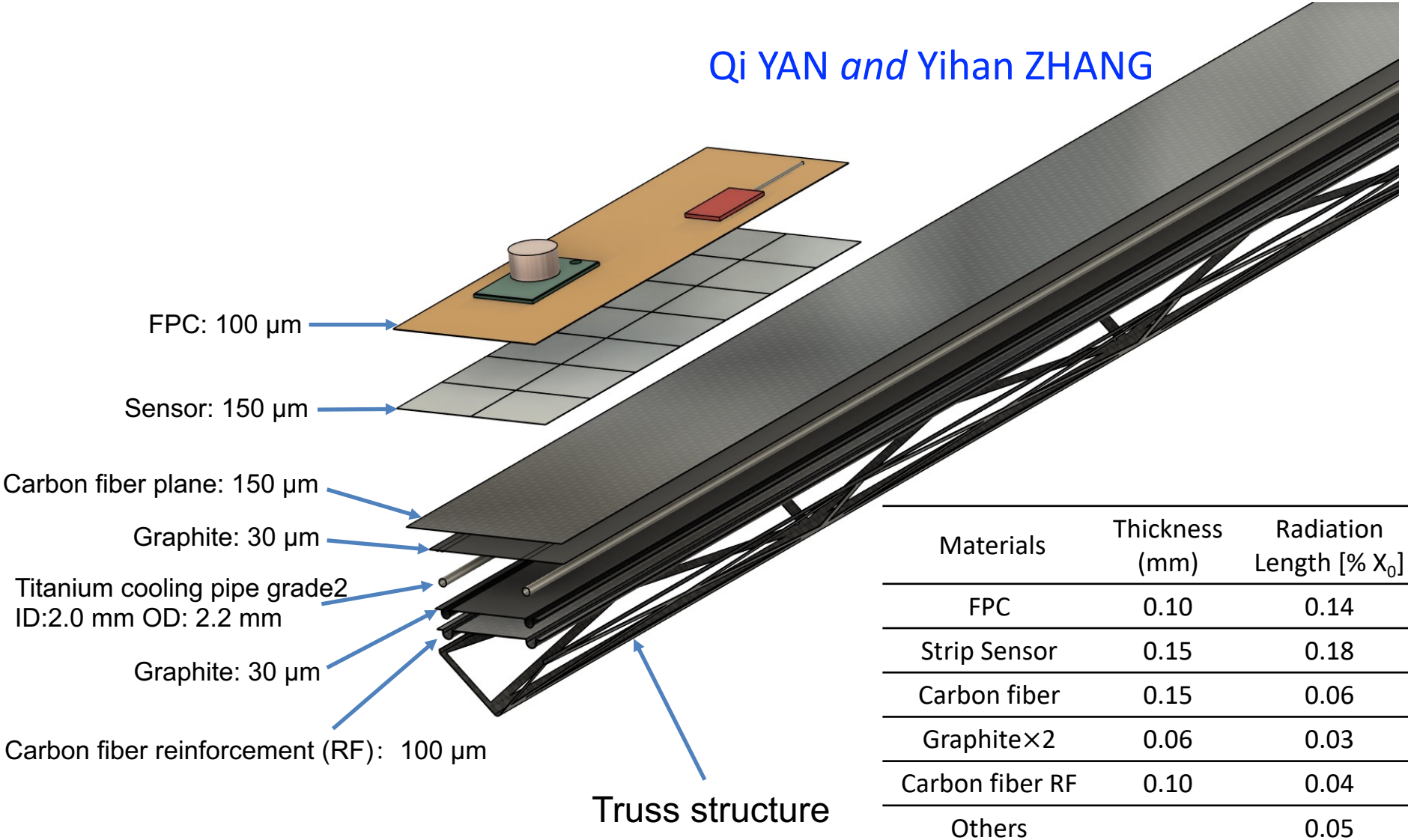


3 Barrels (40-96 Staves Each)



Mechanical and Cooling Design for ITK Barrel

Qi YAN *and* Yihan ZHANG



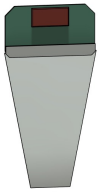
Materials	Thickness (mm)	Radiation Length [% X_0]
FPC	0.10	0.14
Strip Sensor	0.15	0.18
Carbon fiber	0.15	0.06
Graphite×2	0.06	0.03
Carbon fiber RF	0.10	0.04
Others		0.05
Total		0.50

3 Layer ITK Barrels Detector Components

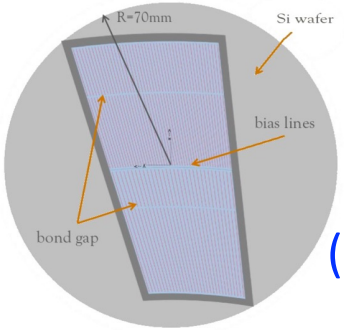
	Modules/Stave	Staves	Modules	Sensors	Sensor area
ITKB1	7	40	280	3920	1.6 m^2
ITKB2	10	58	580	8120	3.2 m^2
ITKB3	14	96	1344	18816	7.5 m^2
Total		194	2204	30856	12.3 m^2

The total power consumption of the chips (excluding other electronic components) is estimated to be 24.6 kW for barrels (200 mW/cm²).

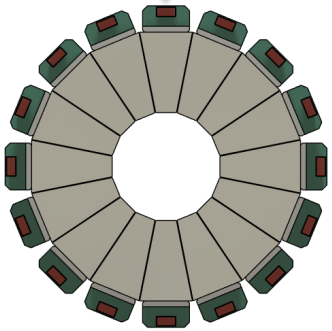
ITK Endcap Design with Trapezoidal Strip Sensor (Plan 1)



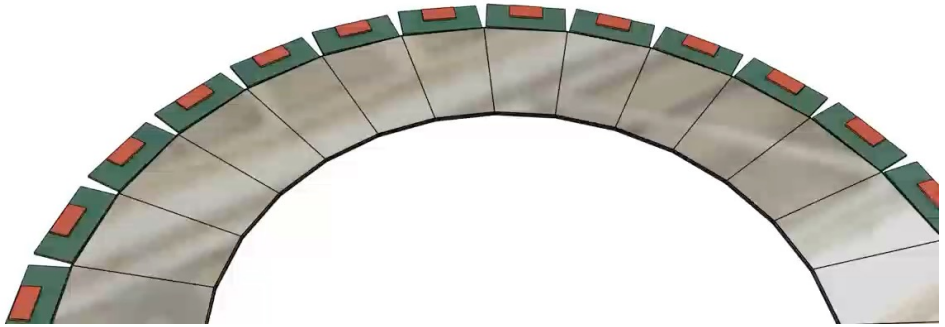
1: sensor

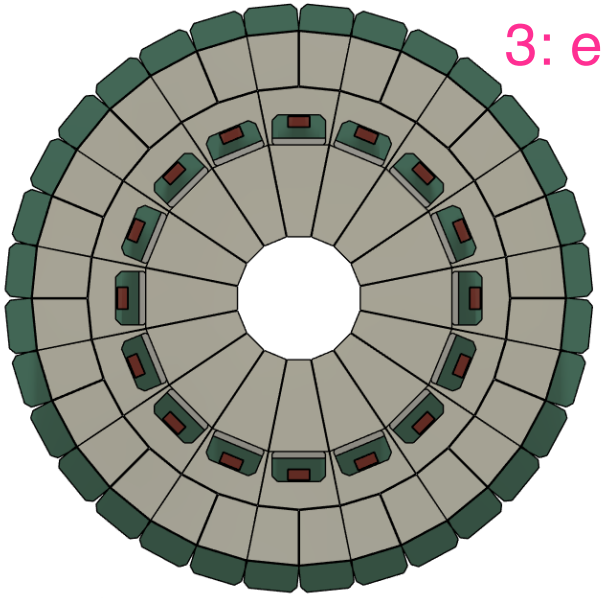


Qi YAN *and* Yihan ZHANG
(CEPC detector meeting, July 16, 2024)



2: ring

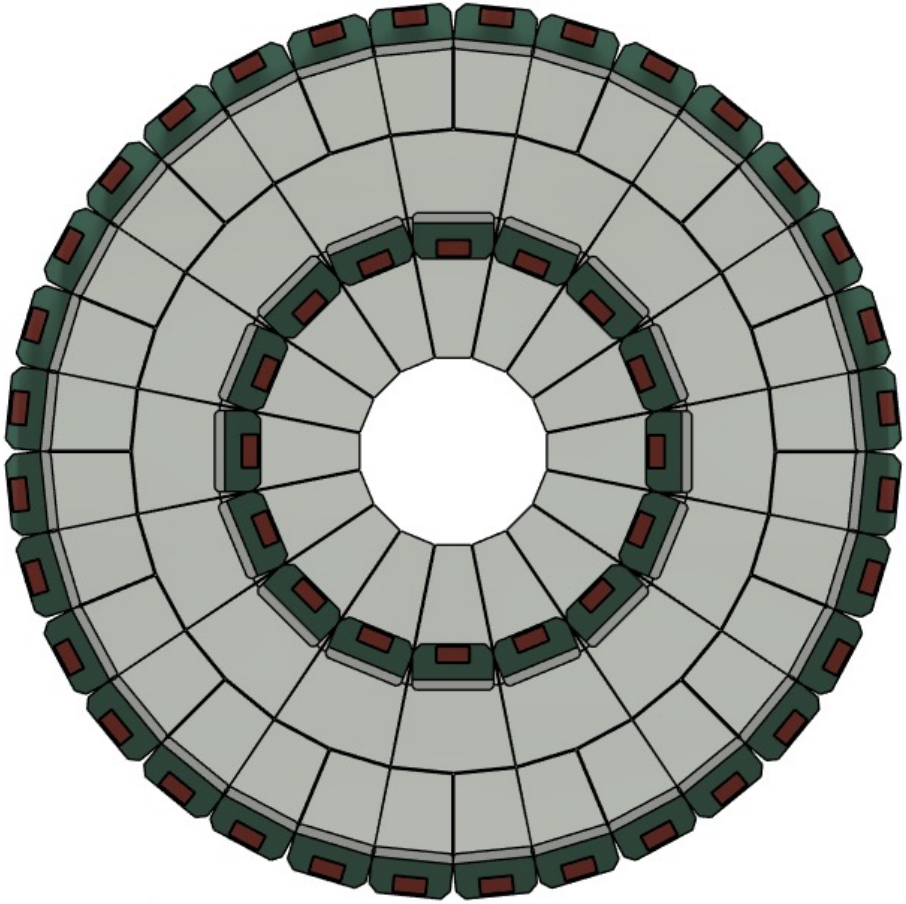




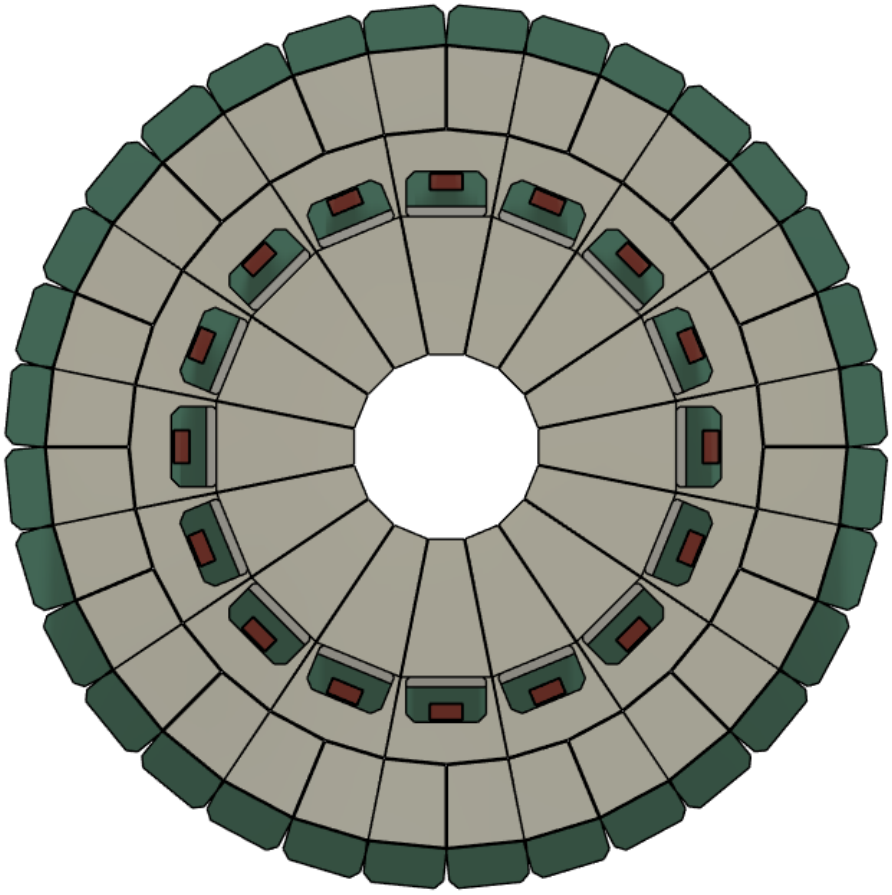
3: endcap

One endcap is divided into 3 rings :
Each ring is composed of trapezoidal sensors.

Qi YAN *and* Yihan ZHANG

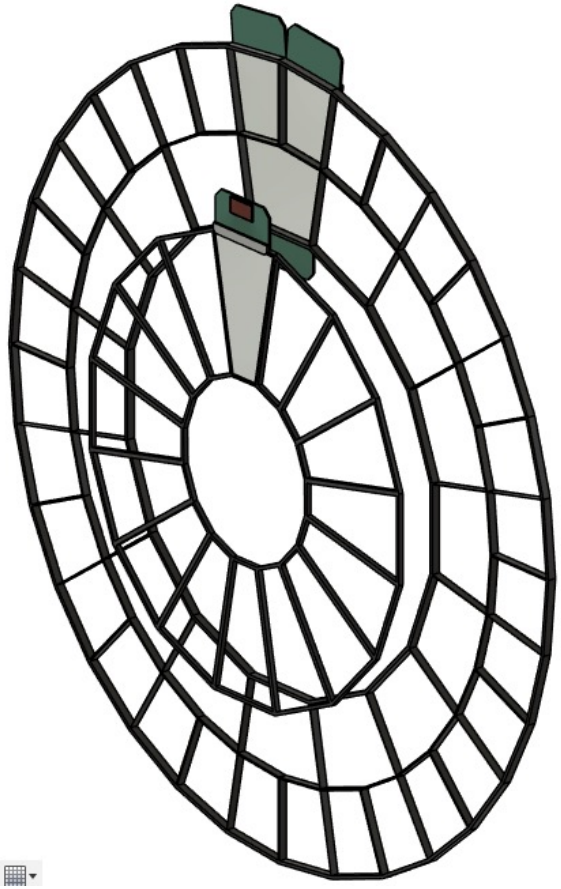


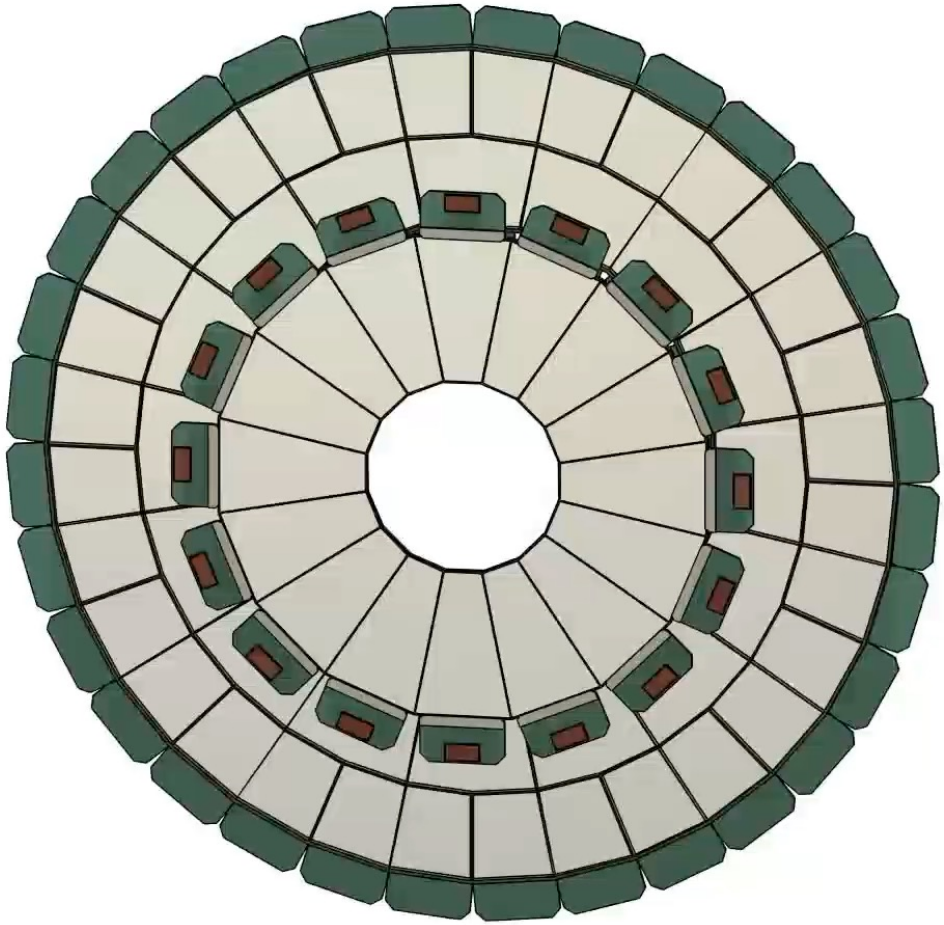
Endcap front view



Endcap back view

Mechanical Design of ITK Endcap (Plan 1)

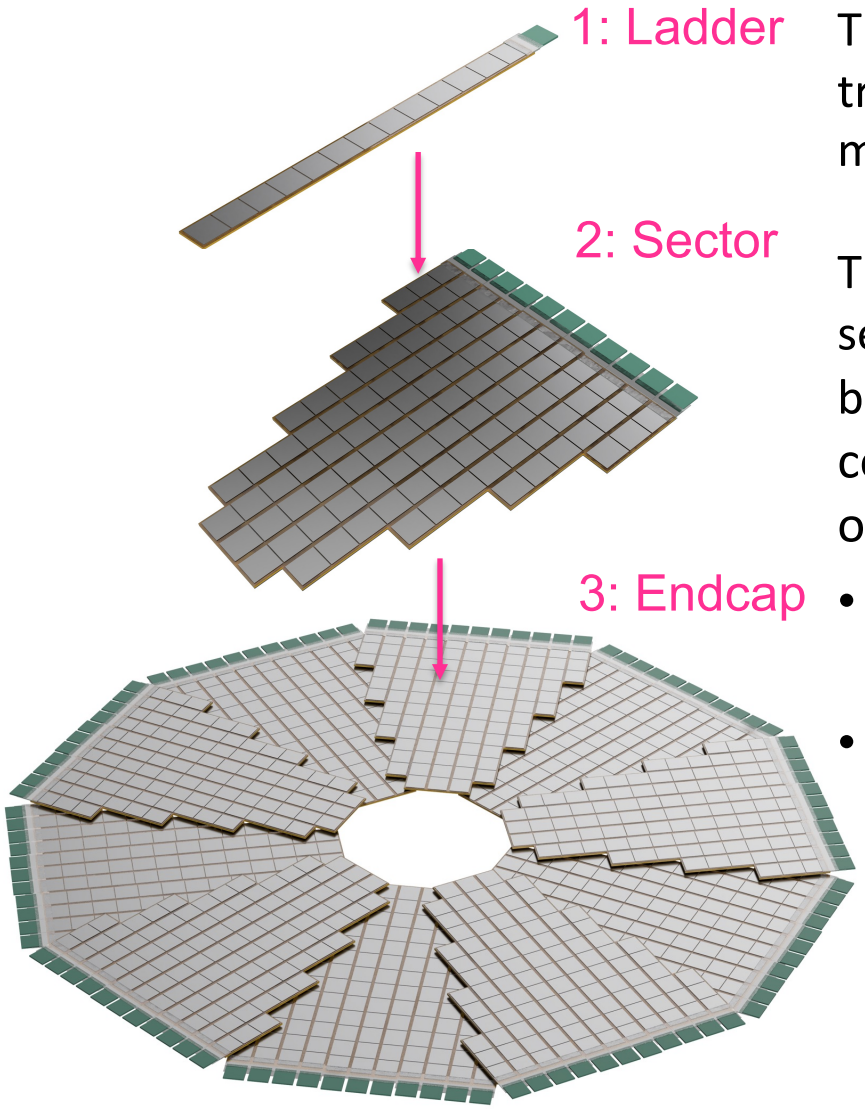




Qi YAN *and* Yihan ZHANG

ITK Endcap Design with Regular Strip Sensor (Plan 2)

Design Iteration 1: Qi YAN *and* Shoudong LUO
(CEPC detector meeting, July 16, 2024)



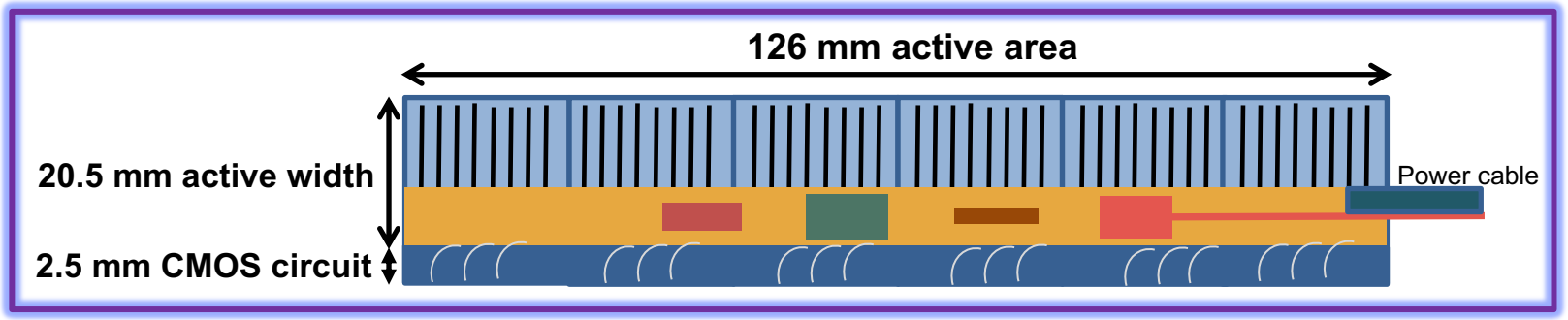
The previous endcap design (Plan 1) requires trapezoidal sensors, which are difficult to manufacture, especially for CMOS sensors.

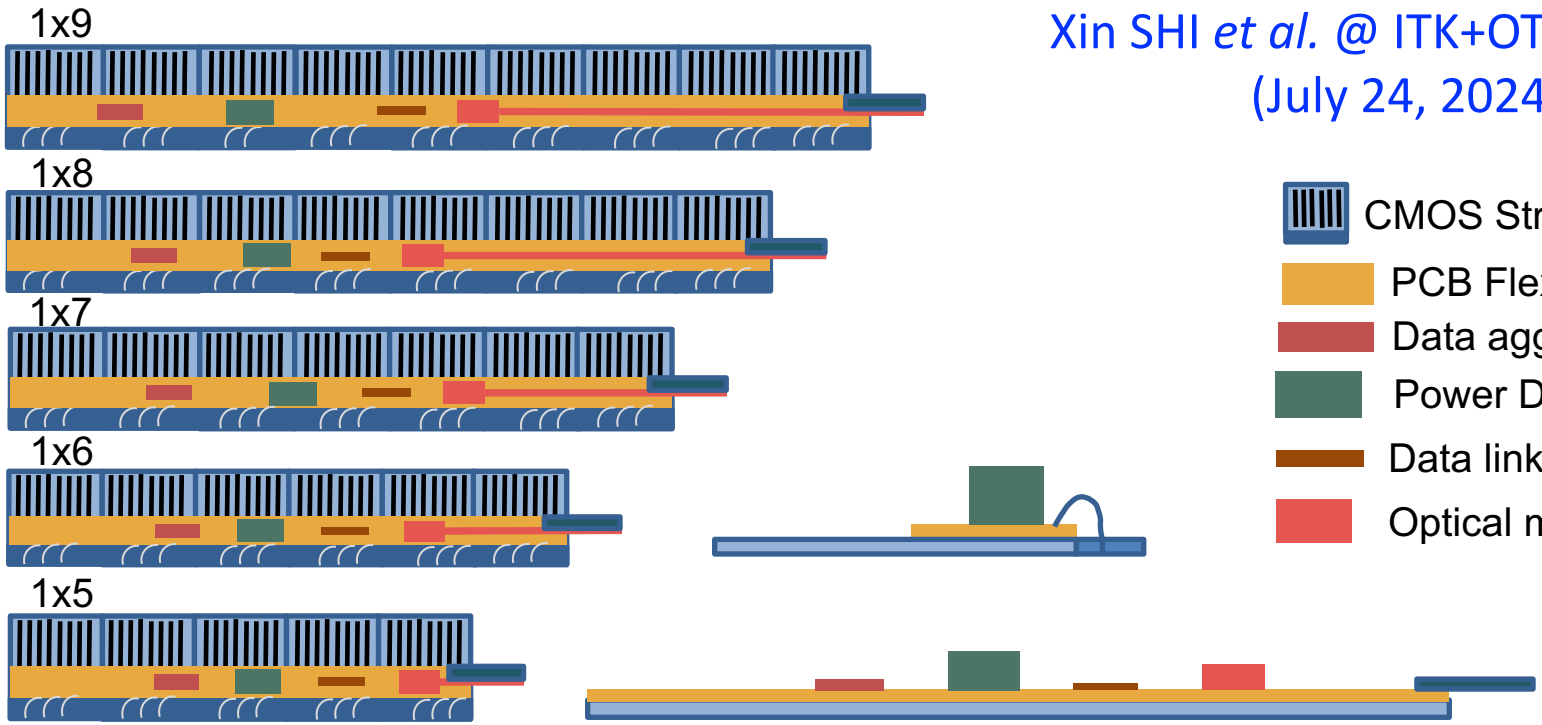
The Plan2 endcap design uses regular CMOS sensor (2.1×2.3 cm^2), which was chosen as the baseline. In this design, each endcap is composed of several sectors with minimal overlapping between neighboring sectors:

- Design Iteration 1: Each sector is composed of longitudinal rectangular ladders.
- Design Iteration 2: Considering the CMOS strip direction and the orthogonal peripheral electronics, the “ladder” structure has been adjusted to be oriented transversely, forming what is called a “module”.

Latest Progress: Strip Sensor Module Design for ITK Endcap

Design Iteration 2: new module design

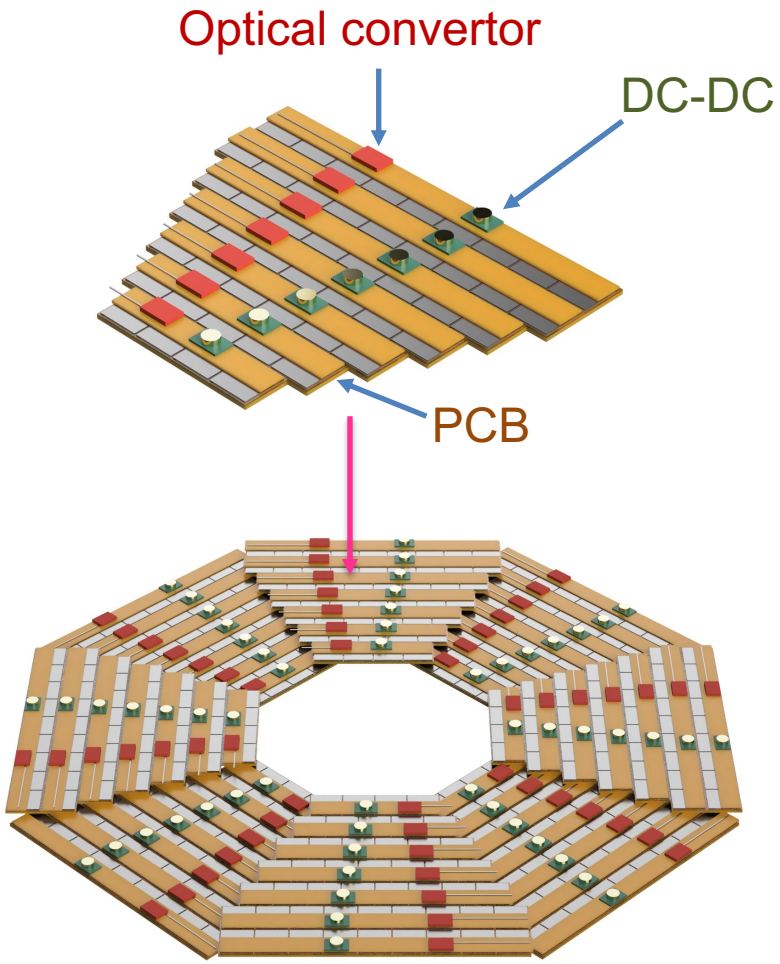




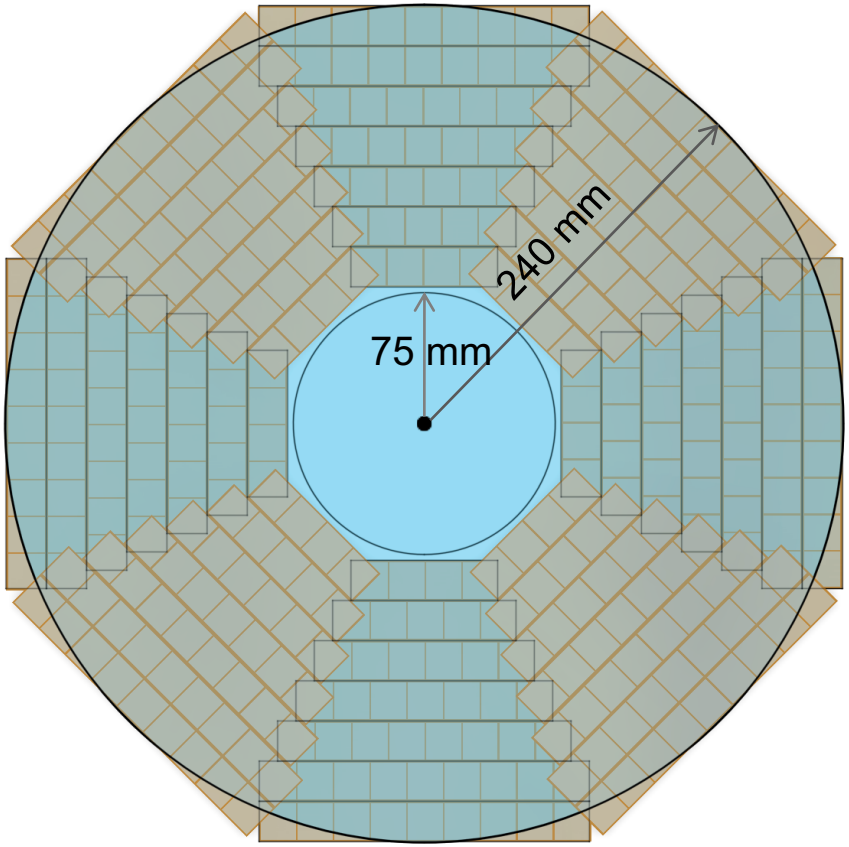
Xin SHI *et al.* @ ITK+OTK meeting
(July 24, 2024)

CMOS Strip Chip - CSC
PCB Flex
Data aggregation
Power DC-DC
Data link (GBTx-like)
Optical module

Latest Progress: The 1st Endcap Baseline Design (ITKE1)



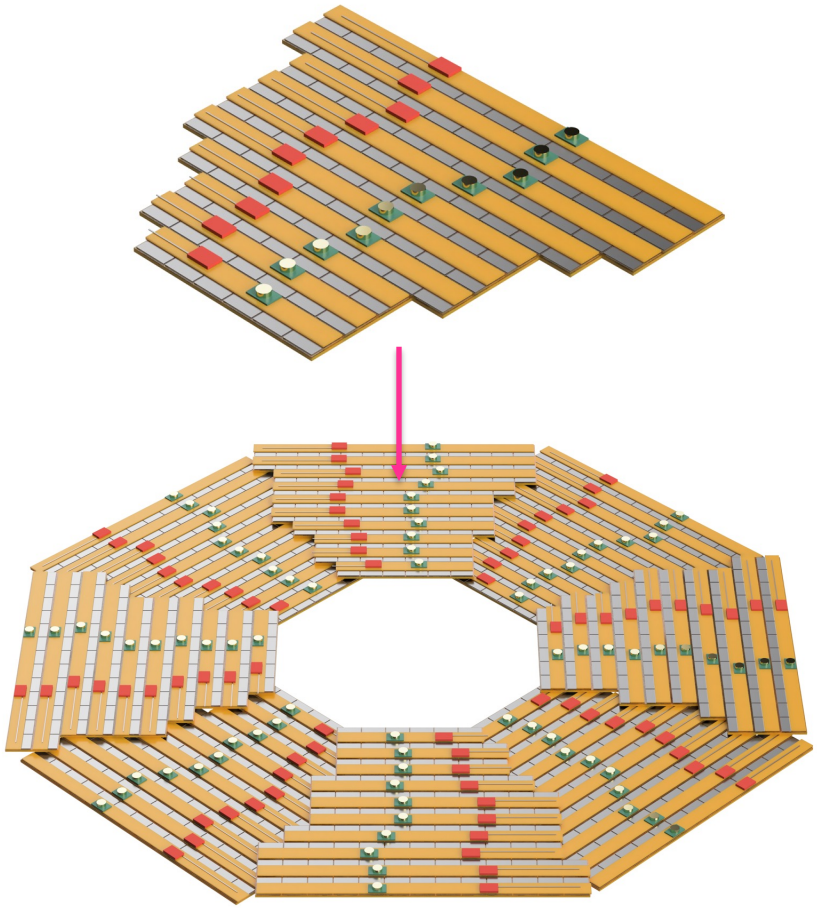
Qi YAN, Shoudong LUO, *and* Xin SHI

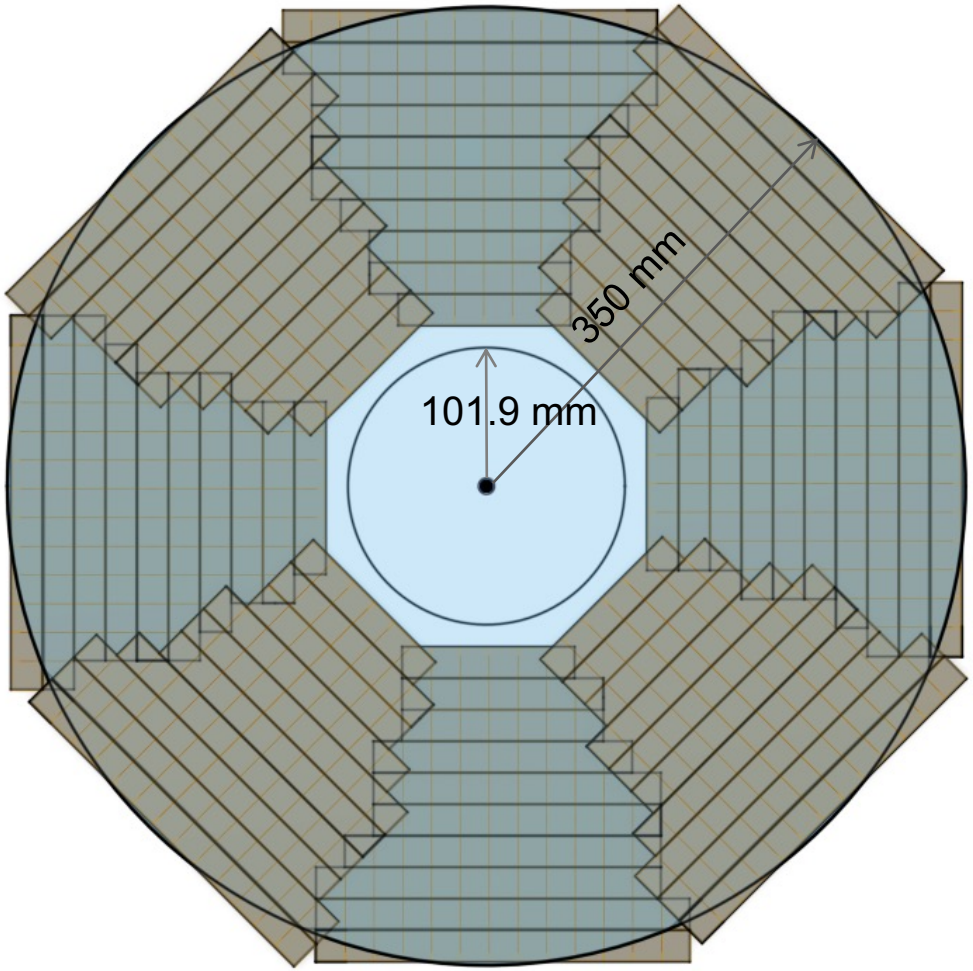


Each half endcap is divided into 8 sectors: Each sector is entirely composed of rectangular modules, with minimal overlapping between sectors.

Latest Progress: The 2nd Endcap Baseline Design (ITKE2)

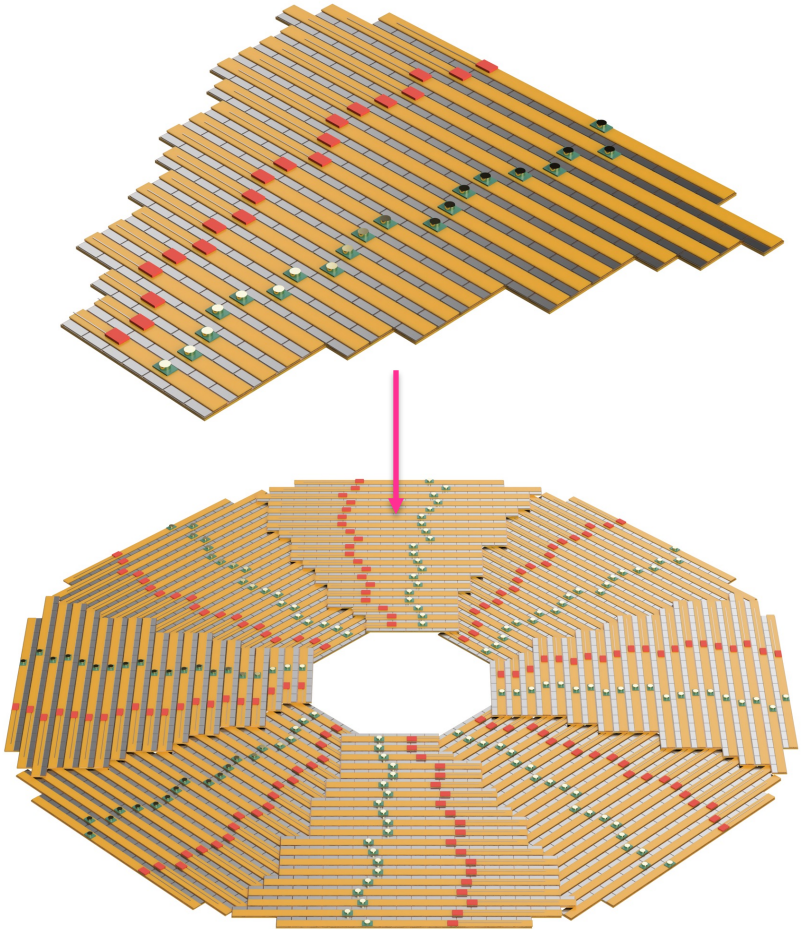
Qi YAN, Shoudong LUO, *and* Xin SHI

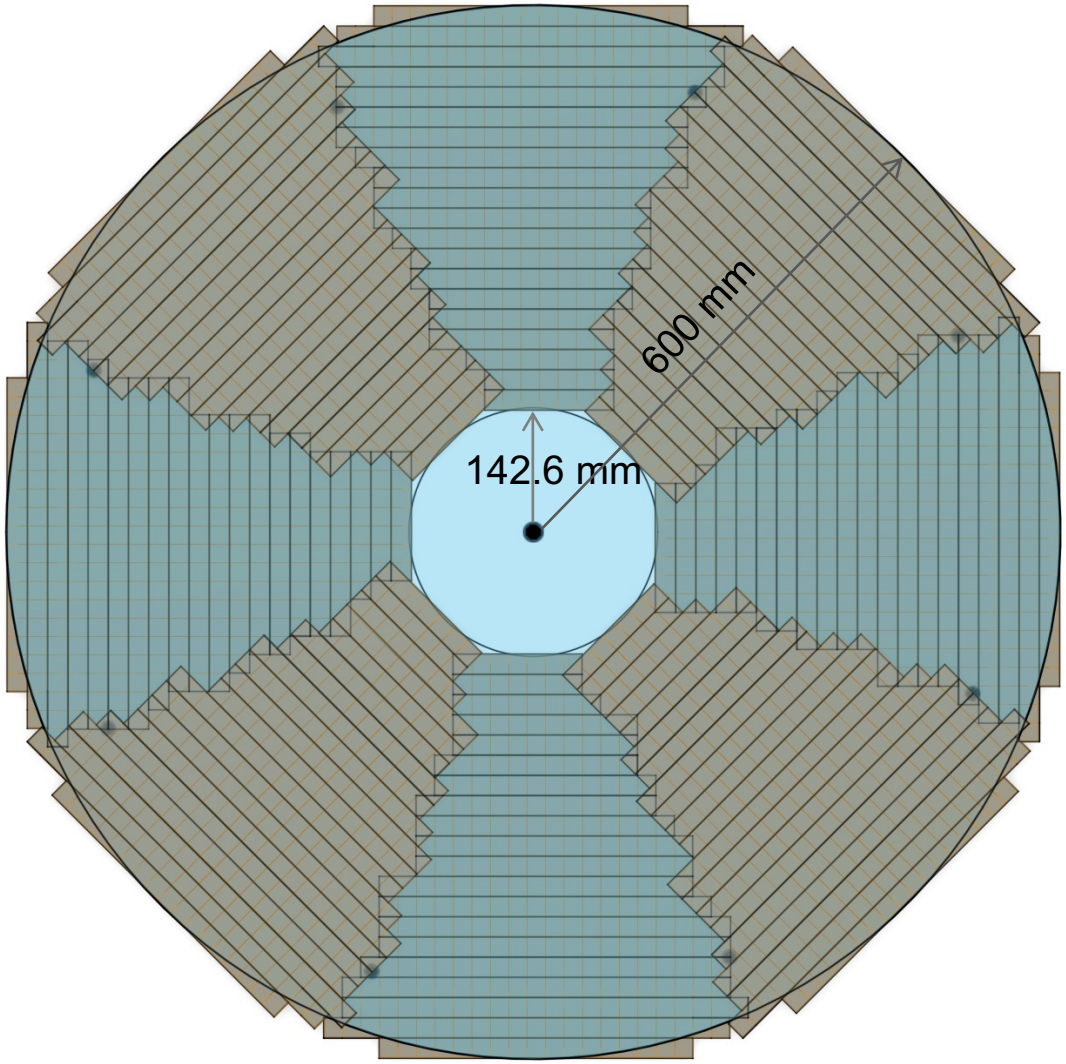




Latest Progress: The 3rd Endcap Baseline Design (ITKE3)

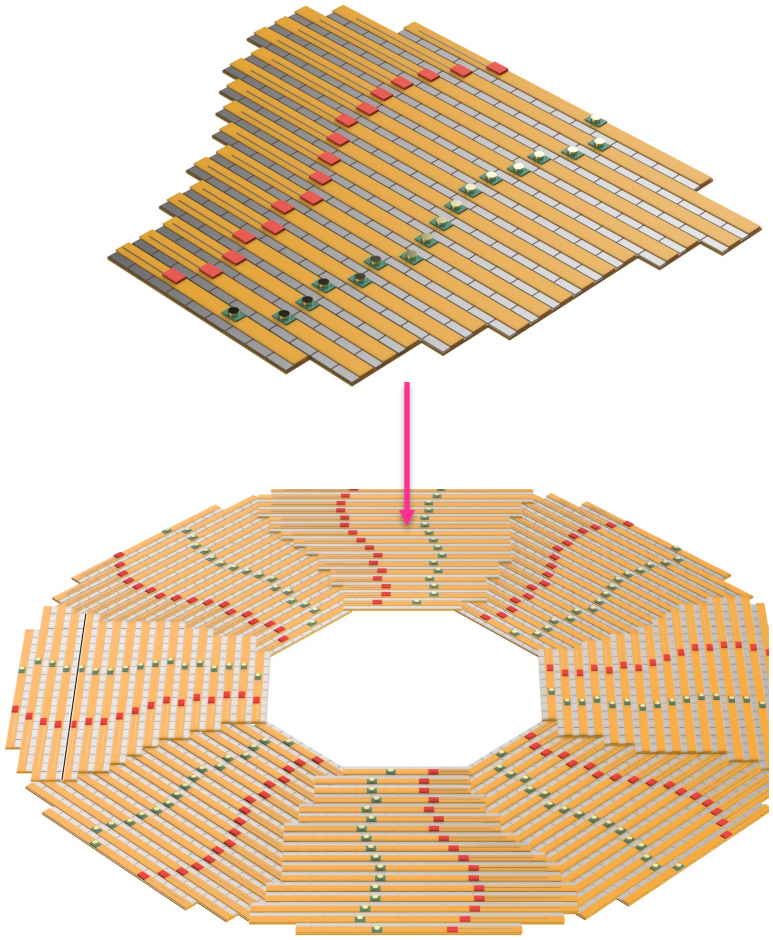
Qi YAN, Shoudong LUO, *and* Xin SHI

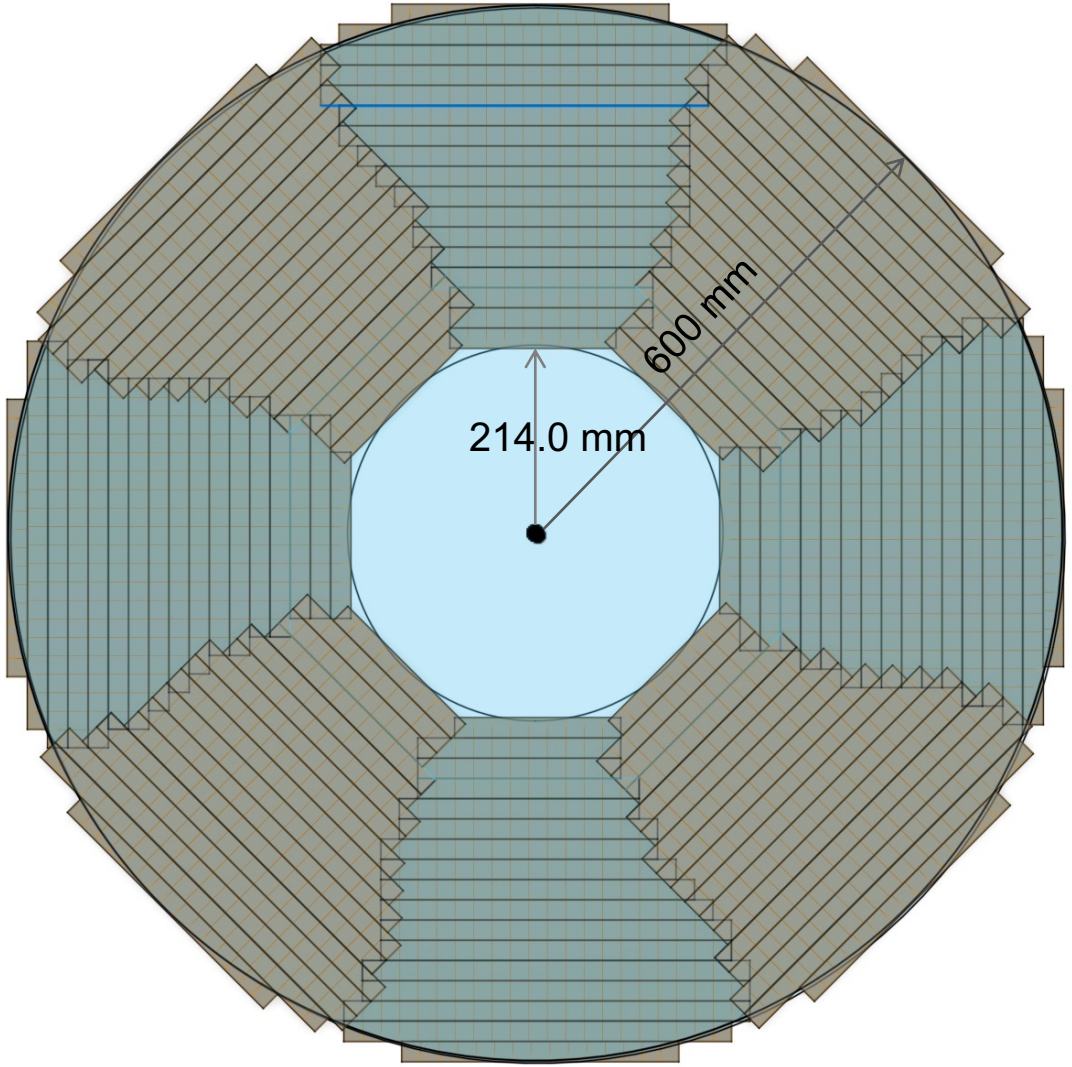




Latest Progress: The 4th Endcap Baseline Design (ITKE4)

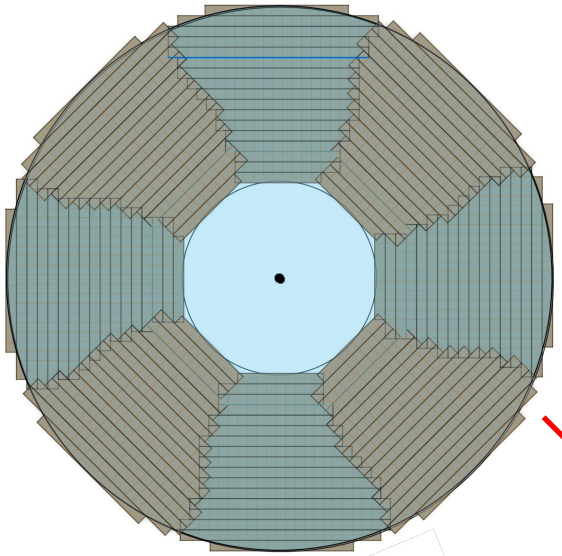
Qi YAN, Shoudong LUO, *and* Xin SHI



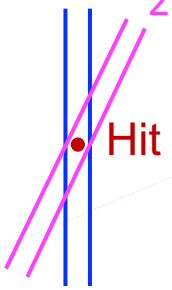


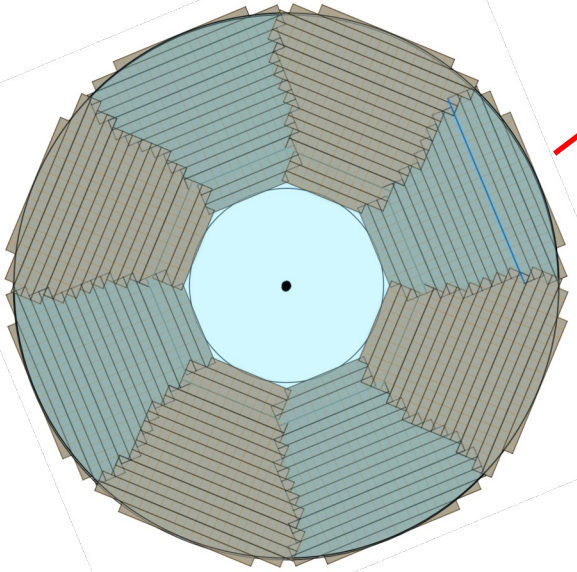
Complete Endcap Design Using Single-Side Strip Sensor

Qi YAN, Shoudong LUO, *and* Xin SHI

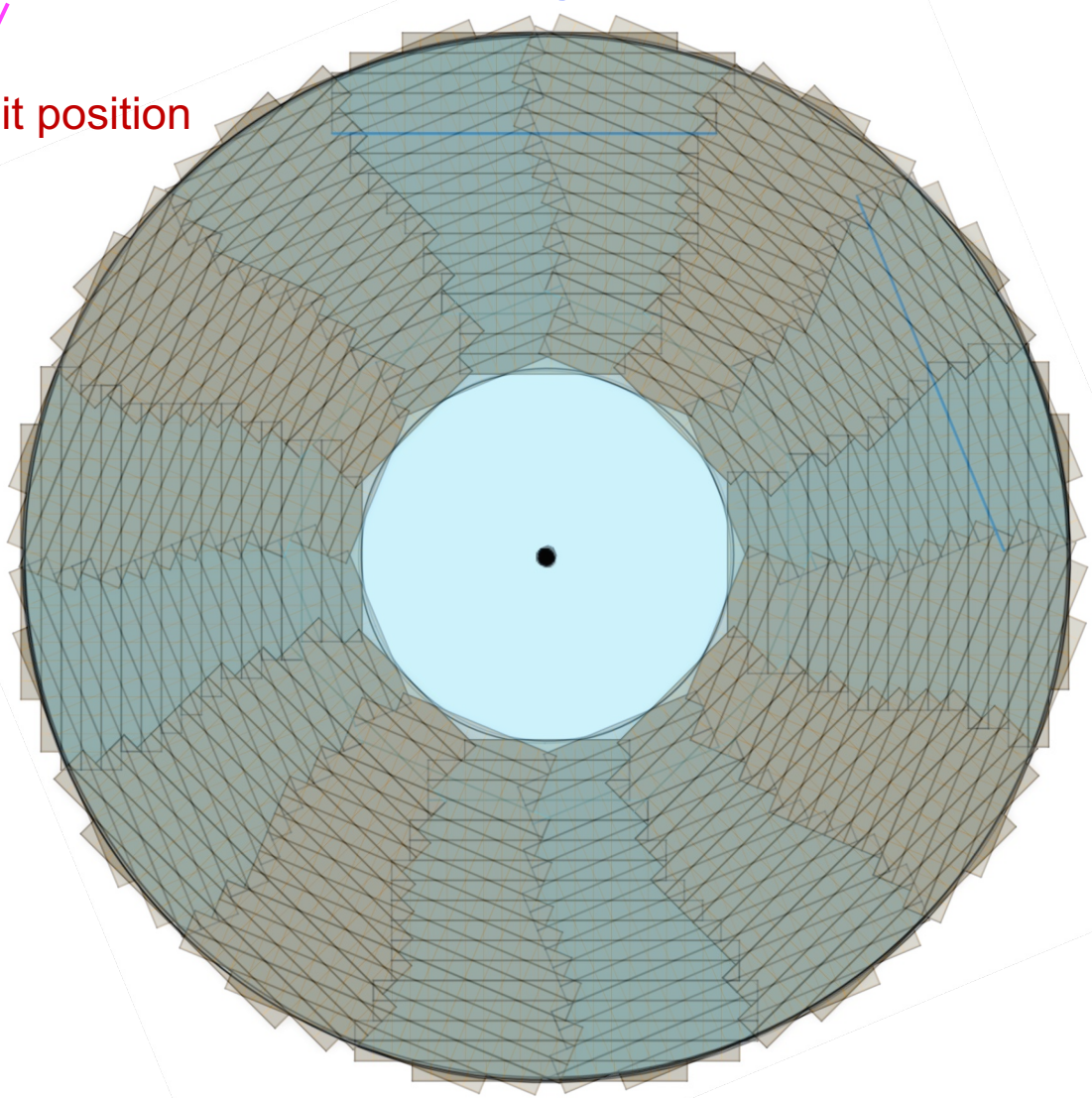


Normal half endcap

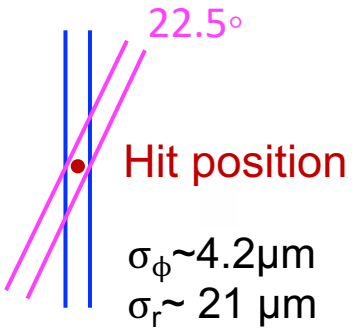




22.5◦ half endcap



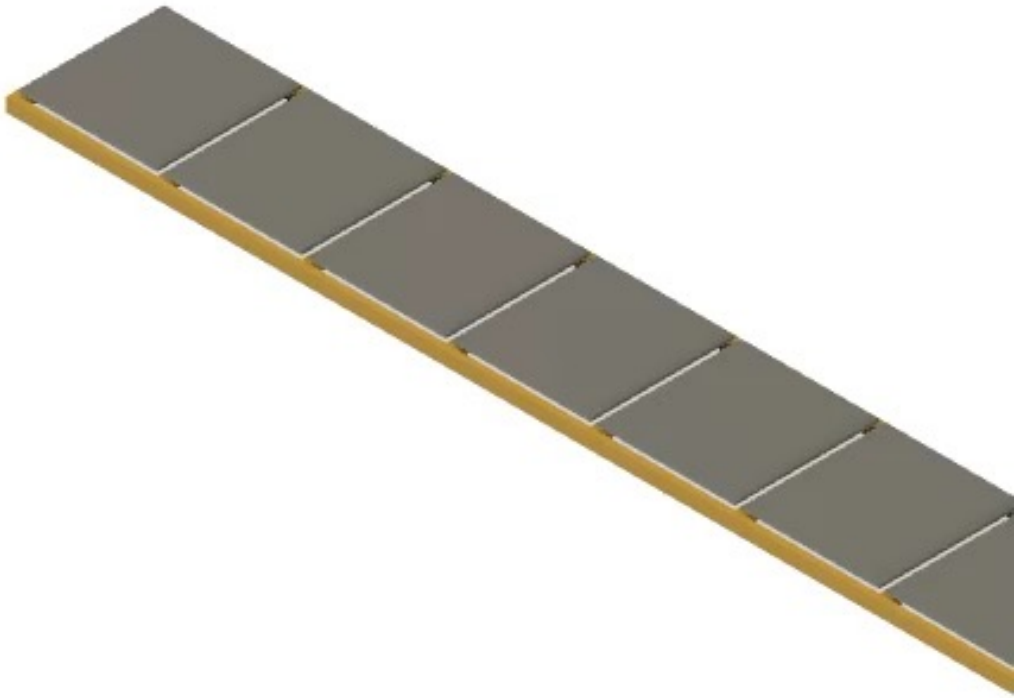
One complete endcap

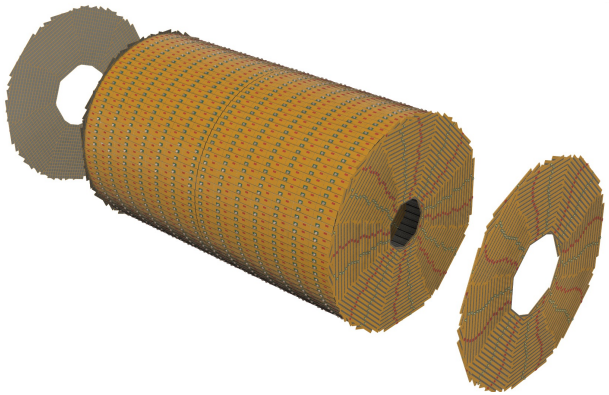


Basic detect concept

Two half endcaps are rotated 22.5° relative to each other to form one complete endcap:

- Minimize track ambiguity
- Maximize track resolution in bending direction ϕ





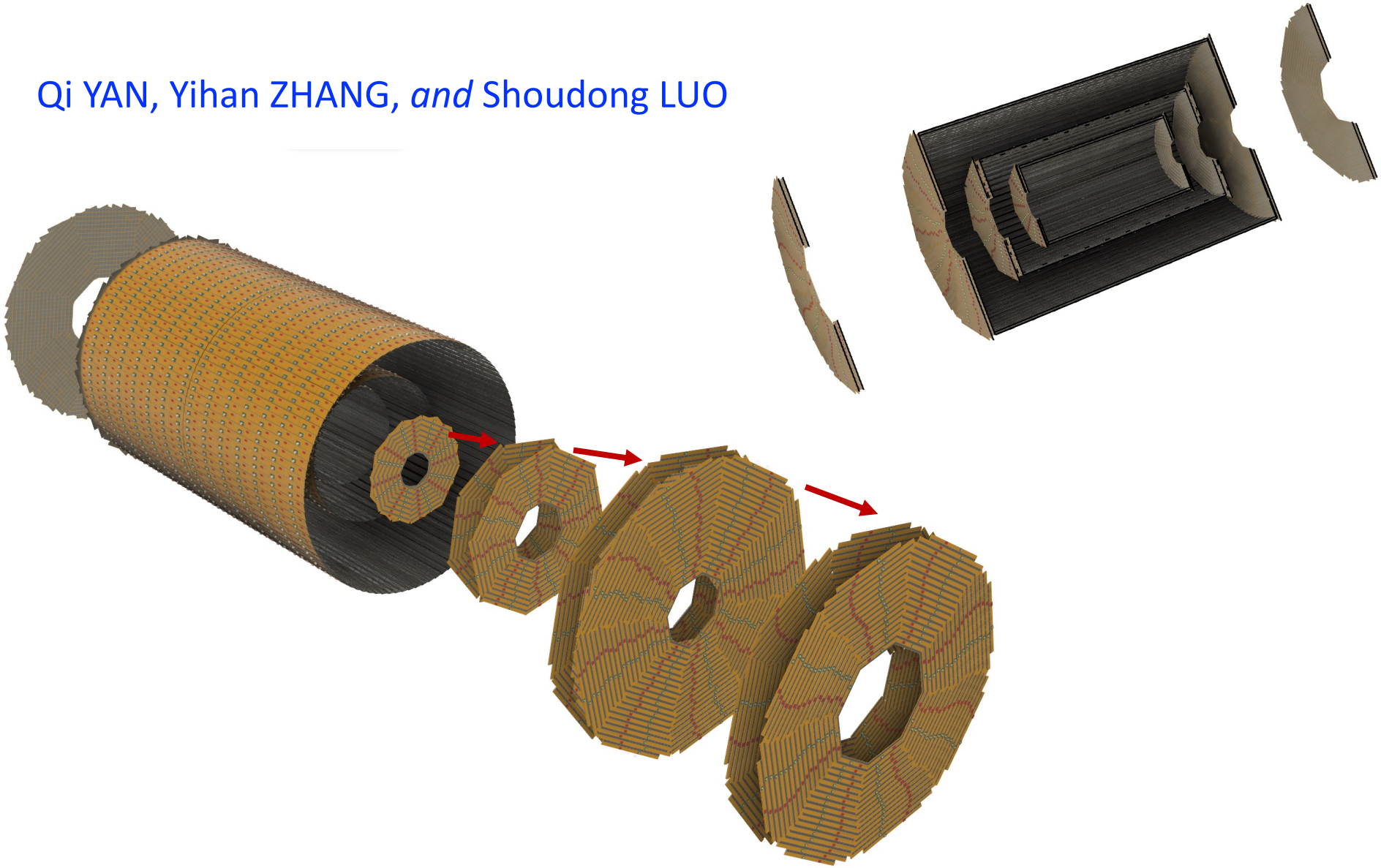
4 Layer ITK Endcaps Detector Components

	Module Types	Sensors	Sensor area	Overlap area Fraction
ITKE1	6	1536	0.74 m^2	0.074
ITKE2	8	3136	1.51 m^2	0.053
ITKE3	14	9504	4.59 m^2	0.035
ITKE4	12	8768	4.23 m^2	0.056
Total	19	22944	11.08 m^2	

The total power consumption of the chips (excluding other electronic components) is 8.9 kW for barrels (80 mW/cm^2).

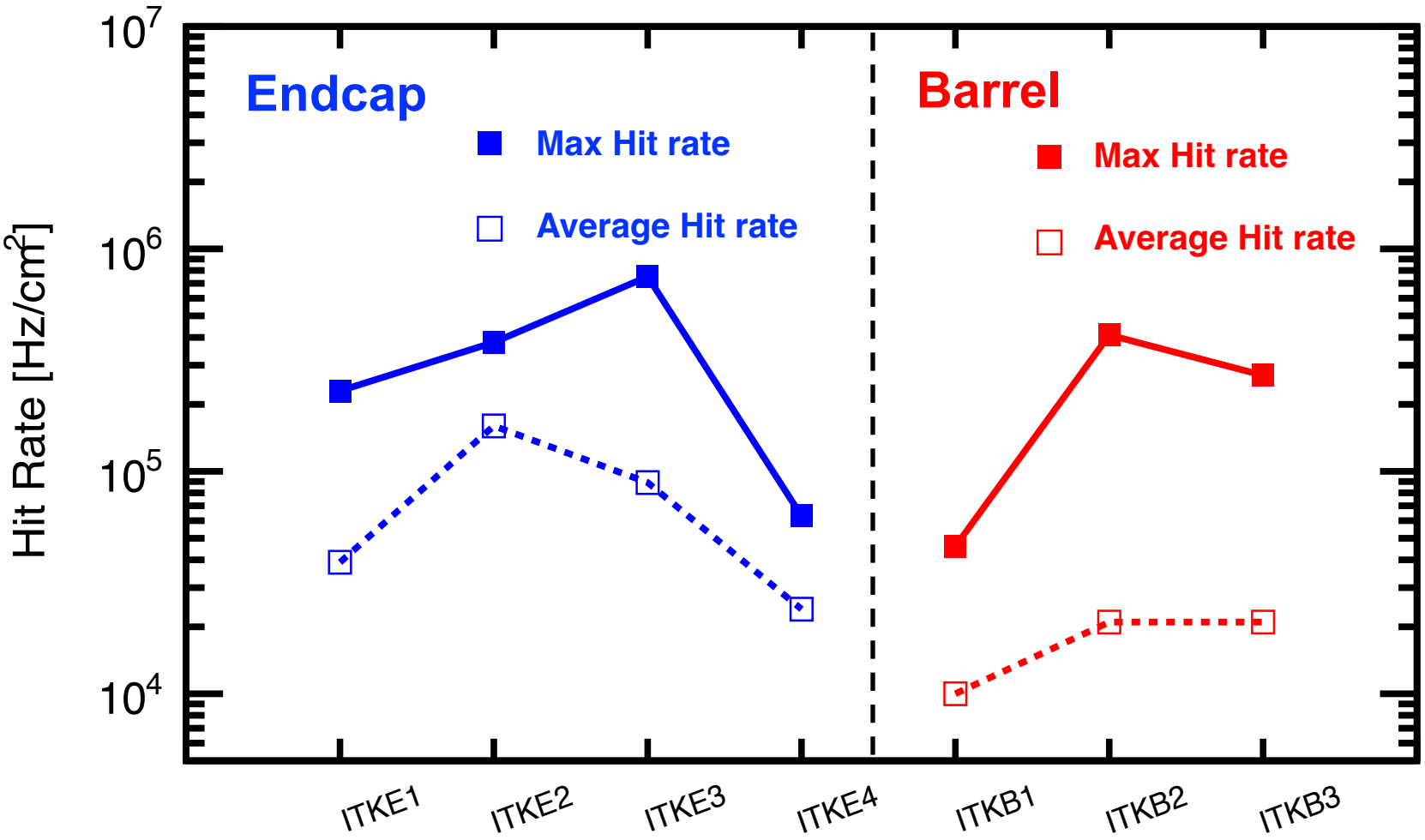
Full ITK with 3 Barrels and 8 Endcaps

Qi YAN, Yihan ZHANG, *and* Shoudong LUO



Latest Result of ITK Hit Rate Estimation

Zhan LI, Qi YAN, Xin SHI, *and* Haoyu SHI
(ITK+OTK meeting, July 24, 2024)



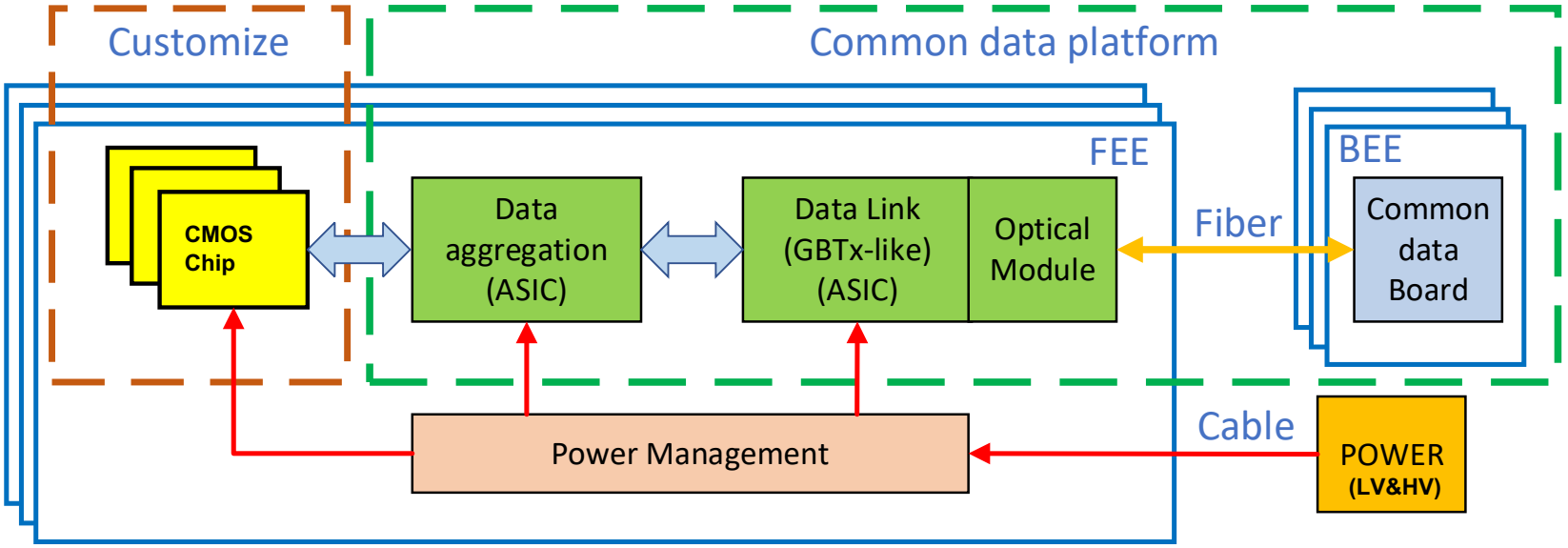
Summary of CMOS Chip Parameters

	HVCMOS Pixels (Barrel)	CMOS Strips (Endcap)
Pixel Size (Strip Pitch Size)	$34 \times 150\ \mu m^2$	20 μm
Chip size	$2 \times 2\ cm^2$ (active area: 1.92x1.74 cm^2)	2.1×2.3 cm^2 (active area: 2.05x2.05 cm^2)
Array size (Strip number)	512 rows × 128 columns	1,024
Spatial resolution	σ_φ ~8 μm, σ_z~40 μm	σ_φ~4.2 μm, σ_r~21 μm
Timing resolution	~3-5 ns	~3-5 ns
Data size per hit (1 readout)	42 bit (14b BXID, 7b+9b address, 6b TOT, 5b fine TDC, 1 polarity*)	32 bits (10b BXID, 10b address, 6b TOT, other 6 bits)
Data rate per chip	Maximum ~0.1 Gbps* (pair production)	Maximum ~0.2 Gbps* (pair production)
LV / HV	1.2V / 150 V	1.5V / 150 V

* Maximum hit rate: barrel~4.1×10^5, endcap~7.5×10^5

Baseline Design for ITK Electronics

Xiongbo YAN *et al.*



- Data transmission: common data platform
- Trigger mode: triggerless

Summary

- The first version of the ITK baseline is nearly complete, although it's not perfect. I appreciate all the efforts from the ITK group members： Xin SHI, Yiming LI, Xiongbo YAN, Yang ZHOU, Gang LI, Yihan ZHANG, Shoudong LUO, Zhan LI, and others.

- After this initial phase, we will move on to the second round of the silicon tracker baseline design.

- Sub-detectors must align with the overall detector design. We will incorporate and reconsider the basic OTK design, such as changing from the current curved sector sensors to trapezoidal sensors in the endcaps to facilitate mechanical and electronic assembly.

- The layout optimization study will continue to:
  a) Determine the optimal positioning of ITK layers.
  b) Explore the possibility of increasing the ITK barrels to 4 layers to create a more robust and standalone tracking system .
  c) Consider using CMOS strips and CMOS pixels for both ITK endcaps and barrels.

- We aim to accelerate R&D for both HVCMOS pixels and CMOS strips. Regular discussion will be organized during our ITK+OTK meeting to promote progress.

- We currently lack expertise in mechanical and thermal design and welcome professionals to contribute to our silicon tracker team.