The design, production and QC test of GEM electronics board for CMS ME0 project

Zhe Li (on behalf of PKU Group)

Outline

Outline:

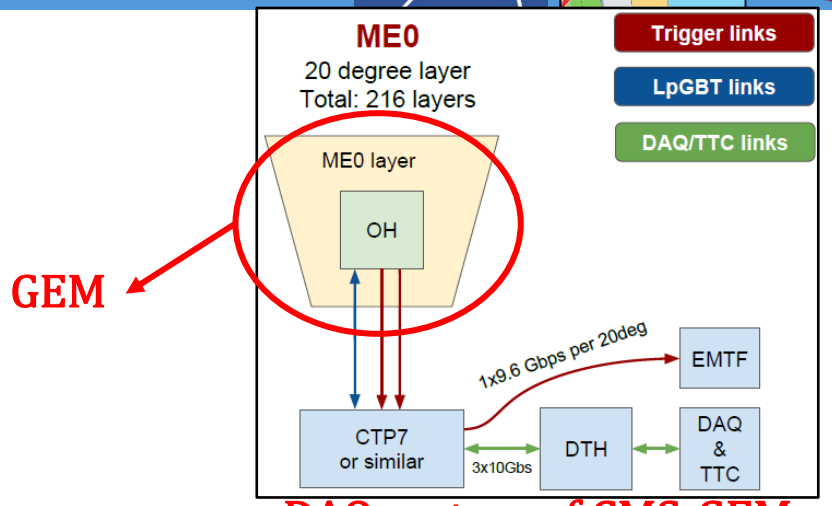
1. Introduction of CMS ME0 GEB
2. Requirements of CMS ME0 GEB
3. Design of CMS ME0 GEB
4. Production and QC test of ME0 GEB
5. Summary

Introduction of CMS ME0 GEB

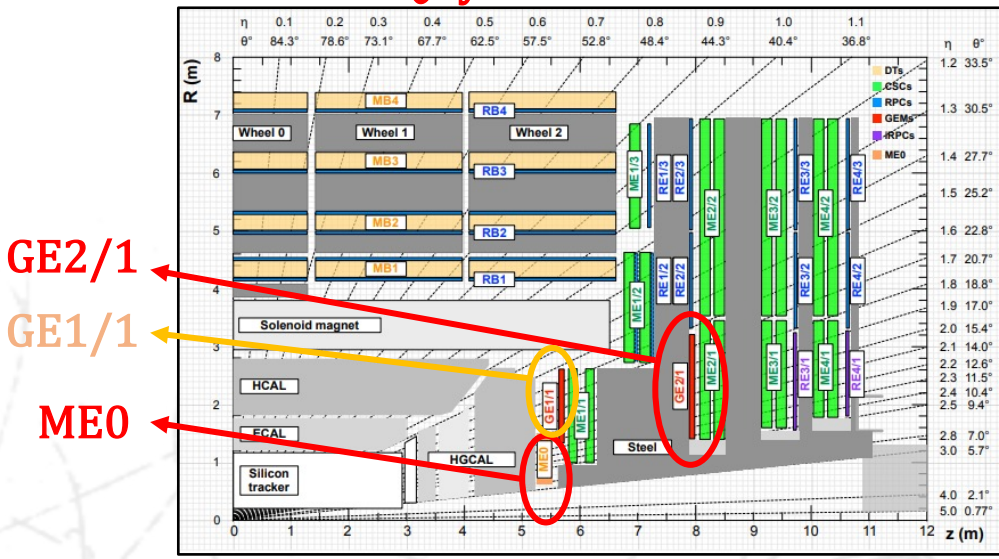
- GEB: front-end electronics board of GEM detector for upgraded CMS muon system (GE1/1, GE2/1, ME0)

- Function of GEB:
  - Carrier of front-end and back-end electronics system
  - Front-end signal transmission carrier
  - Provide direct shielding for GEM detectors

- Works of CMS China HEP group:
  - Production and test of GE1/1 GEB
  - Design、production and test of ME0 and GE2/1 GEB
  - Development of automatic tester



DAQ system of CMS-GEM



CMS detector cross section

Requirements of ME0 GEB

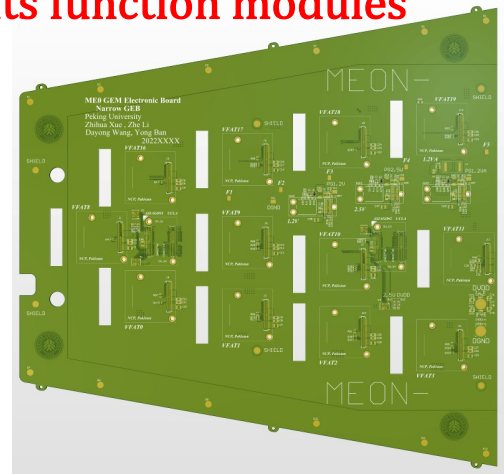
- **Signal transmission:**
  - Ensure that the **characteristic impedance** is 100 Ohm for differential line, and small fluctuations in characteristic impedance to reduce signal reflections
  - Ensuring that **time delay** of the signal lines are the same to meet isochronism requirement
  - Low **BER (Bit Error Rate)** and **noise**

- **Power Supply:**
  - Meet the different power requirements of VFAT and OH board
  - Effective power distribution systems
  - Power monitor, current, voltage and temperature monitor
  - Prevent large voltage drop during transmission
  - Validate the voltage to set value

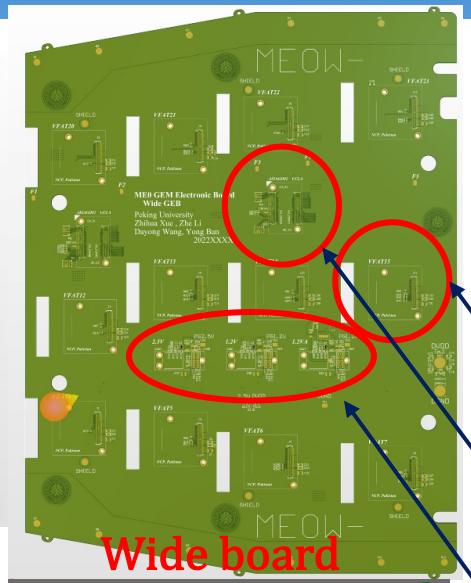
- **Mechanical performance:**
  - Total board thickness is less than **1.1mm**, limited by installation space.
  - Surface flatness lower than the IPC standard curvature **0.75%**.
  - standoffs (holding VFAT and OH boards) aligned and firmed mounted

Design of CMS ME0 GEB

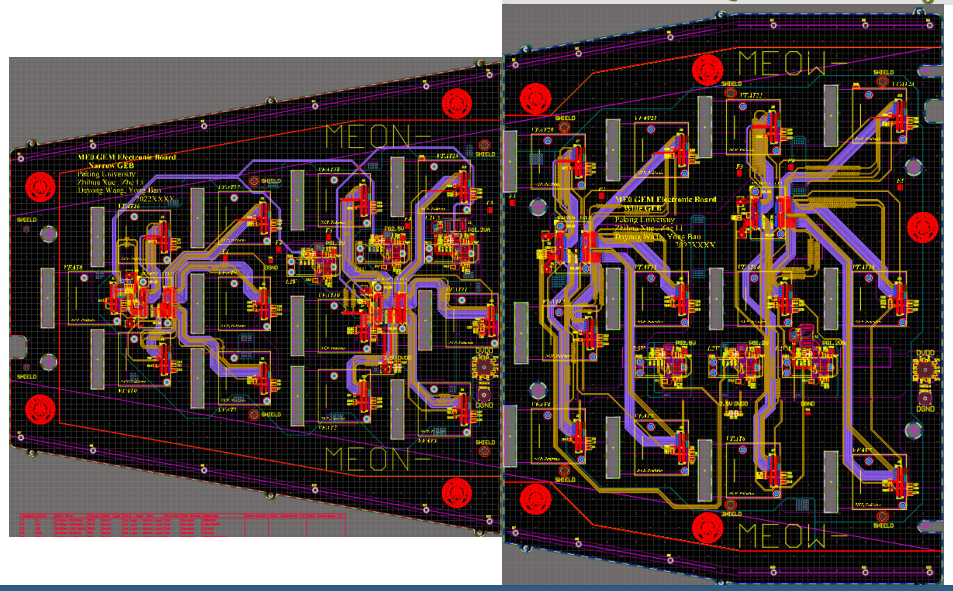
GEB with its function modules



Narrow board



Wide board

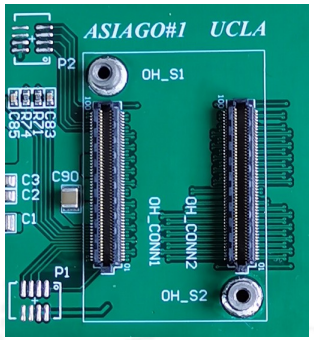


A set of GEB connects to:

- 24 VFATs
- 4 ASIAGO boards (2 OH-CONN on each)
- 6 FEAST (1.2VA, 1.2VD and 2.5V)

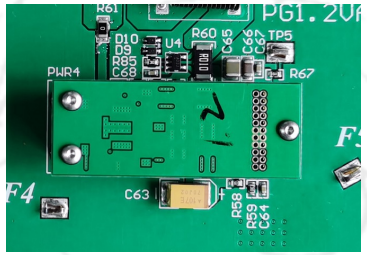
VFAT Connector and standoff

The VFAT chip converts the signal on the readout strips into digital signal



OH Connector and standoff

Electrical components on OH board convert the signal from GEB into an optical signal on the optical fiber



FEAST Connector and standoff

FEASTs provide voltage to chips on VFAT and OH board

Stacks of GEB board

To meet characteristic impedance requirement:

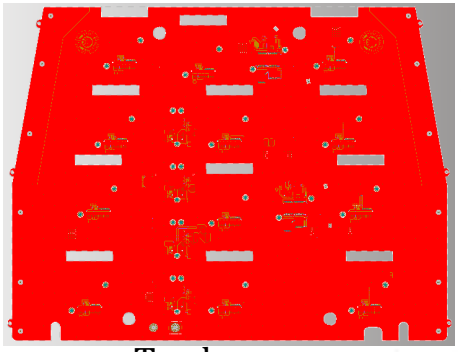
- Choose proper dielectric constant: surface solder 3.5 medium 4.2
- Copper thickness for signal stack: 0.5Oz
- Mini number of vias for each differential line: 2 vias (Reduce the fluctuation of characteristic impedance)

To meet mechanical performance requirement:

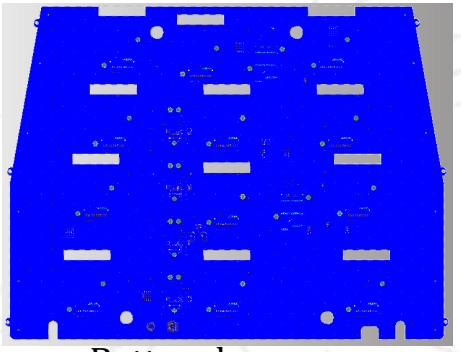
- Board thickness: 1.05mm (within the requirement 1.1mm)
- Symmetrical arrangement and the same copper laying method (Reduce the curvature)
- Use halogen-free boards

Stacks structure

	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask	0.01mm	3.5	
1	Top Layer		Signal	0.035mm		1oz
	Dielectric 1	FR-4	Core	0.16mm	4.2	
2	Signal 1		Signal	0.018mm		1/2oz
	Dielectric 2		Prepreg	0.13mm	4.2	
3	DGND1		Plane	0.018mm		1/2oz
	Dielectric 3		Core	0.08mm	4.2	
4	POWER		Plane	0.036mm		1oz
	Dielectric 4		Prepreg	0.076mm	4.2	
5	AGND2		Plane	0.036mm		1oz
	Dielectric 6		Core	0.08mm	4.2	
6	DGND2		Plane	0.018mm		1/2oz
	Dielectric 9		Prepreg	0.13mm	4.2	
7	Signal 2		Signal	0.018mm		1/2oz
	Dielectric 7		Core	0.16mm	4.2	
8	Bottom Layer		Signal	0.035mm		1oz
	Bottom Solder	Solder Resist	Solder Mask	0.01mm	3.5	
	Bottom Overlay		Overlay			



Top layer



Bottom layer

For example, top layer and bottom layer are laid with the same copper arrangement, in order to reduce the board curvature

Characteristic impedance and routing

Characteristic Impedance

Set to 100Ohm for differential lines:

Factors that affects characteristic impedance:

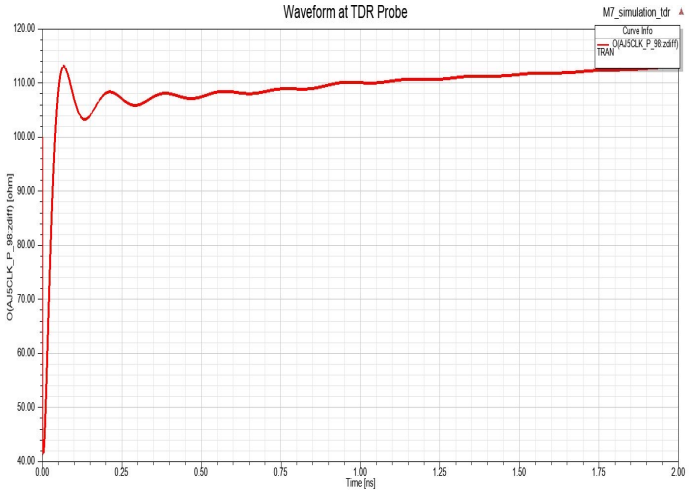
(1) W1,W2:Line width

(2) S1:Differential line separation

(3) D1:Ground strip separation

(4) H1,H2:Stack thickness

(5) Er1, Er2: Dielectric constant of the medium



Characteristic impedance fluctuation of most differential line is within 10%

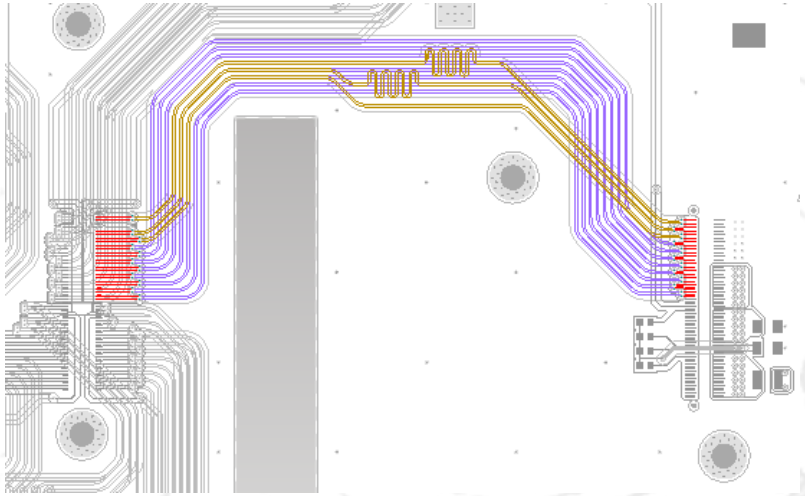
Routing:

Characteristic Impedance fluctuation: <10%

(1) Differential signal lines: linewidth / gap / linewidth: 0.1/0.25/0.1 mm (Considering coupling effect)

(2) Other parameters: Minimum distance to another pairs / DGND: 0.55mm / 0.6mm.

(3) Simpler routing design: Reduce routing corner

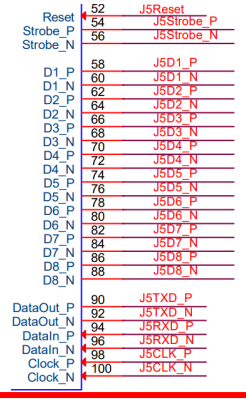


Signal

Signals introduction:

VFAT trigger unit outputs 9 differential signals:
VFAT communication E-port has 3 pairs of differential signals

VFAT reset signal
LVCMOS level signal: RESET



To meet time resolution requirement of signals:
Equal length(CLK and RXD):
J1-J6,J7-J12 To ensure signal isochronism

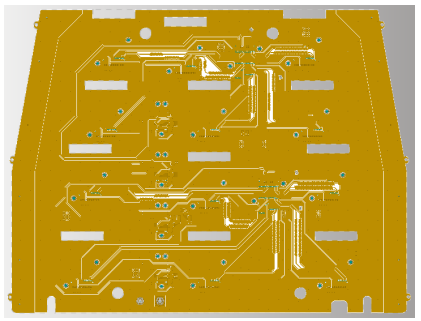
Designator	Average Leng.
J1CLK	208.835
J1RXD	208.835
J2CLK	208.835
J2RXD	208.835
J3CLK	208.835
J3RXD	208.83
J4CLK	208.835
J4RXD	208.835
J5CLK	208.835
J5RXD	208.835
J6CLK	208.835
J6RXD	208.835

Designator	Average Leng.
J10CLK	276.24
J10RXD	276.24
J11CLK	276.24
J11RXD	276.24
J12CLK	276.24
J12RXD	276.24
J7CLK	276.24
J7RXD	276.24
J8CLK	276.24
J8RXD	276.24
J9CLK	276.24
J9RXD	276.236

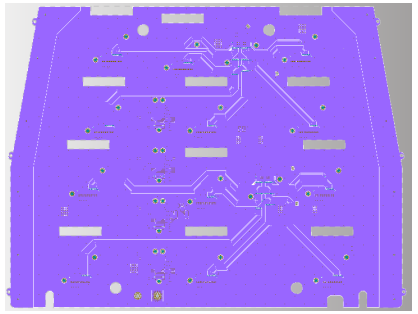
Signals are arranged on two layers:

Signal1 and signal2

Prevent crossover of signal lines as in GE1/1 case

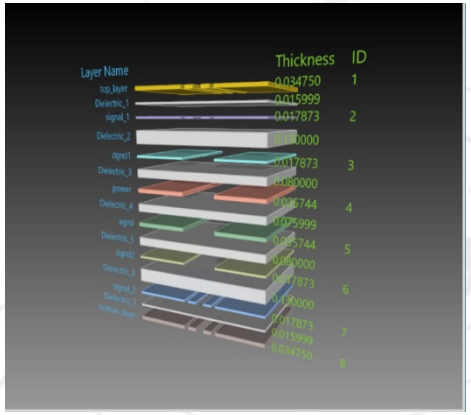


Signal1 Layer



Signal2 Layer

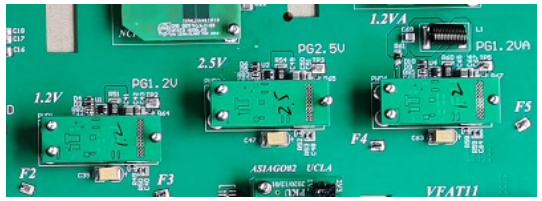
Both signal layers have upper (Top layer or bottom layer) and lower shielding layers (DGND1 and DGND2) to reduce signal interference



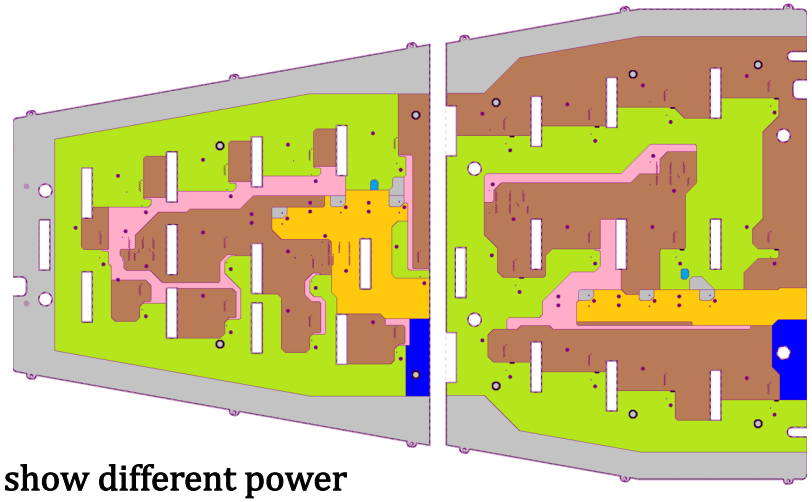
Power distribution system

- Chip of VFAT and OH requires a different FEAST power supply
- 3 FEASTs provides 3 voltages to the corresponding chips of VFAT and OH board

FEAST →



- GEB distribute the voltage from FEAST to VFAT and OH board through vias and power plane.
- In addition, grounding operation is achieved through the DGND and AGND planes.



Different colors show different power supply areas and link to different FEAST

Prevent voltage loss:

(1) The thickness of the power supply layer is 1oz

(2) For high current power supply, we provide large area power plane

Power monitor

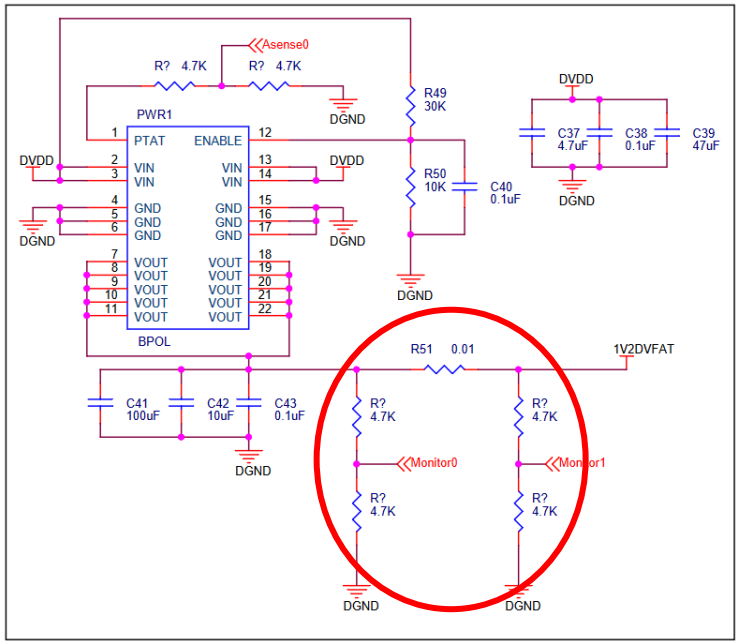
Power monitor:

introduced to ensure that the voltage value of the supply is normal

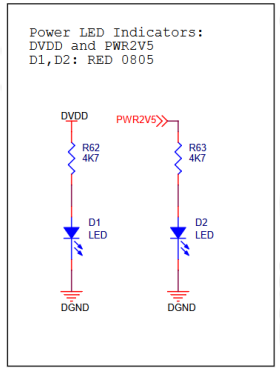
- The output **monitoring voltage** show whether the FEAST is working properly.
- To monitor the current output of each power supply, we use Monitor to detect the voltage drop through the current sensing resistor with a resistance of 0.01 Ohm.
- The GEB power supply is designed **with 2 sets of LED lights**, corresponding to the main power input terminal and 2.5V power output seperately , which can display the power supply status of both in time.

- OH power supply;
  - PWR1: 1V2DVFAT ---1.3A for one ASIAGO, total is 2.6A.
  - PWR2: PWR2V5 --- 0.2A for one ASIAGO, total is 0.4A.
- VFAT power supply:
  - PWR1: 1V2DVFAT ---70mA for one ASIAGO, total is 840mA.
  - PWR2: PWR2V5 --- <1mA for every VFAT
  - PWR4: 1V2AVFAT ---140mA for one VFAT, total is 1.68A

- Voltage measurement:
  - Monitor1 and Monitor0 are 0.6V ($1.2V \times 0.5$)
- Current measurement:
  - If Ir51 = 3.44A, voltage of Monitor0 –Monitor1 = 17.2mV
  - $(3.44A \times 0.01\Omega \times 0.5)$



Power monitor of 1V2DVFAT



LED

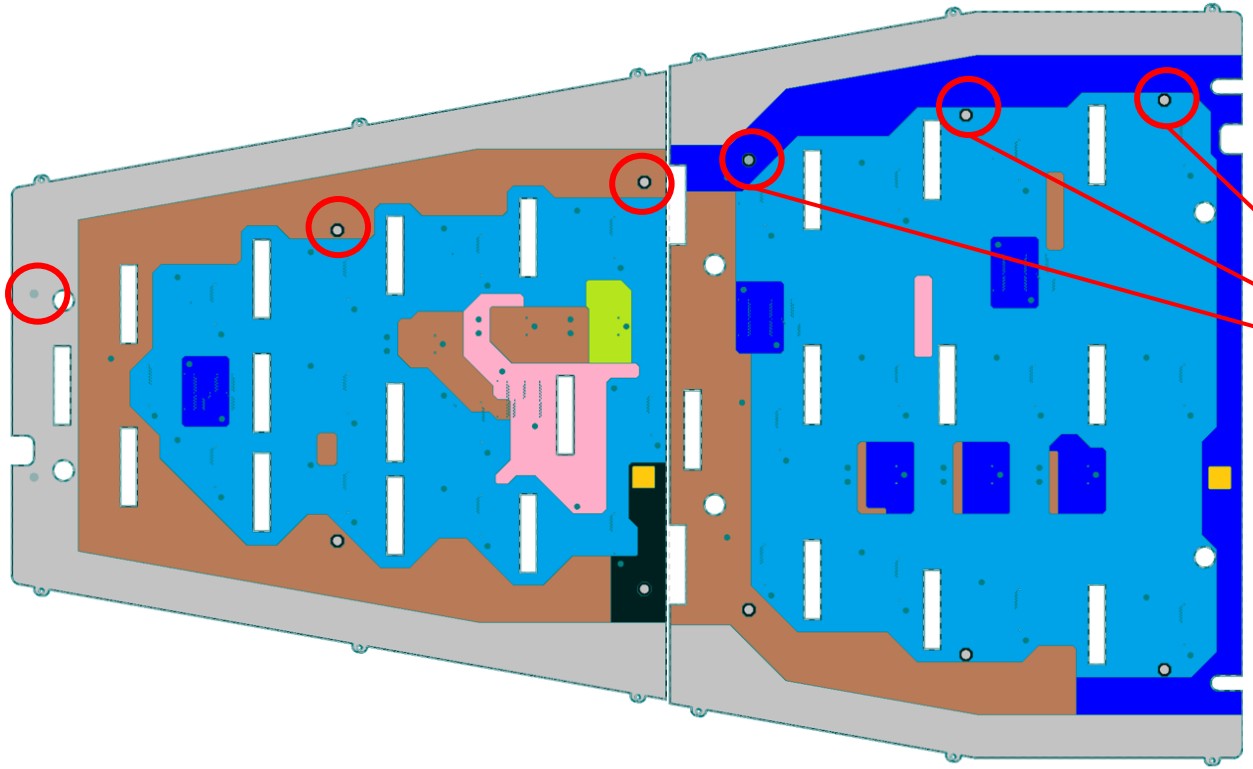
Grounding system and shielding system

Grounding system:

- 2 DGND layer(digital ground) and 1 AGND(analog ground) layer.

Shielding system:

- The signal layer is between top/bottom layer and grounding layers to avoid electromagnetic interference.
- Shielding pads which connected to the external frame are added to reduce noise.

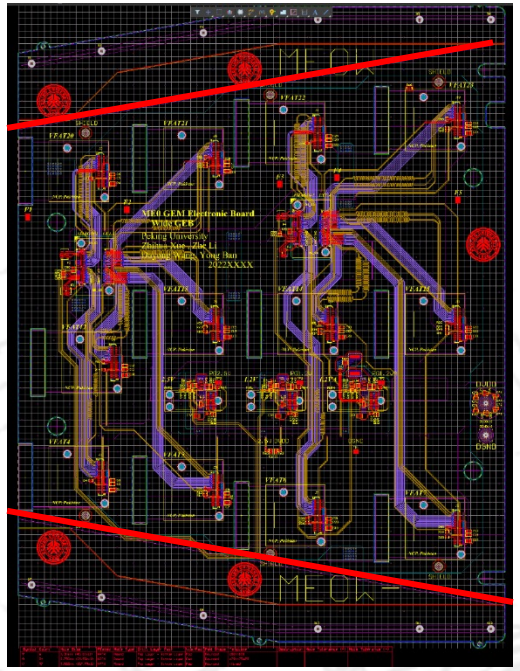


Split plane of AGND layer

Shielding Pads
12 in total

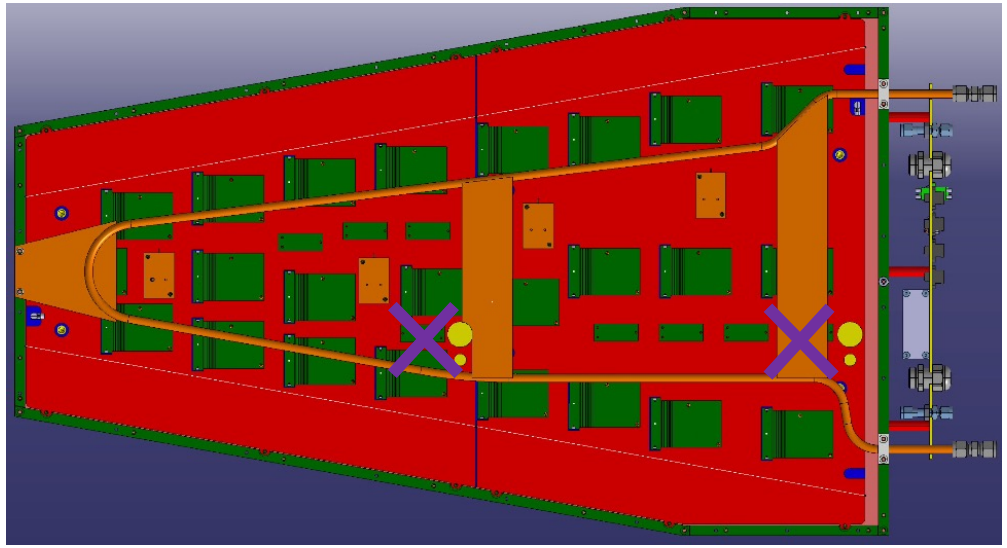
chimney

chimney



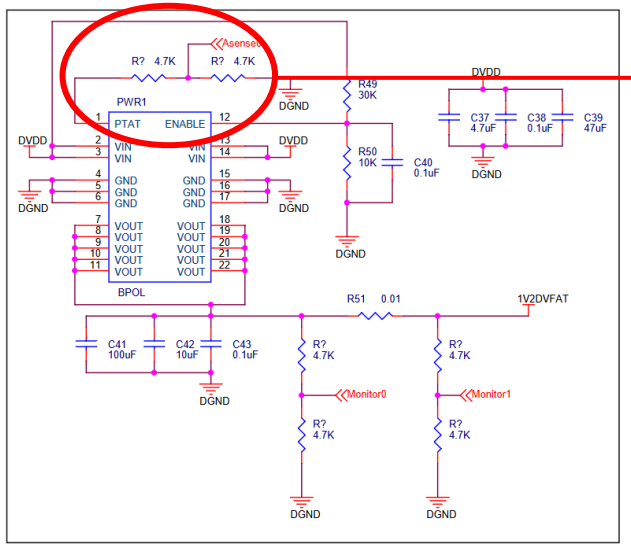
Cooling system and temperature measurement

Cooling system to cool down the DAQ system:
The cooling system is modified as the number of FEAST is from 4 to 3.



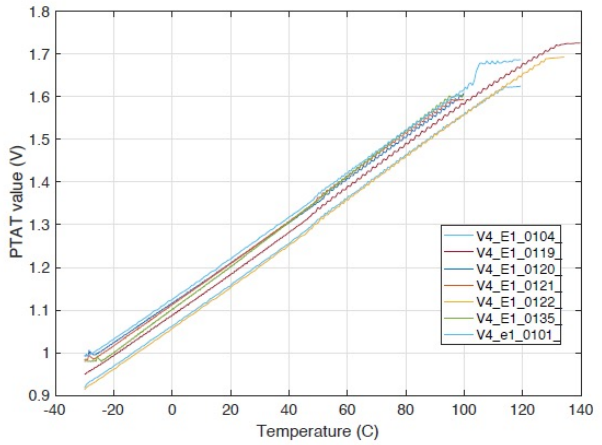
Cooling system

- Remove the 1.2VD FEAST which is located in the positions marked by the purple X

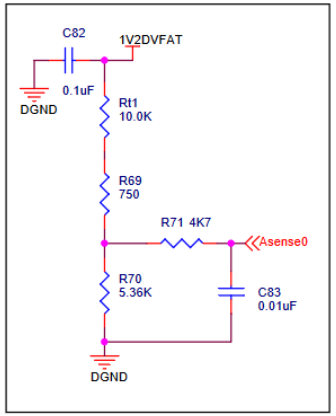


Temperature measurement:

- Temperature is measured by the pin of PTAT on the BPOL with divided resistors.
- The output of the divider of PTAT is 0.45V --- 0.85V(2.425mV/℃).
- PTAT output change with temperature shown as below picture.

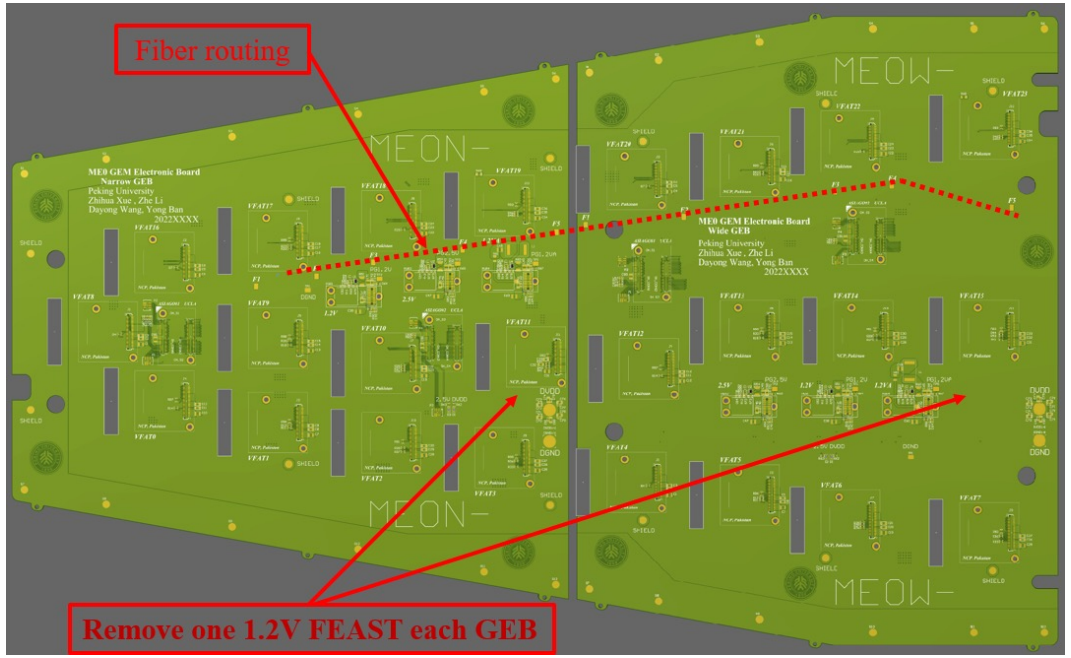


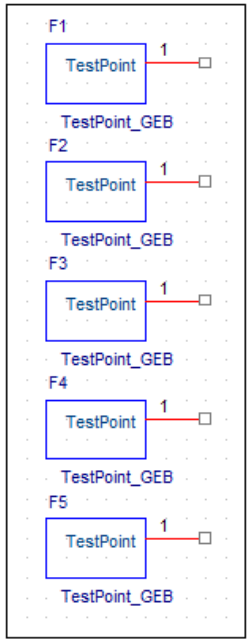
Temperature curve

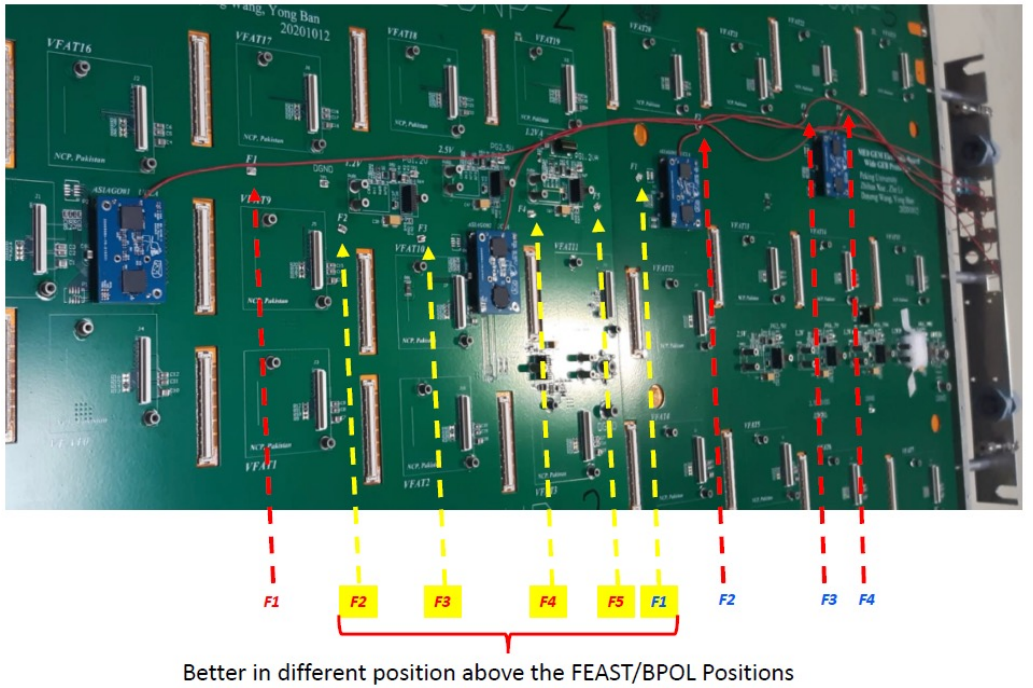


Previous temperature measurement system

Fiber routing







Better in different position above the FEAST/BPOL Positions

- Fiber fixing

5 KEYSTONE 5016 for narrow GEB

5 KEYSTONE 5016 for wide GEB

attach optical fiber to zipline

- In order to ensure it is firm, many through holes are placed on the keystone.
- In order to avoid signal interference ,
  - 1. The keystone is not grounded
  - 2. No signal routes through the occupied position

Production site of ME0 GEB

- **Sinofast** in Shenzhen, China has long term collaboration with CMS-GEM team, has produced all GE1/1 & GE2/1 GEBs and ME0 GEB, including their prototypes

Laminating Machine

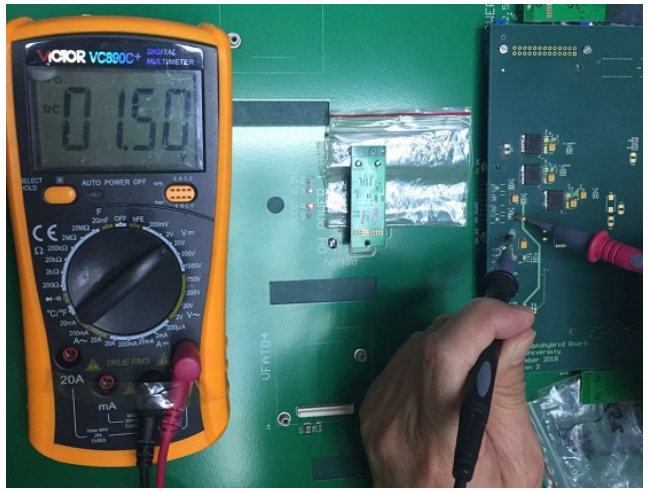
Etching Machine

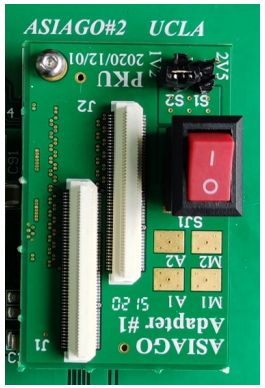
CNC drilling machine

Production and QC test of ME0 GEB

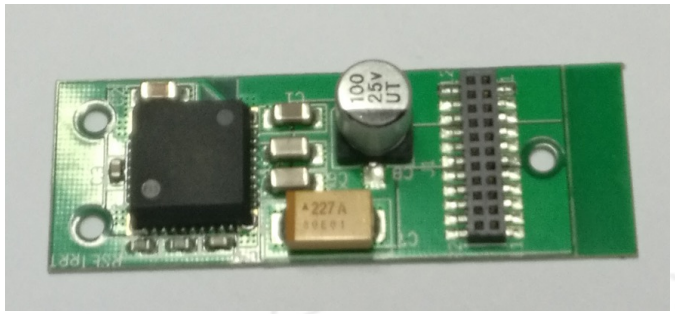
- **Milestone of ME0 GEBs production:**
  - Designed finalized in June 2022, 1st batch of 15 sets of ME0 GEBs produced on Jan. 2023, completed test at CERN in Apr. 2024
  - 240 sets of the remaining GEBs production completed in Feb. 2024, 2nd batch of 95 sets of GEBs tested in China and shipped to CERN in April 2024
  - 3rd batch of 145 sets of GEBs tested at China completed in Nov. 2024, shipped to CERN ~15 Nov.
- **Test at GEB production site in Shenzhen Sinofast Ltd., China:**
  - Flying Probe test and characteristic impedance test (by the factory)
  - Power module test
  - Signal connectivity test and BER test (new tool)
  - Bending degree test and mechanical compatibility test
- **Acceptance test at CERN:**
  - Similar as GE2/1 acceptance test at CERN, to make sure no damage caused by shipment.

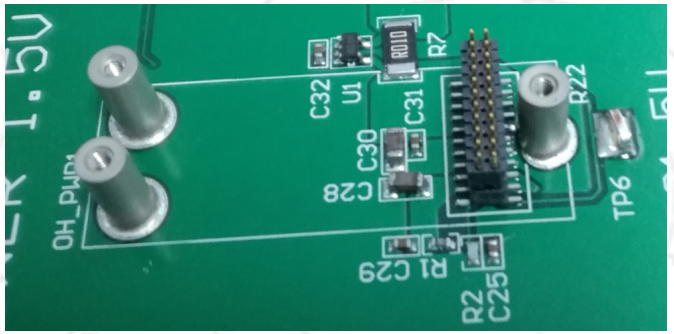
Power module test





Load board





Voltage and current test of 3 power modules:

- 2.5V on OH board
- 1.2V digital power、1.2V analog power supply on VFAT

→ The power test has been done with the ME0 GEB(wide & narrow) prototypes, the results meet the GEB design requirements, and the fluctuations are within a reasonable range

Signal Connectivity Test: FPGA-computer based device

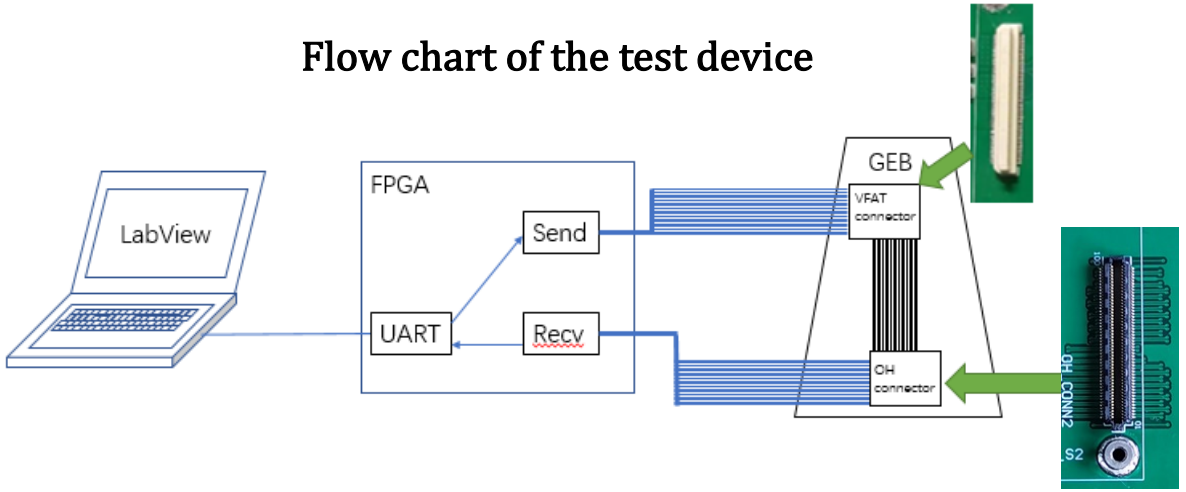
Device:

using Xilinx Spartan-6 FPGA and LabVIEW

Used in acceptance test of GE2/1 GEB

The device was verified and successfully used in GE2/1 mass production

Flow chart of the test device

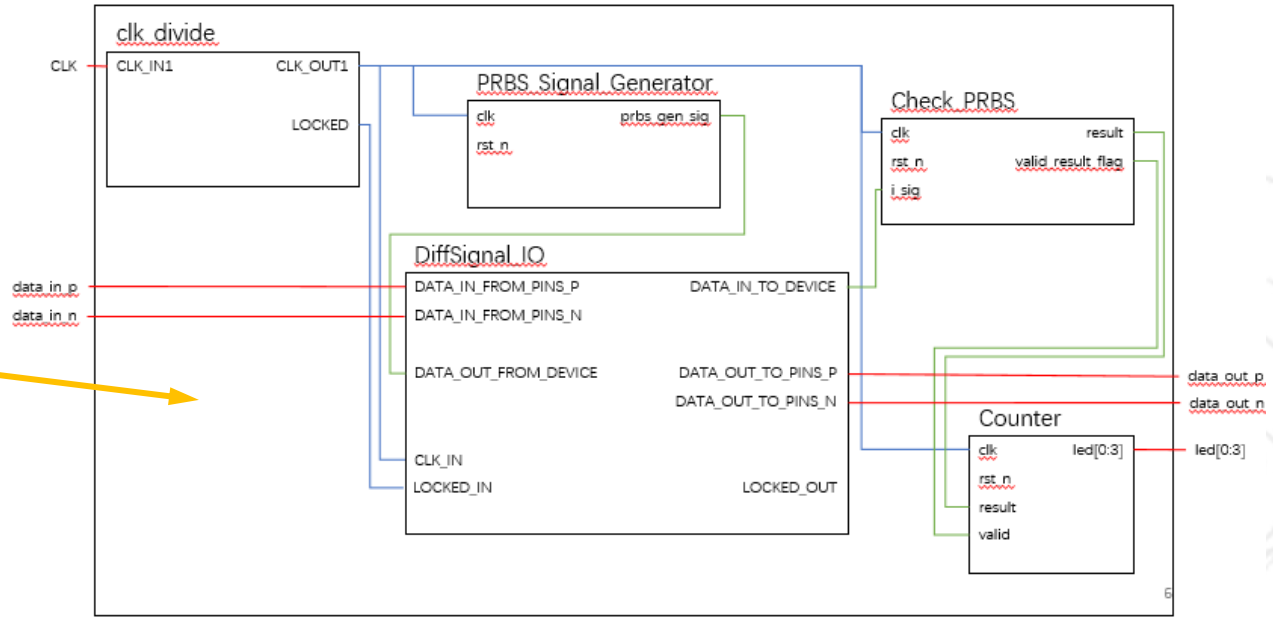


- **Connectivity test:**

all VFAT signal channels and power supply pins

- **BER test:**

schematic diagram



- **Test Criteria:**

No short and open circuit (connectivity)

No error occurs in one minute (BER)

Characteristic Impedance test

Characteristic Impedance test results (provided by Sinofast company)

IMPEDANCE MEASUREMENT REPORT

阻 抗 测 量 报 告

TESTING QTY: 1 DATE CODE: 4620

Measuring Equipment 测量仪器及型号: Agilent E5071C (TDR Time Domain Reflectometer)时域反射仪

Impedance Measurement 阻抗测量于: Finished Board 成品板

SampleNo. 样品编号	Layer 层号	Line Width 线宽(mm) +/-10%	Type of Impedance 阻抗类别		Impedance Requirement (ohm) 阻抗值要求	Tolerance		Impedance Value 阻抗测试数值	Result 结果
			Single Ended 单端	Differential 差动		+	-		
1	L1	0.192	/	√	100	10	10	100.23	ACC
	L2	0.098	/	√	100	10	10	98.56	ACC
	L7	0.098	/	√	100	10	10	99.48	ACC

Remarks:

Disposition: Acc ☑ Rej ☐

TESTED BY: GWEI DATE: 2020.11.22

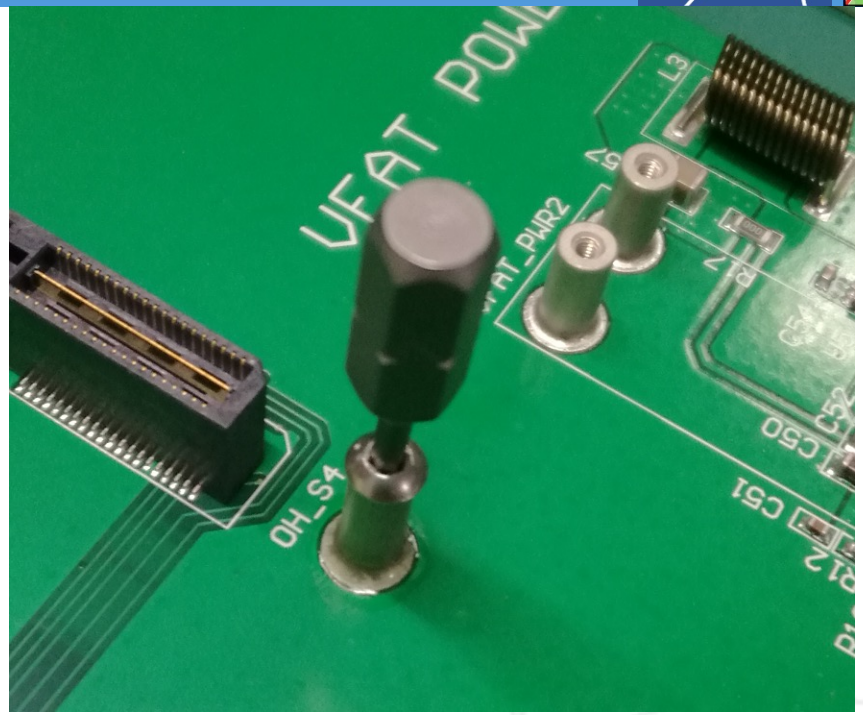
APPROVED BY: DQCAI DATE: 2020.11.22

Documentation NO.QA-2019-08 Rev:1.2

Mechanical Compatibility & Flying Probe Test

Mechanical compatibility test

- Mount VFAT (Plugin Card), OH board, and FEAST to check the collimation of Standoff.
- Test results of ME0 GEB prototypes: Standoff has good collimation



Automated flying probe test machine

Flying probe test:

- The factory performs automated flying probe test during GEB production.

Test At UCLA and FIT

Integration test with OH and VFATs

1. The goal:

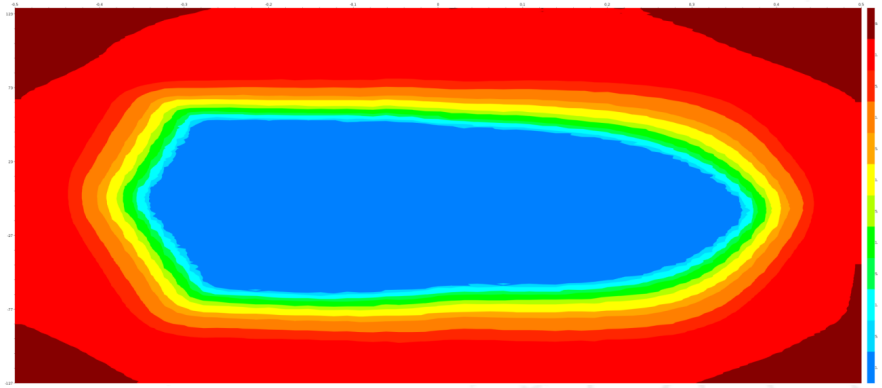
6 ME0 GEBs (2N + 4W) arrived and underwent full-loaded test at UCLA

2. Test process:

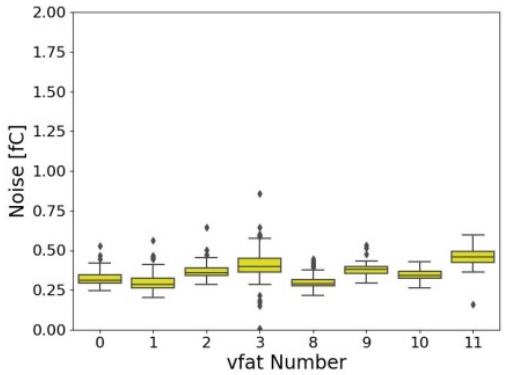
- Check voltages with only FEASTs loaded onto GEB
- Load one ASIAGO (ME0 Optohybrid) and one VFAT
- **Check ASIAGO is ready and can communicate with VFAT**
- **Fully load GEB and check communication with all VFATs** (tests full communication chain and DAQ elinks)
- Take current measurements using current sensing chips + thermistors on ME0 GEB and reading out through ADC of ASIAGO
- **Check uplink and downlink** error rates and eye diagrams

GEB Slot	Component	Status
ASIAGO #1	ASIAGO_v1 #5 (Unfused)	•Receiving power •READY (frontend & backend) •I2C working •IC/EC working
ASIAGO #2	ASIAGO_v1 #10 (Fused)	•Receiving power •READY (frontend & backend) •I2C working •IC/EC working
All VFAT slots	Hybrids	•Receiving power
Any 1 slots	Plugin cards	•Receiving power •Slow Control Firmware being implemented (Needs Addressing)

Test result of full-loaded test



eye diagram



Noise test

Summary

- The design, production and test of all CMS-GEM GEB are completed (except the acceptance test of the last batch of ME0 GEBs at CERN)

- We developed the GEB test criteria, procedure and automatic device, all GE1/1, GE2/1 and ME0 GEBs produced in China passed the test and shipped to CERN

- The CMS-GEM upgrade project is on schedule, Chinese group completed its shared tasks on GEBs (GEM electronics boards).