MTD ETL senor test setup at USTC

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2024.11.14

Outline

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2. Post process for wafers
3. ETL LGAD QA&QC plan
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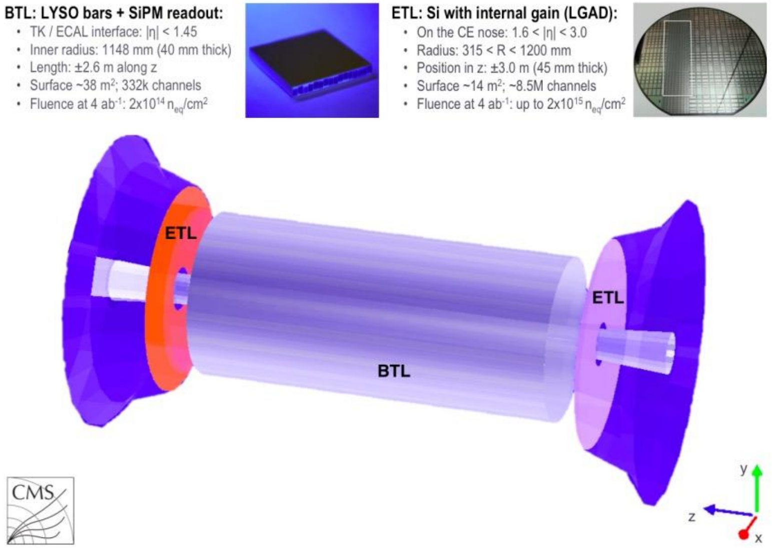
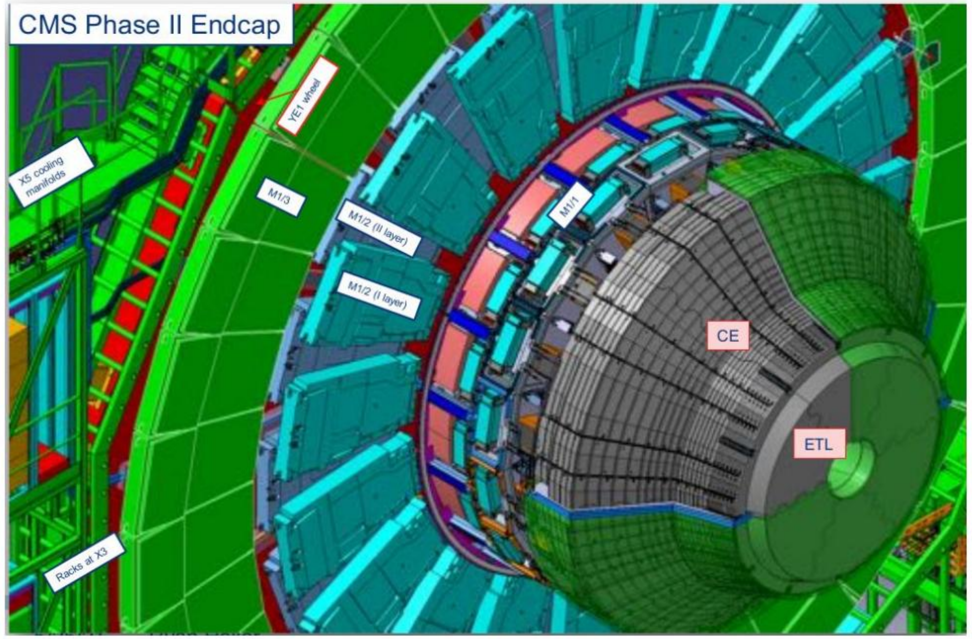
Introduction of the MTD Project

The CMS is going to introduce a new timing detector to measure timing of minimum ionizing particles (MIP) during the High Luminosity LHC (HL-LHC) era. The MIP Timing Detector (MTD) will reduce the effects of up to 200 pileup per bunch crossing, and thus, will provide better reconstruction of particles, and new capabilities for searches for the long-lived particles.





A schematic view of the MTD Endcap Timing Layer. The ETL will be instrumented with thin (50 um) silicon sensors based on the LGAD technology

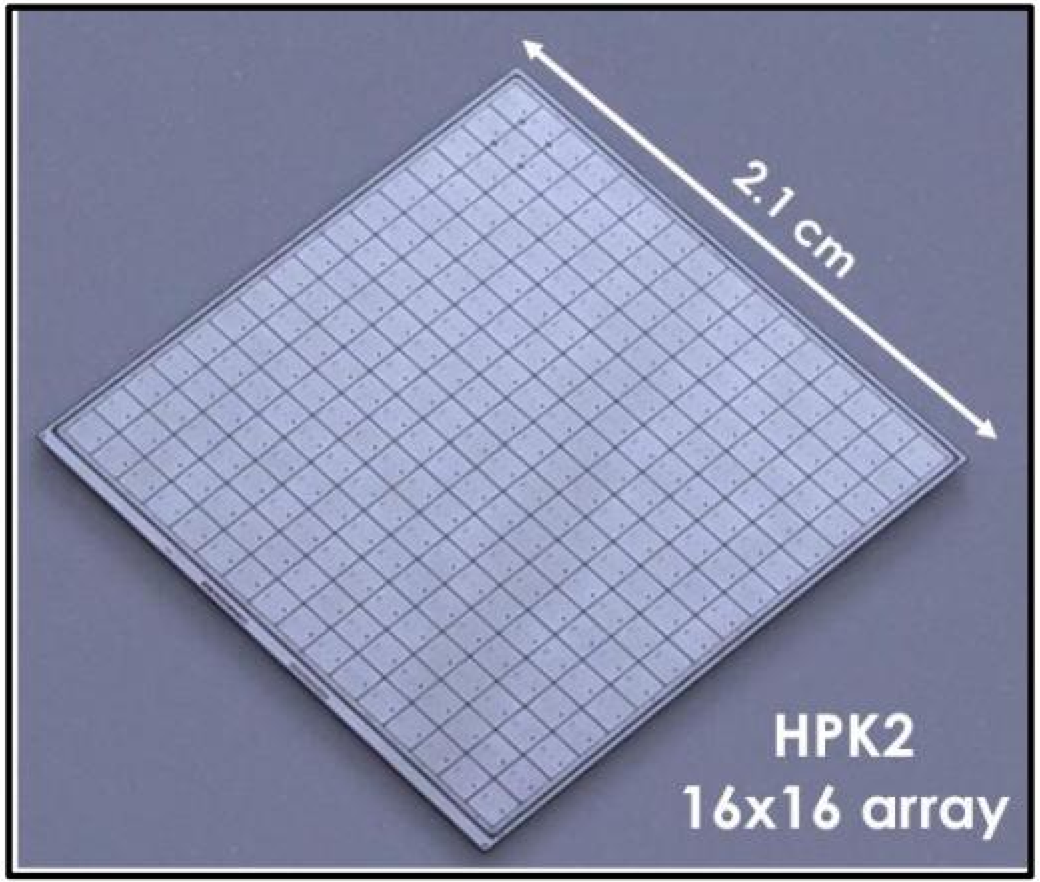
LGAD sensors for ETL

The final ETL sensor will be a 16x16 LGAD, to be bump-bonded to the ETL read-out chip (ETROC)

- 1.3 x 1.3 mm2 pads for a total surface of 21.4 x 21.6 mm2

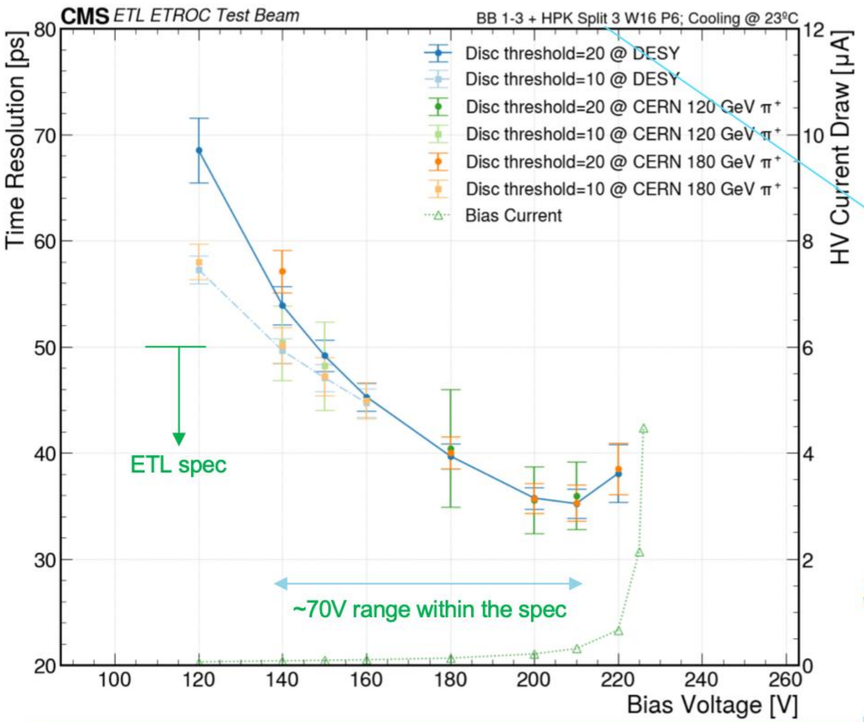
- From the beginning to the end of HL-LHC lifetime, sensors are expected to:
  - achieve time resolution < 50 ps
  - deliver > 8 fC

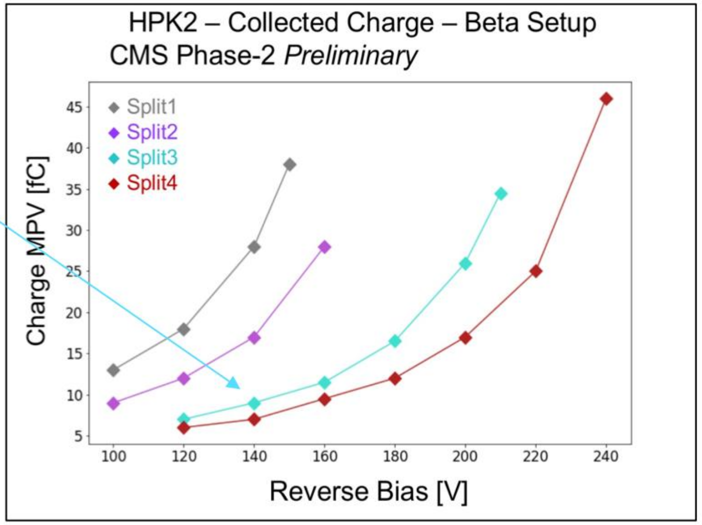
ETL sensors need also to be radiation-hard to survive the harsh radiation environment @ HL-LHC. The 1e15 neq/cm2 threshold is set as it represents the turning point in terms of LGADs performance degradation.



Beam test result for 16x16 sensor bump—bonding to ETROC

ETROC2 beam test at DESY (June) and CERN (Aug and Sep 2024)





Successfully reproduced ~35ps res. with this board.
Results from CERN 120-180 GeV π^+ beams agree with those from DESY 4GeV e^- beam

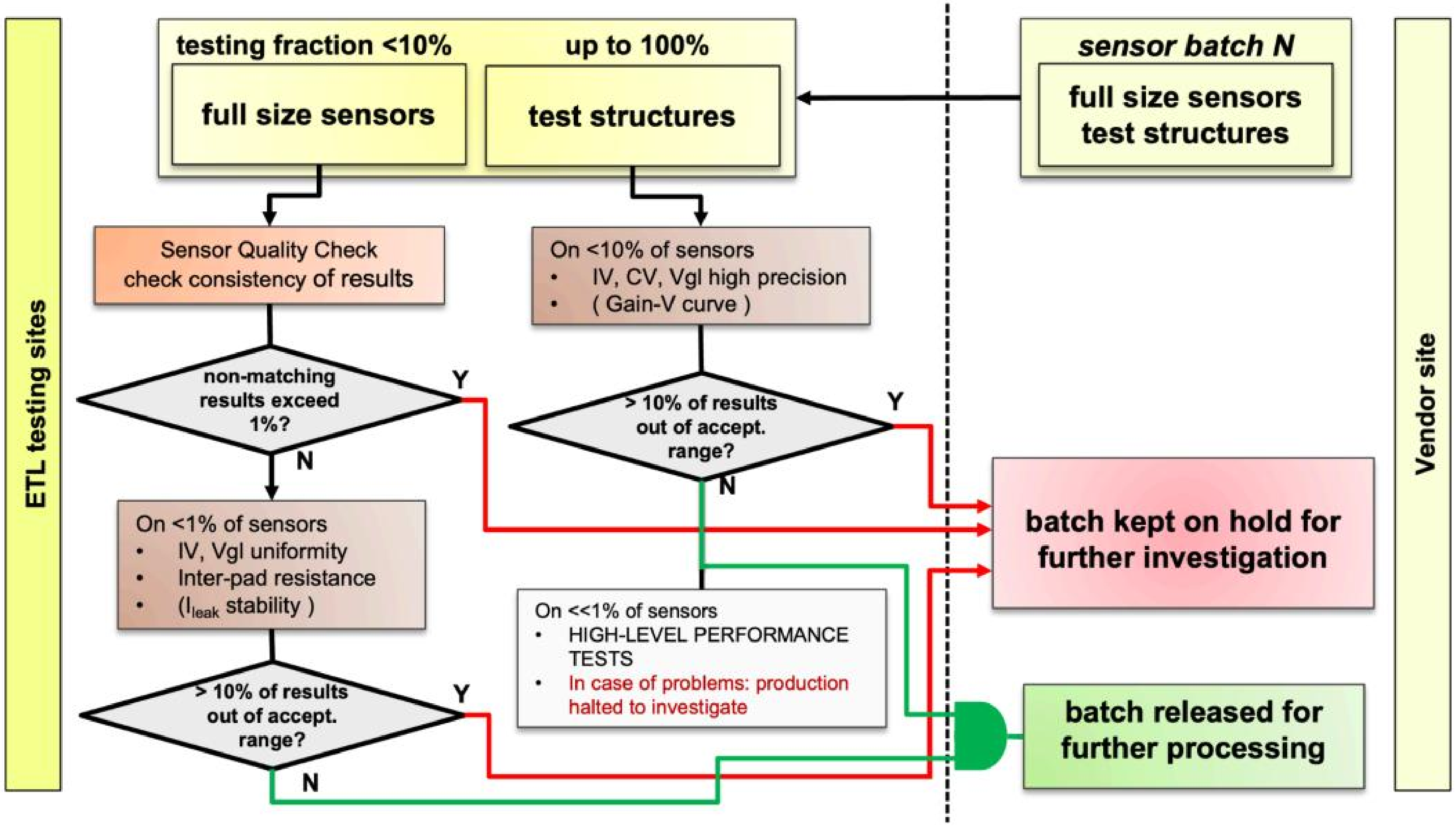
13 10/1/2024 Ted Liu, ETROC2 Testing and Performance Fermilab

To be done: test in cold, and w/ irradiated sensors

Our ETL colleagues have done a series of beam tests for 16x16 sensor bump—bonding to ETROC. Check details below:

https://indico.cern.ch/event/1381495/contributions/5988475/attachments/2938155/5161178/ETROC2—TWEPP—2024—final.pdf

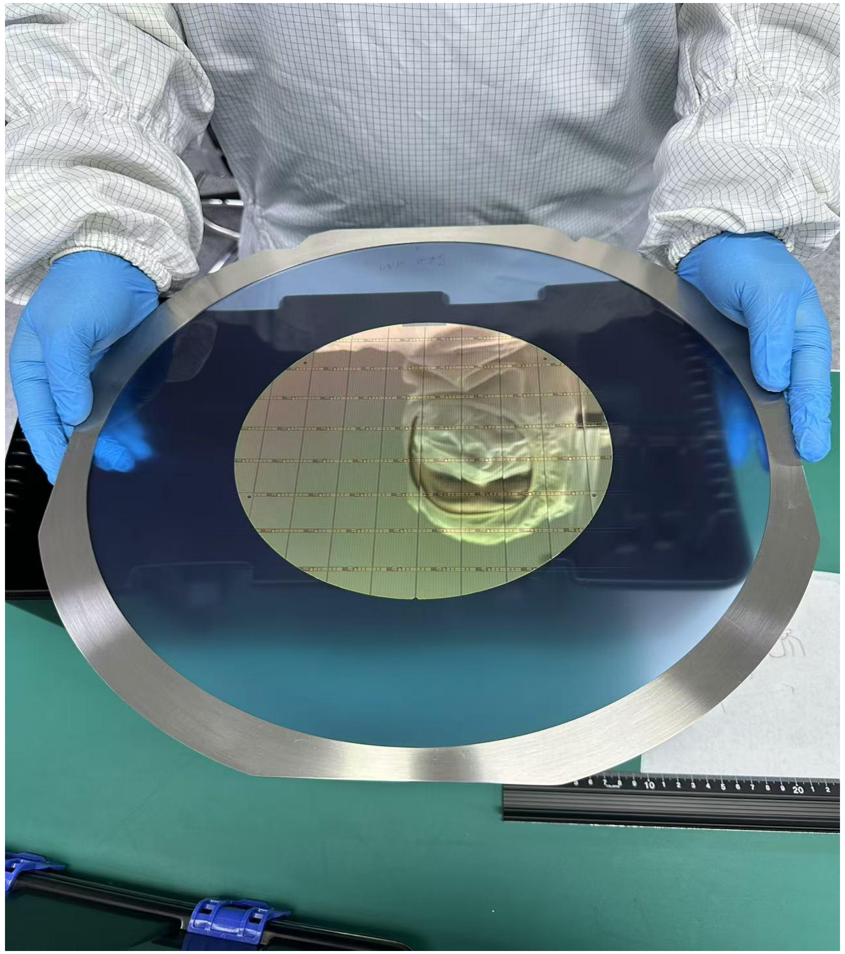
ETL LGAD QA&QC plan

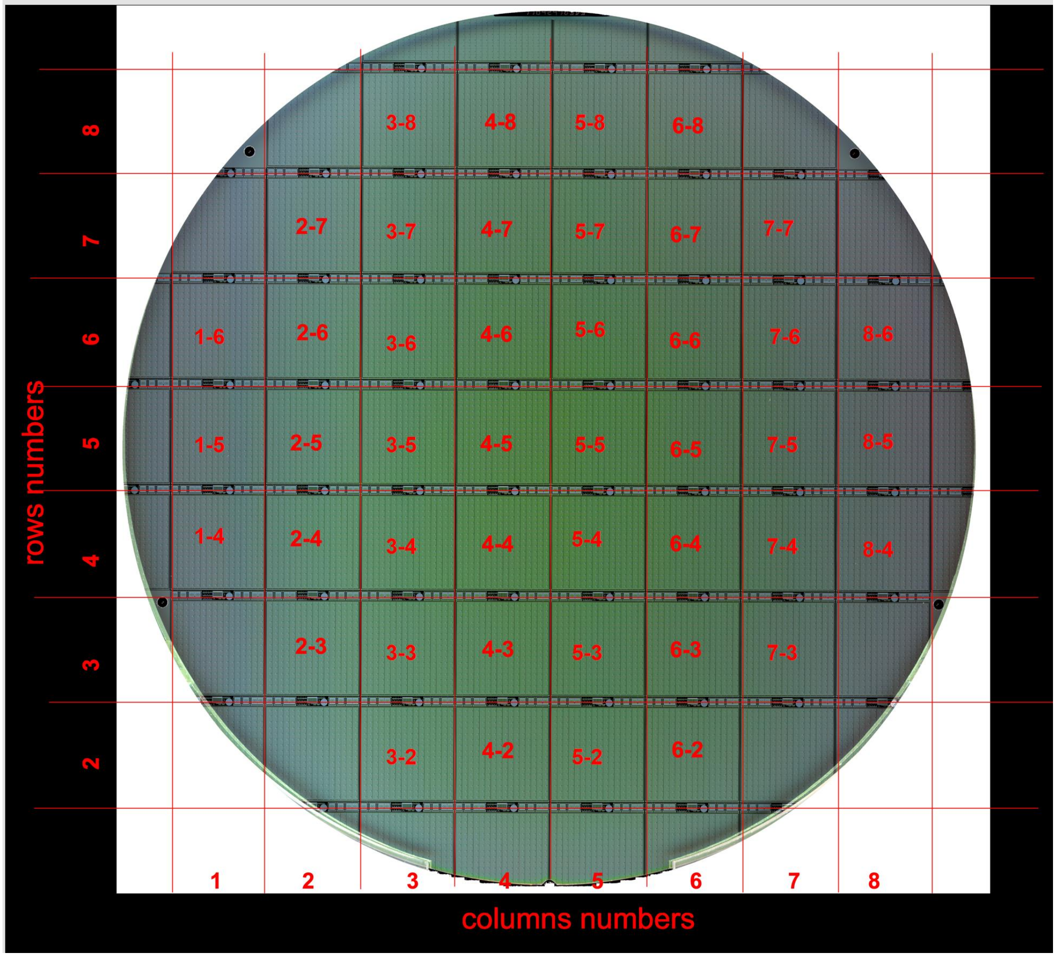


USTC will take both sensor and structures task.

And we have the unique capability to do the precise per channel IV measurement.

Post process for FBK wafer





We have 4 FBK wafers post—processed by NCAP. This wafer will be tested in USTC&Torino lab to verify the post—processing result and the sensors will be used in the module assembly.

Test environment in USTC

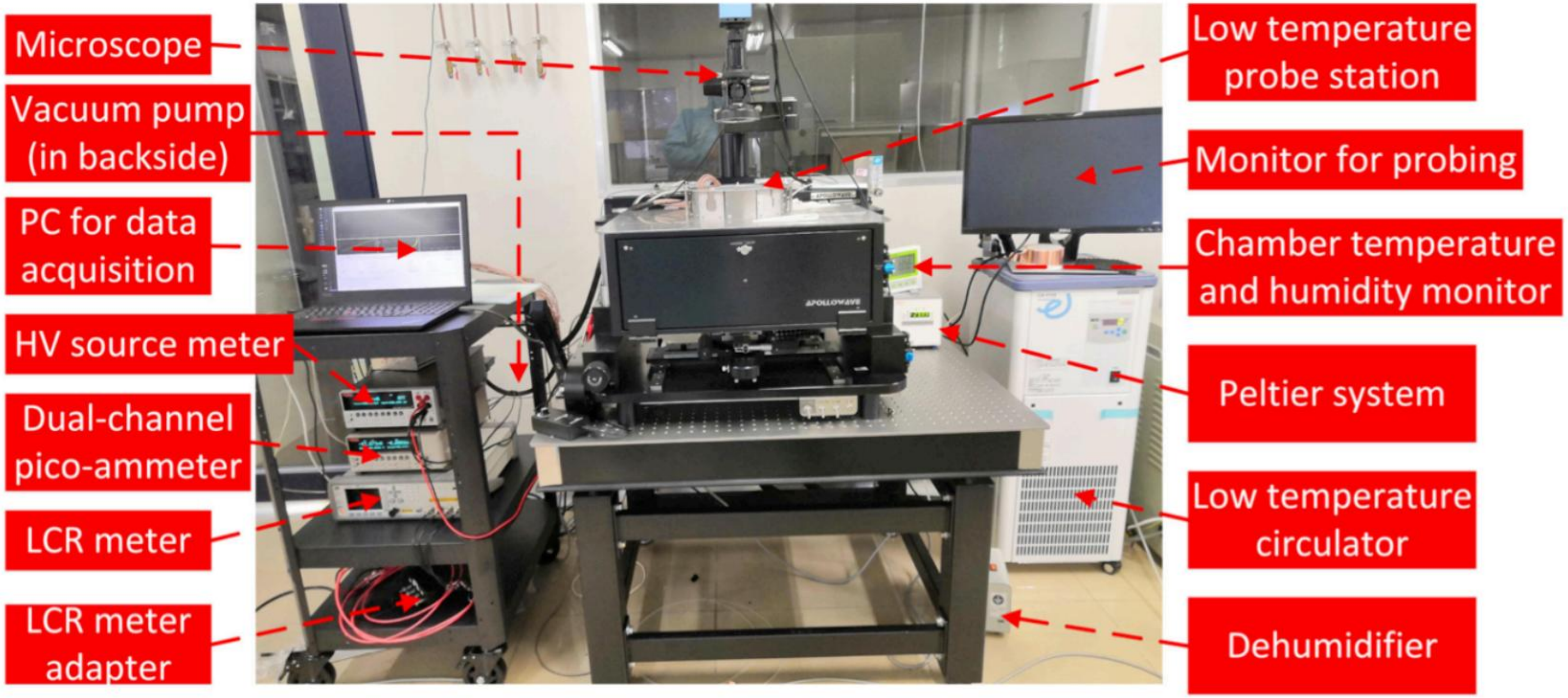
—single needle test system

‣ Stable but slow, suitable for small number of sensors

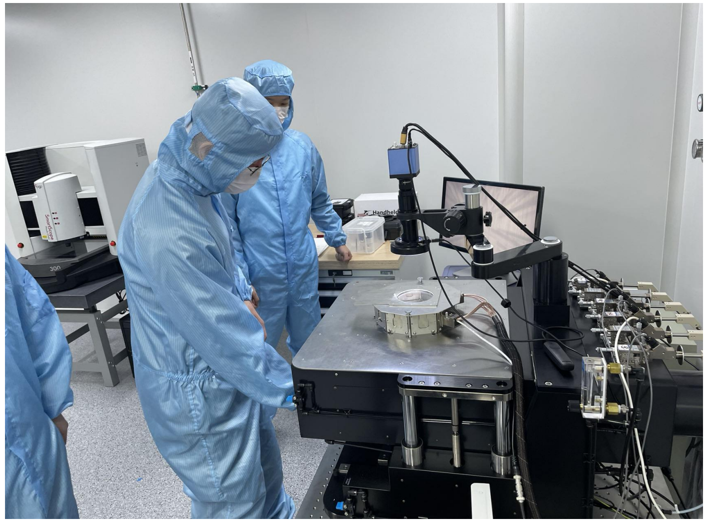
— probe card test system

‣ Complex but fast, suitable for large number of sensors

— Both systems are available at USTC.

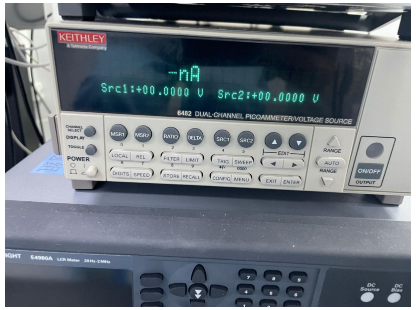


Test environment in USTC



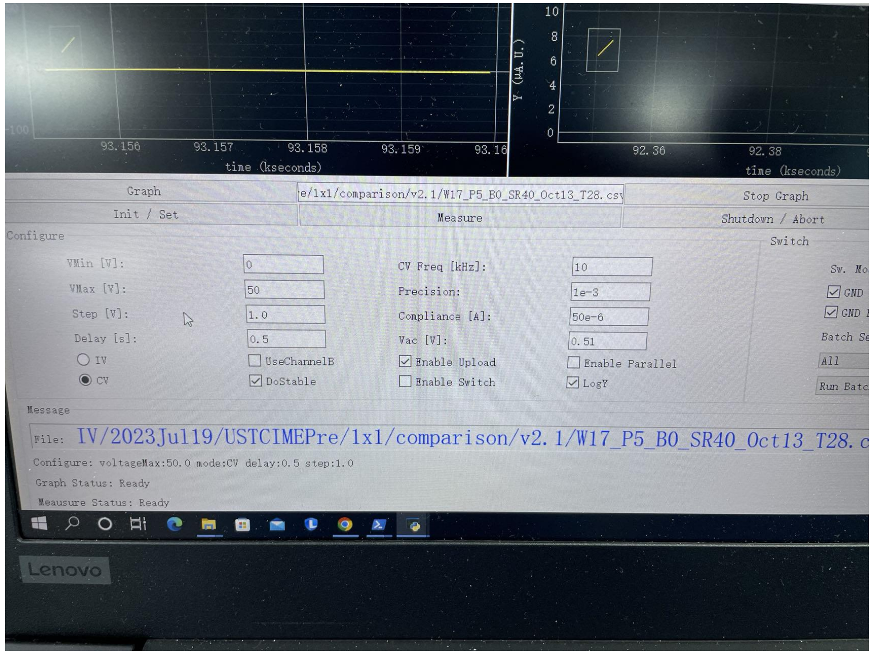
The probe station is apollowave alpha-200CS.
The HV power supply Keithley 2410, range from 0 to 1100 V. Current precision 1 pA.
The pico-ammeter Keithley 6482. Current precision 1 fA.
The LCR meter Keysight E4980A. Frequency from 20 Hz to 2 MHz.

Keithley 2410



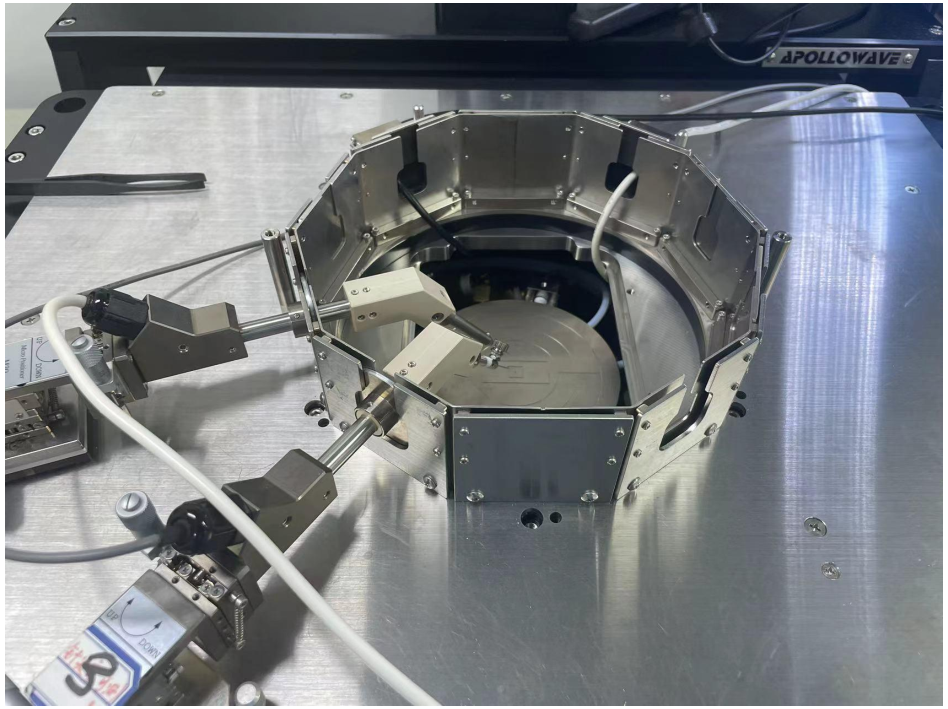
Keithley 6482

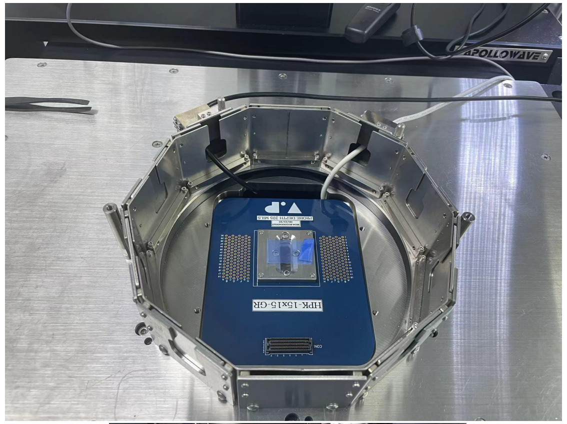
Keysight E4980A

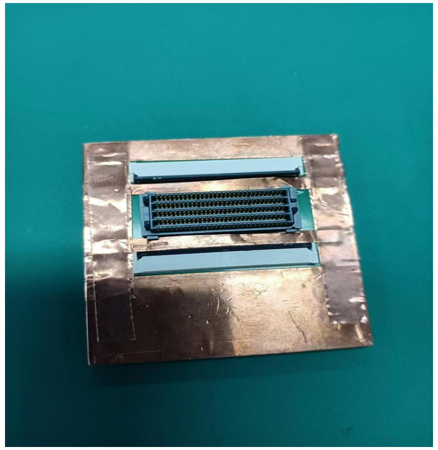


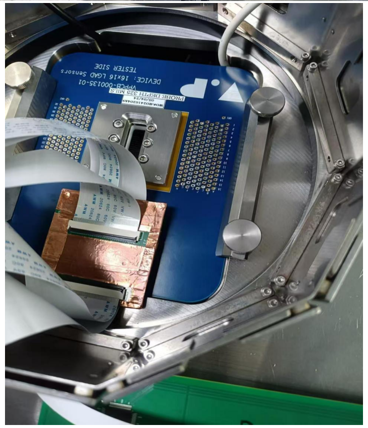
The software UI we used to control the test parameter.

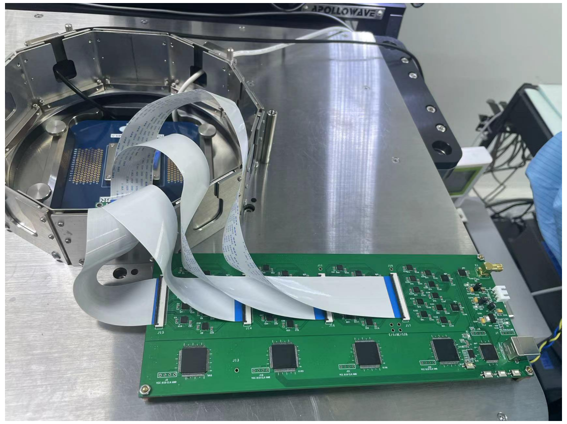
Test environment in USTC











Probe station with up to 5 probes placed in the clean room. Temperature from −40 to 25 degrees.

16*16 probe card controlled by the switch matrix via interface pad

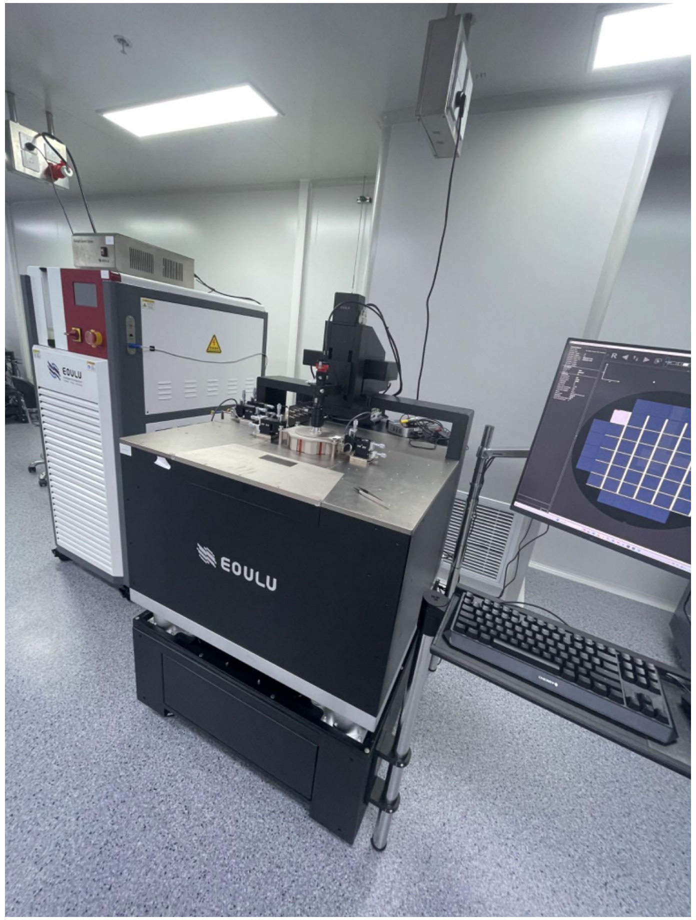
The details of the electronics can be found below:

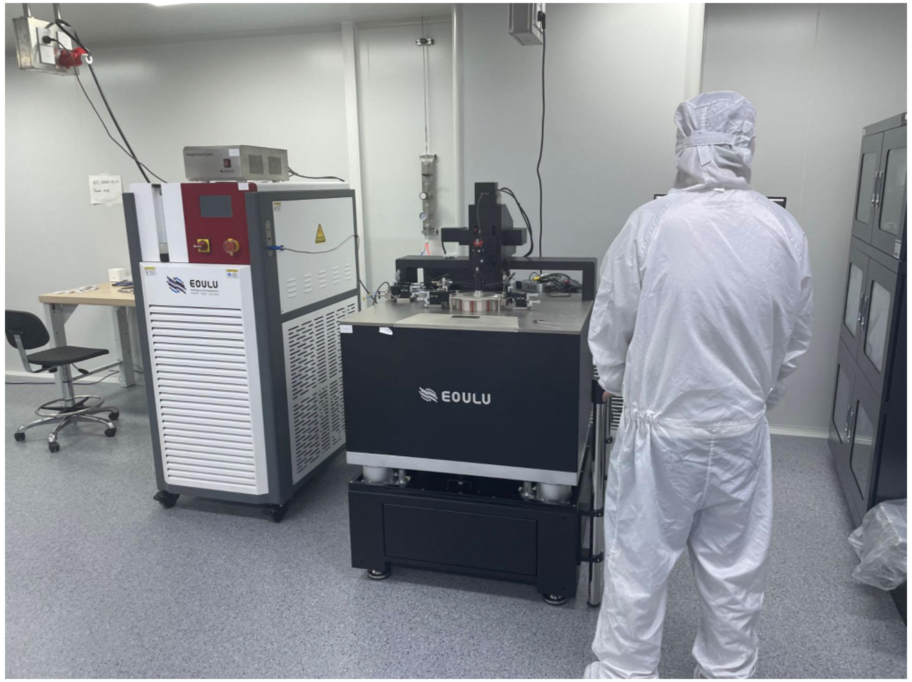
https://www.sciencedirect.com/science/article/pii/S0168900221003843

Test environment in USTC

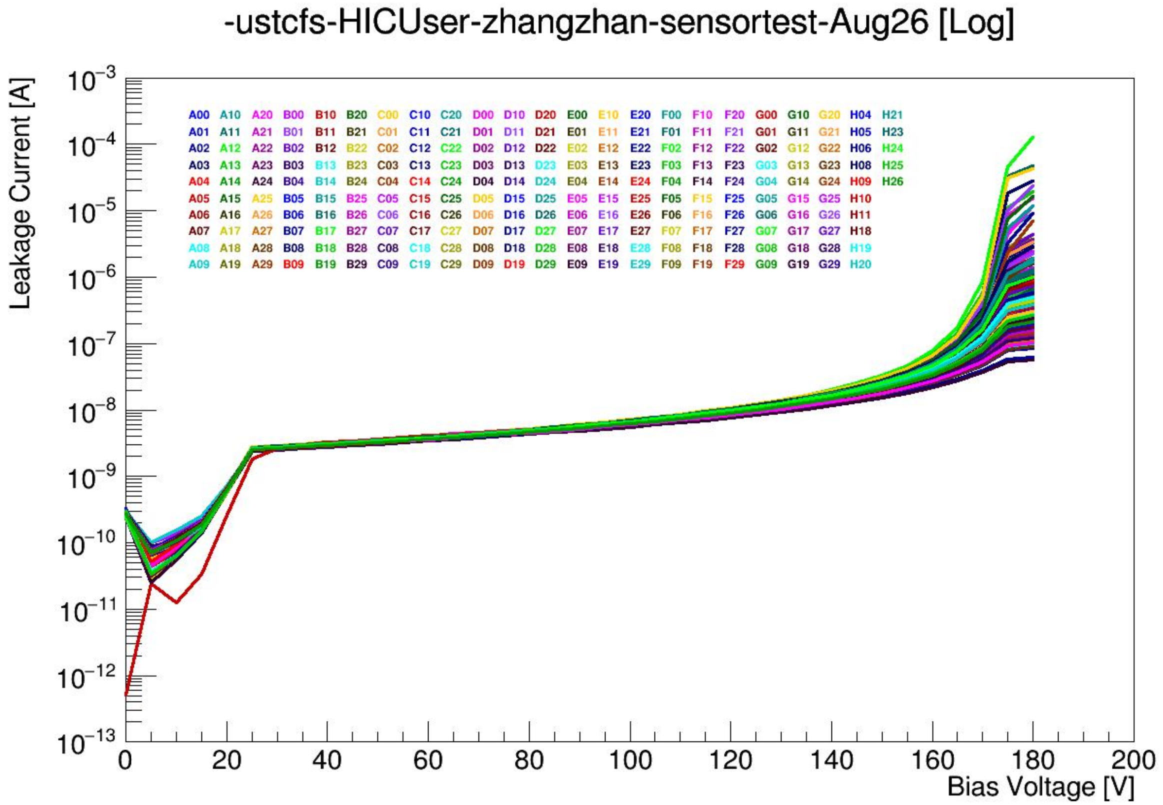
We also have an automatic probe station. Suitable for the wafer test.

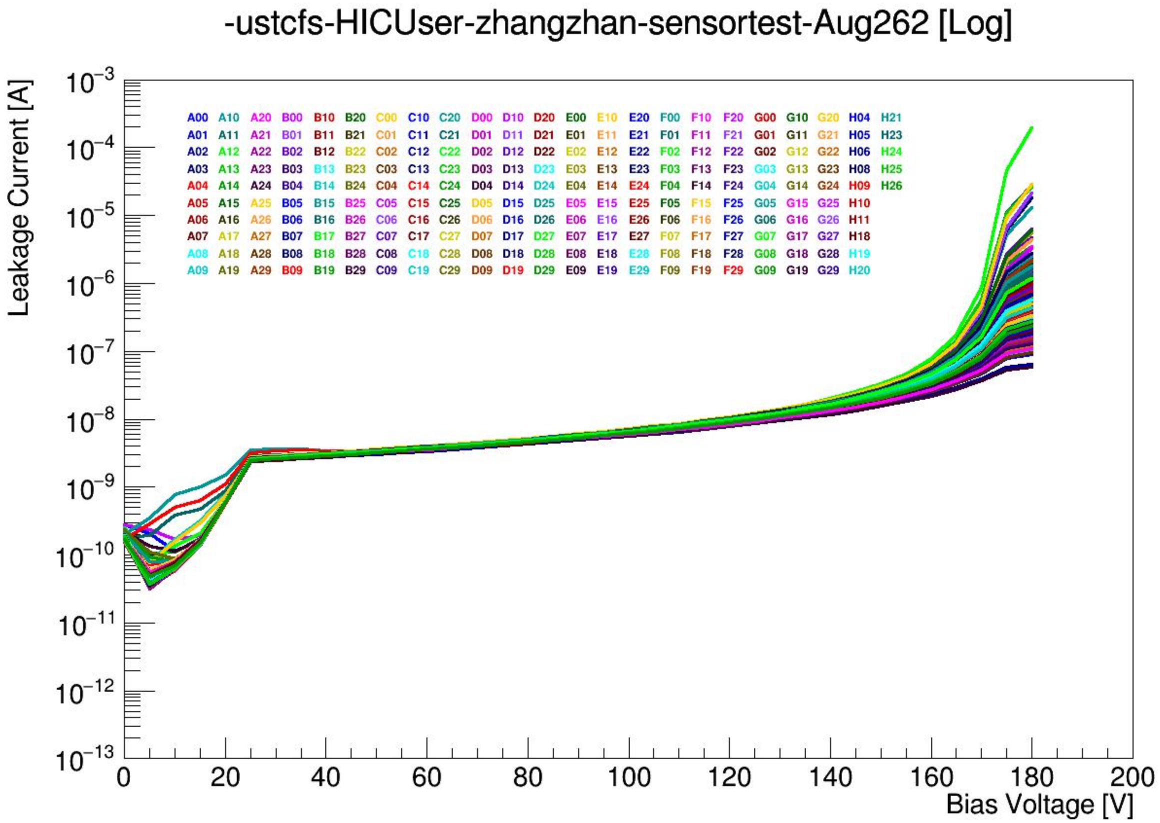
This system is still under test. It will be put into use soon.





Test result, 15*15, IV





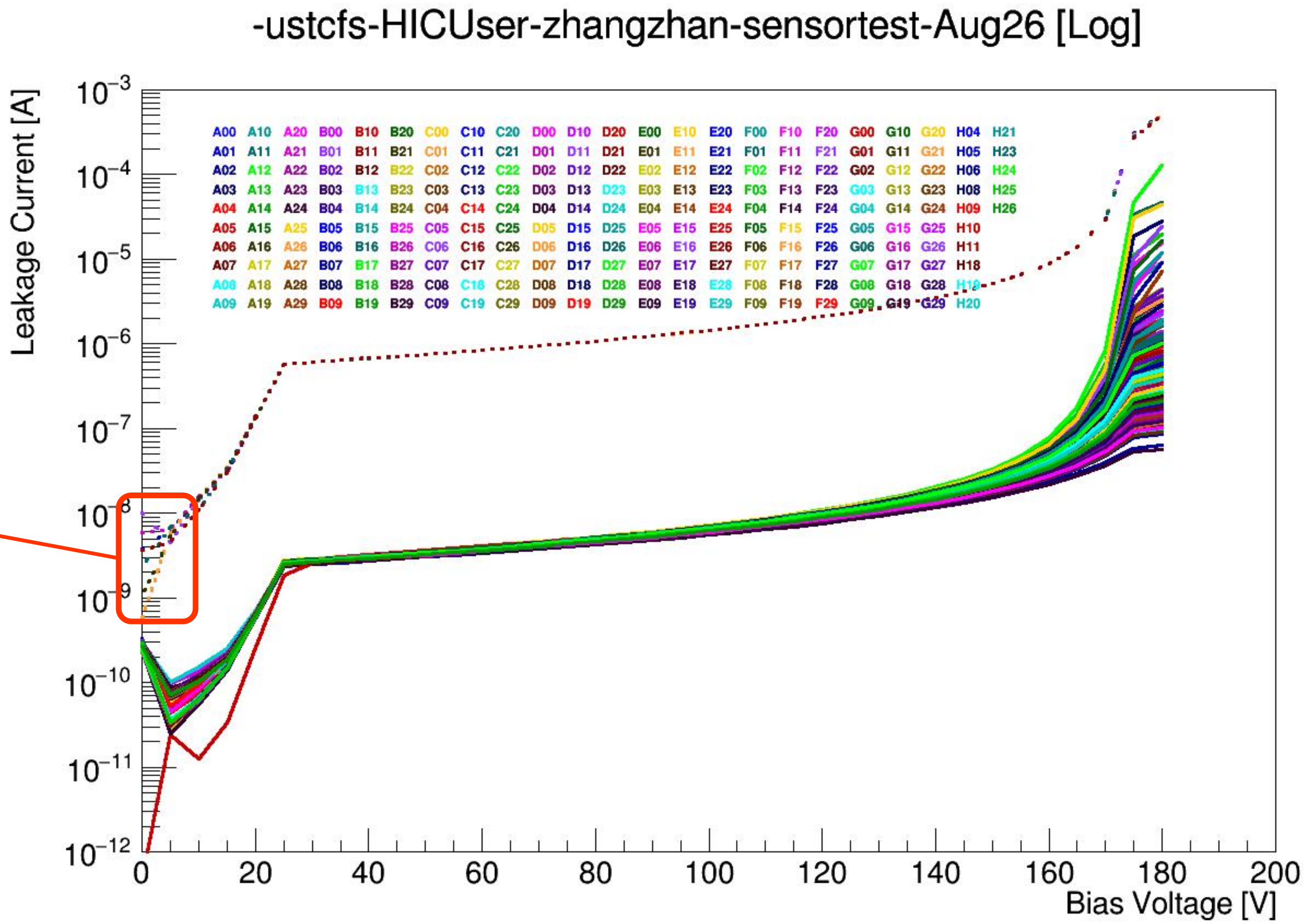
The 15x15 test results using our electronics. We tested a 15x15 sensor (225 sensor pads) with 2 sets of electronics (same design). The voltage step is 5V. Delay is 0.5 s. The total scan time for a 15x15 sensor is about 5 hours. The single pad scan time is about 2 s.

Test result, 15*15, IV

The total current and per channel current in the same plot.

The difference here is because of the 1 pA current precision of Keithley 2410.

We use the Keithley 6482 to read the per channel current and 2410 to read the total current. After depletion of sensor, the total current tend to be consistent.



Summary

- Our test environment and setup are reliable and can perform both IV/CV tests from −40 to 25 degrees. We also have the capability to conduct electrical property tests for Quality Control Test Structures (QC-TS).

- USTC plan to set up the LGAD QC site by Q1 2025.

- We will also participate in the ETL DAQ R&D process.