Construction and Upgrade of ALTIROC Chip Testing System

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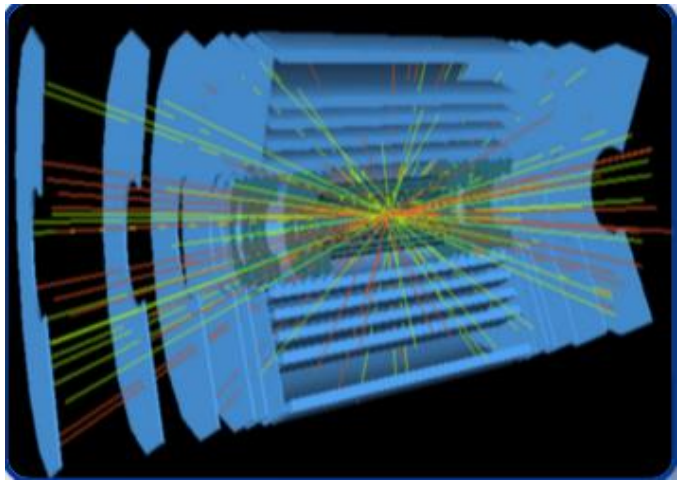
CONTENTS

Background

➢ High-Luminosity Large Hadron Collider(HL-LHC)

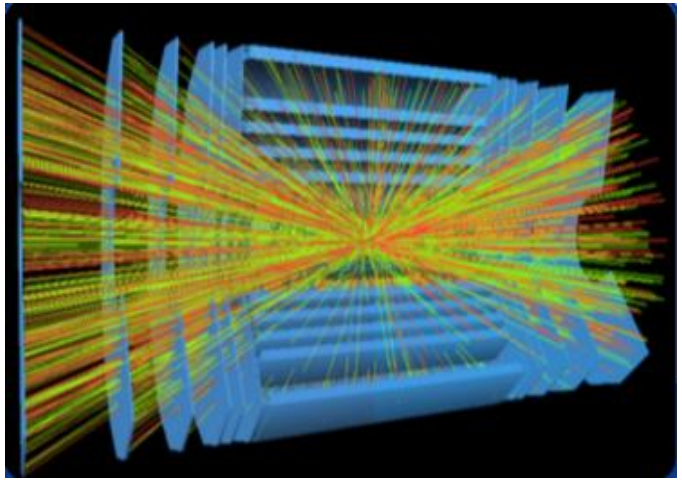
- The HL-LHC will increase the number of collisions to study fundamental components of matter in more detail
- The large increase of pileup interactions is one of the main experimental challenges for the HL-LHC physics programme



The current ATLAS detector

➢ High-Granularity Timing Detector(HGTD)

- **Target**
  - Improve particle arrival time measurement accuracy(ns—>30ps)
- **Requirements**
  - Millimeter granularity
  - Over 3 million readout channels
  - Radiation hardness: 2.5×10^{15} neq/cm^2

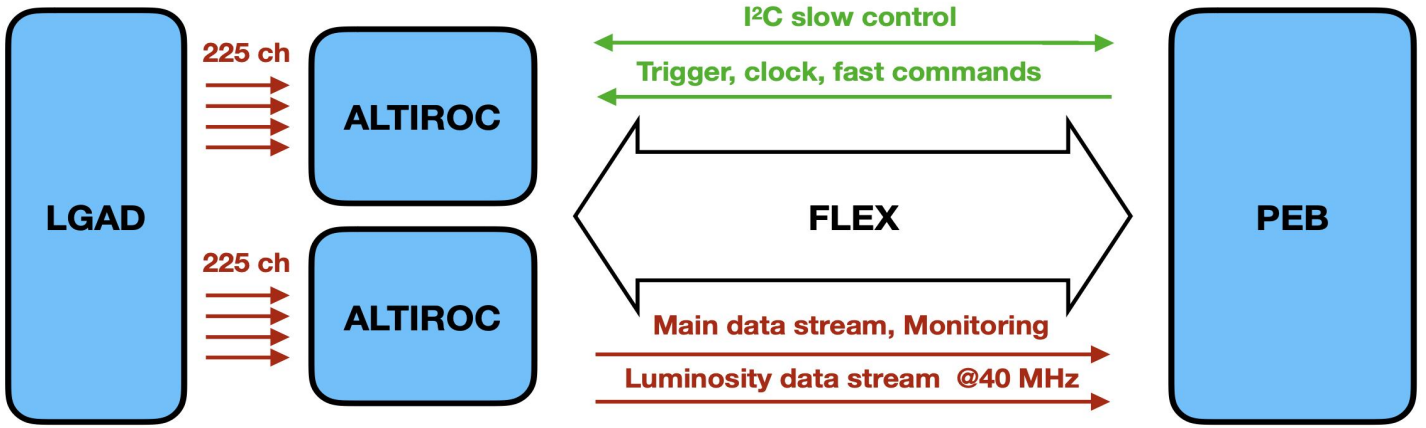


The HL-LHC upgraded ATLAS detector

Background

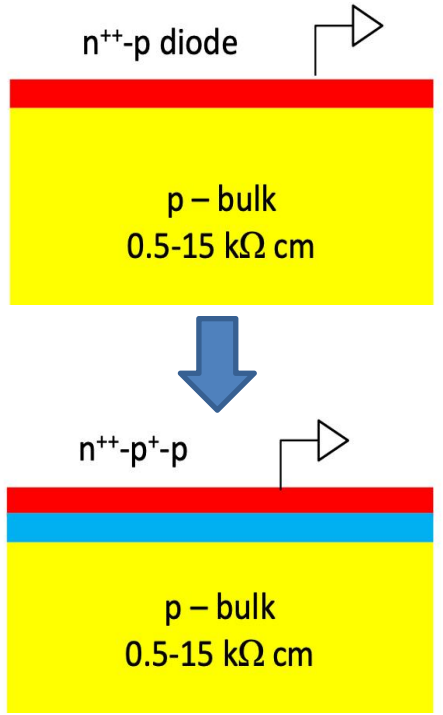
➢HGTD module

- Module components
  - ◆ LGAD
  - ◆ Two ALTIROC chips
  - ◆ Flex cable



➢Low Gain Avalanche Detector (LGAD）

- Good Signal/Noise ratio
- Thin depletion layer (~50um) to decrease t_{rise}
- Moderate gains (10~50) compared to APD and SiPM



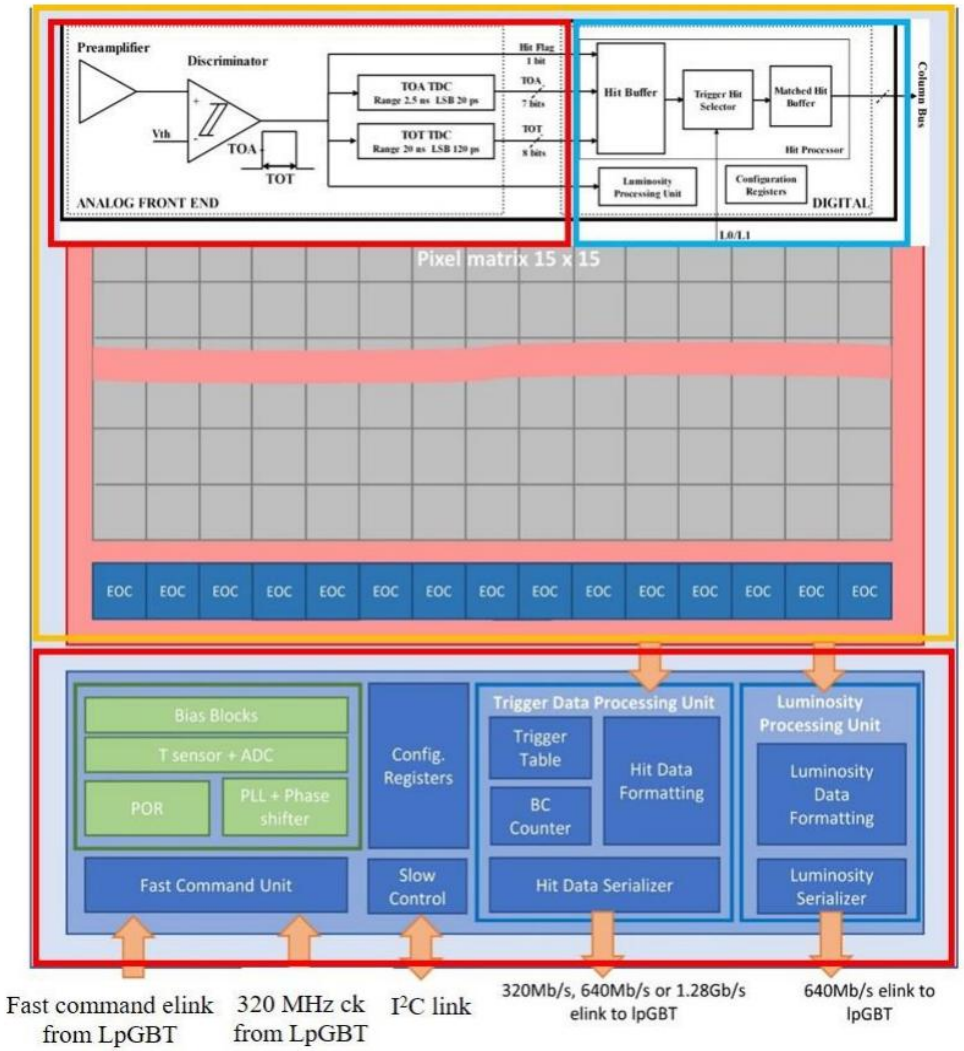
pin diode

LGAD sensor

ALTIROC chip

➢ ALTIROC:ultrafast read ASIC

- **Requirements**
  - Withstand high radiation levels
  - Low power dissipation
  - Read out signals from 4 fC up to 50 fC
- **Structure**
  - Pixel matrix 15*15
  - A Fast Command Control Unit (FCCU)
  - Trigger Data Processing Unit (TDPU)
  - Luminosity Processing Unit (LPU)
  - I2C module



ALTIROC3 general architecture

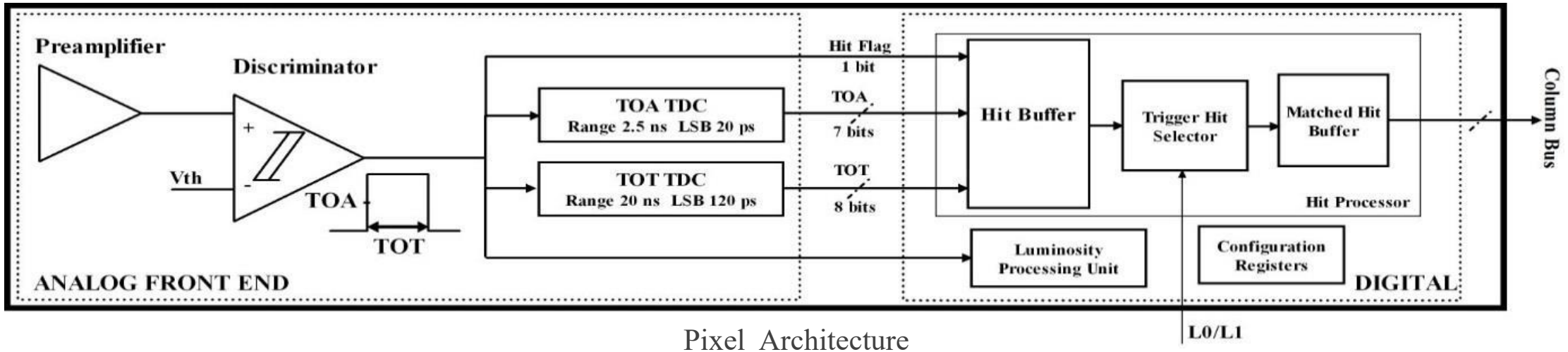
ALTIROC chip

➢Analog part：

- The analog part is composed of a Transimpedance preamplifier(TZ) followed by a discriminator that is connected to two TDCs (Time to Digital Converter)
- Two TDCs: Time of Arrival (TOA)TDC and Time over Threshold (TOT) TDC

➢Digital part:

- When a Hit comes, the timing data are stored in a Hit buffer， which is a 1536 x 19 bits SRAM
- When a L1 trigger signal is received,data are stored in a Matched Hit buffer that is 8-depth FIFO

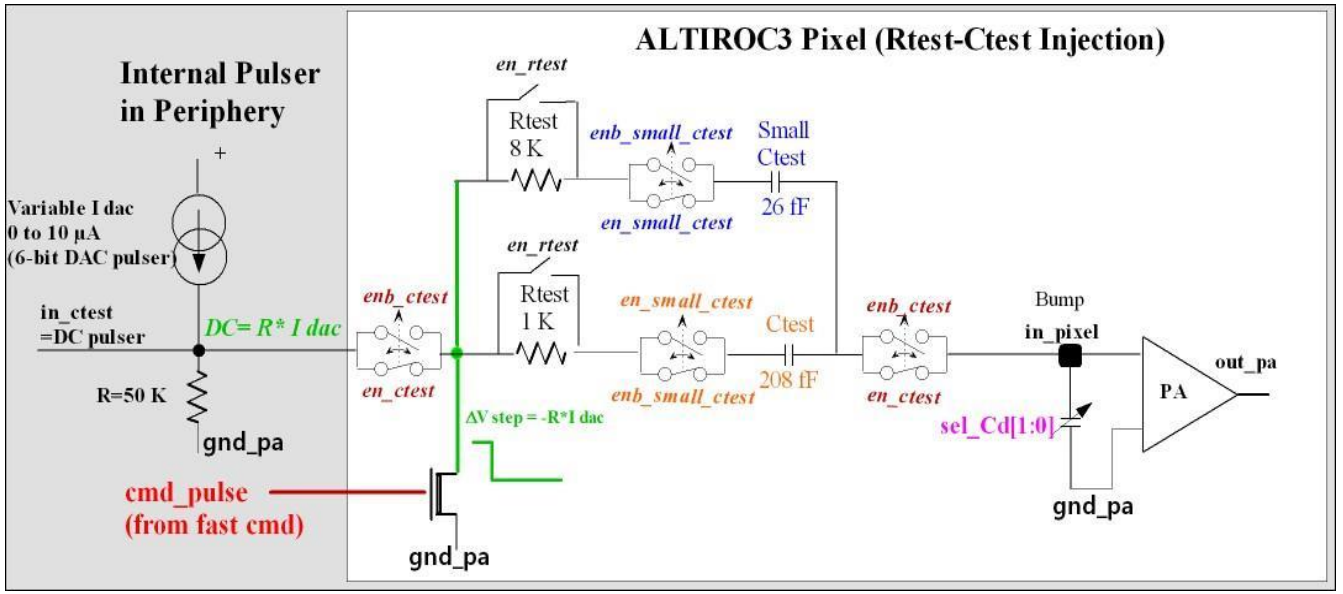


Pixel Architecture

ALTIROC chip

➢ Altiroc3 calibration system

- The injection charge circuit is used to mimic and inject Dirac or LGAD charges in each channel
- The pulser is made of a programmable DC current and that is interrupted by "cmd_pulse"



➢ Fast command

- The CAL fast command is used to inject a calibration pulse
- We can achieve the acquistion of timing data by using fast commands correctly

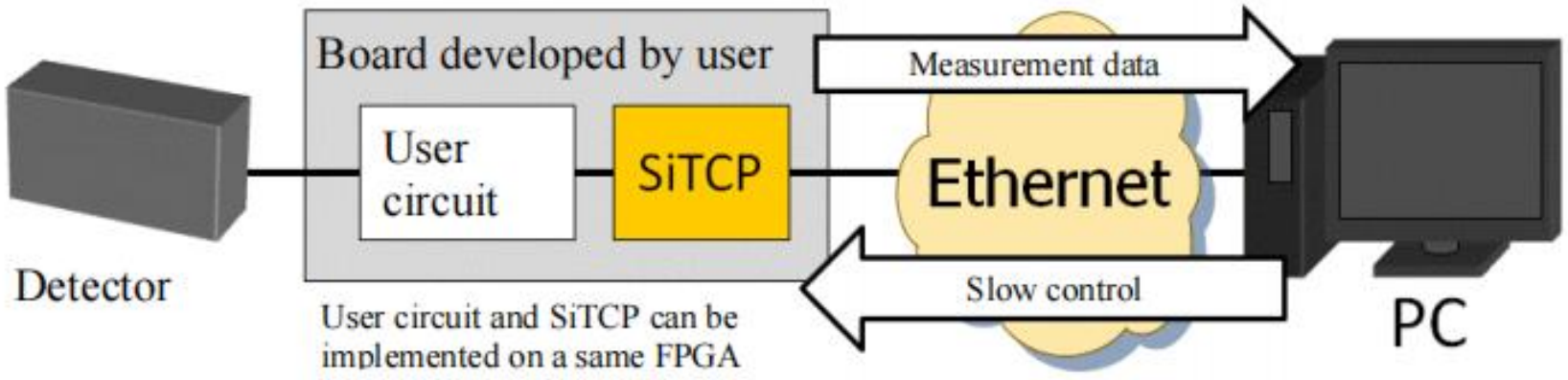
ALTIROC3 Fast command table and effects

Fast Commands	Binary Code	Comments	Trigger data path (Configurable latency from 2 to 1536 BCs)
IDLE	8'b11110000	Needs to be sent continuously and is used to keep the fast command unit aligned	
TRIGGER	8'b10110010		L1 counter incremented of 1, the first packet will have L1ID = 1 N.B. : After packet with L1ID = 4095, next L1ID = 1
CAL	8'b11010100	Calibration pulse used for: • pedestal adjustment • TOA and TOT resolution	N.B.: If more than 127 pixels are stimulated in the same BC the readout is stuck

Testing system

➢SiTCP features

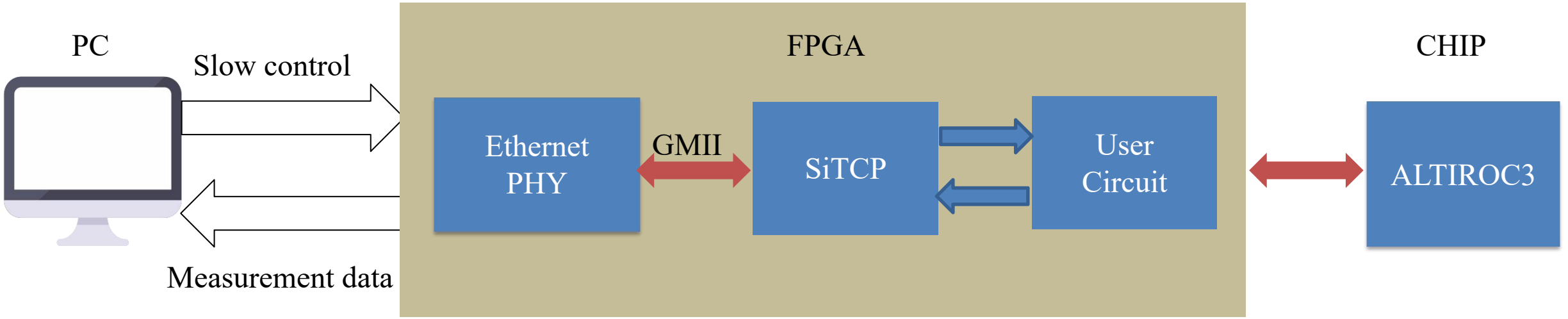
- **Hardware TCP/IP/Ethernet communication**
  - ➢ 10Mbps to 1Gbps Ethernet
  - ➢ High speed communication stable at the upper limit of TCP
  - ➢ Slow control function (Using UDP)
- **Easy implementation**
  - ➢ Small circuit scale
  - ➢ Provided as FPGA library (Xilinx)
  - ➢ Simple user I/F easy to handle



Testing system

➢System framework

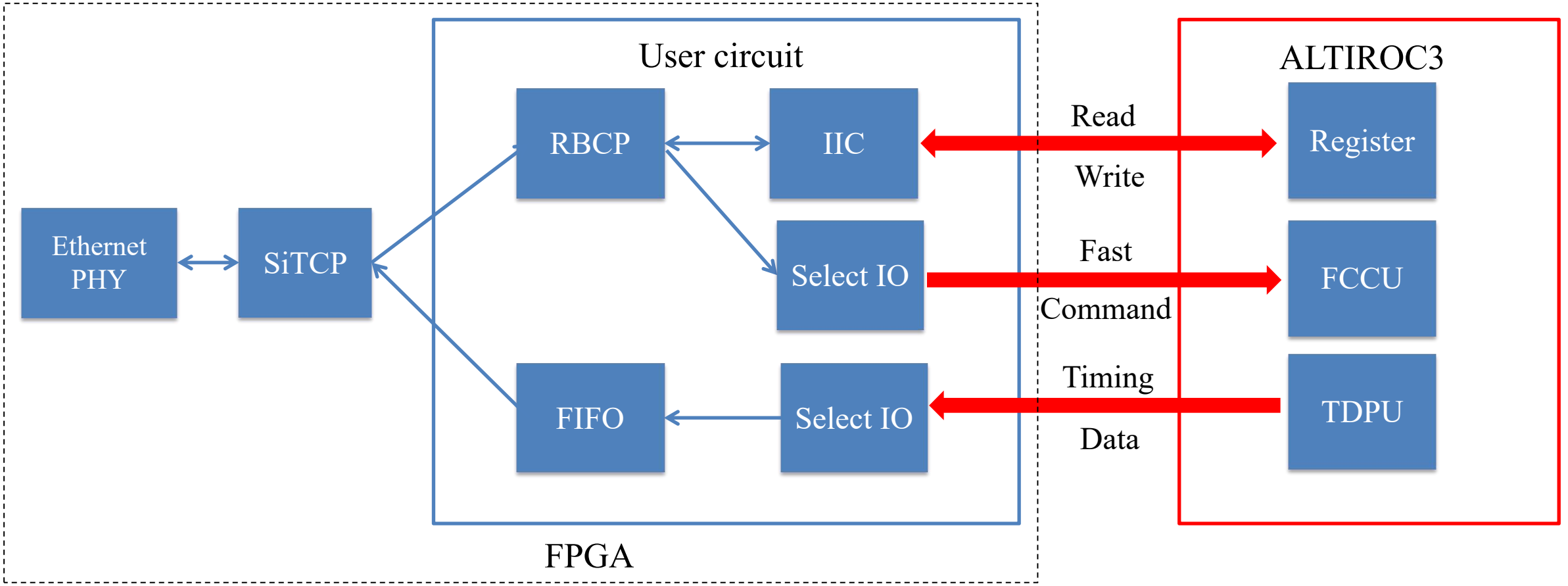
- Measurement data:use TCP protocol， for data transfer
- Slow control :use UDP protocol ,for control of register



Testing system

User circuit

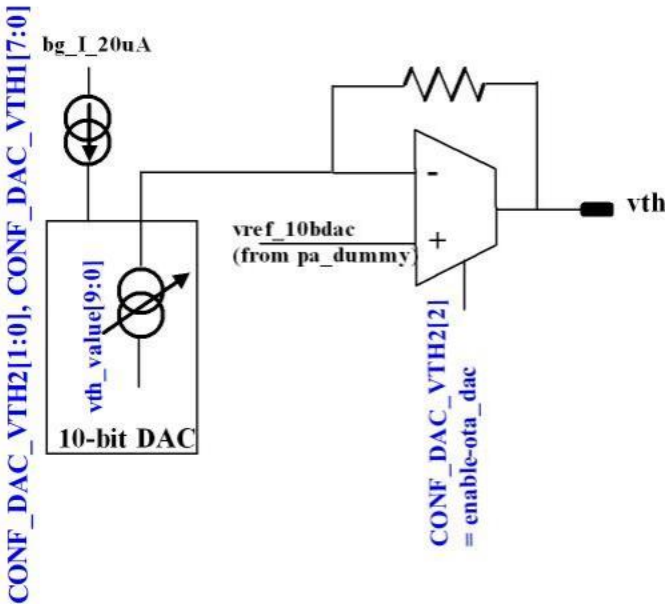
- RBCP --> Select IO Parallel to serial FIFO --> Select IO Serial to parallel
- Data readout:send one CAL command followed by 5 IDLES then send one TRIGGER (L1) command



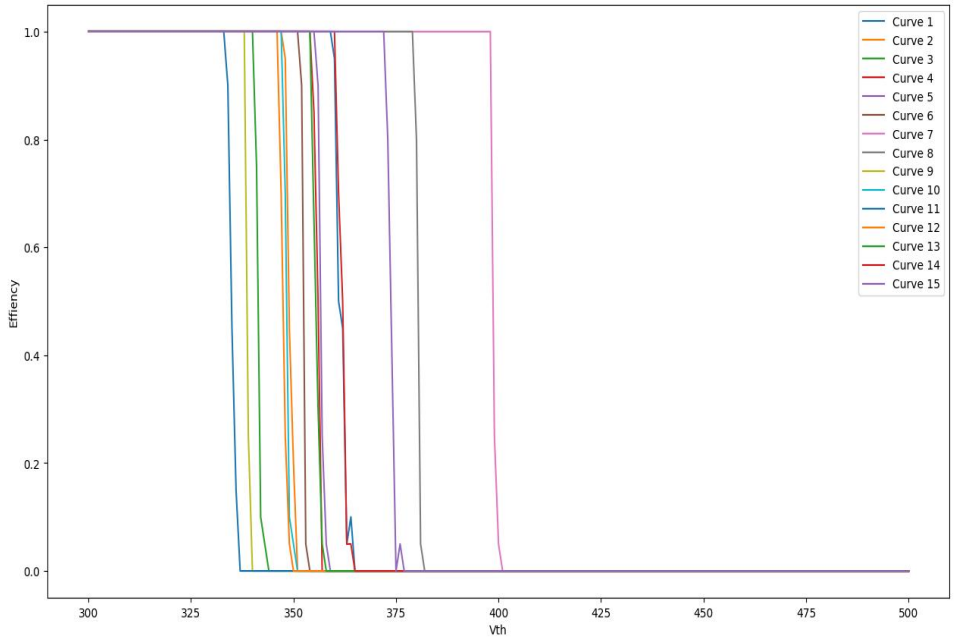
Testing system

➢Results

- A common 10bit-DAC is used to set the common threshold of all the discriminators.
- VthScan:Select the first column,set a fixed charge,set threshold from small to large



10-bit DAC for Vth settings



VthScan_col0

Testing system

➢Results

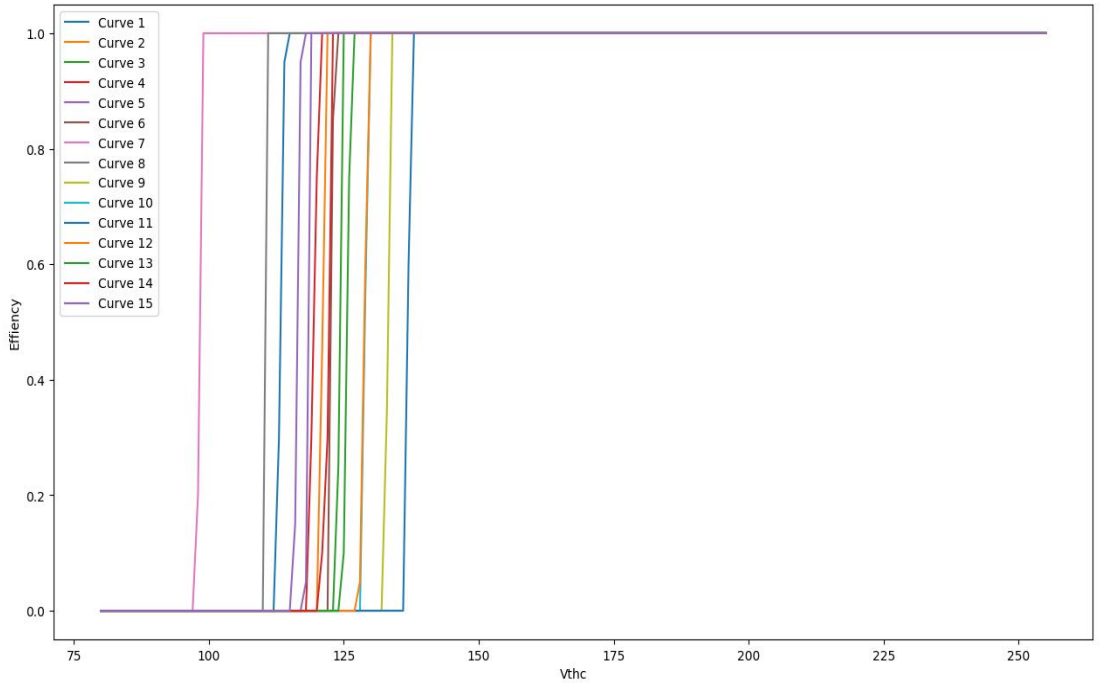
- For each pixel, a local 8-bit DAC correction (vthc) is used to compensate for the non-uniformity of the preamp output DC voltage
- VthcScan:

  Select the first column, set a fixed charge

  set suitable Vth,set Vthc from large to small

CONF_DAC_VTH_OTA Range Table	
CONF_DAC_VTHC_OTA2_RANGE[4:3]	VTHc range/slope
00	slope -0.27 mV/DACU range 68 mV
01	slope -0.35 mV/DACU range 90 mV
10	slope -0.5 mV/DACU range = -0.5 mV/DACU range 130 mV
11	slope -1mV/DACU range 250 mV

vthc range and slop



VthcScan_col0

Summary and outlook

Summary

- If we want to get data from Altiroc3,we should send a sequence of fast command
- We have achieved the construction of ALTIROC3 testing system with no 8b10b.
- We have drawn the picture of the VthScan and VthcScan

Outlook

- Implement other functions of the chip
- Complete data transmission with 8b10b code
- **Upgrade the testing system**
  - Achieve ten gigabit network function
  - Add the external trigger function
  - ……

Thank you for listening