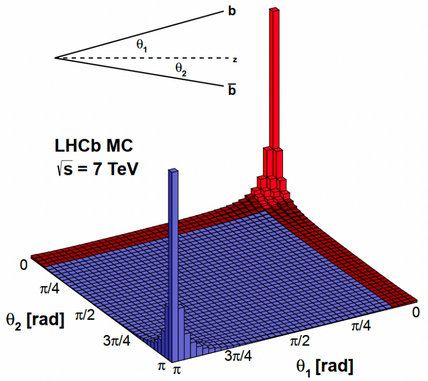
# UT commissioning and performance

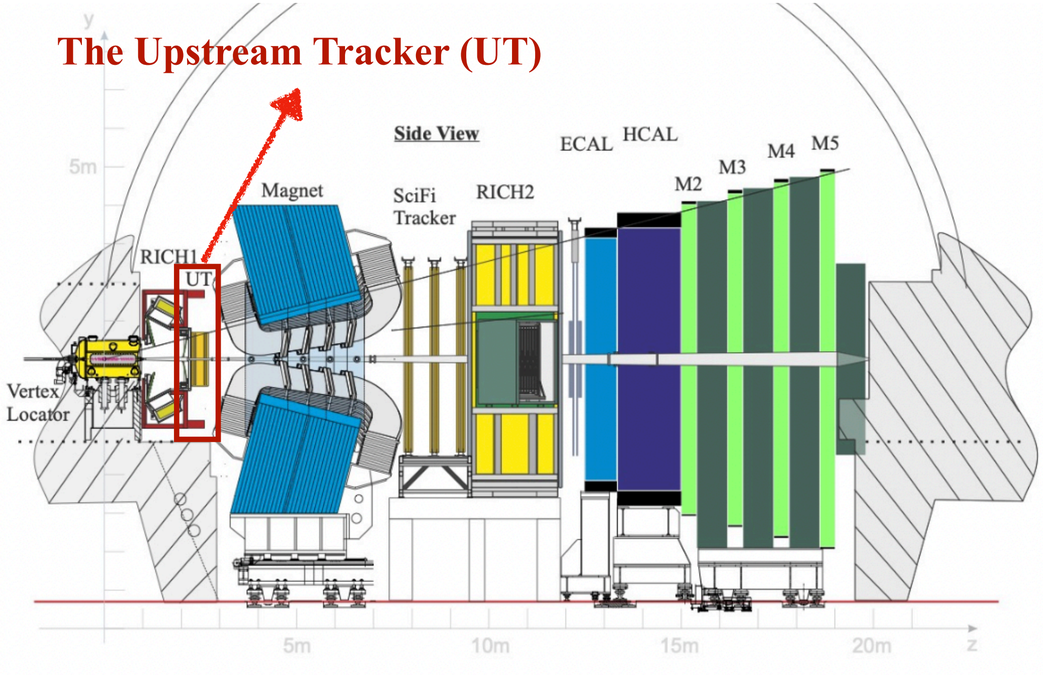
**Mingjie Feng (冯铭婕, IHEP) on behalf of the UT Working Group**

**The 10th China LHC Physics Workshop (CLHCP2024)**
**13-17, November, Qingdao**

- Single arm forward spectrometer ( 2<η<5 )
  - Designed to study CP violation and rare decays in hadrons containing b- and c-quarks

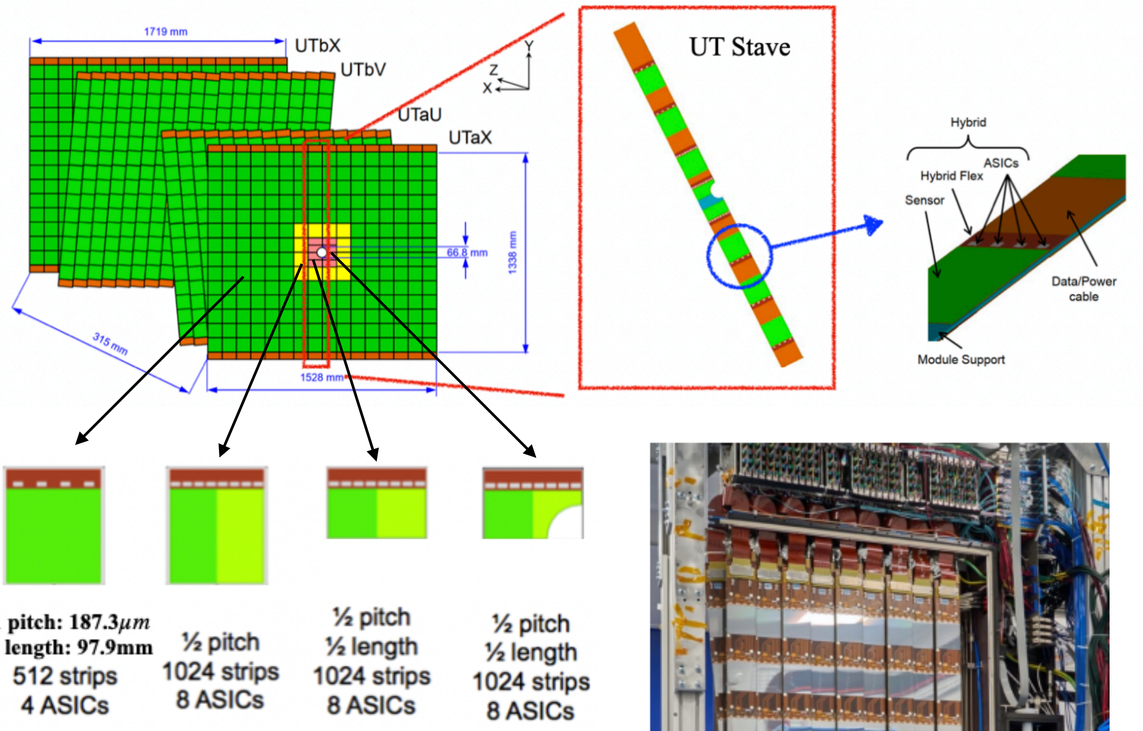


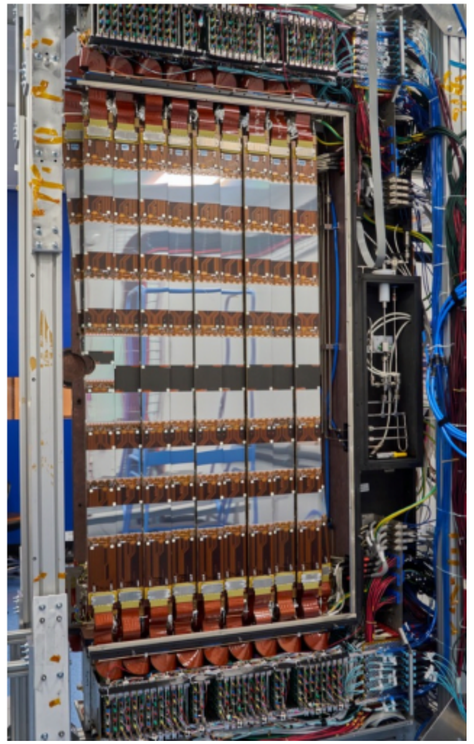

- LHCb data-taking phases
  - Run1(2010 - 2012) and Run2 (2015 - 2018)
    - Running with luminosity leveling at $4 \times 10^{32} cm^{-2} s^{-1}$
    - Total of $9\, fb^{-1}$ (3+6) collected
  - **Run3 (2023 - ) — LHCb Upgrade**
    - Luminosity increased by a factor of 5 → $\mathscr{L} = 2 \times 10^{33} cm^{-2} s^{-1}$
    - Software-only trigger to 40 MHz readout
    - Sub-detector upgrade



# UT Detector

- Silicon strip detector, located upstream of the LHCb bending magnet
- Side × 2, Layer × 4, Stave × 68, Module type × 4 with different silicon strip densities
  - Full coverage
  - Higher segmentation sensors in the region surrounding the beam pipes
- 40MHz readout with SALT (Silicon ASIC for LHCb Tracker) chip
  - 4192 (ASICs) × 128 (channels) = 536,576 (Strips)
  - CMOS 130nm technology
  - Fast shaping time: Tpeak < 25ns

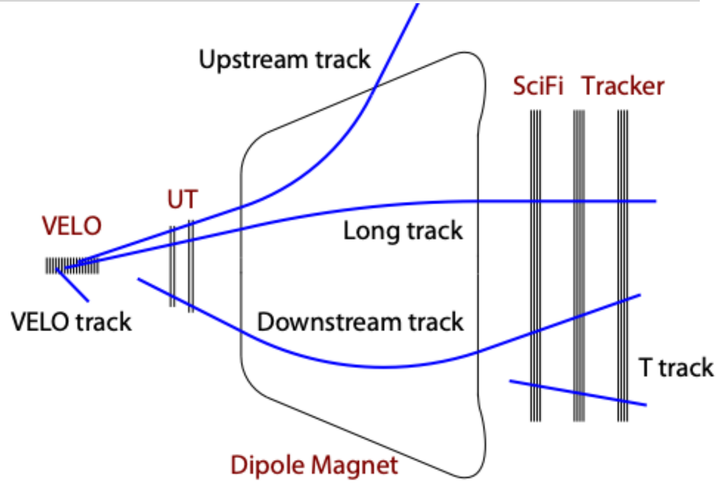


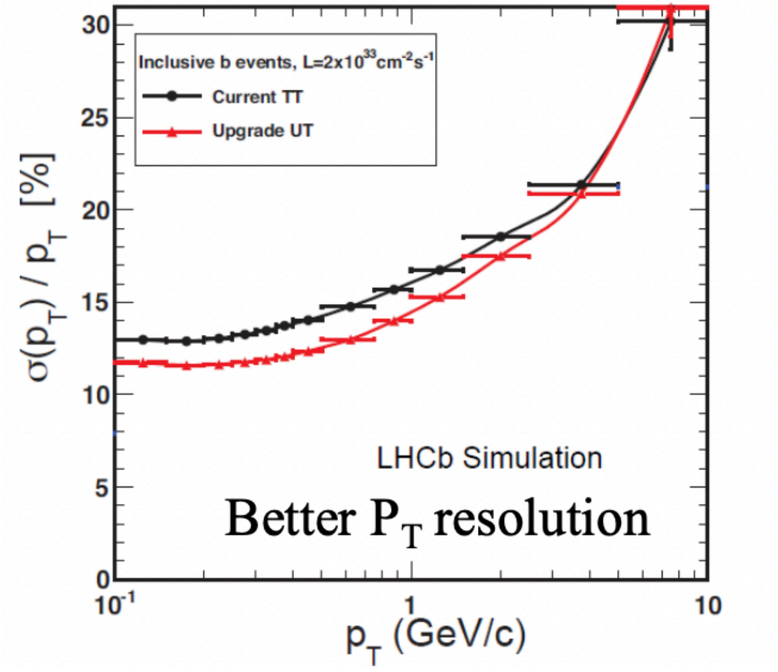
# UT in LHCb Tracking System

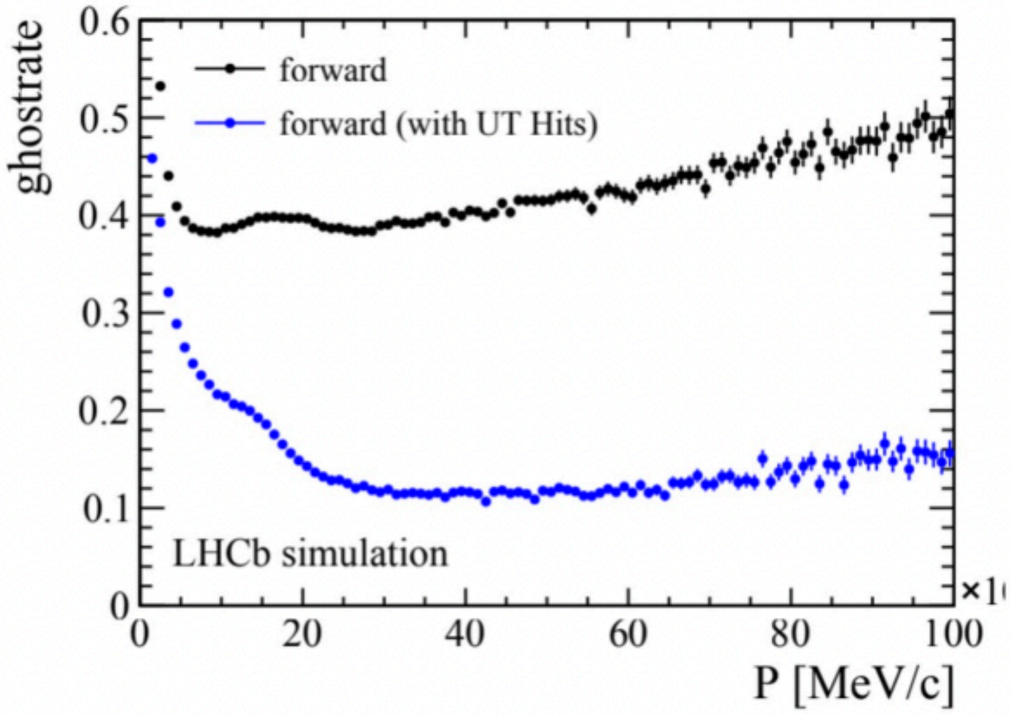
**UT plays a key role in LHCb tracking system**

- Fast estimates momentum for trigger system
- Improve momentum resolution
- Reduce ghost rate in track
- Increase reconstruction efficiency for $\Lambda_0$ $K_S^0$…



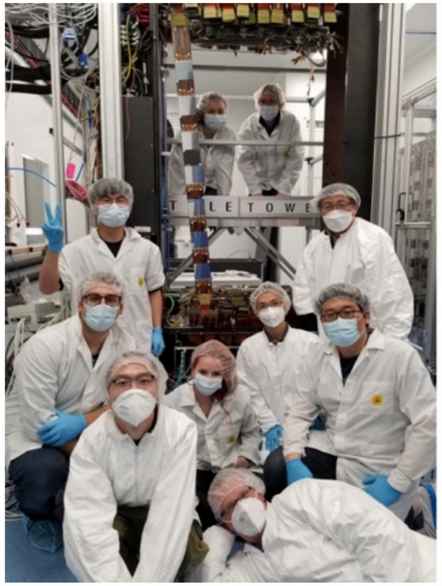

**LHCb Tracking System**



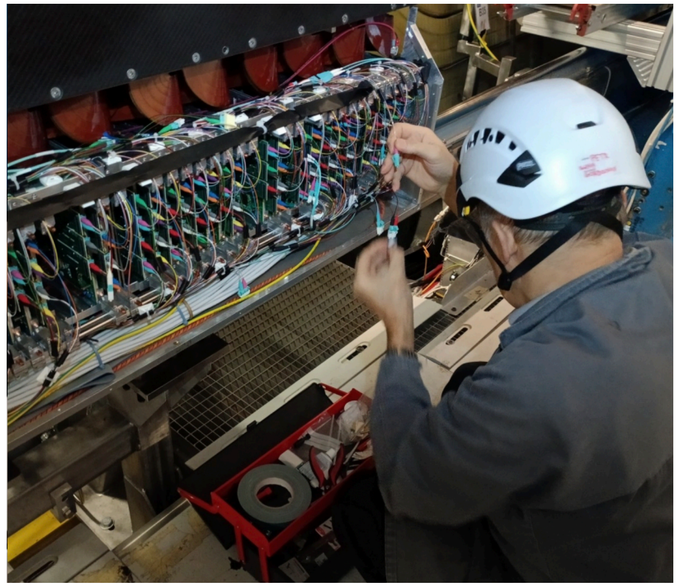



# UT Timeline

- **July 2021 - 3/2023: UT Installation**
- April 2023 - : Firmware and software development
- Nov. 2023 - Jan. 2024: Hardware issues fixing during the YETS23 (The year-end technical stop )
- **Feb. 2024 - May 2024: Commissioning with/without beam to get the suitable configuration**
- **June 2024 - : Stable data taking in global with both proton and heavy ion collisions**

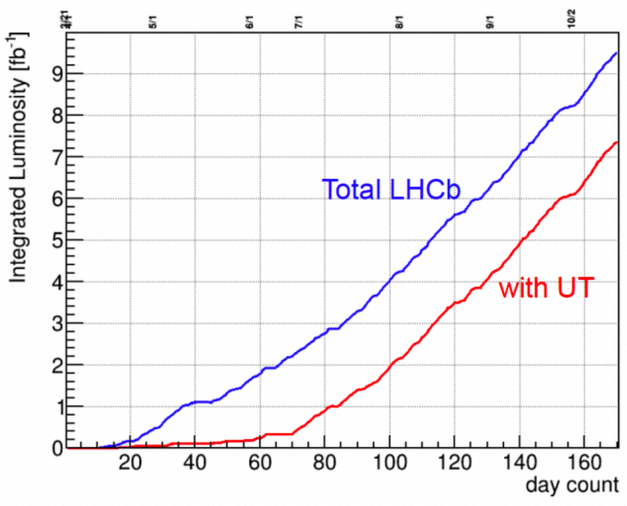


**UT Installation**



**Fixing PEPI during YETS23**

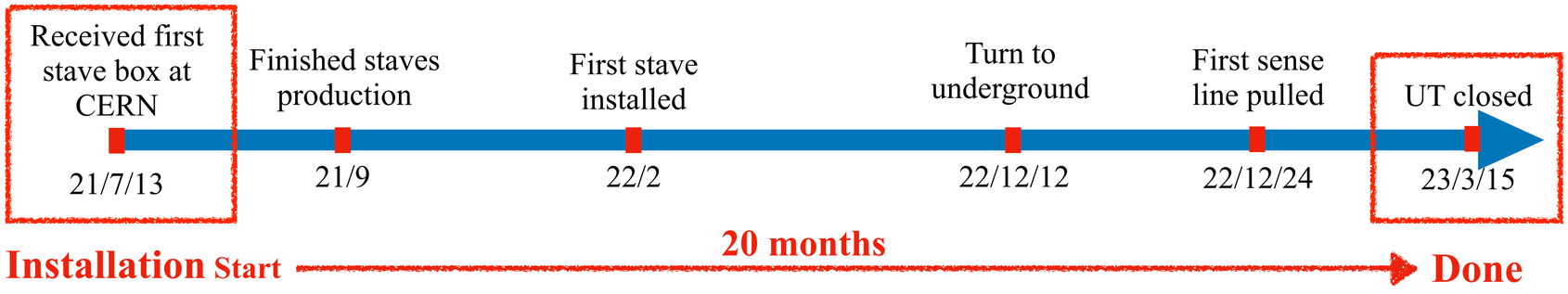
**UT Group in LHCb control room**



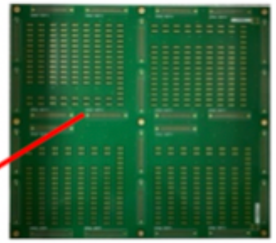

**Taking data in global**

# UT Installation

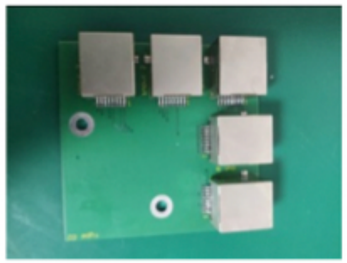
Details for UT Installation can be found in Shuqi Sheng and Xiaojie Jiang's talks



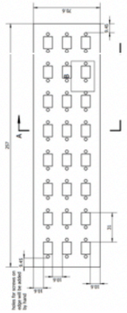

- Chinese groups have significant contributions in design and installation
  - HV patch panel, LV splitter, PEPI (Peripheral Electronics Processing Interface) patch panel, HV cable designed and produced by HNU & IHEP
  - IHEP/HNU/CCNU/LZU/THU/SCNU all participated in installation during COVID19



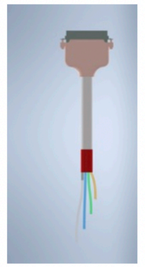
HV patch panel



LV spliter in SBC region



PEPI patch panel

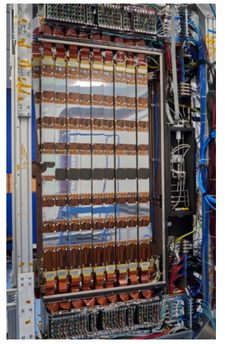


HV cable

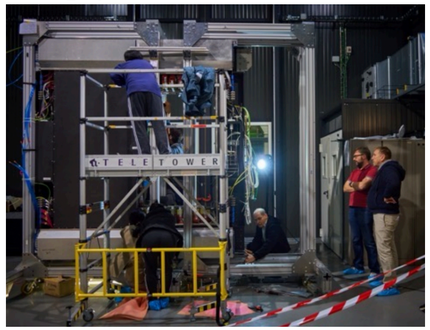
**Installation**

Empty Box

Installed a stave



Finish one side




A+C side mate

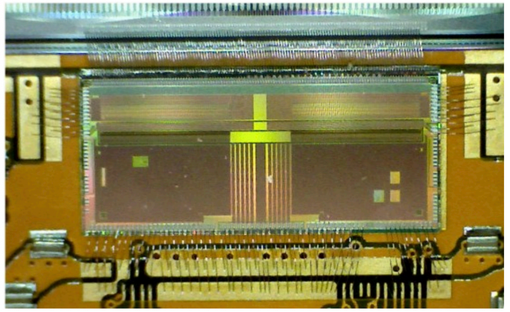
Transport to underground

UT Closed

# UT Commissioning: Optimizing with/without Beam

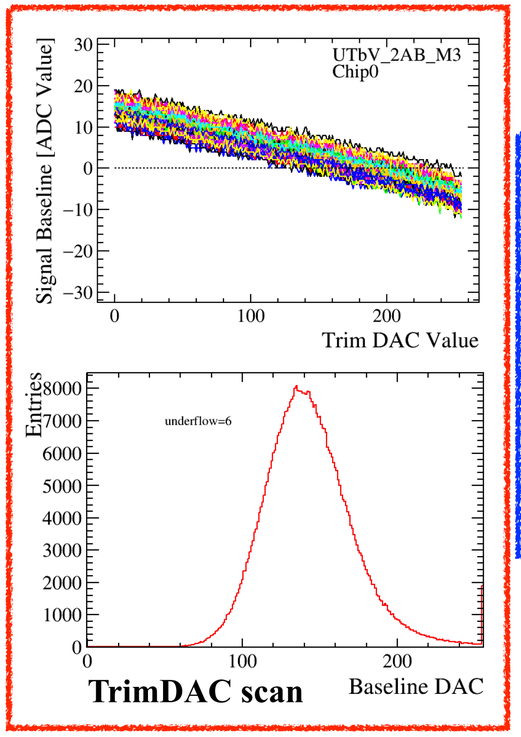
## UT front-end readout, SALT chip

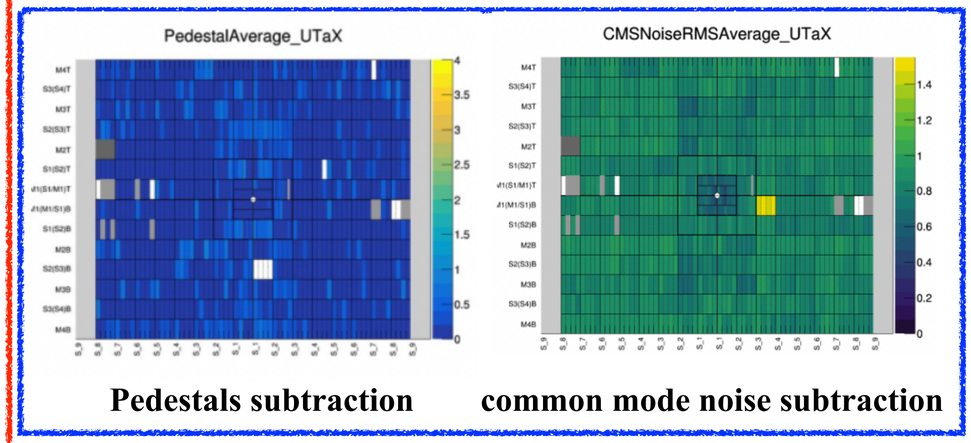
- Digital signal processing providing pedestal & common mode noise subtraction, zero-suppression

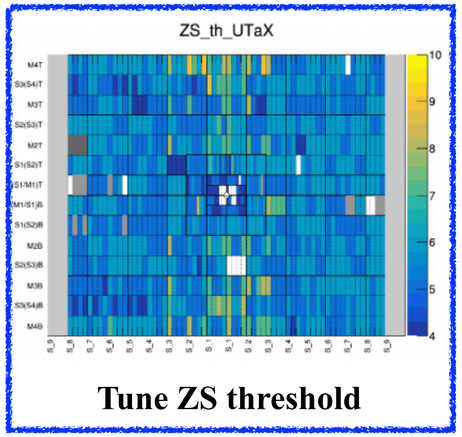


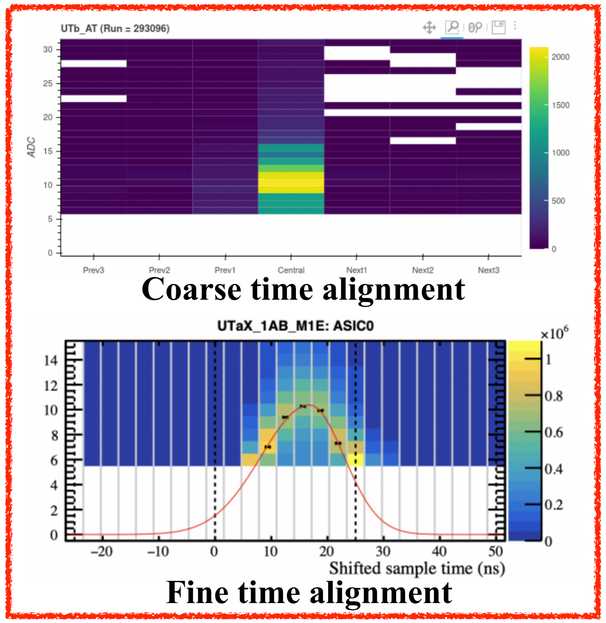
## Tune SALT chip

- DLL/PLL, serializer delay, ADC, deserializer, TrimDAC, Pedestals, ZS threshold, MCM thresholds, Pulse-shape, Gain



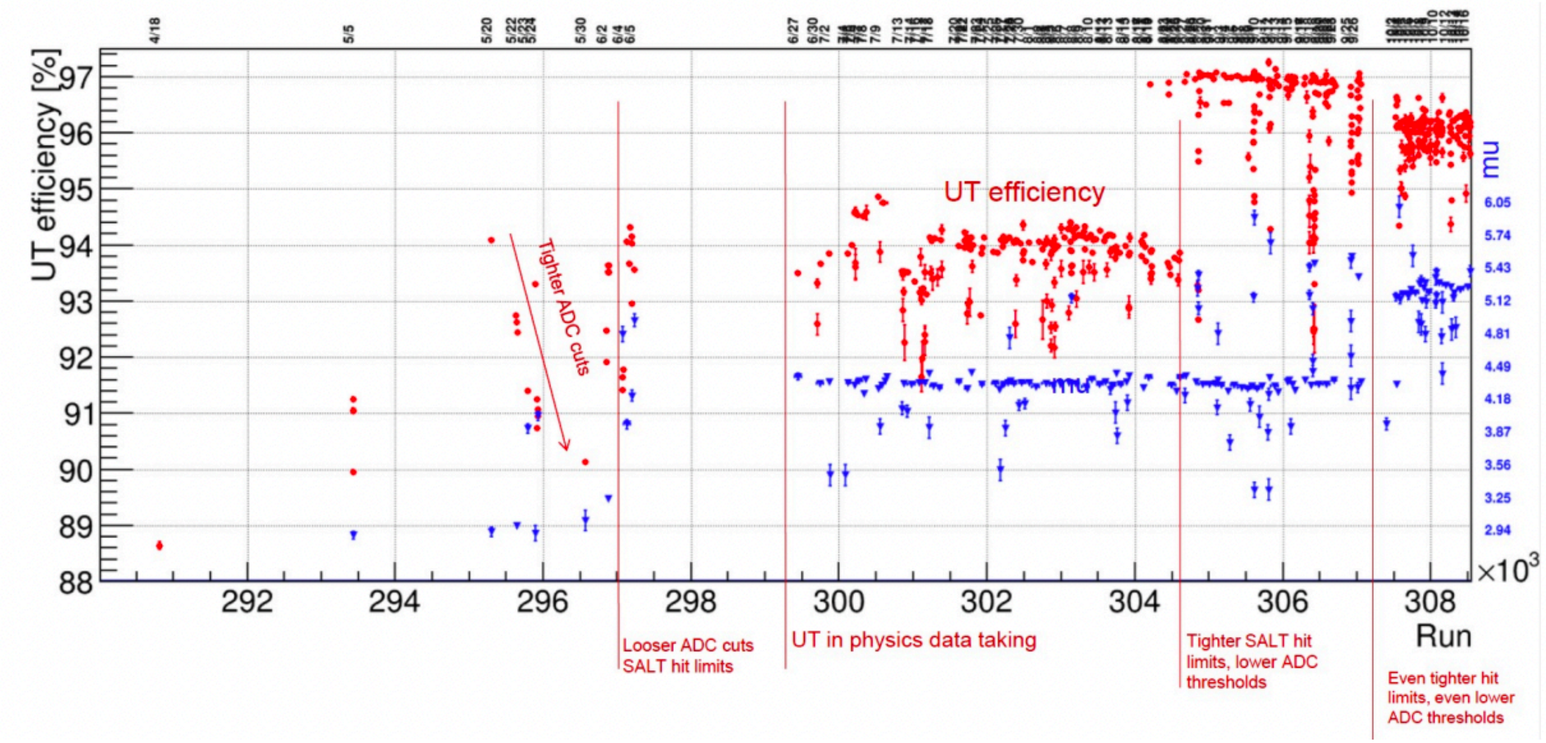



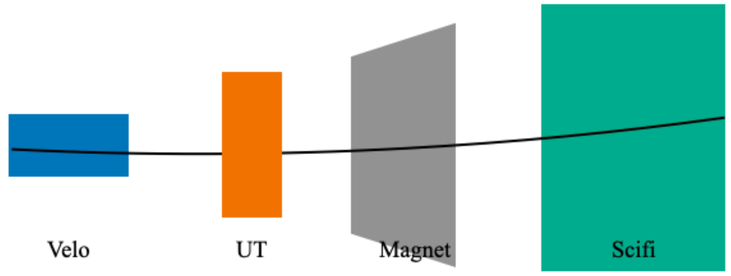



# UT in Global Data Taking

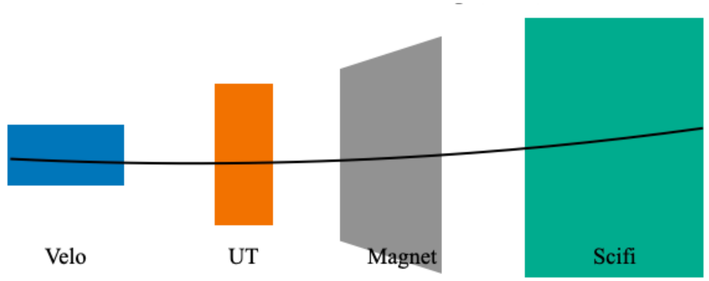
- Start taking data in global since May 2024
- Improve firmware and tune SALT parameters for better UT efficiency




**UT efficiency on long tracks (3-4 UT layer match)**



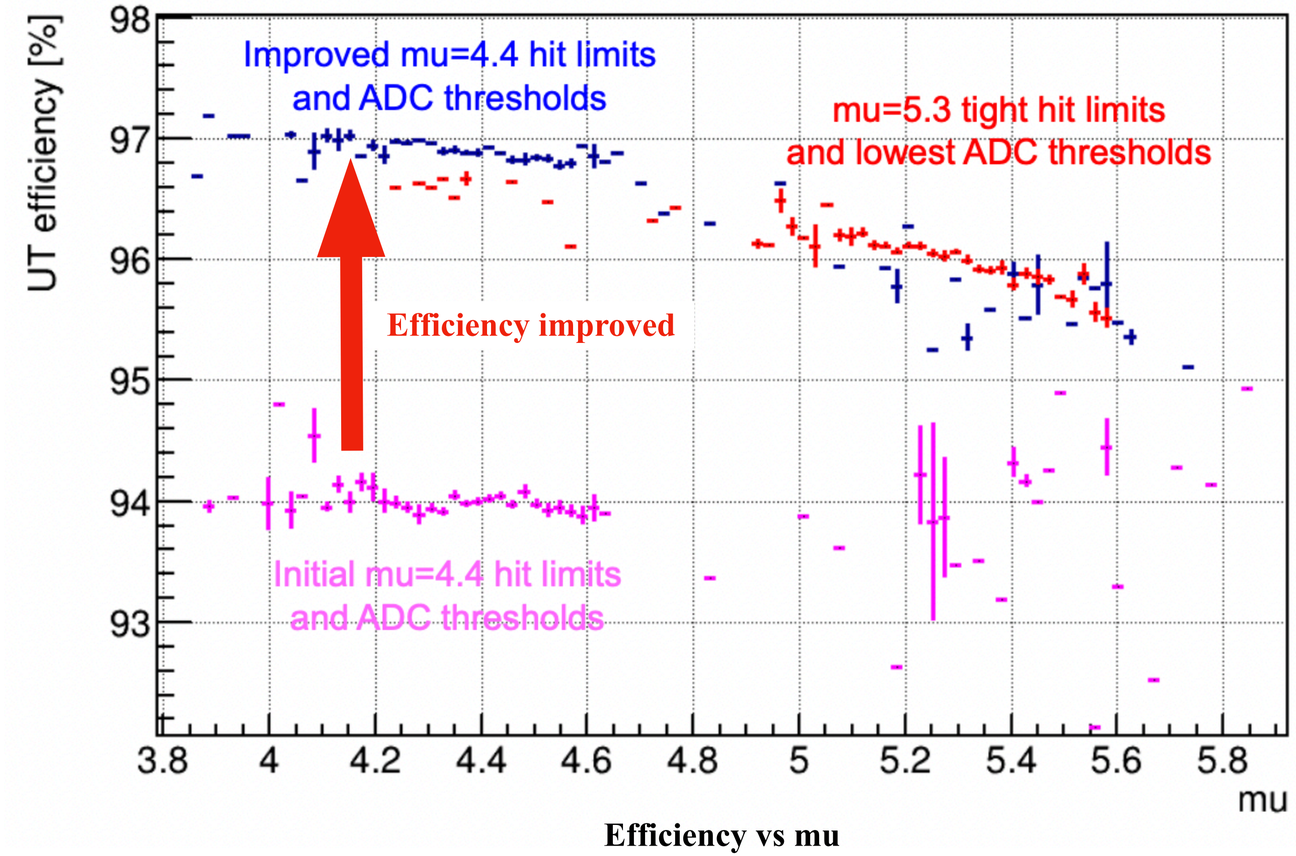

Velo-SciFi matched long track without UT




Add UT Hits into matched long track

# UT in Global Data Taking

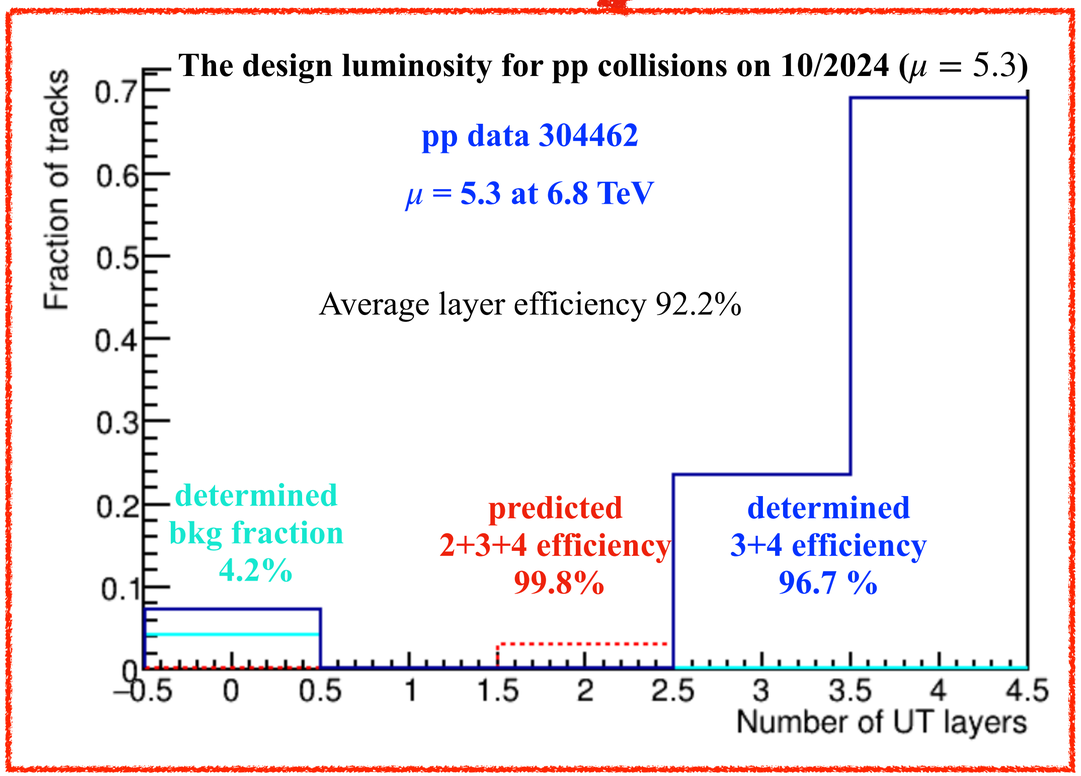
- Adjust hit limits and ADC threshold to reach better performance in different collision rates ($\mu$)
  - Hit limits: max number of hits from SALT to Tell40
  - Tell40 systems experience efficiency loss at high hit rates due to FPGA/firmware
  - Tight hit limits in SALT to improve Tell40's efficiency

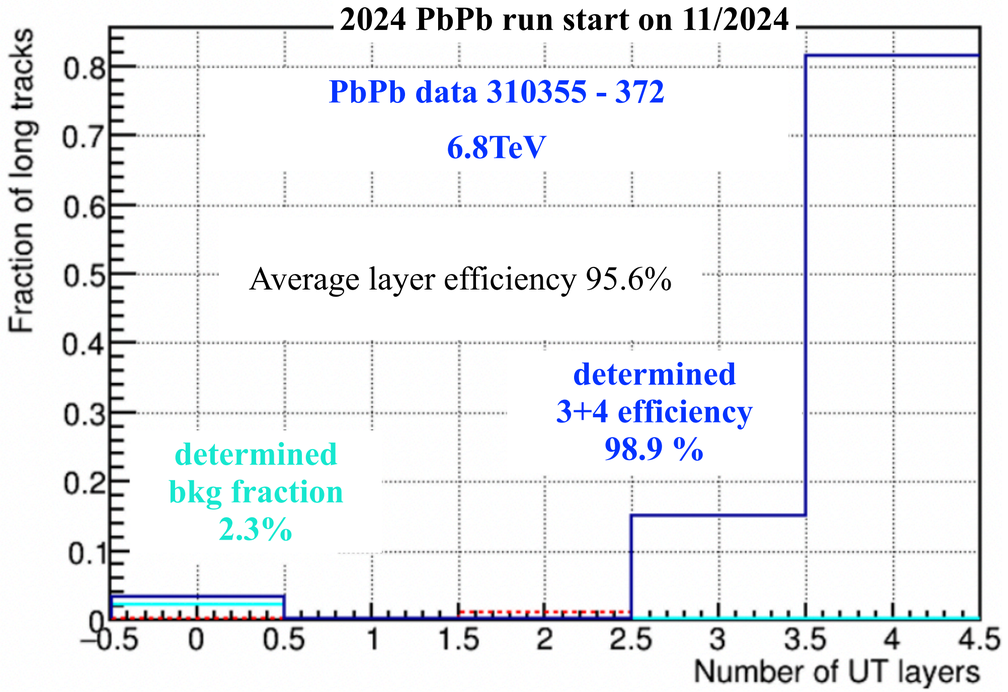



**Efficiency vs mu**

# UT Tracking Efficiency

Achieved stable and efficient operation for pp/PbPb at designed condition ($\mu = 5.3$ for pp)



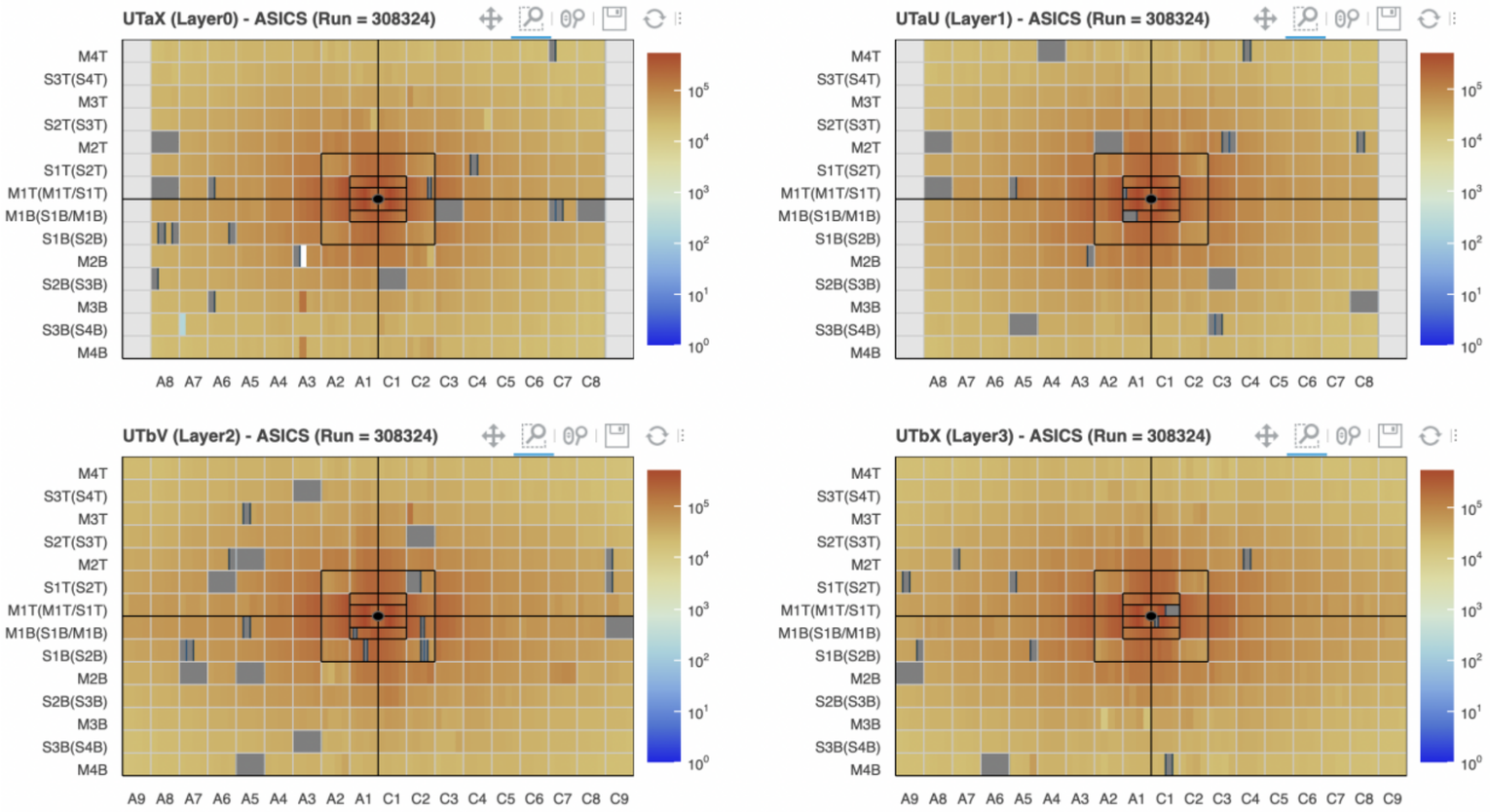

**Number of UT layers matched to a long track and the relative tracking efficiency**

# UT Online Monitor: Monet

Real time plots during data taking

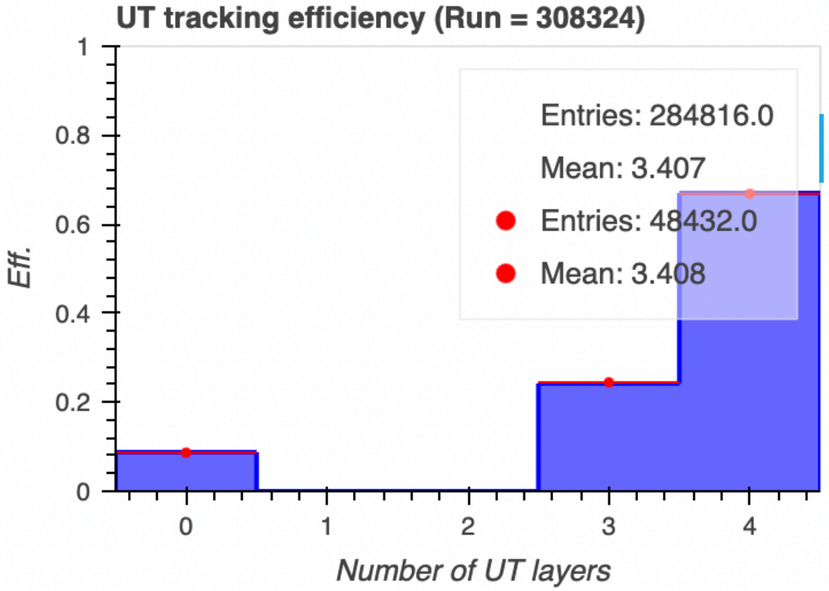
- **Most of the ASICs work properly (96.7%)**
- **The hit distribution is consistent with expectations**

**Run 308324 $\mu$ = 5.25 at 6.8 TeV**




**Number of hits in each UT chip**

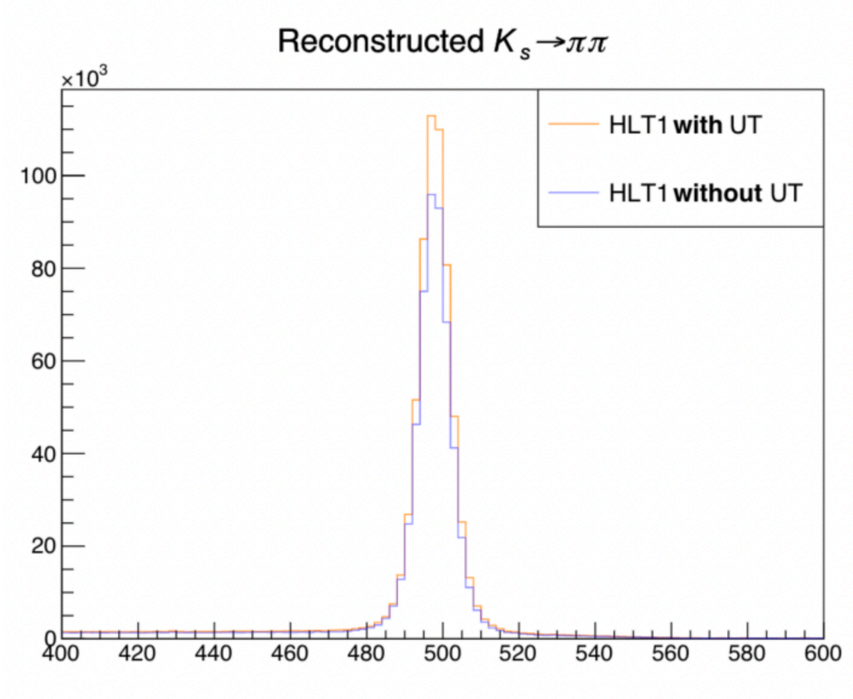
White gray: not occupied slot
Gray and dark gray: disabled



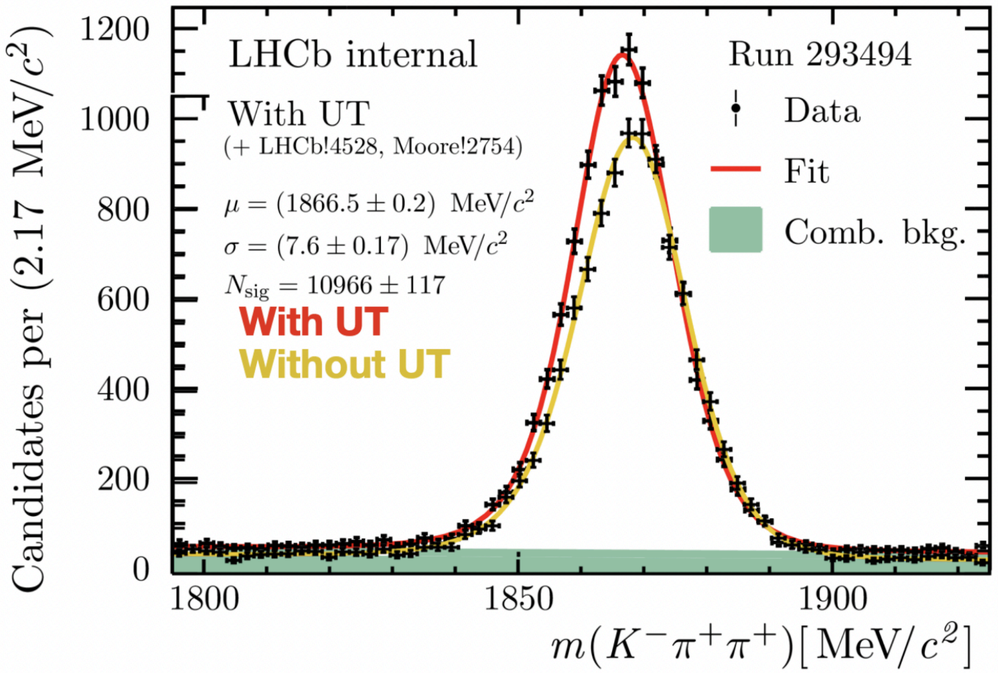

**UT tracking efficiency**

# Tracking Improvement with UT

- Increase reconstruction efficiency for $\Lambda_0$ $K_S^0$ — UT allows downstream track (UT+SciFi)
- Improvement in mass resolutions




**Add downstream tracks (UT+SciFi) in HLT1**




- **~ 10% improvement in $D^+$ yields**
- **~ 12% improvement in mass resolution**

# Summary

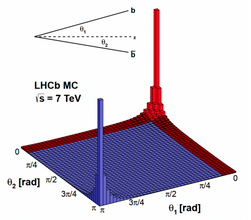
- Chinese groups have significant contributions in design, installation, and system commissioning
- Found a properly configuration for the design luminosity ($\mu = 5.3$)
- Achieved stable and efficient operation for pp/PbPb collision
- The tracking performance improved with UT

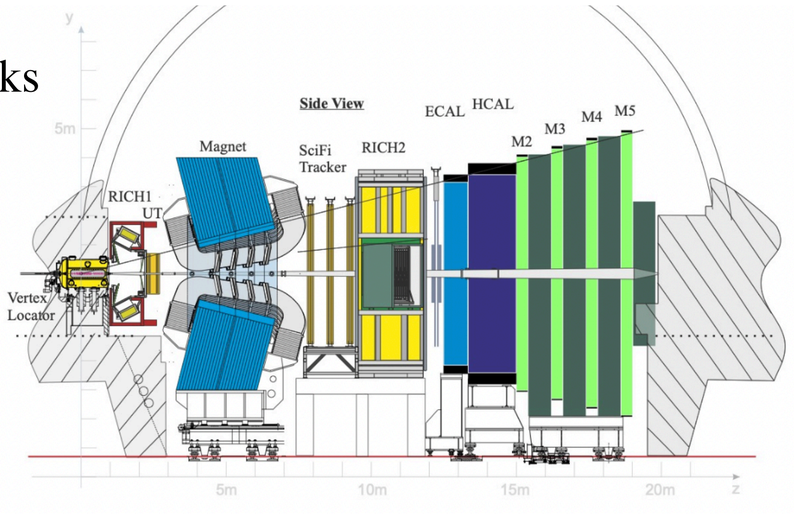
Thank you!

# Backup

# LHCb Detector

- Single arm forward spectrometer ( 2<η<5 )
  - Designed to study CP violation and rare decays in hadrons containing b- and c-quarks

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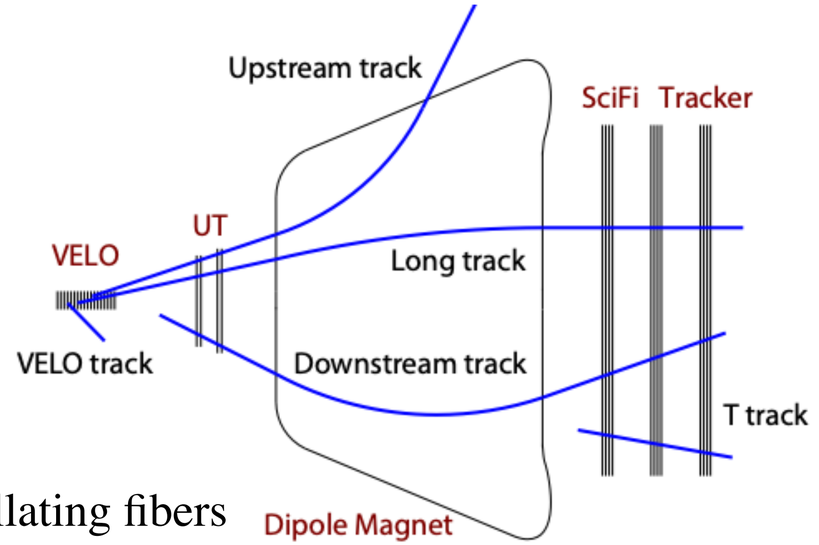
    - Software-only trigger to 40 MHz readout
    - Sub-detector upgrade

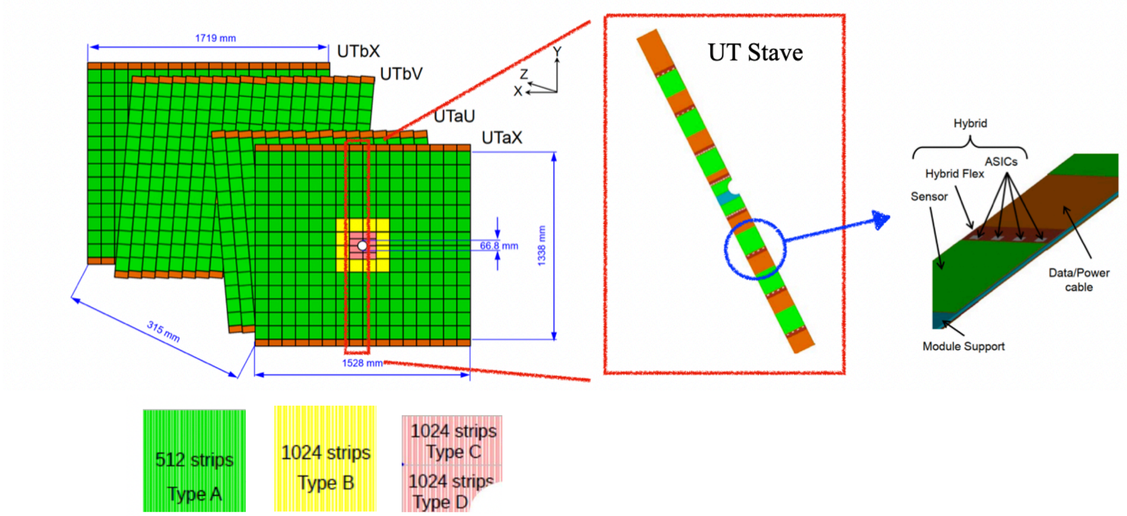



- LHCb Tracking System (all sub-detector upgraded after LS2)
  - Vertex Locator (Velo): Silicon strips → Silicon pixel
  - Upstream Tracker (UT): Silicon strips (Tracker Turicensis, TT) → Silicon strips
  - Scintillating Fiber Tracker (SciFi): Silicon strips + straw tubes (IT + OT) → Scintillating fibers

# UT Detector

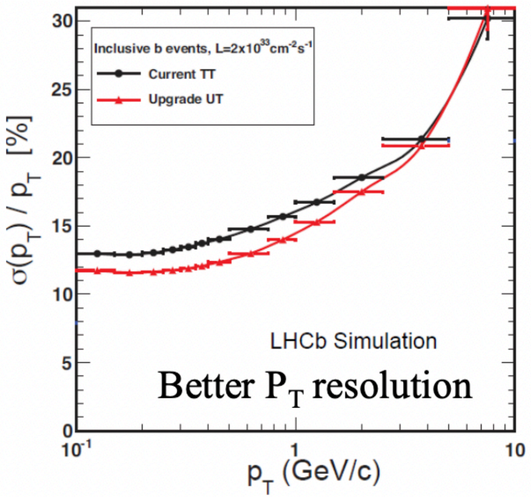
## The Upstream Tracker (UT)

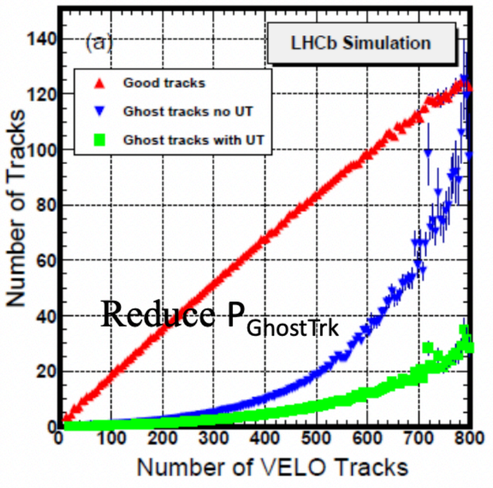
- Replace TT, located upstream of the LHCb bending magnet
- Silicon strip detector with four layers
  - 4 UT layers (aX, aU, bV, bX) at (0°,+5° ,-5°, 0°)
  - (16, 16, 18, 18) staves on UT layers (aX, aU, bV, bX)
  - 4 types of modules with different silicon strip densities
  - 4192 ASICs of 128 channels each, with a total of 536,576 strips
- Full angular coverage
- Higher segmentation sensors in the region surrounding the beam pipes
- 40MHz readout with SALT (Silicon ASIC for LHCb Tracker) chip




## An important component of LHCb track system

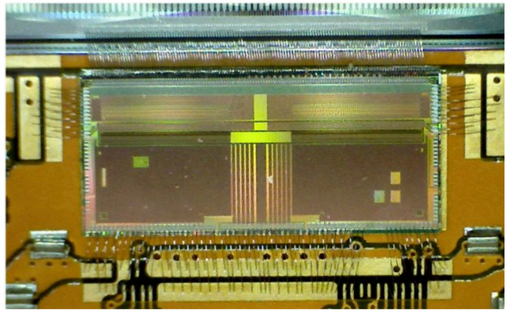
- Provide fast estimates of momentum in the software trigger
- Improve momentum resolution
- Reduce ghost rate in long tracks
- Increase reconstruction efficiency of long lived particles

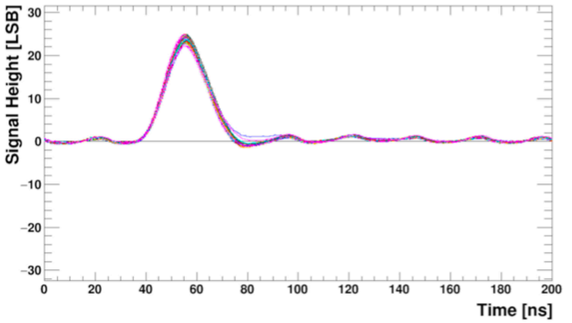


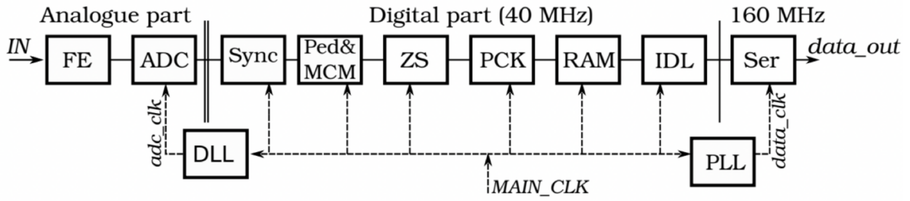
# SALT chip and UT commissioning

## UT front-end readout, SALT






- 128 Channels with 6-bit ADC, 40MHz readout
- CMOS 130nm technology
- Fast shaping time: Tpeak < 25ns
- Digital signal processing providing pedestal & common mode noise subtraction, zero-suppression

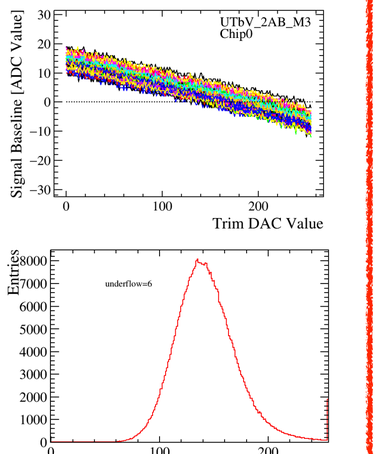


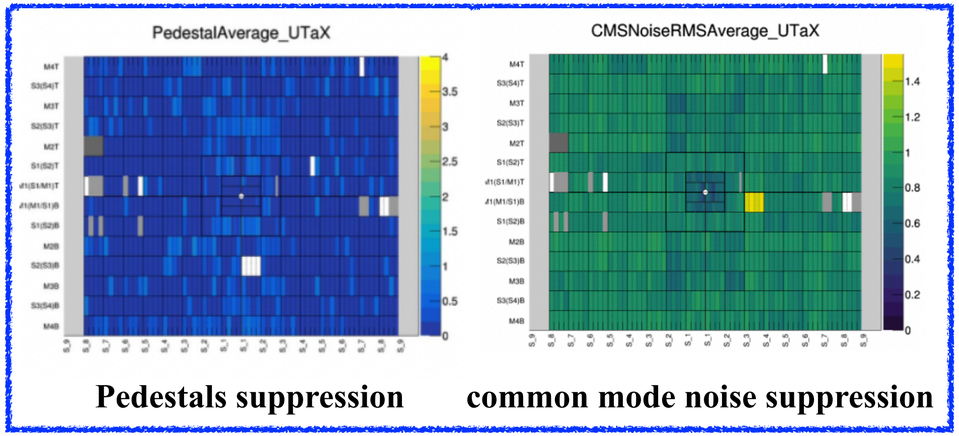

## UT Commissioning with/without beam to get the suitable FE parameter

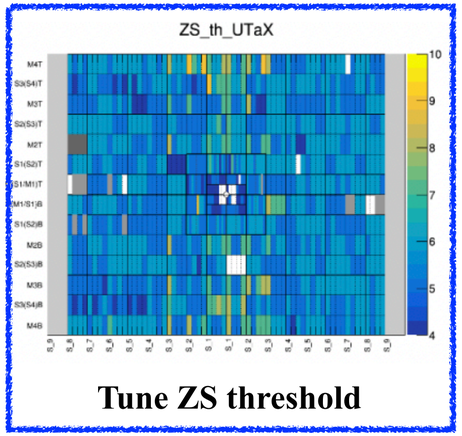
Tune DLL/PLL, Scan serializer delay, Tune e-link phase on GBTx, Tune ADC,

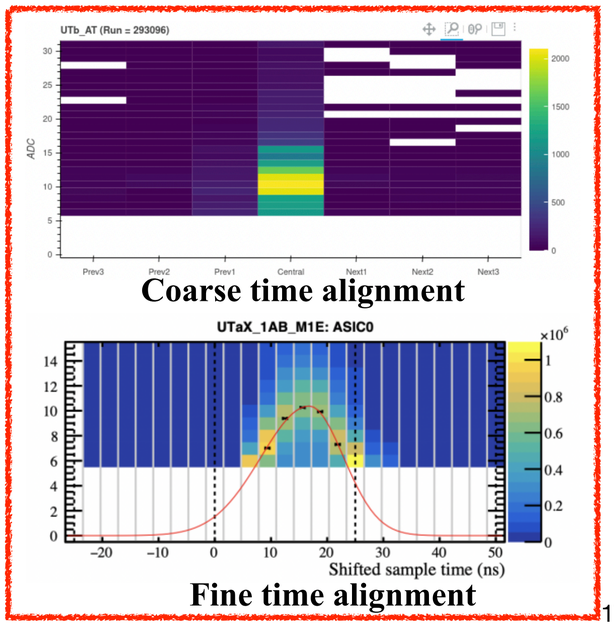
Tune deserializer, TrimDAC scan, Pedestals, Tune ZS threshold, Tune MCM thresholds,

Pulse-shape scan, Gain scan, Run DAQ with random triggers @ 30MHz



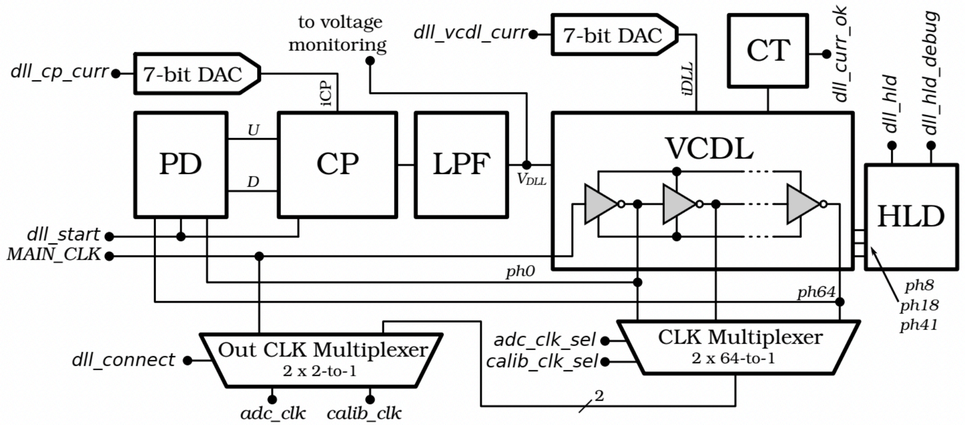



# Tune DLL

Details for Tune DLL/PLL can be found in Mark Tobin's talk

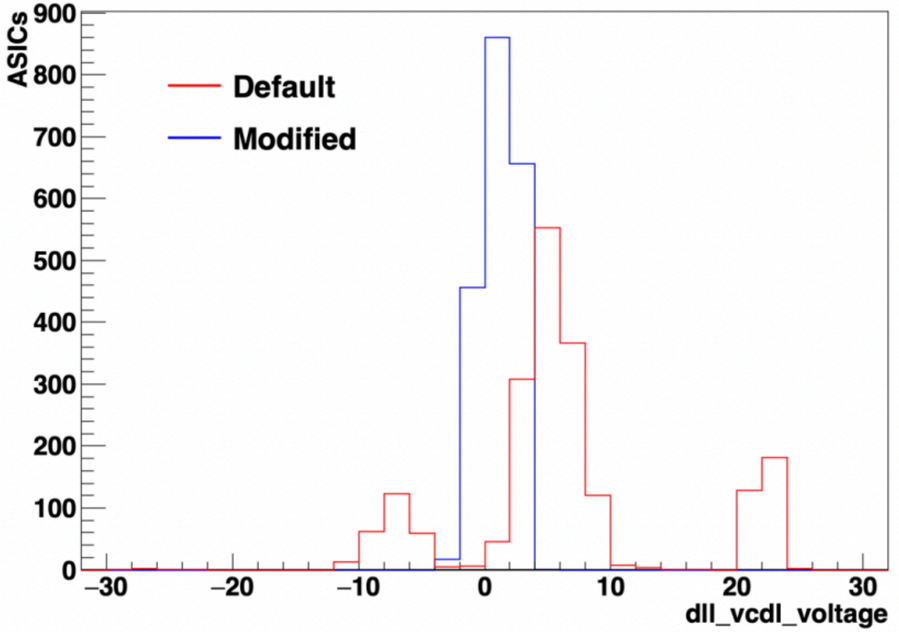
## DLL in SALT

- Input frequency 40 MHz
- Provide 64 independent clock phases selection




## Tune DLL

- The dll_vcdl_voltage means the difference between $V_{DLL}$ and $V_{vdd/2}$
  - **Best setting when dll_vcdl_voltage around 0**
- The dll_vcdl_cfg register sets the Voltage Controlled Delay Line (VCDL) bias current
- Adjust dll_vcdl_cfg since the default settings are not optimal

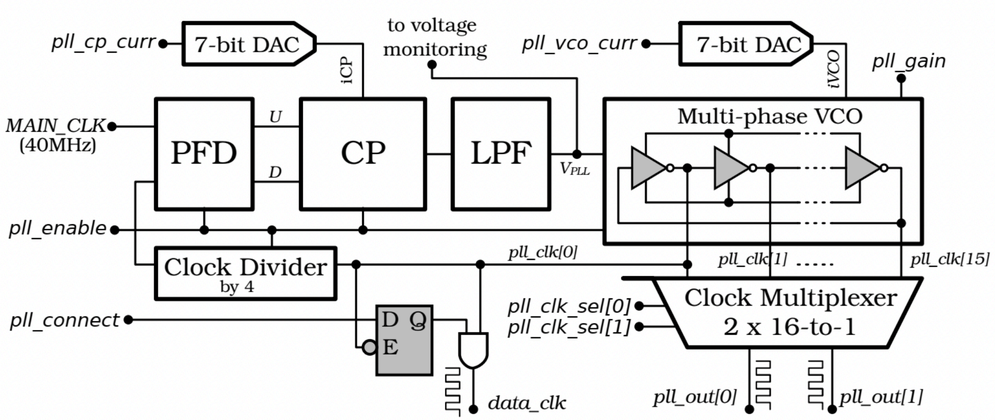


# Tune PLL

Details for Tune DLL/PLL can be found in Mark Tobin's talk

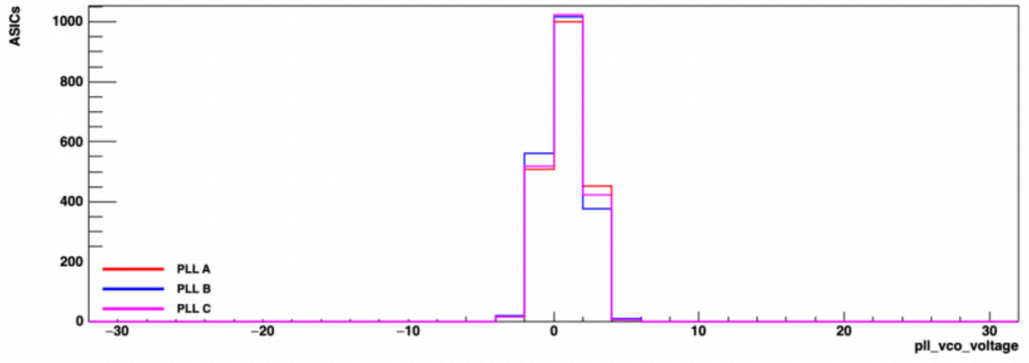
## PLL in SALT

- Input frequency 40 MHz
- Generates a stable high-frequency (160 MHz) clock signal for the Double Data Rate (DDR) serializer
- Triple Modular redundancy (TMR) design enhances reliability against Single Event Upsets (SEUs) — **Three PLLs in the SALT**




## Tune PLL

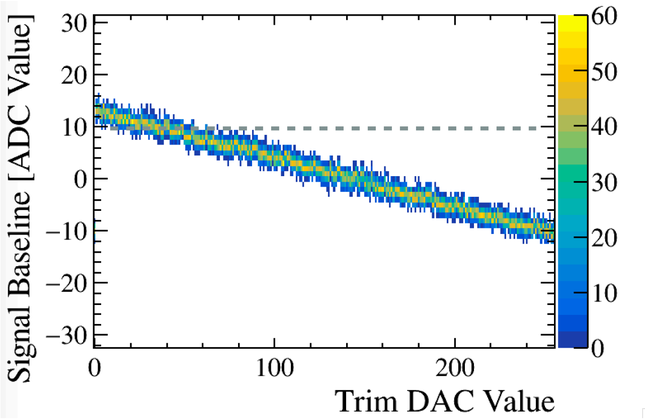
- Check the Voltage Controlled Oscillator (VCO) for all three PLLs
- The pll_vco_voltage means the difference between $V_{PLL}$ and $V_{vdd/2}$
  - **Best setting when pll_vco_voltage in all three PLLs are around 0**
- The pll_vco_cfg register allows to change the VCO bias current which is directly related to the output frequency



# TrimDAC scan

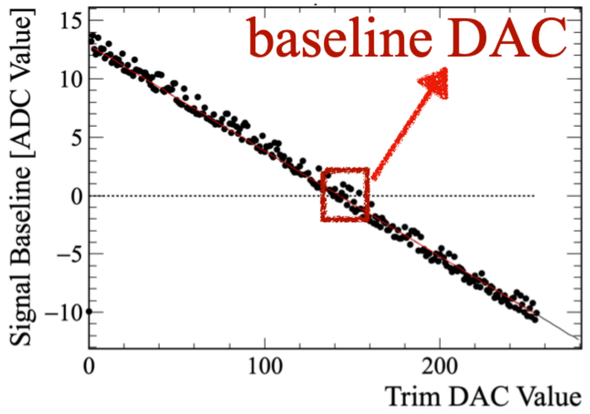
**Each ASIC channel contains an 8-bit trimming DAC for a precise baseline setting**

- Scan the TrimDAC from 0-255 with step of 1. Each step took 100 events
  - the ADC value = 0 → Baseline DAC

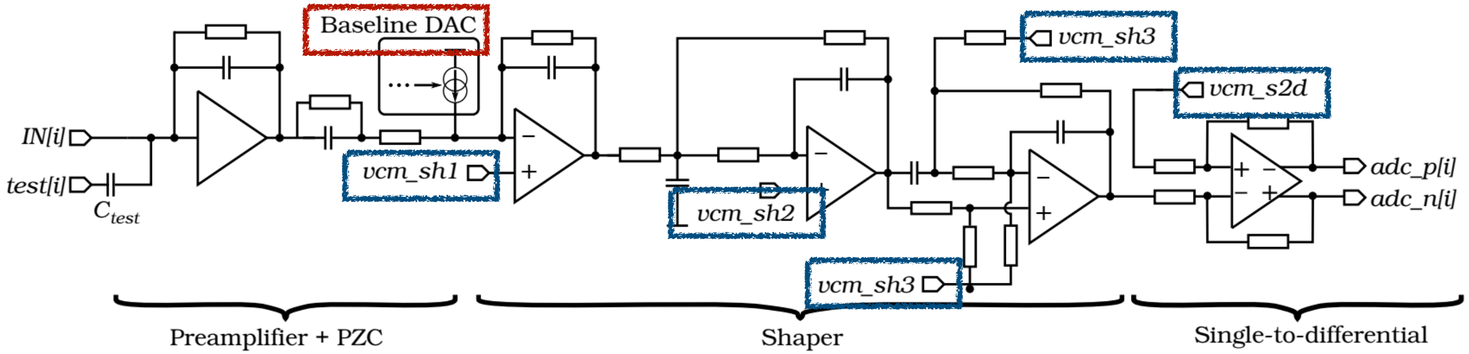



**Each ASIC contains 6-bit DAC setting the $I_{vcm}$ for generation of common voltages**

- The single common mode voltage setting couldn't cover all cases, TrimDAC scans at 4 different common mode voltages allow almost all channels to be compensated



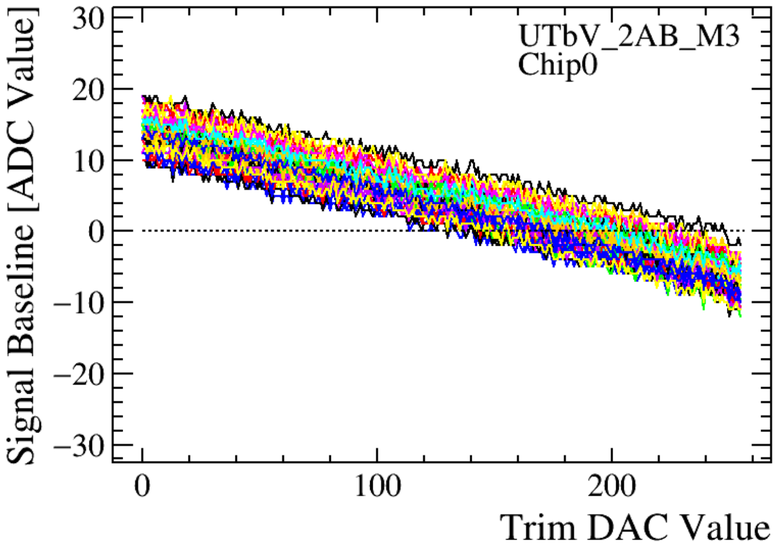

**8-bit trimming DAC**



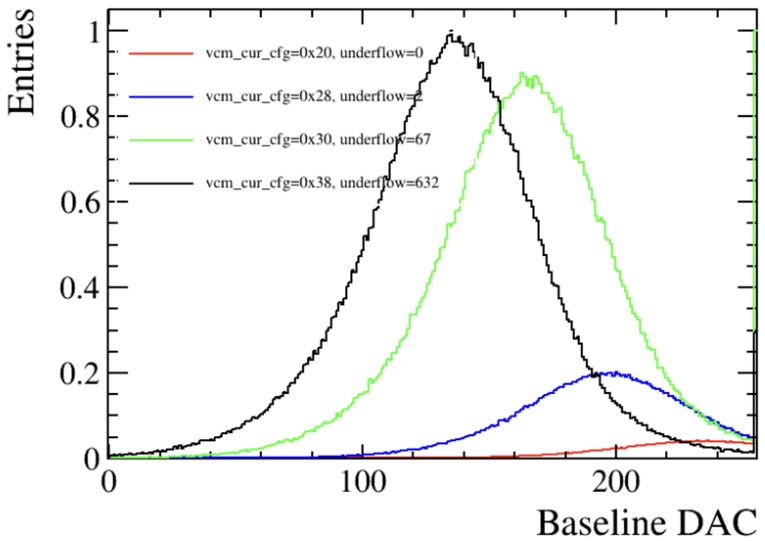

**6-bit DAC setting the reference current $I_{vcm}$**

# TrimDAC scan

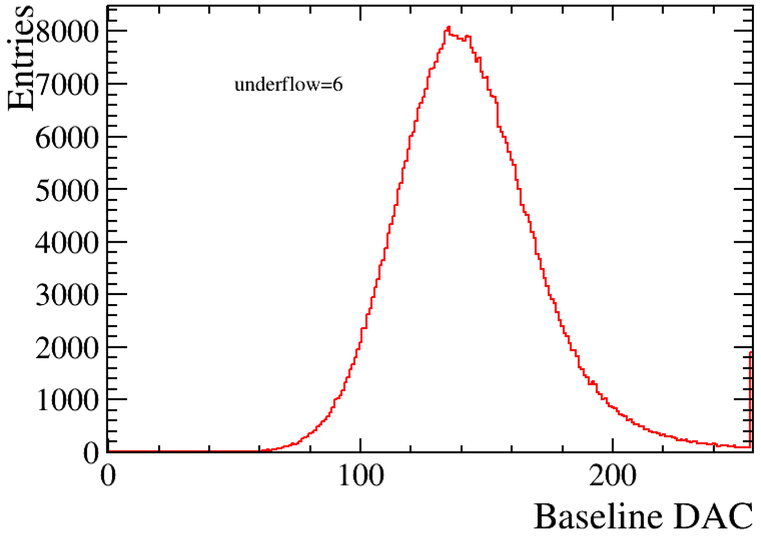
TrimDAC scan for UTbV_2AB_M3 chip0




TrimDAC scan with 4 common mode voltage settings




Final resulte



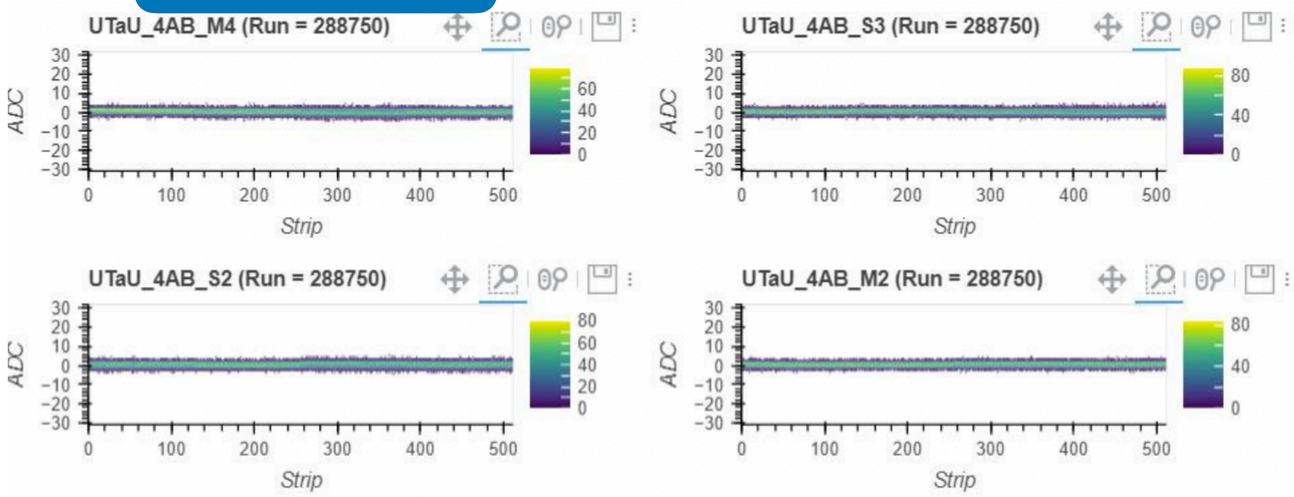

99.97% channels work properly at the TrimDAC scan stage!

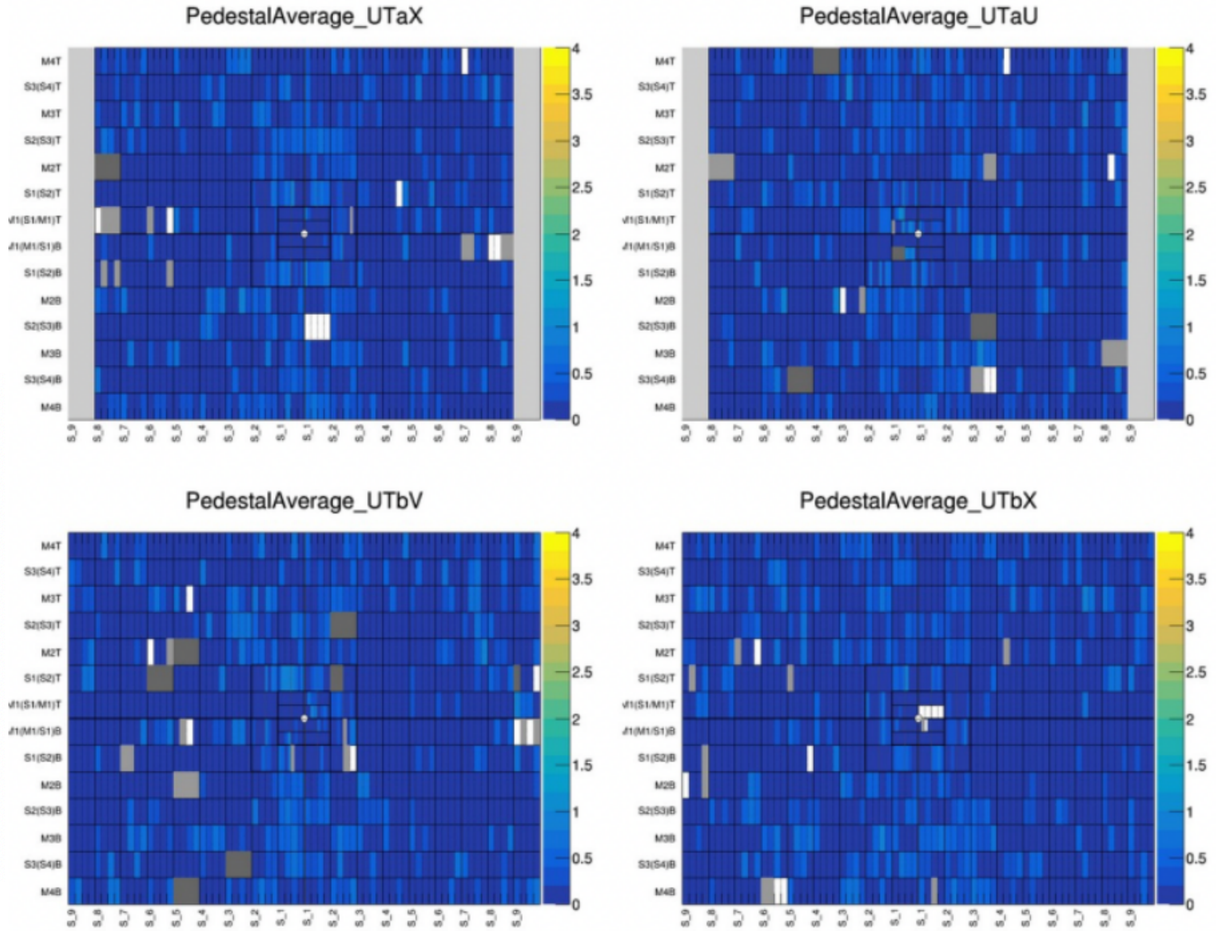
# Pedestals subtraction

Details for Pedestals subtraction can be found in Wojciech Krupa's talk

- Performed after TrimDAC scans
- After TrimDAC calibration the pedestal values close to 0
- Subtraction in each channel

Raw ADC per channel

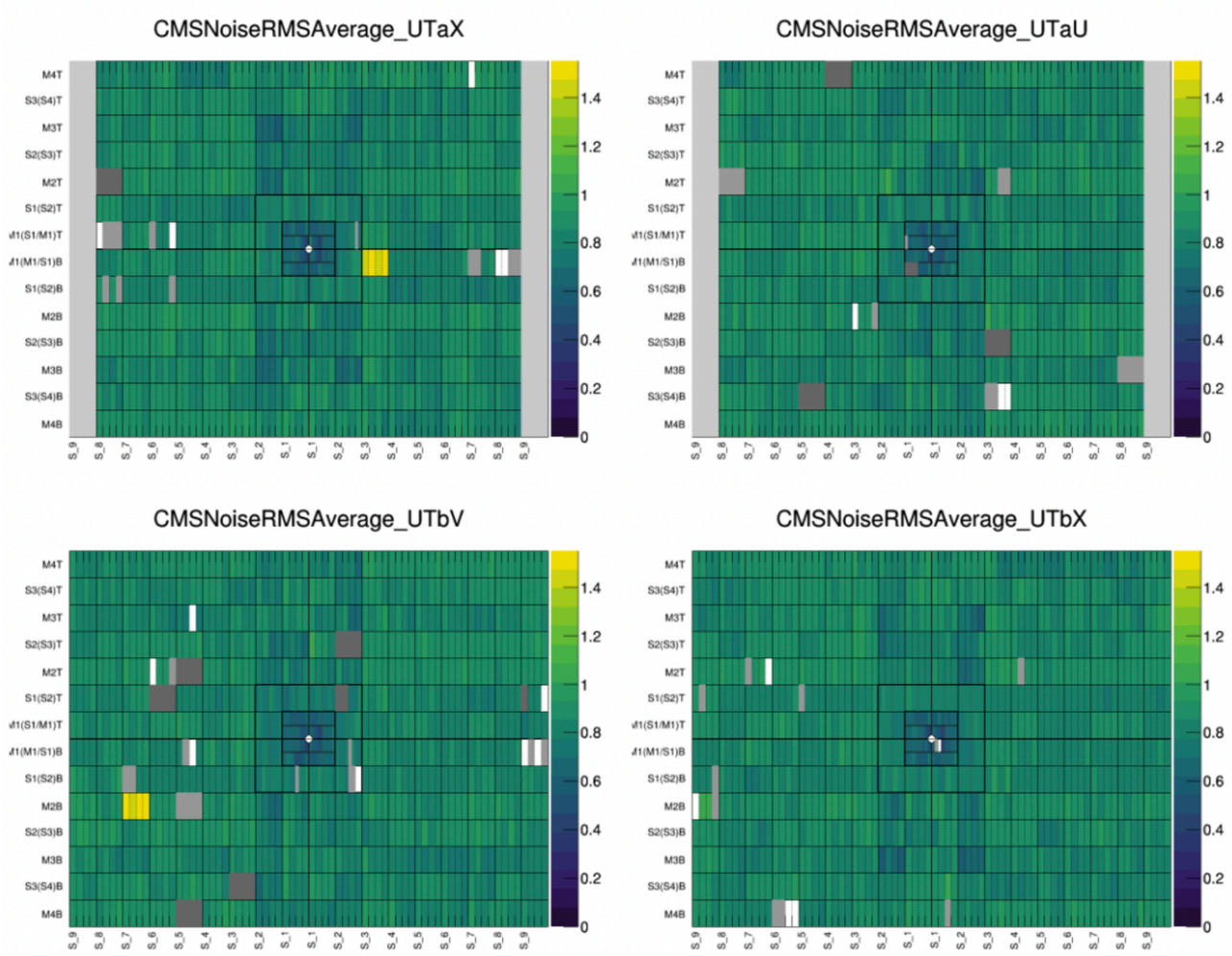


# MCM thresholds subtraction

Details for Tune MCMS can be found in Wojciech Krupa's talk

- Calculate an average value of all channels without a hit and subtract this value from all channels
- MCMS run (after pedestal subtraction and MCMS in the chip)
- Very uniform distribution of CMS noise

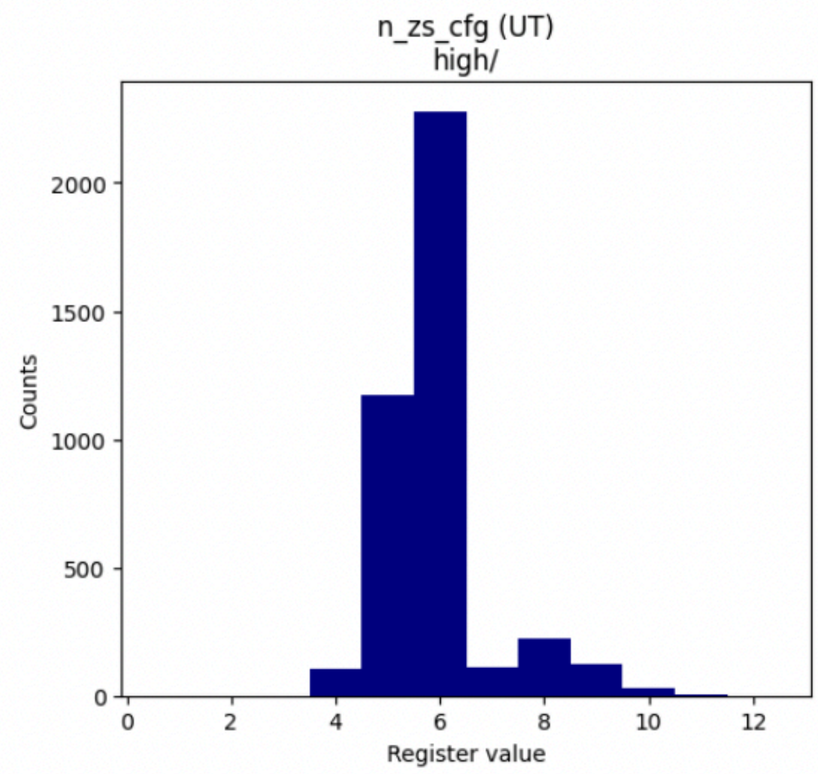


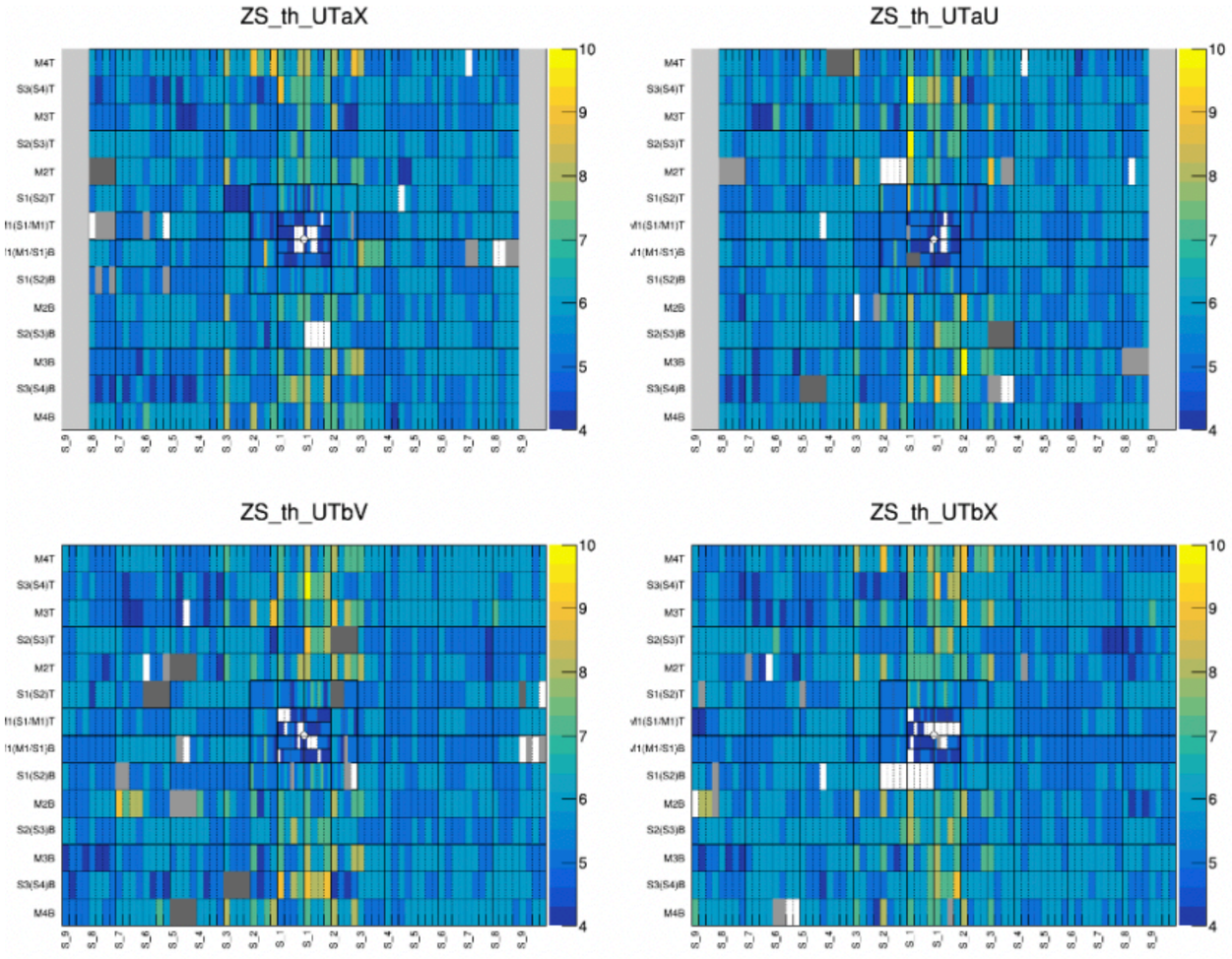
# Tune ZS threshold

Details for Tune ZS threshold can be found in Wojciech Krupa's talk

Calculation of ZS thresholds based on CMS-noise

$$z_{s_{th}} = \begin{cases} 5 \cdot \sigma_{ADC}(\text{mcms}) \\ 5 \cdot \sigma_{ADC}(\text{mcms}) + \max(\mu_{ADC}(\text{mcms})) \end{cases} \quad \text{if } \max(\mu_{ADC}(\text{mcms})) = 0{,}1$$



# Pulse scan

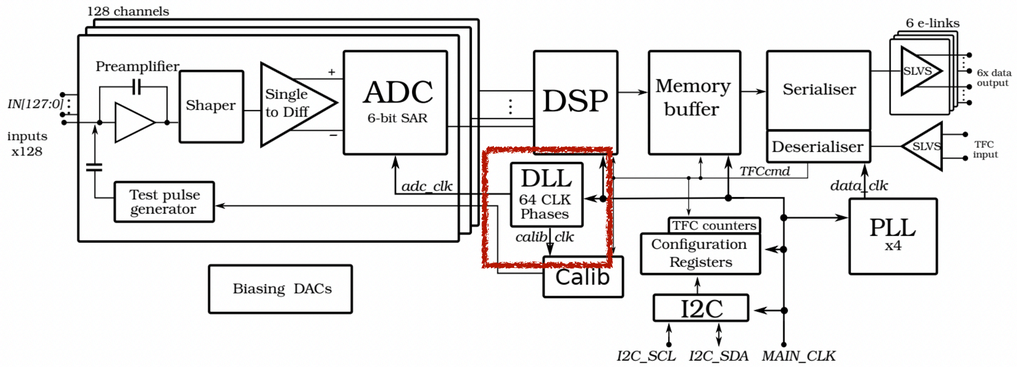
**Using test pulse to check the whole processing chain in the SALT chip**

SALT contains a dedicated internal DLL block to provide 64 independent clock phases selection

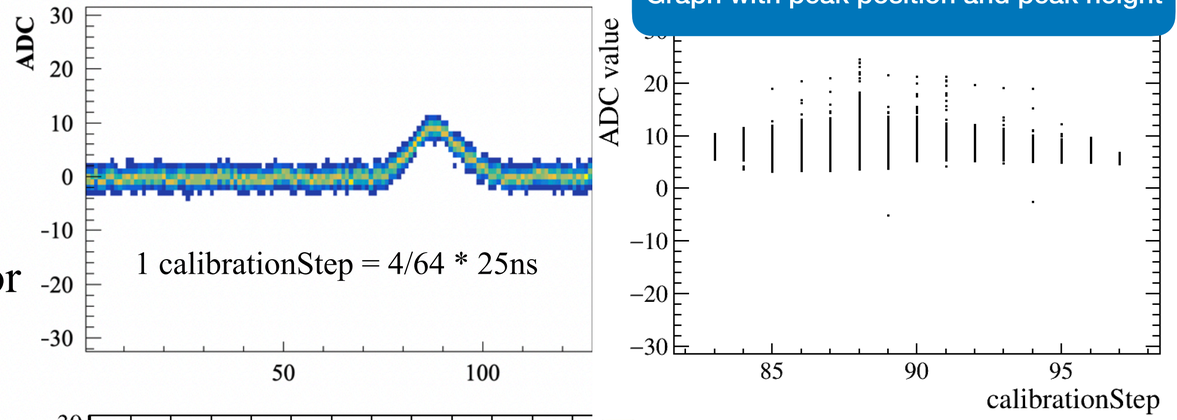
- We generate test pulse and take data with different clock phase (**adc_clk_sel**)

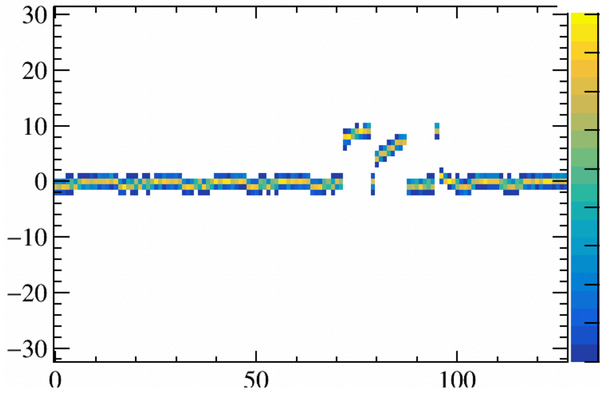
**Most of ASICs have the correct pulse shape**

- 32 (4192 in total) ASICs need to recorrect adc_sync_sel bit setting for different DLL delays




Graph with peak position and peak height



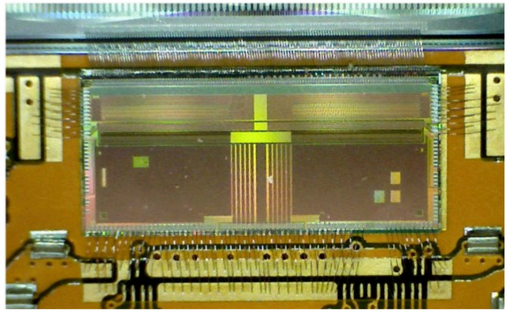



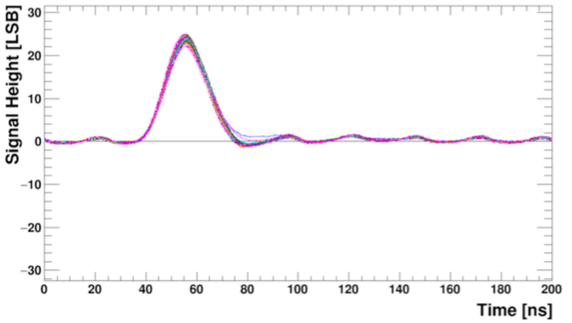
| *adc_clk_sel* | *adc_sync_sel* | time shift [ns] |
|---|---|---|
| 0 – 7 | 1 (falling edge) | $adc\_clk\_sel \cdot \frac{25}{64} + 25$ |
| 8 – 39 | 0 (rising edge) | $adc\_clk\_sel \cdot \frac{25}{64}$ |
| 40 – 63 | 1 (falling edge) | $adc\_clk\_sel \cdot \frac{25}{64}$ |

Default setting

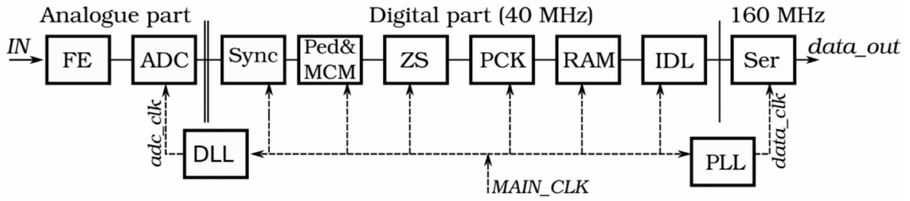
# SALT chip and UT commissioning

## UT front-end readout, SALT






- 128 Channels with 6-bit ADC, 40MHz readout
- CMOS 130nm technology
- Fast shaping time: Tpeak < 25ns
- Digital signal processing providing pedestal & common mode noise subtraction, zero-suppression

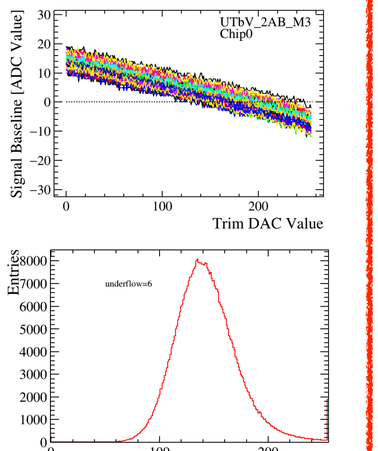



## UT Commissioning with/without beam to get the suitable FE parameter

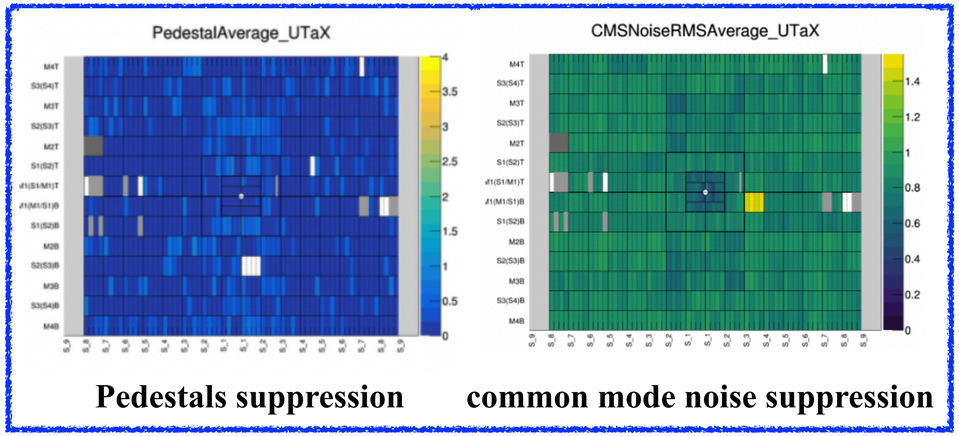
Tune DLL/PLL, Scan serializer delay, Tune e-link phase on GBTx, Tune ADC,

Tune deserializer, TrimDAC scan, Pedestals, Tune ZS threshold, Tune MCM thresholds,

Pulse-shape scan, Gain scan, Run DAQ with random triggers @ 30MHz

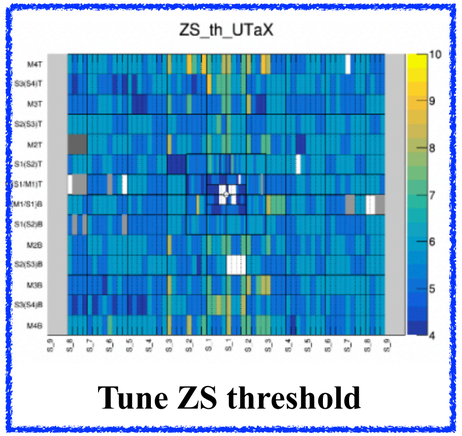



**TrimDAC scan** Baseline DAC



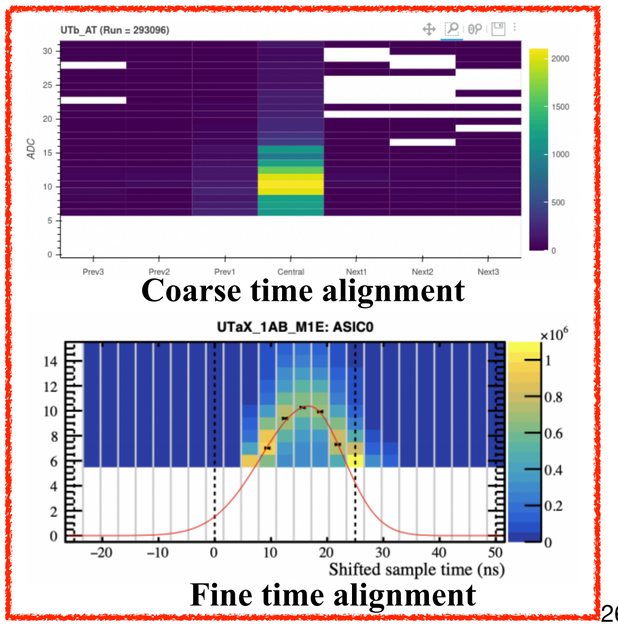

**Pedestals suppression** **common mode noise suppression**

**Subtraction in each channel**




**Tune ZS threshold**

**Tune in each ASICs**




**Coarse time alignment**

**Fine time alignment**

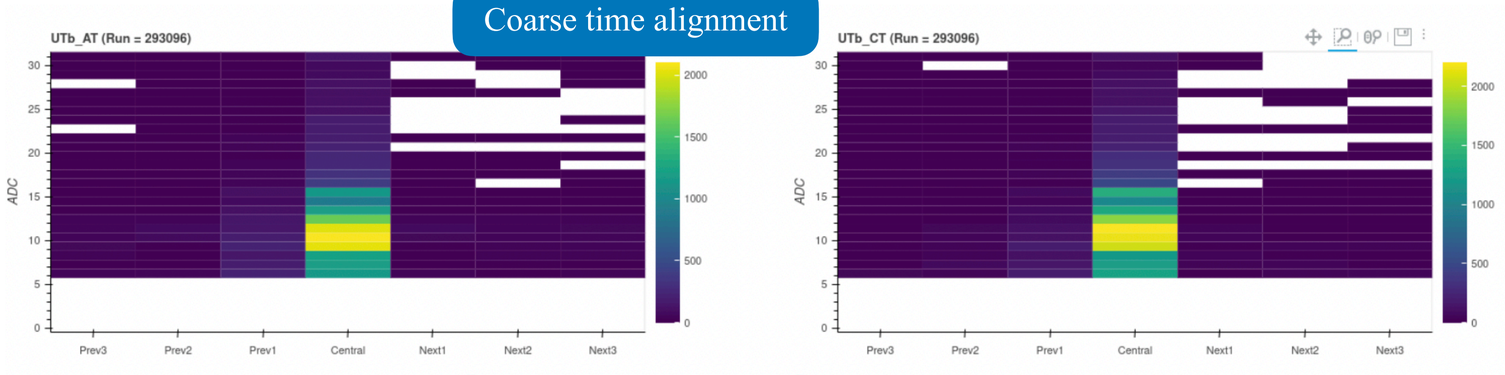
# Time alignment

Details for UT fine time alignment can be found in Christos Hadjivasiliou's talk

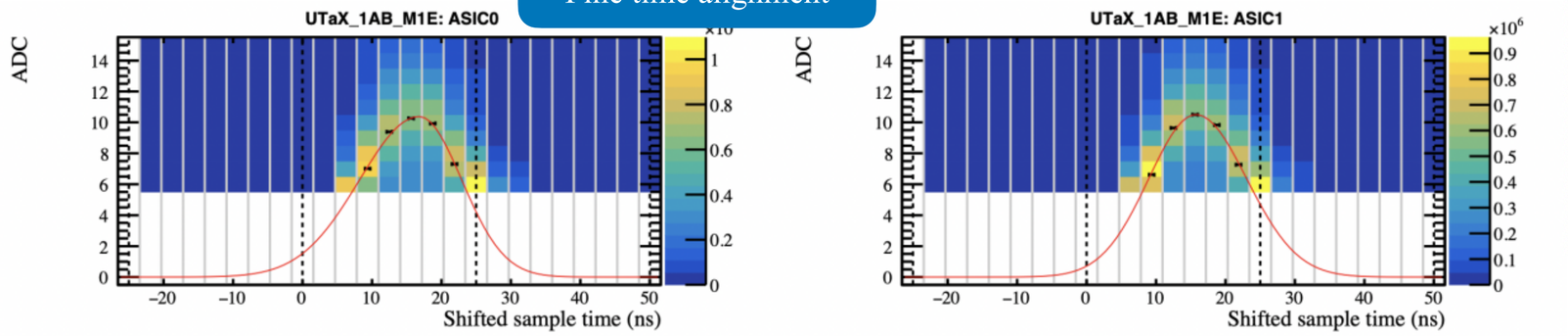
Time alignment was done using the TAE events produced by the LHC during its 2024 luminosity ramp-up

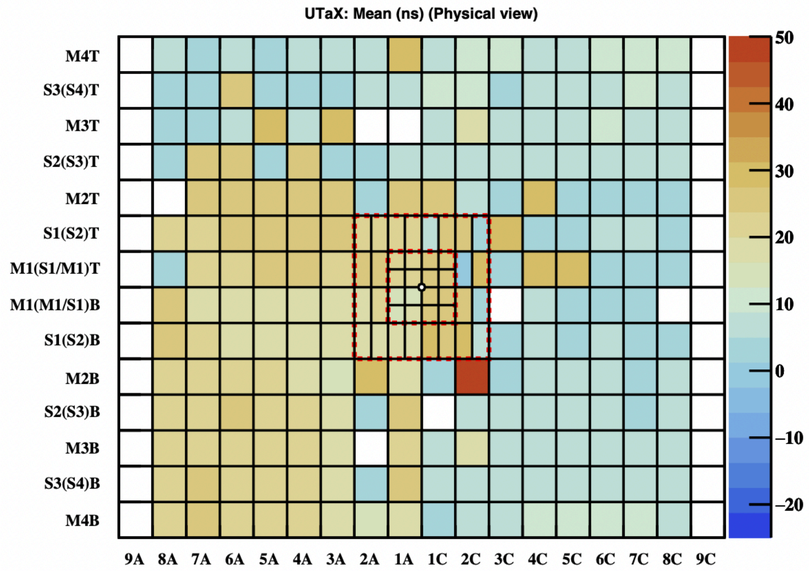
- **Coarse time alignment**
  - Done per DCB (Data Control Boards), it makes sure that all ASICs correctly identify a bunch crossing with its corresponding bunch crossing ID within the LHC orbit
- **Fine time alignment**
  - Done per module, done by scanning the ADC sampling phase, which adjusting the delay for each ASIC by fitting a known signal shape to the actual detector signals, resulting in precise time synchronization across the detector

Coarse time alignment



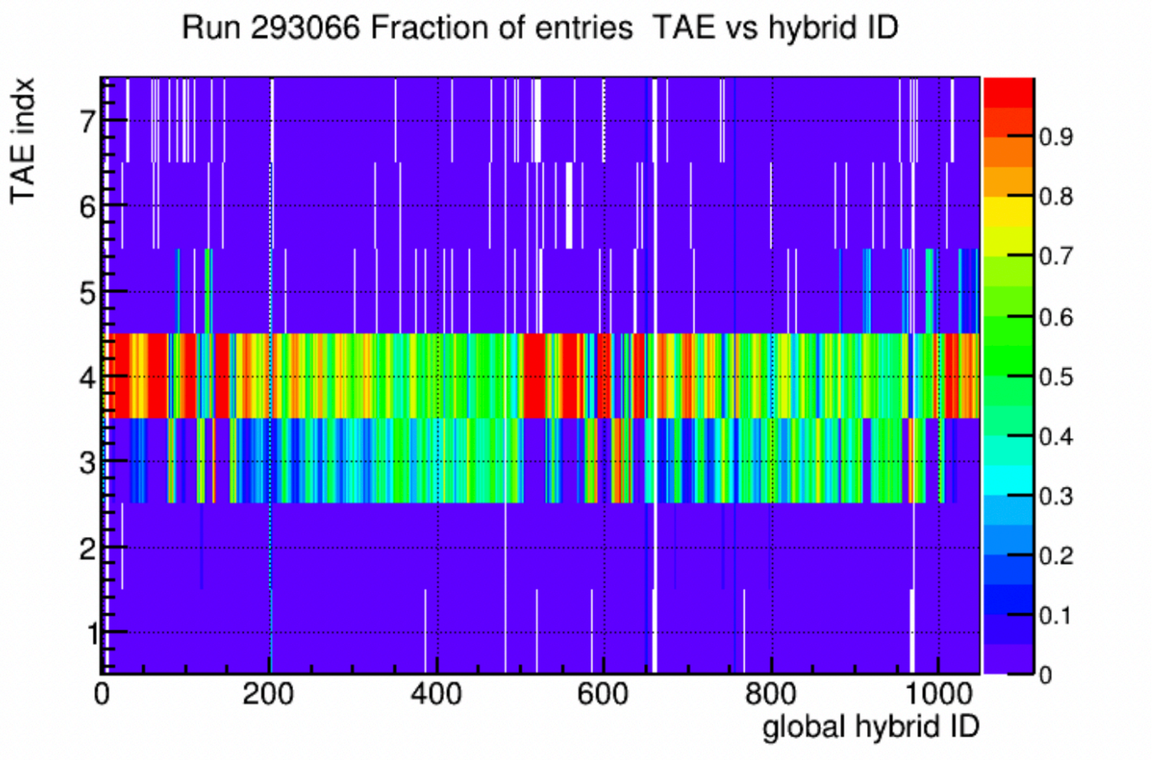

Fine time alignment



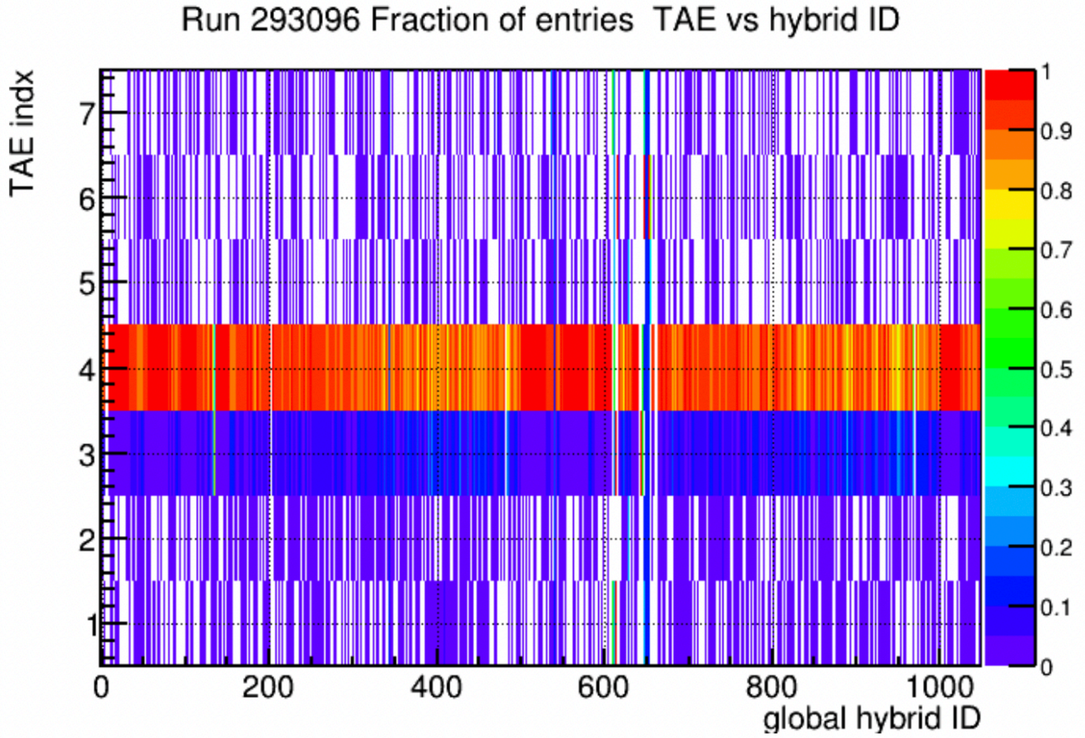



# Time alignment

Details for UT fine time alignment can be found in Christos Hadjivasiliou's talk

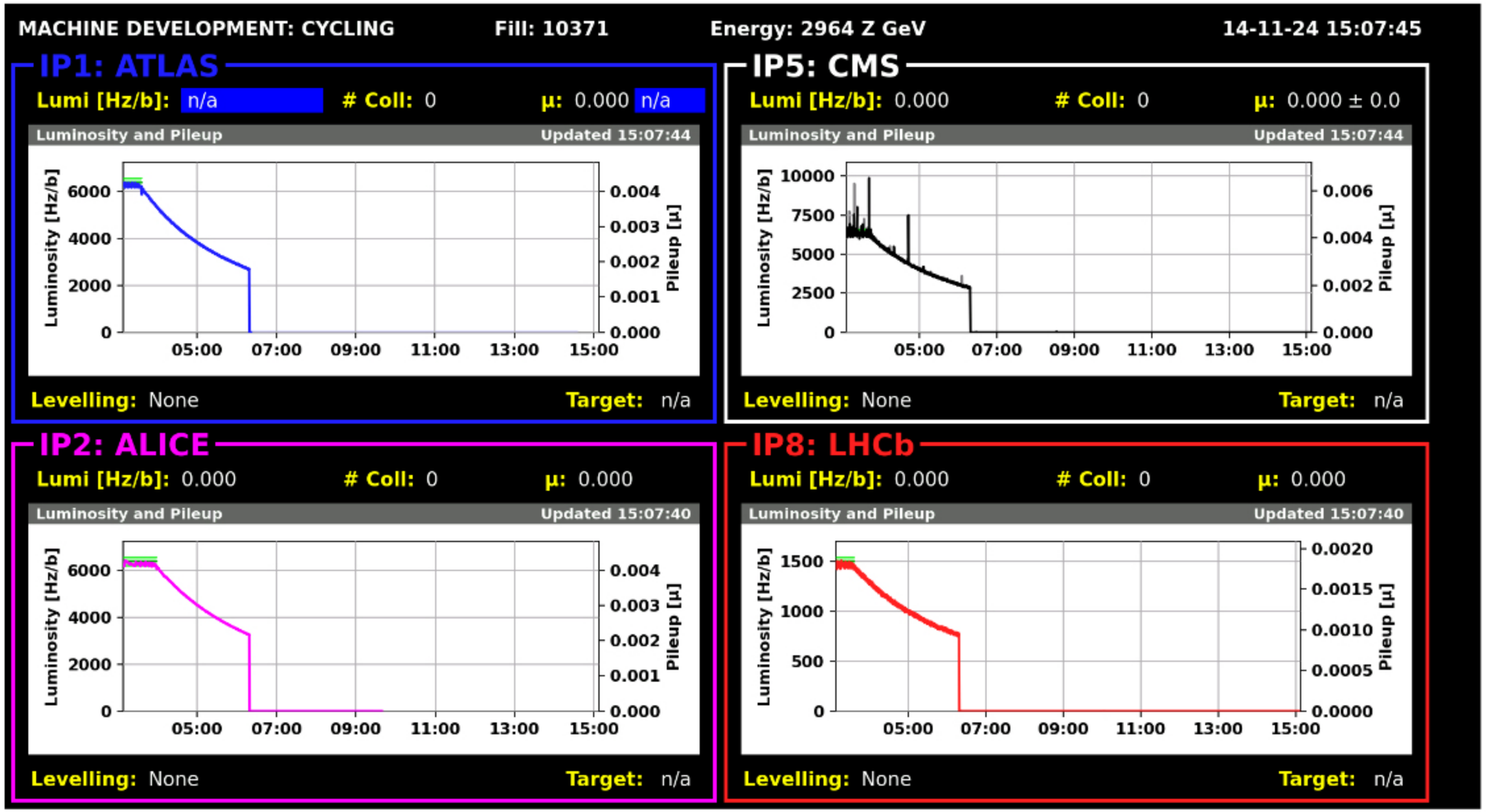



Before fine time alignment

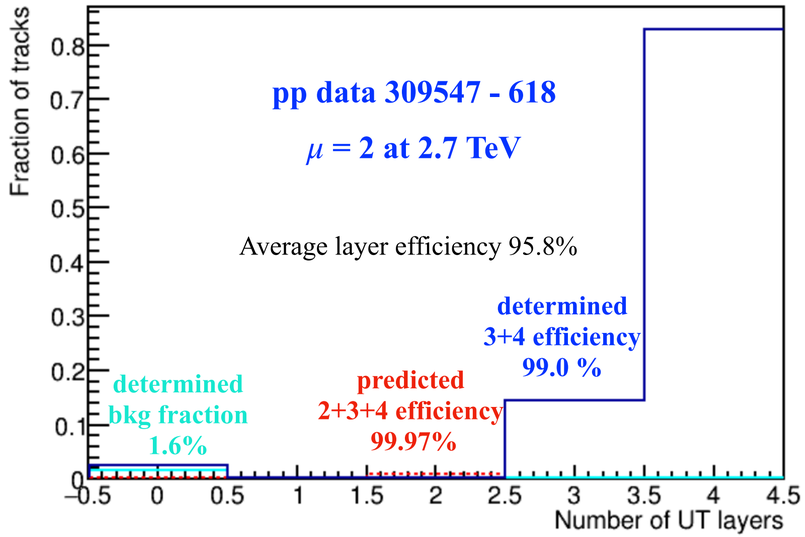



After fine time alignment

# PbPb


MACHINE DEVELOPMENT: CYCLING
Fill: 10371
Energy: 2964 Z GeV
14-11-24 15:07:45
IP1: ATLAS
Lumi [Hz/b]: n/a
# Coll: 0
μ: 0.000 n/a
Luminosity and Pileup
Updated 15:07:44
Luminosity [Hz/b]
Pileup [μ]
Levelling: None
Target: n/a
IP5: CMS
Lumi [Hz/b]: 0.000
# Coll: 0
μ: 0.000 ± 0.0
Luminosity and Pileup
Updated 15:07:44
Luminosity [Hz/b]
Pileup [μ]
Levelling: None
Target: n/a
IP2: ALICE
Lumi [Hz/b]: 0.000
# Coll: 0
μ: 0.000
Luminosity and Pileup
Updated 15:07:40
Luminosity [Hz/b]
Pileup [μ]
Levelling: None
Target: n/a
IP8: LHCb
Lumi [Hz/b]: 0.000
# Coll: 0
μ: 0.000
Luminosity and Pileup
Updated 15:07:40
Luminosity [Hz/b]
Pileup [μ]
Levelling: None
Target: n/a

# UT Tracking efficiency

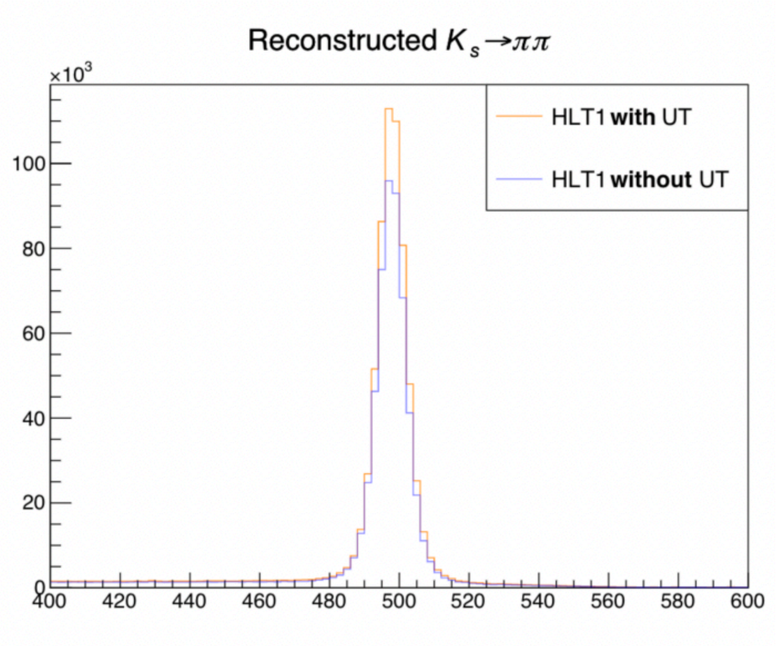



**Number of UT layers matched to a long track and the relative tracking efficiency**

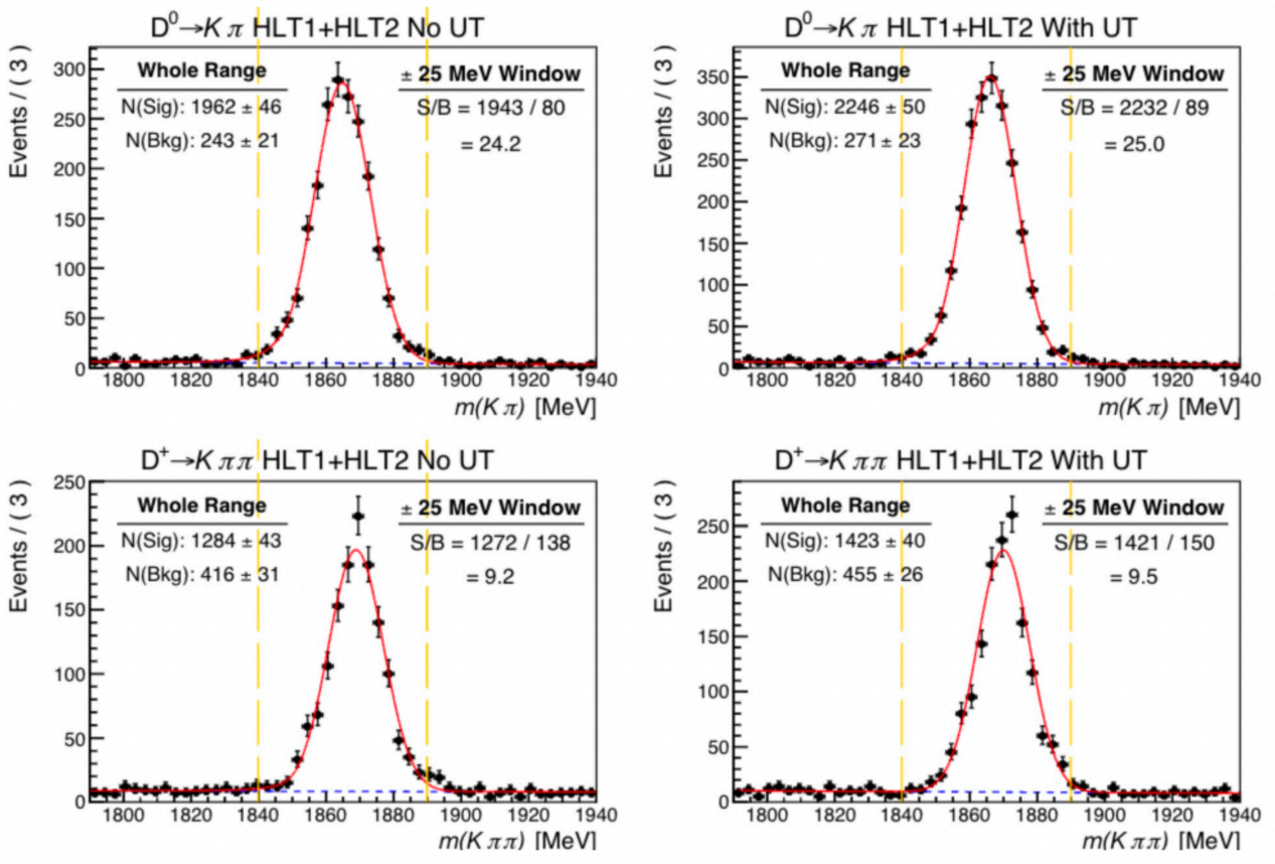
- Low energy pp reference run from 28/10/2024 to 04/11/2024

# Tracking improvement with UT

- Add downstream tracks (UT+SciFi) in trigger is able to reconstruct decays outside the VELO in real time, which is able to reconstruct and select long-lived particles
- Reconstruction performance of long tracks improved with UT since the improvement of momentum resolution




**Add downstream tracks (UT+SciFi) in HLT1**




**Long tracks in HLT1 + HLT2**