CMOS R&D for LHCb UT in Upgrade II

Zhiyu Xiang （项治宇）
On behalf of COFFEE team

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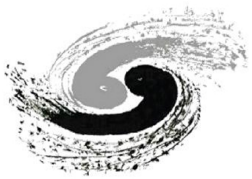
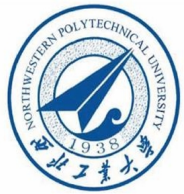
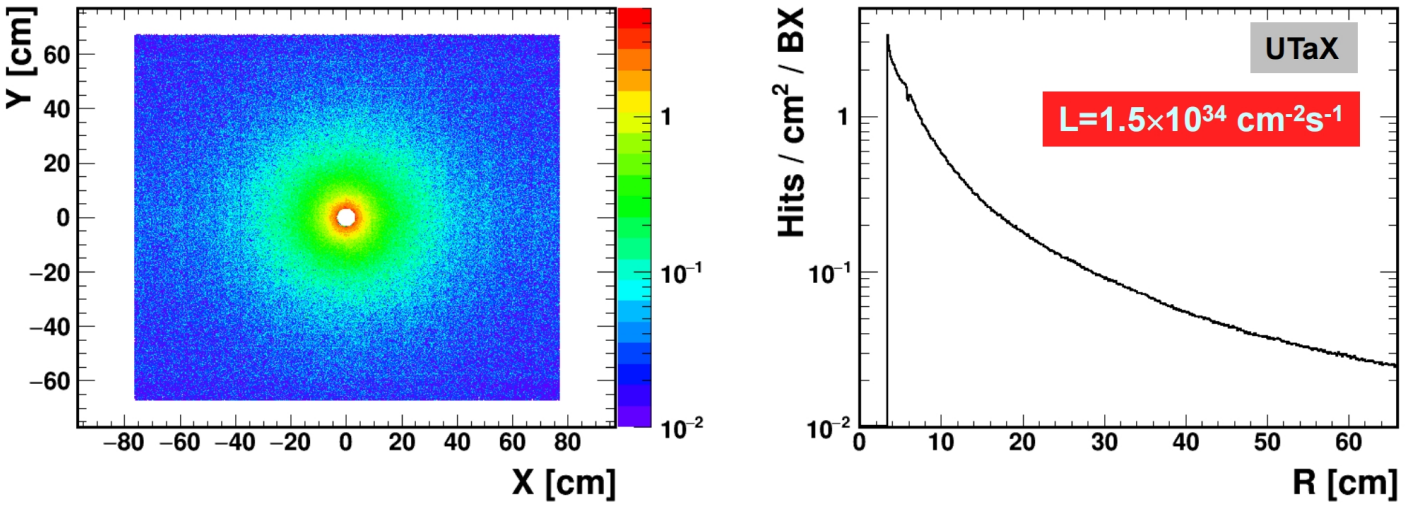
CMOS SENSOR IN
FIFTY-FIVE NM PROCESS





UT @ Upgrade II

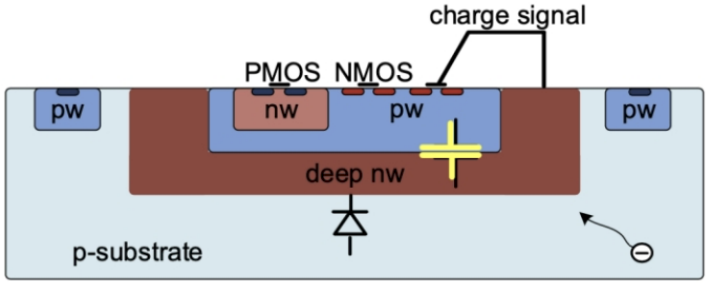
- The future of LHCb, Run5, will evolve into high-luminosity. Increased multiplicity require a finer grained and more radiation-hard Tracker
- For Upstream Tracker (UT),max hit density up to 5.92 Hits/cm2/BX, or 4.0 averaged over all bunch crossings
  - The occupancy (max $\sim$ 10%) can not handle by current UT
- A new UT for the Upgrade II is mandatory: Si-strip $\rightarrow$ Si-pixel



FTDR for the LHCb Upgrade II @LHCB-TDR-023

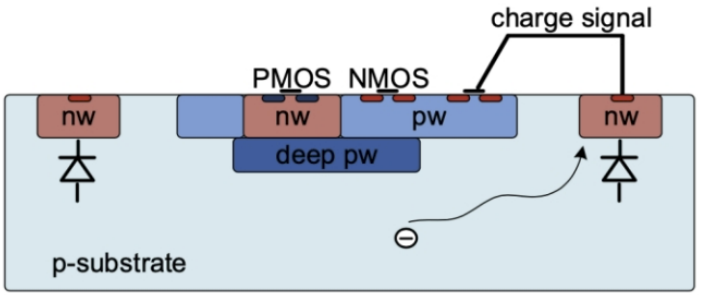
CMOS MAPS as Possible Solutions

HVCMOS



Large collection electrode

CMOS with small electrode



Small collection electrode

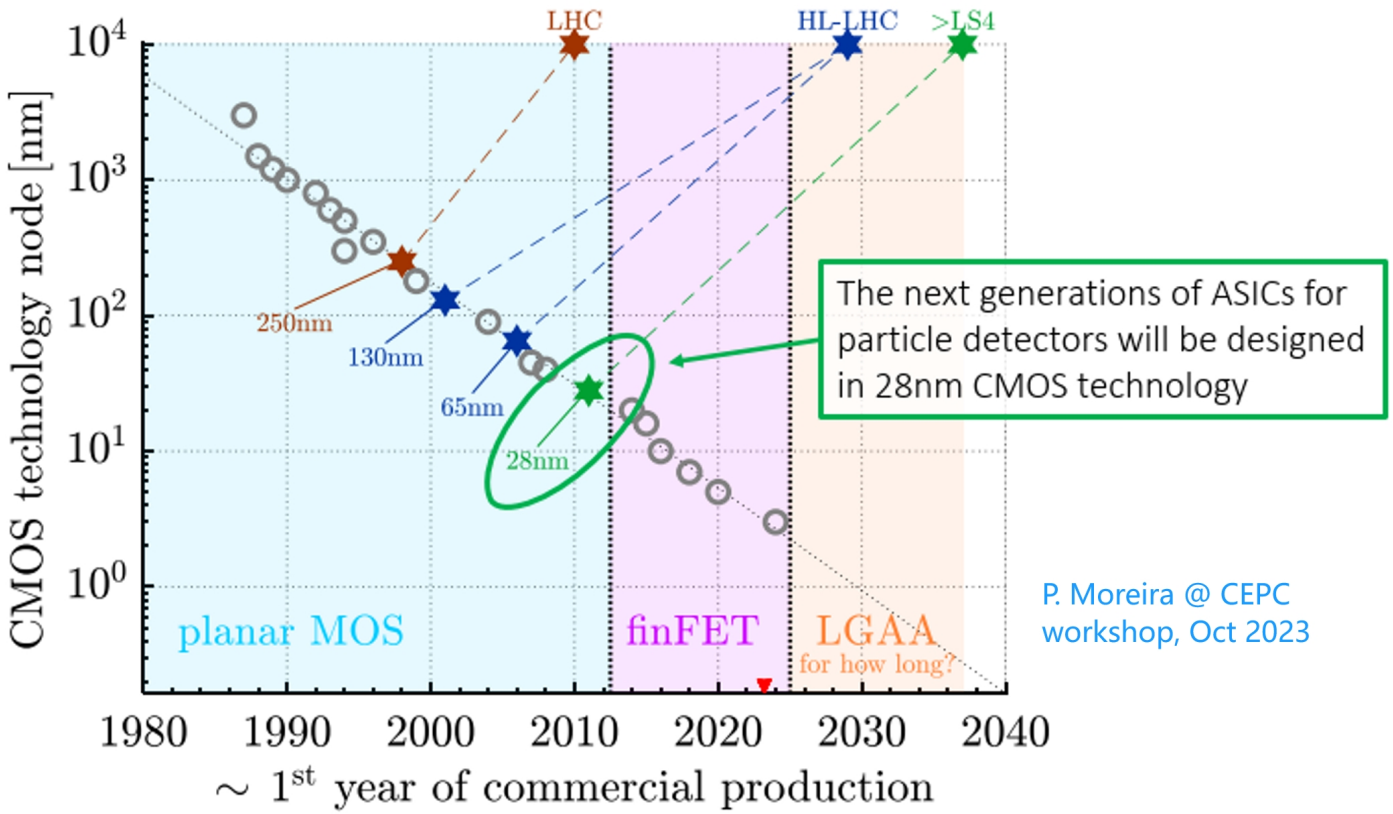
UT needs: radiation hardness $3 \times 10^{15} \mathrm{n_{eq}/cm^2}$, 240 Mrad TID, time resolution $8\mathrm{ns}$, power consumption 100-300 $\mathrm{mW/cm^2}$

HVCMOS for UT:

- Front-end circuit inside the charge collection well for individual pixel
- Large uniform electric field
- On average shorter drift path, faster signal collection
- High radiation tolerance (less trapping)

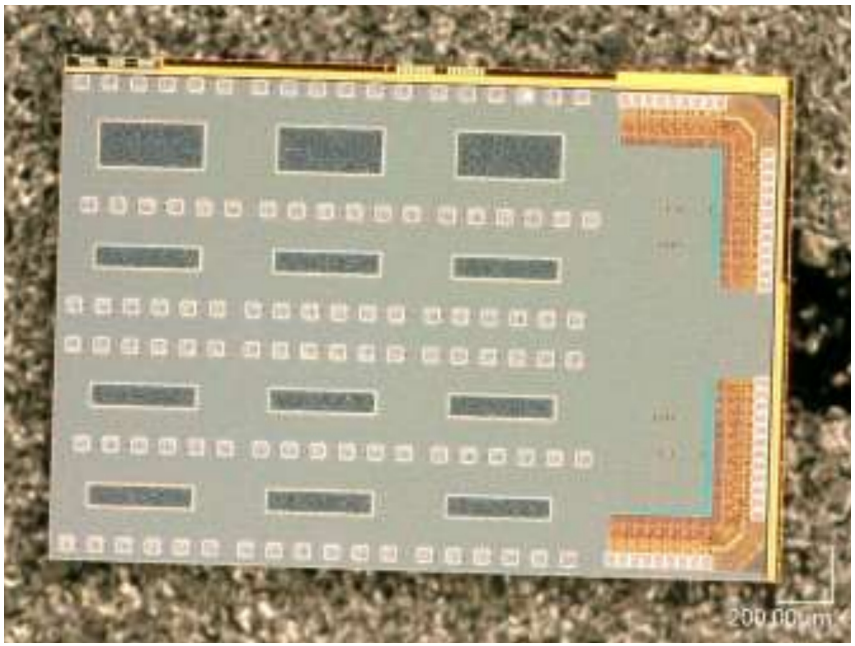
Choice of HVCMOS with 55nm Process

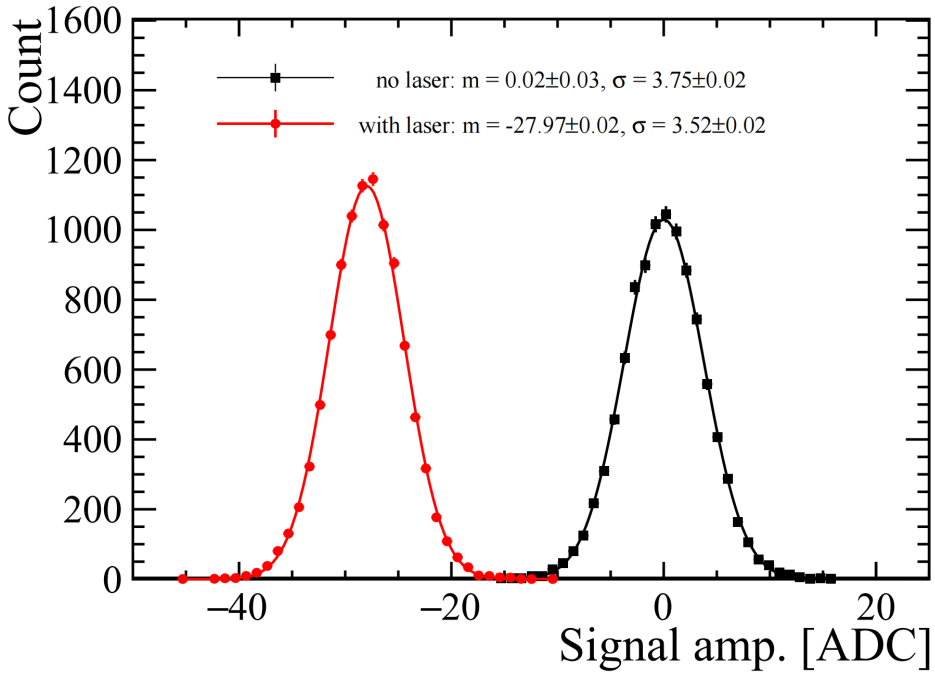
- The international mainstream technology is 180/150 nm process. HV-CMOS pixel sensor has been applied to Mu3e experiment
- Motivation of chip R&D in 55nm process:
  - Supporting concern: 55nm process should provide stable support for mass production in next decades
  - Technological benefits: lower power, higher irradiation tolerance ...



CMOS sensOr in Fifty-FivE nm procEss (COFFEE)

- COFFEE1 chip, $3 \times 2\mathrm{mm}^2$, verify the feasibility of 55nm process
  - Variation of passive diode arrays with pixel size of $25/50 \times 150\mu\mathrm{m}^2$
  - Similar deep N well inserted
  - Simple amplifier circuit added
- Sensor can responds to red laser, test with IDE1140 read-out chip

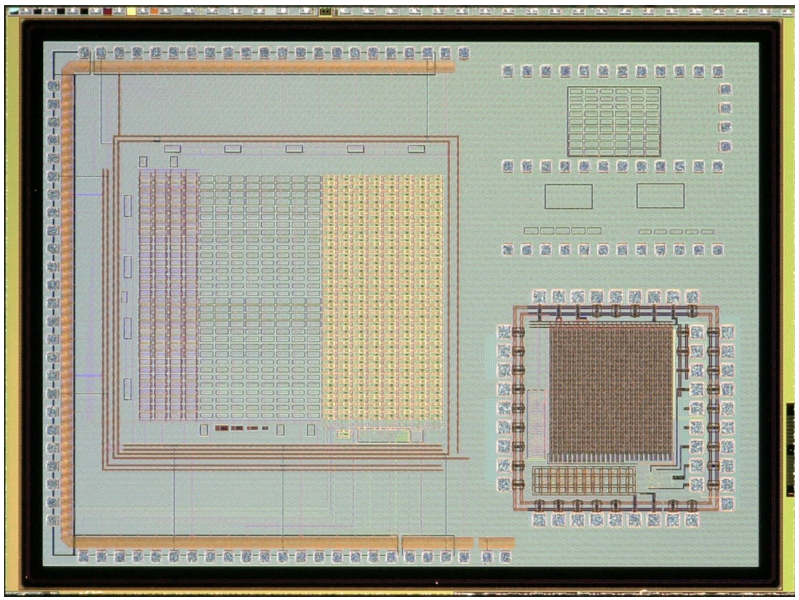


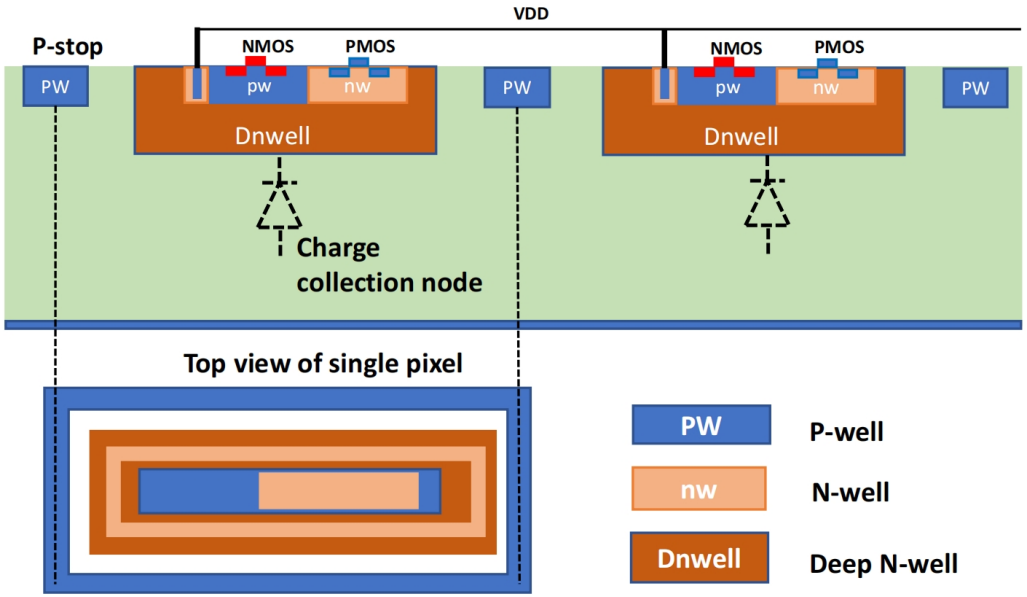


CMOS sensOr in Fifty-FivE nm procEss (COFFEE)

The first HVCMOS chip in 55nm process

- COFFEE2 chip ($4 \times 3\mathrm{mm}^2$): (test results shown today)
  - Real validation of the sensor structures with electronics included
  - Variation of passive diode arrays with pixel size of $40 \times 80\mu\mathrm{m}^2$
  - Integral analog amplifier and switch circuit to select certain pixel
  - Discriminator and DAC unit added

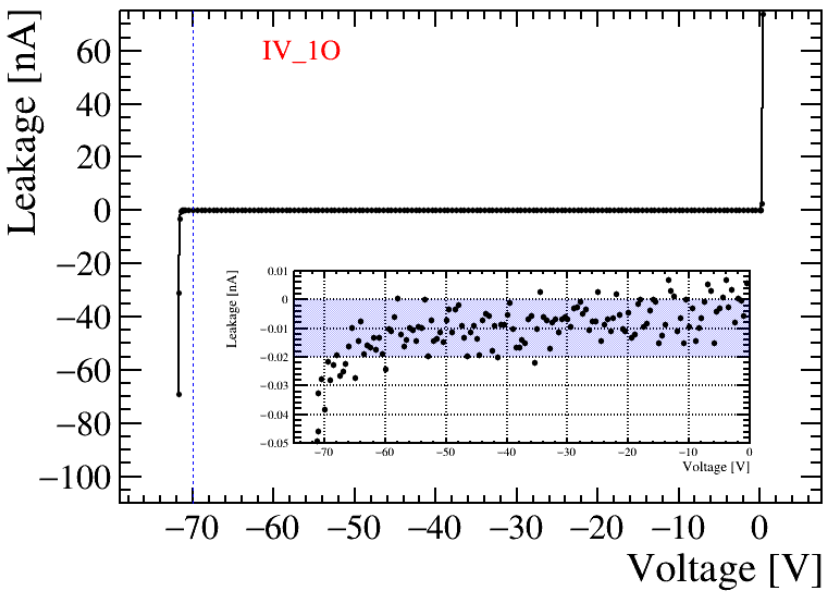


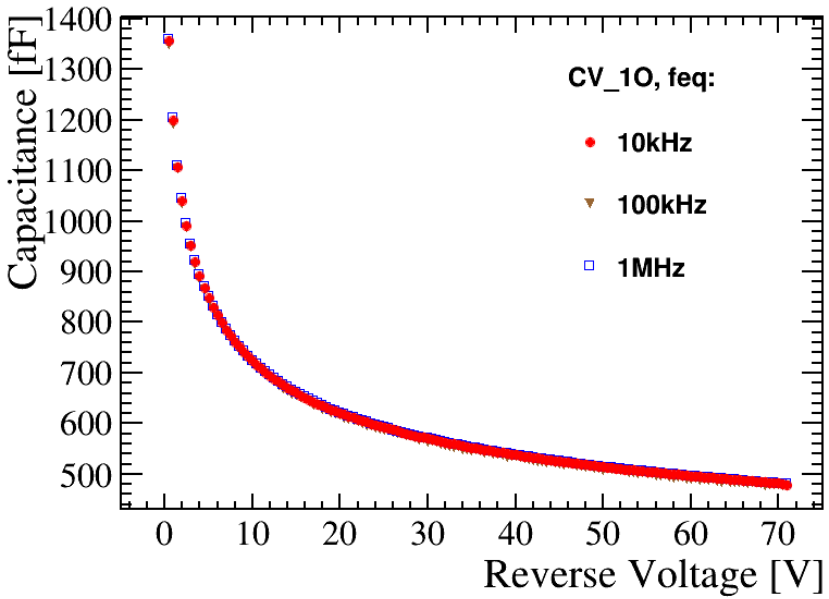


NIMA Volume 1069 P169905 (2024)

Typical IV/CV Test

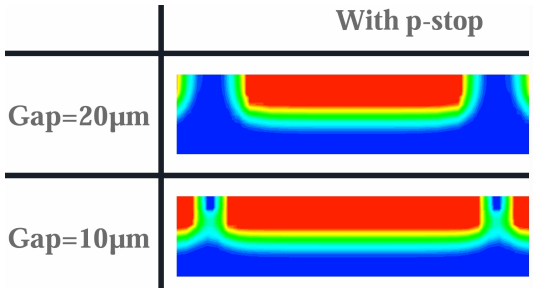
- Verified the low leakage 55nm process
- Breakdown voltage $\sim$ 70V, leakage $\sim$ 10pA
- At 70V, the capacitance of single pixel due to depletion $\sim 30 - 50\mathrm{fF}$

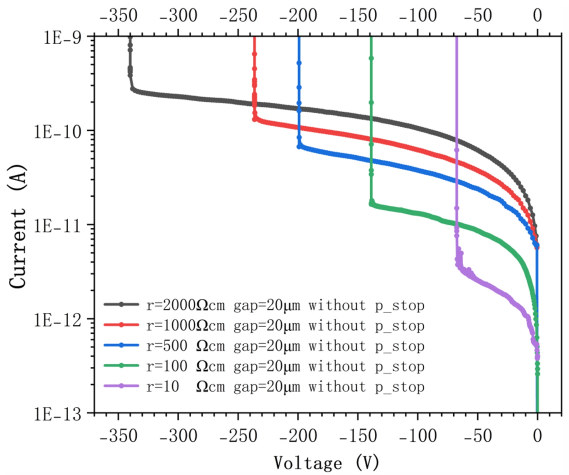


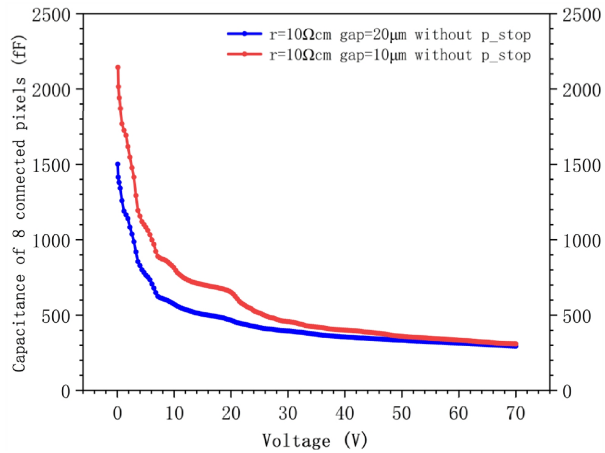


TCAD Simulation

- Test results confirmed by TCAD simulation
- Current substrate resistivity ($10\Omega \cdot \mathrm{cm}$) limits the break down voltage
- Breakdown voltage close to 70V with low leakage $\sim \mathrm{pA}$ (mainly edge breakdown)



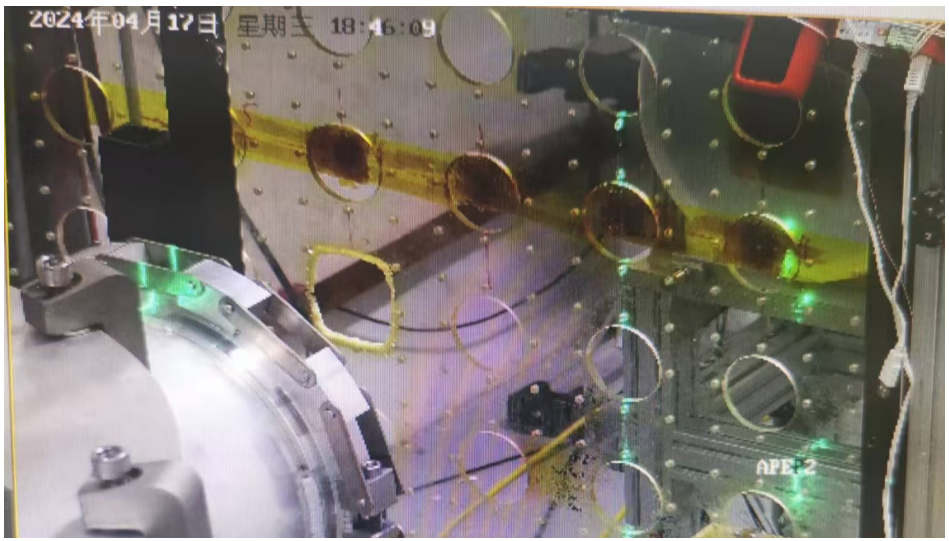


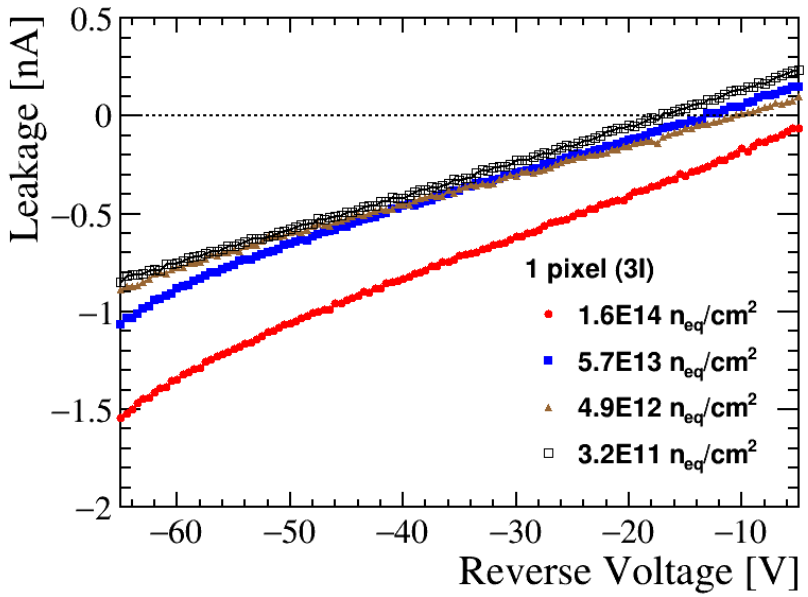


- Not fully depleted. The capacitance also takes into account parasitic effect (i.e. metal electrode/routing wire)

Glance at Irradiation Effect

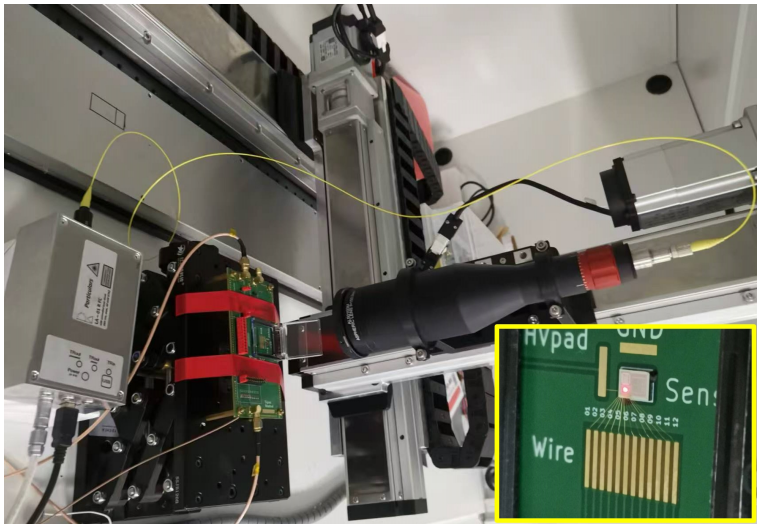
- Proton beam @80MeV of CSNS
- Irradiation up to 1.6×10^{14} $\mathrm{n_{eq}/cm^2}$ at room temperature
- Leakage current increased to 1nA after irradiation

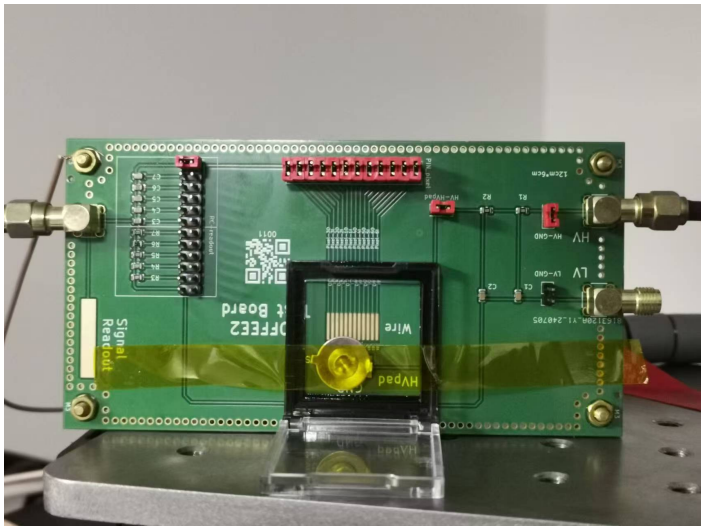


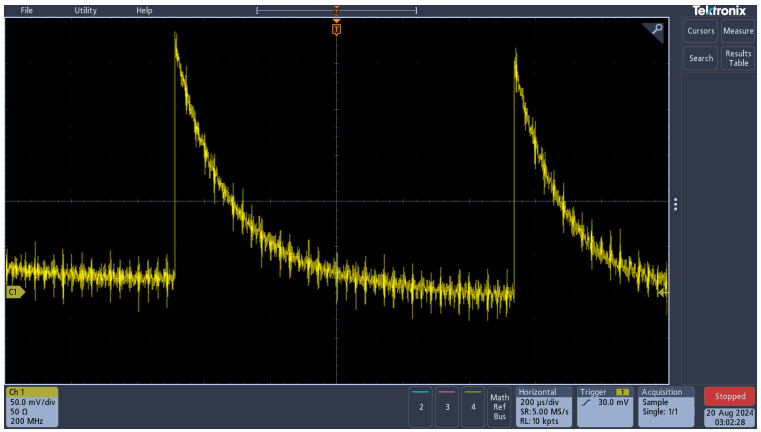


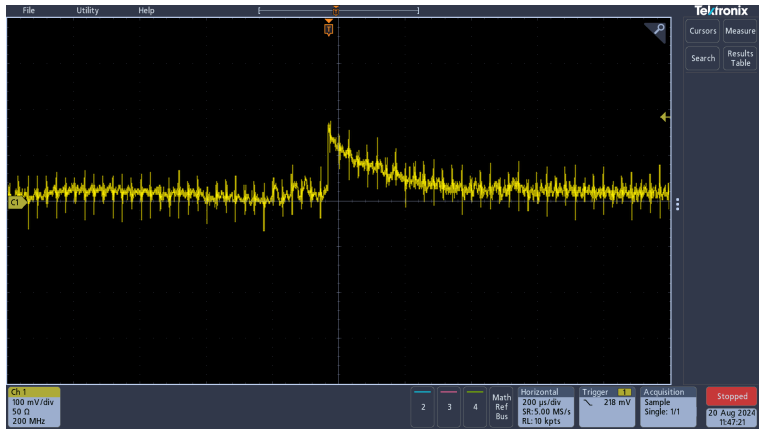
Test of Passive Sensors

- Clear response to both laser ($\lambda \sim 650\text{nm}$) and α radioactive source
  - 54 pixels read out at a time, via external charge sensitive amplifier

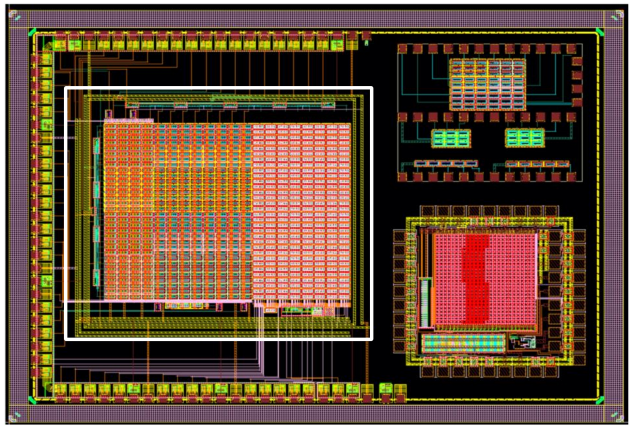






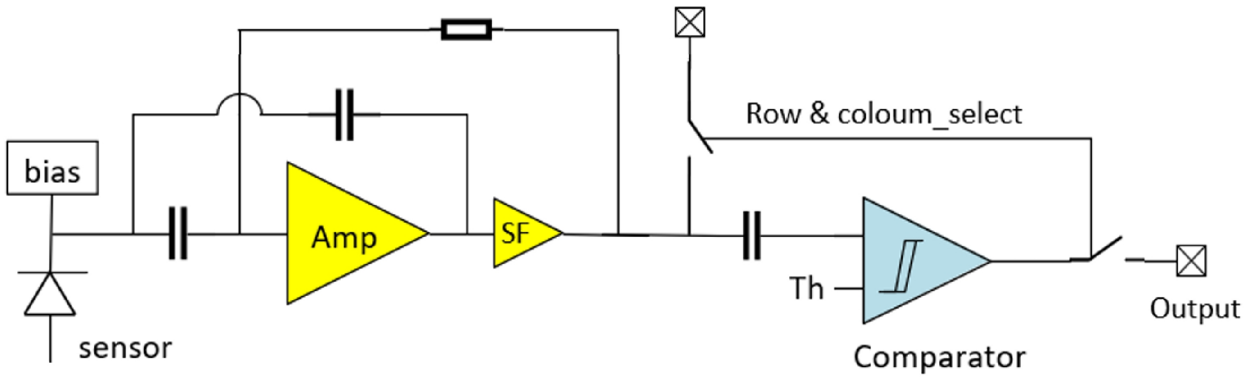


Active Pixel Matrix



- 32×20 active pixel matrix, peripheral modules including analogue buffer, DACs and row/column switch
- CSA, discriminator for individual pixel

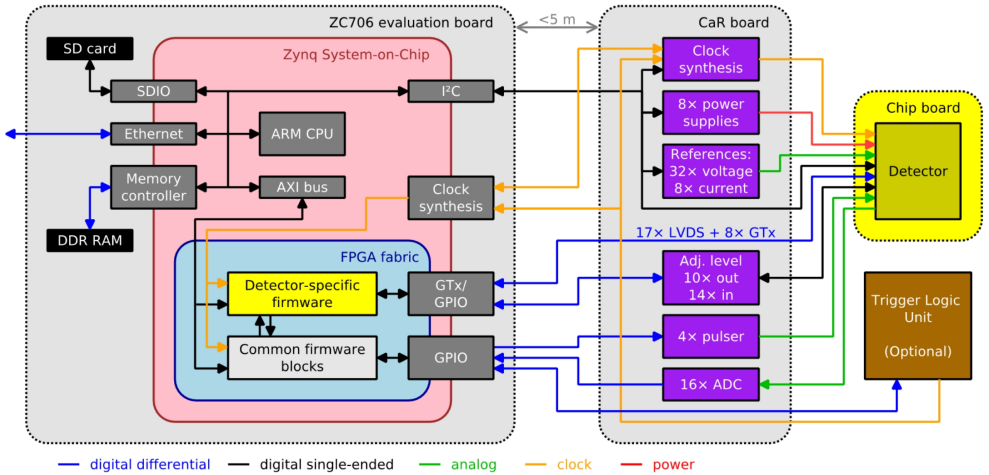
- Circuit simulation performance
  - CSA: ~140e ENC, gain $\sim 57 \mu \mathrm{V/e}$
  - CMOS discriminator: Time walk $\sim 2 \mathrm{ns}$; Time over threshold $\sim 5 \mu \mathrm{s}$
  - NMOS discriminator: Time walk $\sim 9 \mathrm{ns}$; Time over threshold $\sim 5 \mu \mathrm{s}$

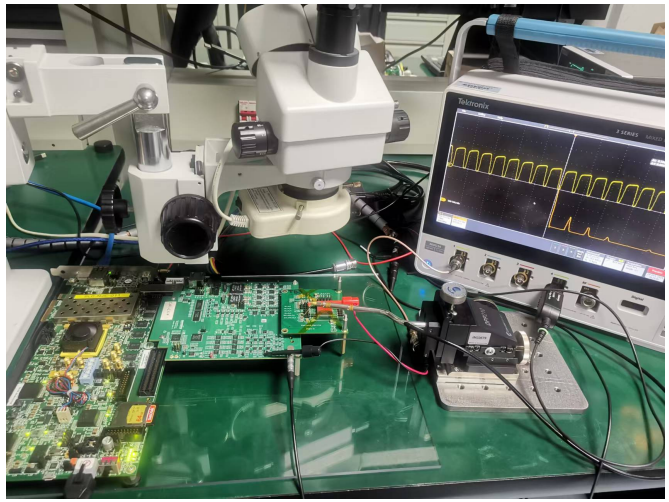


Active Pixel Matrix Test System

PC + ZC706 + Caribou board + specific carrier board

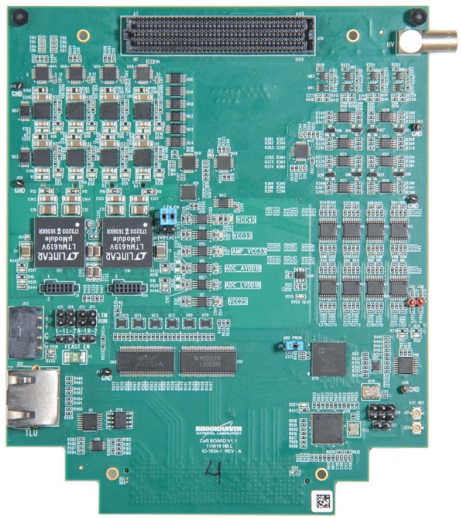
Caribou system architecture





Control and Readout (CaR) board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector



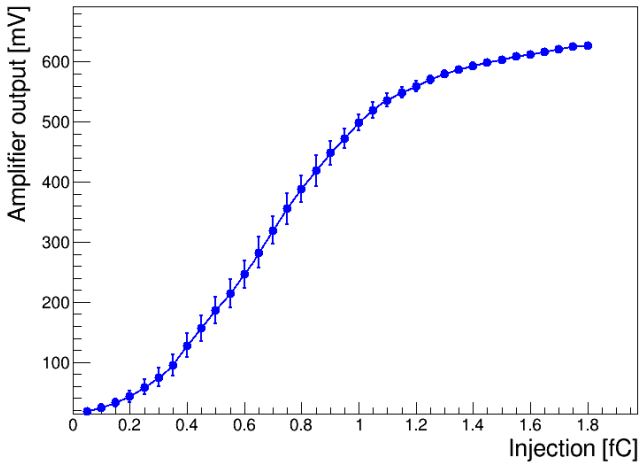
https://gitlab.cern.ch/Caribou/hardware/carboard

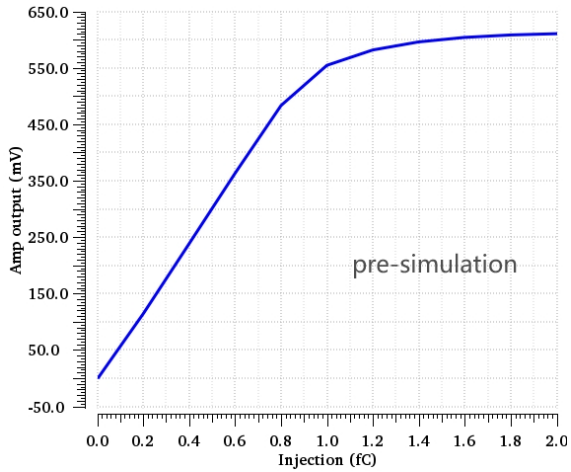
Resources for various target applications

20 CaR boards v1.4 produced and distributed within RD50 common project

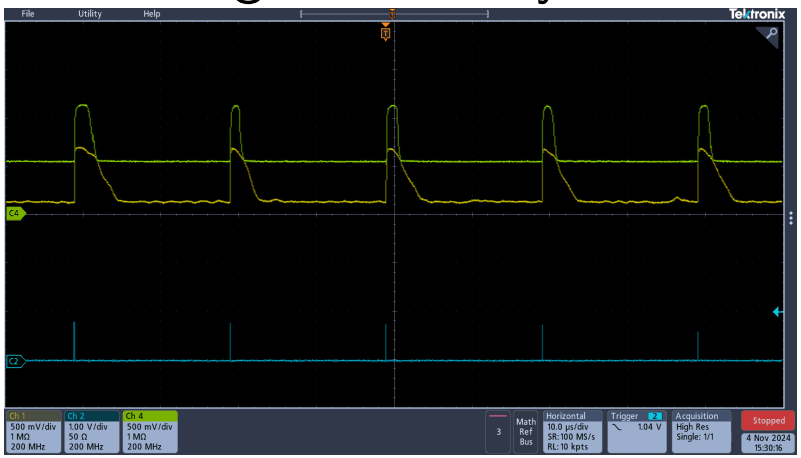
Active Pixel Test Results (preliminary)

- CSA output calibrated with charge injection. Response curve similar as pre-simulation



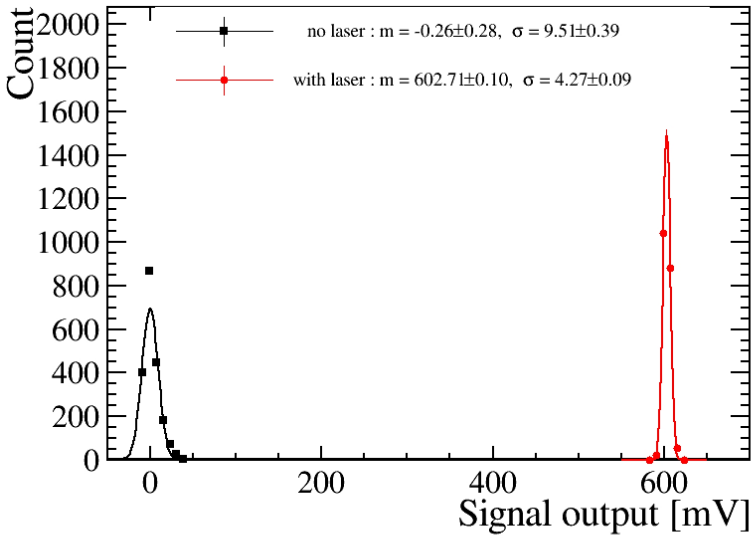


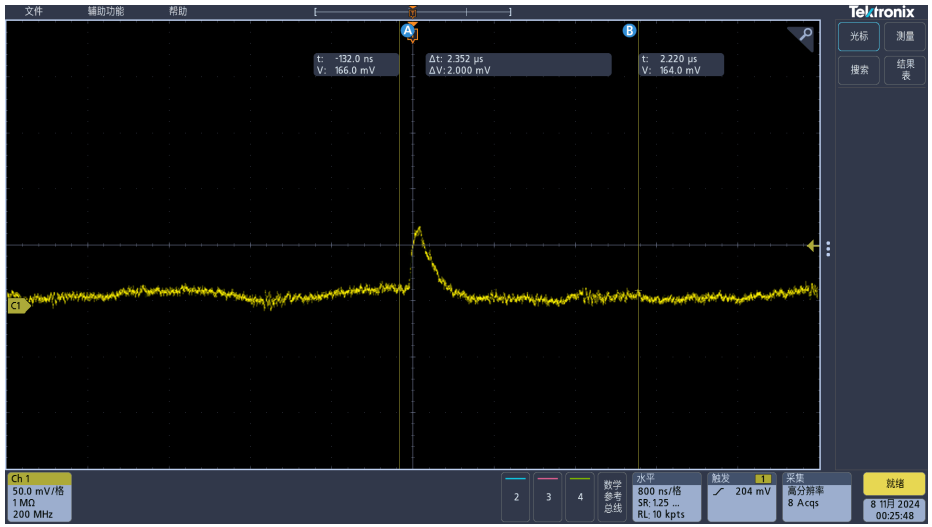
- Discriminator works well, in green while yellow for amplifier output



Active Pixel Test Results (preliminary)

- Clear signal response to red laser (left) and radioactive source (right)
- For $^{55}\mathrm{Fe}$, signal amplitude consistent with expectation (1640e-)





Summary & Future

- Frist HVCMOS prototyping chip in 55nm process for UT@Upgrade II
- Test results for COFFEE2 chip, show encouraging diode properties (breakdown$> 70\mathrm{V}$, leakage $\sim 10\mathrm{pA}$)
- Promising results from test with laser and radioactive source (α, X-ray). Digital circuit works as expected
- Looking for opportunity of MPW with high resistivity substrate
- COFFEE3 is currently being designed to validate the pixel array readout architecture