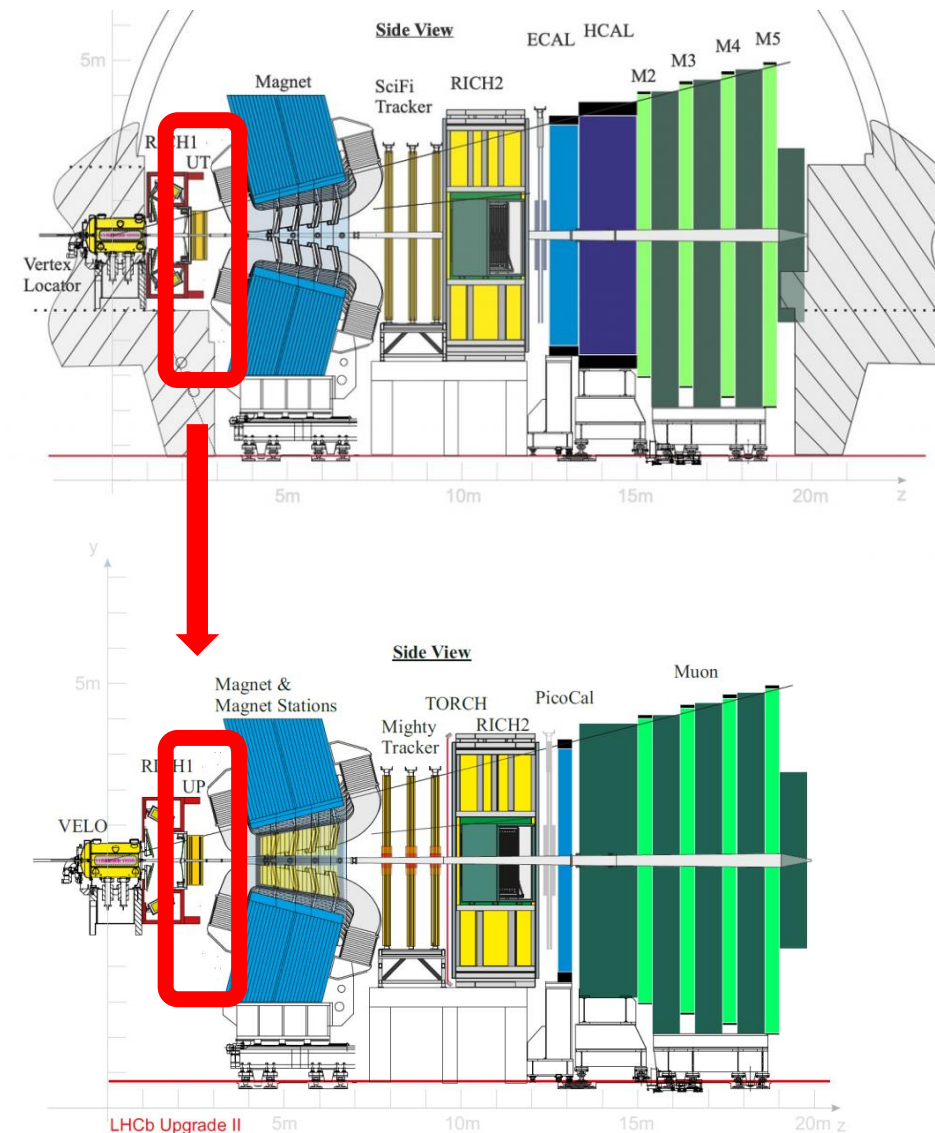




Simulation Study for LHCb UT in Upgrade II

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- Introduction
- Upgrade-II UT design and layout
 - CMOS Chip Options
 - Detector Structure
- The Simulation of Upgrade-II UT
 - Geometry Description in DD4hep
 - Hit Density
 - Material budget
 - UP Digitization
- Summary and Outlook



➤ LHCb

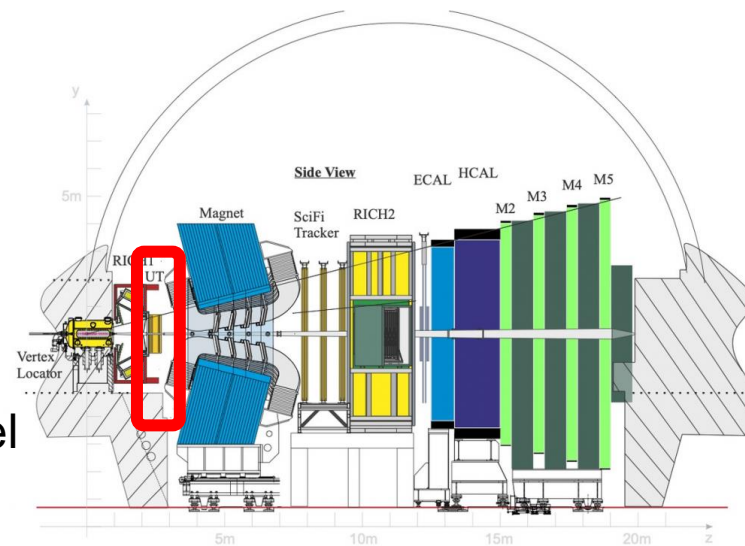
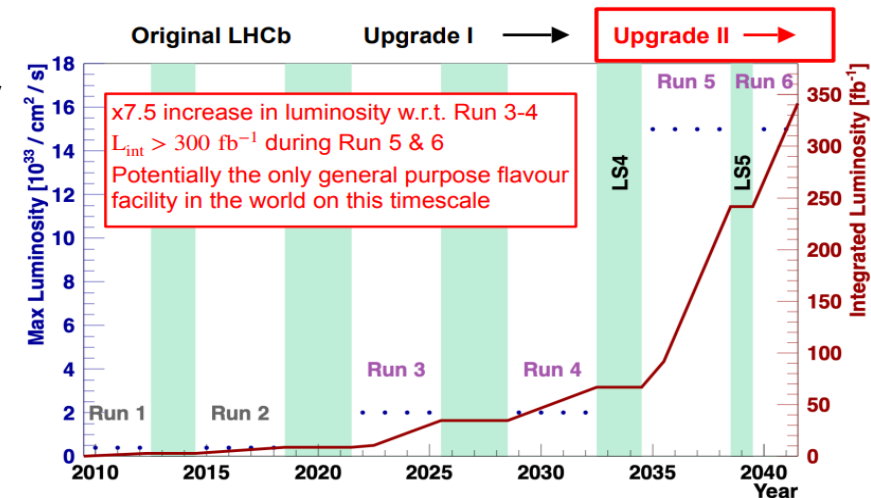
- A single-armed forward spectrometer at the Large Hadron Collider
- Aiming to study flavor physics like CP violation and rare decays

➤ LHCb Upgrade II

- LHCb is planning a major upgrade (**Upgrade II**)
- The High-Lumi LHC ($\mathcal{L} = 1.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$)

➤ Upgrade-II UT

- **Upstream Tracker (UT)** : a key component of the tracking system
- The current UT can't be kept for Upgrade II
 - ❑ Much increased hit density requires higher granularity
 - ❑ Bandwidth for high data rate
 - ❑ Radiation hardness
- Therefore, Upgrade-II UT detector will use CMOS Monolithic Active Pixel Sensors (MAPS) technology, named **Upstream Pixel tracker (UP)**



Two Design for CMOS Chip

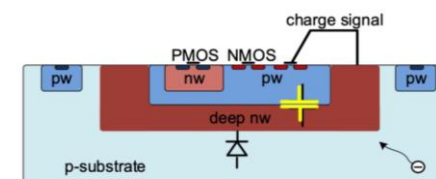
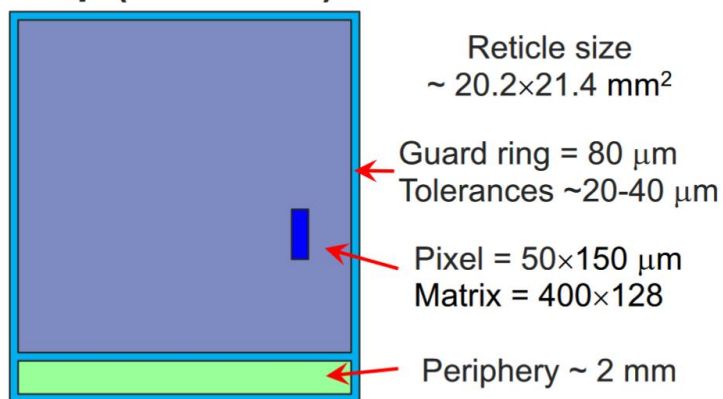
The ongoing R&D studies indicate that monolithic active pixel sensors can be considered as very strong candidates for UP.

Two approaches are being pursued to develop CMOS chips:

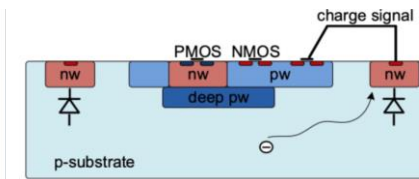
- Large fill-factor or high-voltage (**HV-CMOS**) with large electrode
- Low fill-factor or low-voltage (**LV-CMOS**) with small electrode

More details in Zhiyu's talk.

Chip (HV-CMOS)



High-Voltage CMOS



CMOS with small electrode

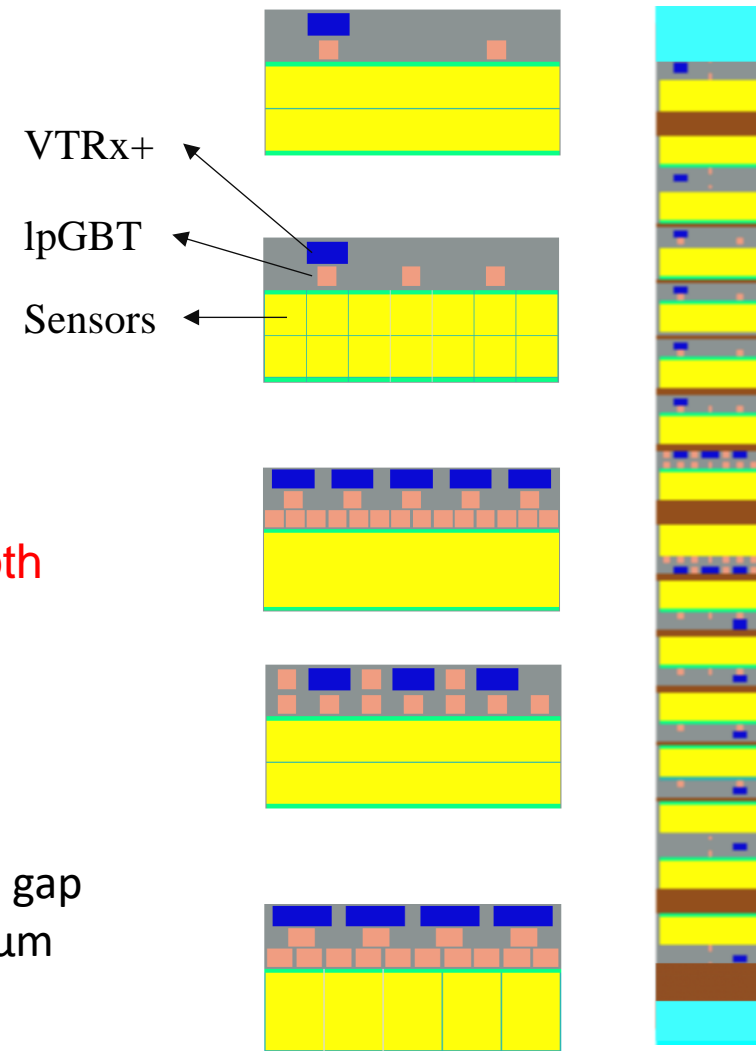
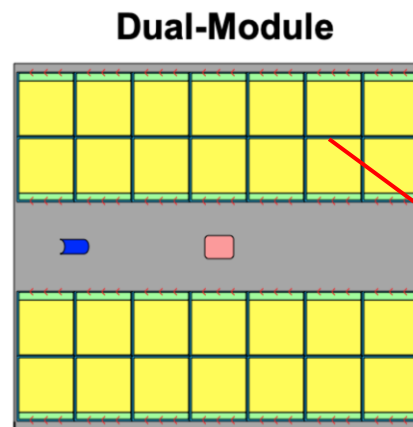
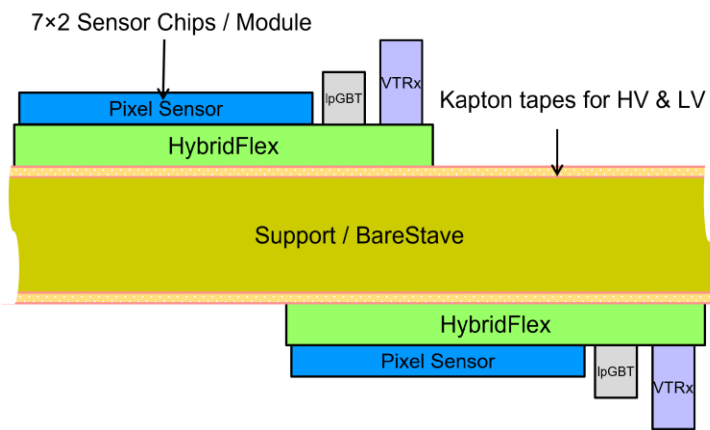
Characteristics	HV-CMOS	LV-CMOS
	Circuitry inside the collection well	Circuitry outside the collection well
Chip size	2.0 × 2.0 cm²	3.5 × 3.5 cm²
Pixel size	50 × 150 μm²	30 × 30 μm²
Chip thickness	~100 μm	
Position resolution	15, 40 μm	5-10 μm
Radiation dose	3 × 15 neq/cm ² , or 240 Mrad TID	
Data rate per chip	Up to 9 Gb/s	Up to 30 Gb/s
Time resolution	O(1) ns	
Power consumption	100-300 mW/cm ²	
Radiation dose	3 × 15 neq/cm ² , or 240 Mrad TID	

➤ UP Modules Structure for HV-CMOS design

14 CMOS chips and supporting electronic components are attached to a hybrid flex to form a UP module

- 14 CMOS sensor chips split in two rows
- VTRx+ and IpGBT: ensure the normal operation and data acquisition
- The expected data rate → the numbers of IpGBT and VTRx+
- Dual modules → regions located further away from the beampipe

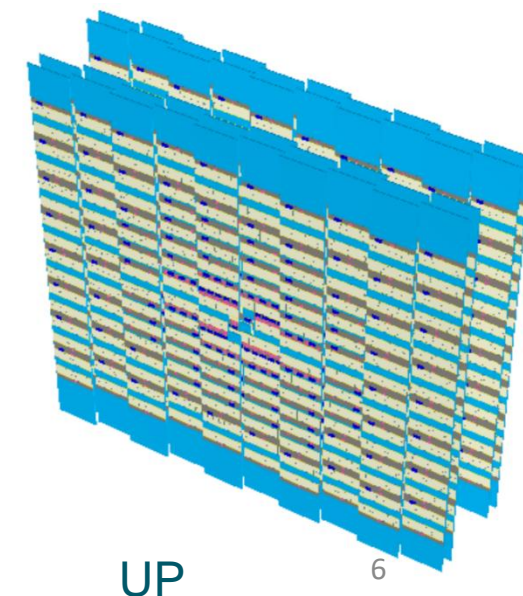
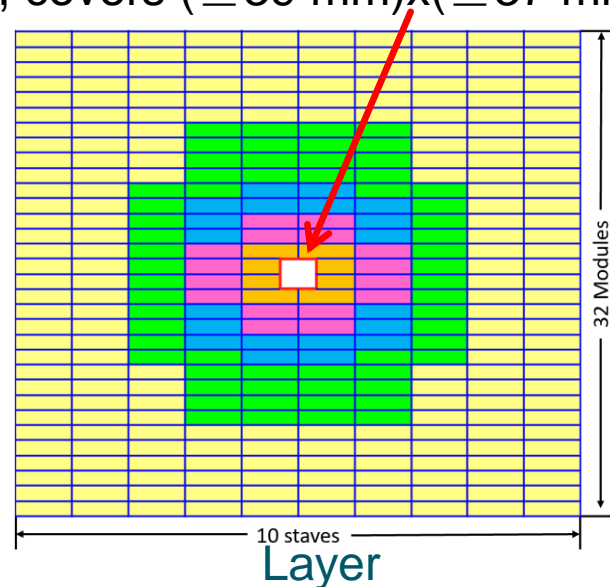
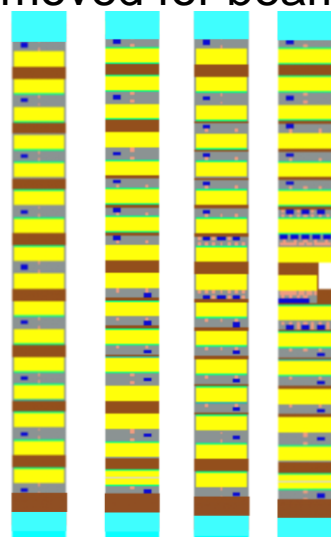
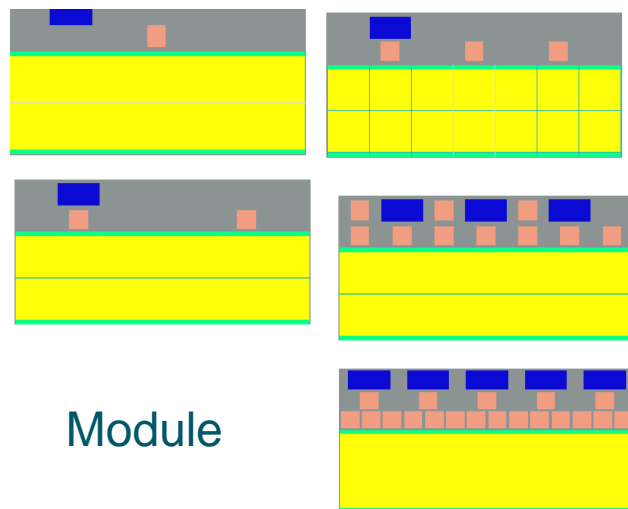
The picture below shows the view from side. Modules are mounted on **both sides of the stave**, ensuring overlaps of sensitive areas at the sensor edges



➤ UP Geometry Structure for HV-CMOS design

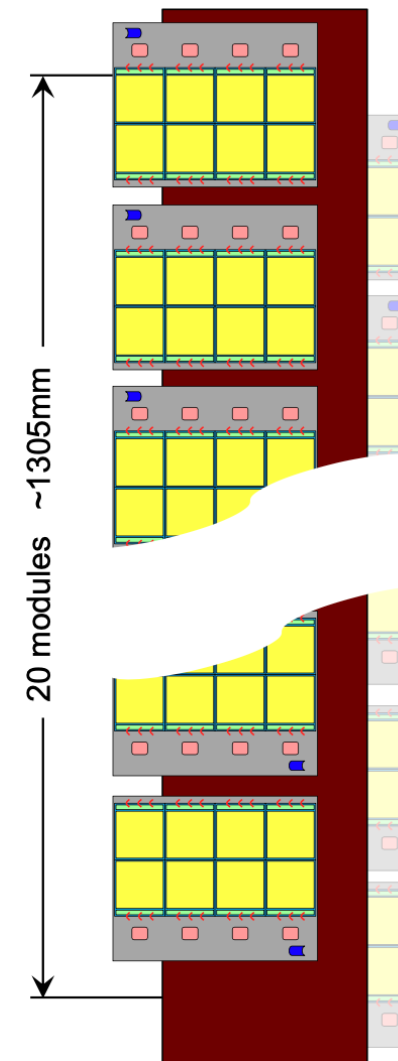
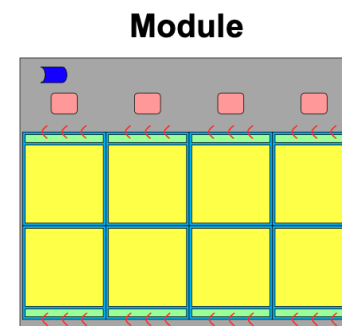
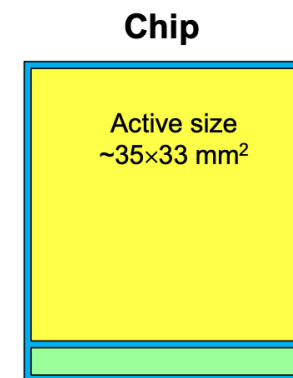
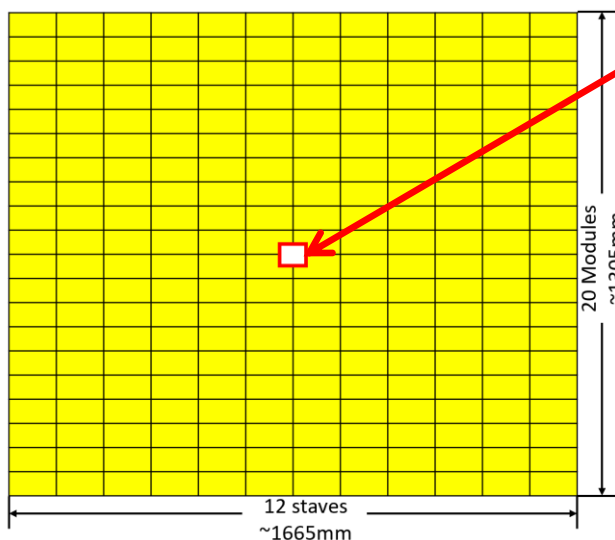
- Geometry modelling of the UP detector is completed, with the following hierarchy
 - Plane: **4 detector planes (layers)**, at Z position similar to the current UT
 - Stave: Each layer consists of **10 staves** in 4 types
 - Module: Each stave equipped with **32 modules** in 5 types
 - Chip: **14 chips in a 7×2 array** are interconnected to a flex circuit to form a module
- The central 4x4 chips are removed for beam pipe, covers $(\pm 39 \text{ mm}) \times (\pm 37 \text{ mm})$

} match with different data rates



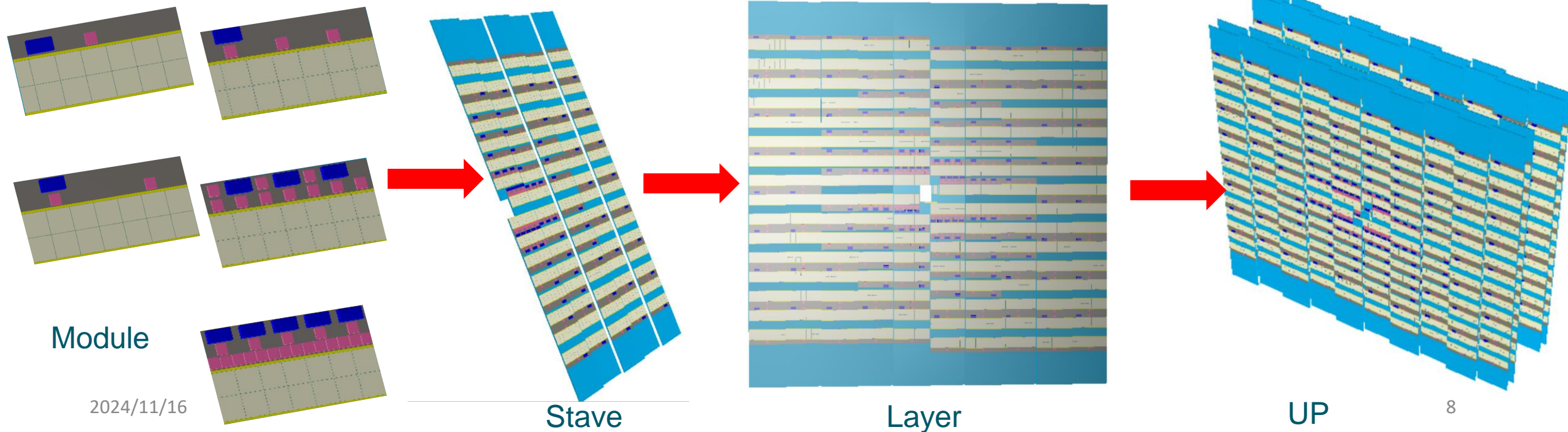
➤ UP Geometry Structure for LV-CMOS design

- Difference between LV-CMOS design and HV-CMOS design
 - Pixel size $30 \times 30 \mu\text{m}^2$
 - Active size by chip $35 \times 33 \text{ mm}^2$
 - Each module consist of **8 chips in a 4×2 array**
 - Only **one type of module**
 - Each stave consists of **20 modules**
- The beam hole inefficient area covers $(\pm 34 \text{ mm}) \times (\pm 32.5 \text{ mm})$



➤ The Simulation of UP (with HV-CMOS)

- The detector description has been implemented in the LHCb software framework with our code
- The plots bellow show the geometry construction using DD4hep
 - The MAPS-based UP has 4 layers, at z-positions similar to the current UT
 - Each layer consisting of 10 staves equipped with 32 modules
 - There are 5 types for module

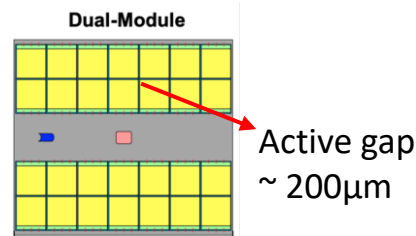


➤ **The simulation study of the UP detector**

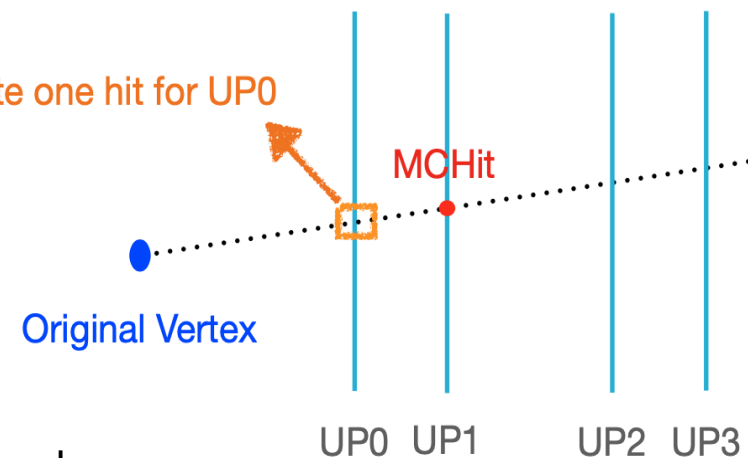
- Using simulation samples generated under Upgrade II conditions
- Described using the DD4hep framework

➤ **Loop through all tracks, for each track**

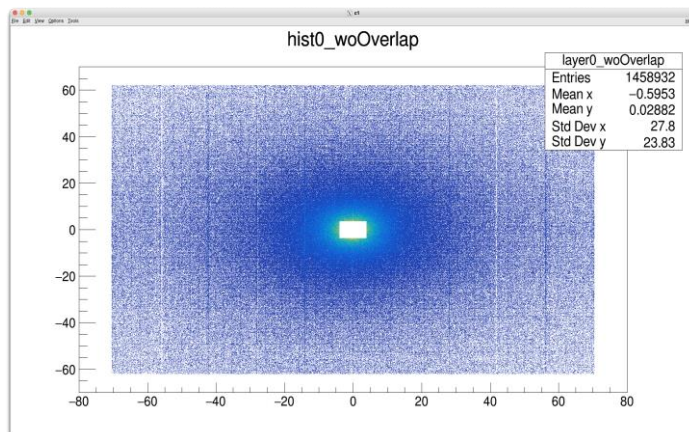
- **Remove overlap** → Save only one MCHit in one layer
- **Generate hits for Gap** → If there is no MCHit in one layer, produce one from other layers



Generate one hit for UP0

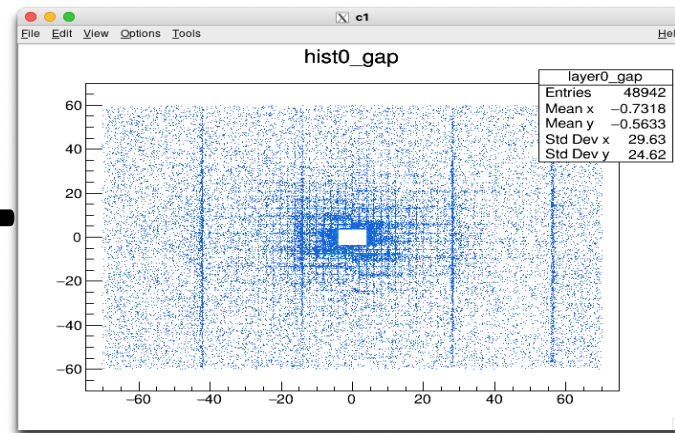


➤ The average hit densities per bunch crossing in proton-proton collisions at HL-LHC is up to **~4.5 hits/cm²/BX**

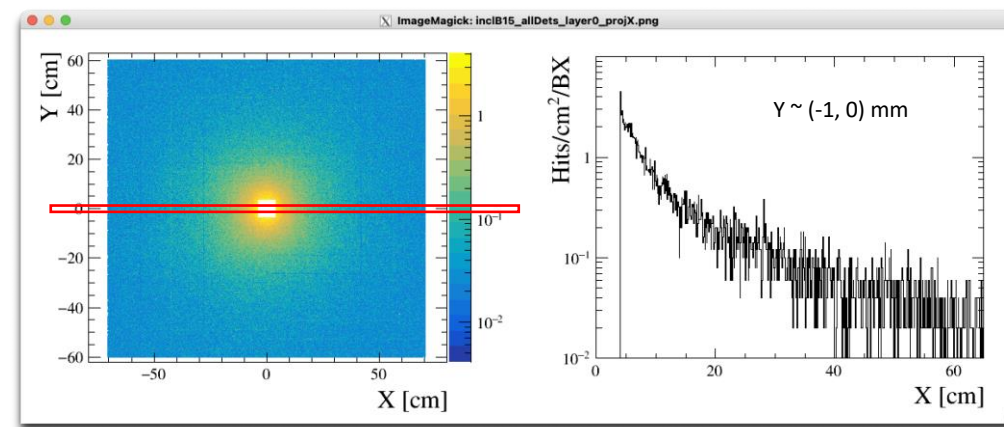


Remove overlap

2024/11/16



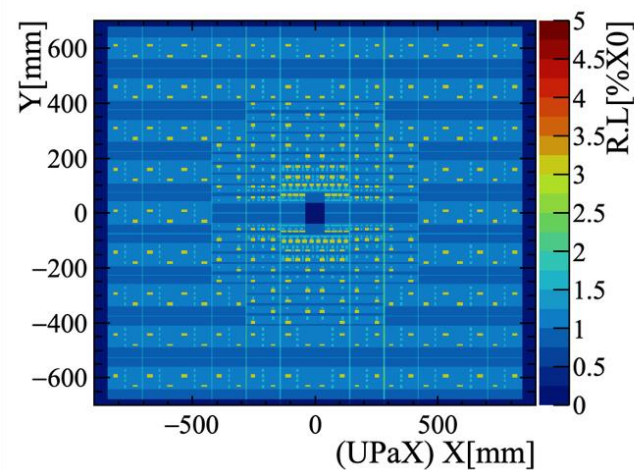
Generate hits for Gap



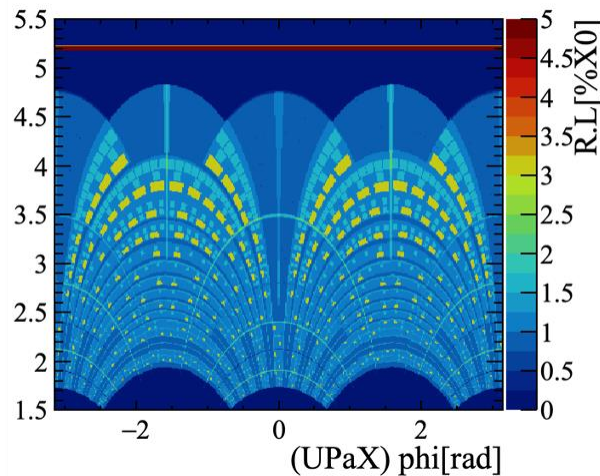
$L=1.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$

➤ Material Budget

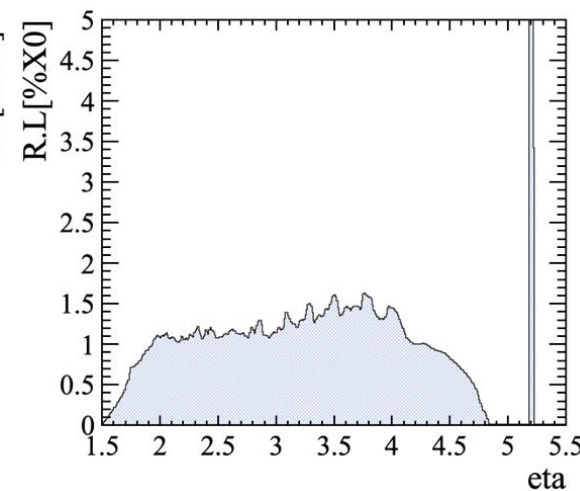
- Detector description has been developed both in **DetDesc** and **DD4hep** framework
- The material budget scan was performed in two frameworks with **consistent results**
 - Plot (a) and (b) illustrate the radiation length of the **first layer** of UP in both x/y and η/ϕ views
 - Plot (c) presents the projection map along the η axis
- A preliminary material budget estimate for **one layer** in the range $2 < \eta < 5$ is **1.2% X_0**
- A careful optimization of the material budget is still ongoing



2024/11/16 (a)



(b)



(c)

	Thickness [mm]	RL ($2 < \eta < 4.5$) [% X_0]
Pixel Sensor	0.200	0.24
<u>IpGBT</u>	1.250	0.07
<u>VTRx+</u>	4.000	0.13
<u>HybridFlex</u>	0.200	0.28
Kapton Tape	0.100	0.27
<u>BareStave</u>	4.000	0.21
One plane	-	1.20

➤ Occupancy distribution

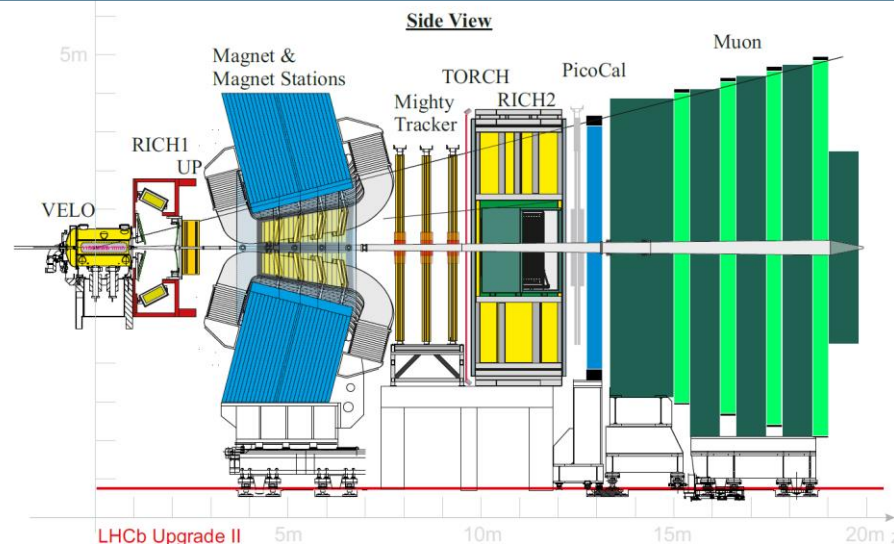
- The distribution of the occupancy rate for the most busy chip on each module
- In the most inner region, the highest occupancy is up to 0.26×10^{-2}

➤ Responding efficiency

- Particle response efficiency was treated as a function of particle momentum per layer compared with the current UT, both with efficiencies **around 95%**

➤ The UPDigits based on DD4hep is currently under developed





- UP detector modelling and the UP part of the **Upgrade II scoping document** is finished
- Simulation Study
 - The average hit densities per bunch crossing in p-p collisions is up to **~4.5 hits/cm²/BX**
 - In the most inner region, the highest occupancy is up to **0.26×10^{-2}**
 - The average material budget for one layer is **1.2% X_0**
- The LHCb Upgrade II is aiming for a TDR in 2026
- The UPDigits based on DD4hep is currently under developed



Thank you !