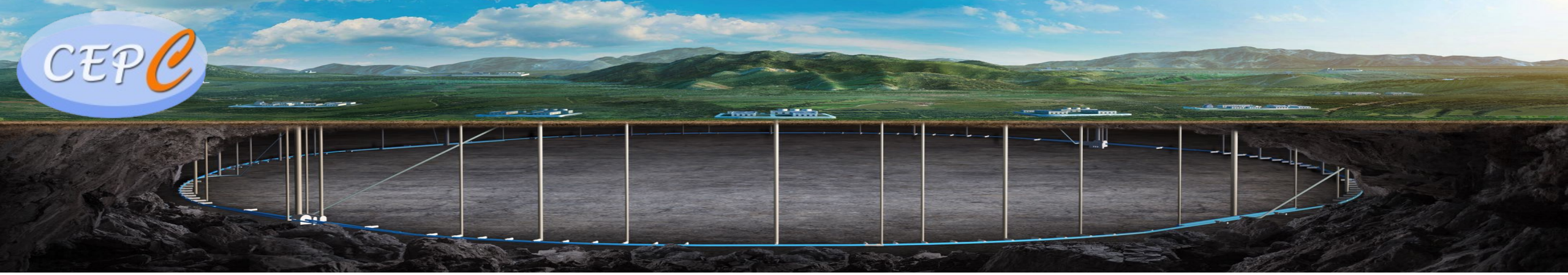

# CEPC vertex Detector

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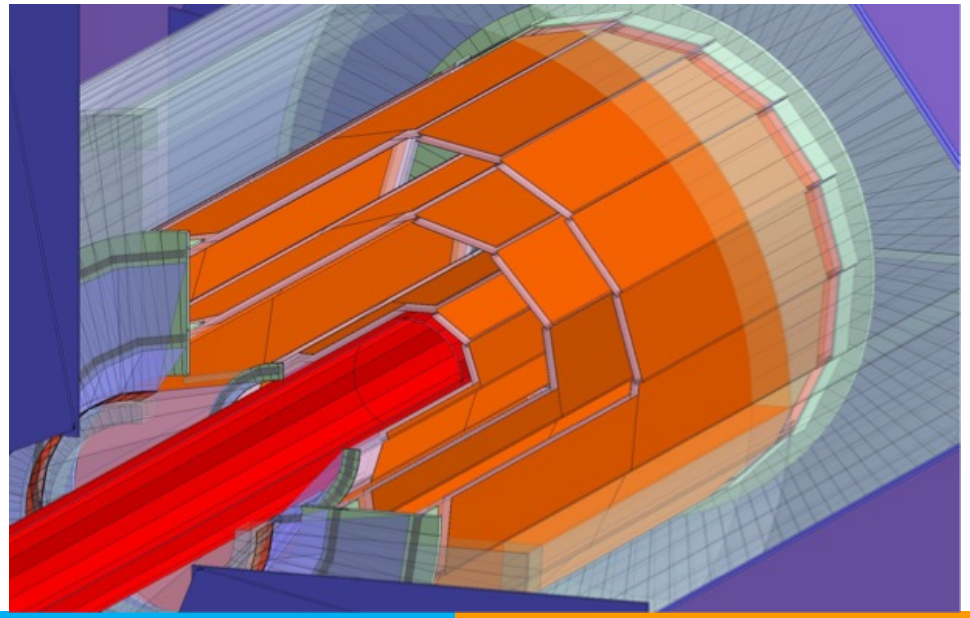
Institute of High Energy Physics
Chinese Academy of Sciences

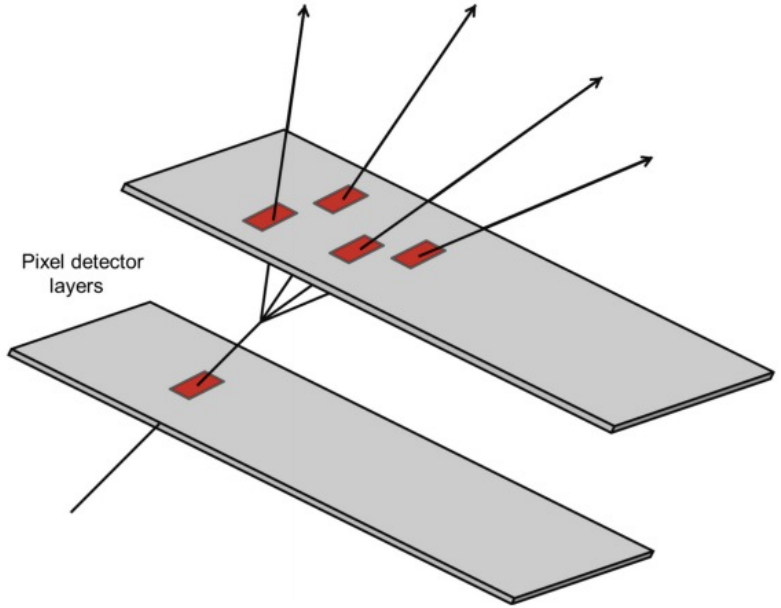
# Content

- Introduction
- Requirements
- Technology survey and our choices
- Technical challenges
- R&D efforts and results
- Detailed design including electronics, cooling and mechanics
- Readout electronics & BEC
- Performance from simulation
- Research team and working plan
- Summary

# Introduction: vertex detector

- Vertex detector optimized for first 10 year of operation (ZH, low lumi-Z )
- Motivation:
  - Aim to optimize impact parameter resolution and vertexing capability
  - Key detector for H → cc and H → gg physics, which is an important goal for CEPC





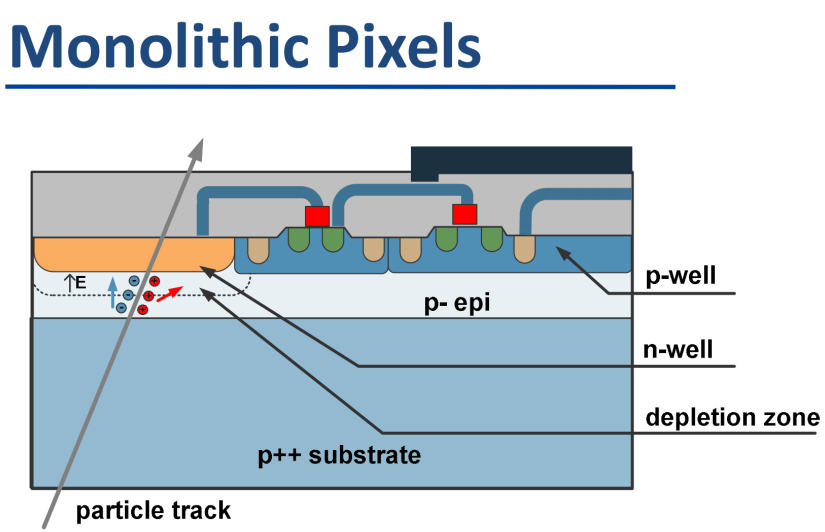
# Vertex Requirement

- Inner most layer (b-layer) need to be positioned as close to beam pipe as possible
  - **Challenges:** b-layer radius (11mm) is smaller compared with ALICE ITS3 (18mm)
- High data rate: (especially at Z pole , ~43MHz, 1Gbps per chip )
  - **Challenges**: 1Gbps per chip high data rate especially at Z pole
- Low material budget ( less than 0.15%X0 per layer)
- Detector Cooling with air cooling (power consumption<=40 $mW/cm^2$)
- Spatial Resolution (3-5 um)
- Radiation level (~1Mrad per year in average)

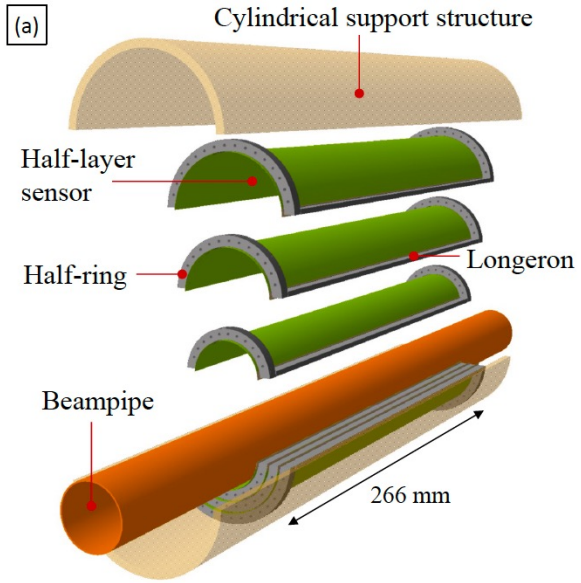
# Technology survey and our choices

- Vertex detector Technology selection
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design[1] )
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: Ladder design based on CMOS MAPS

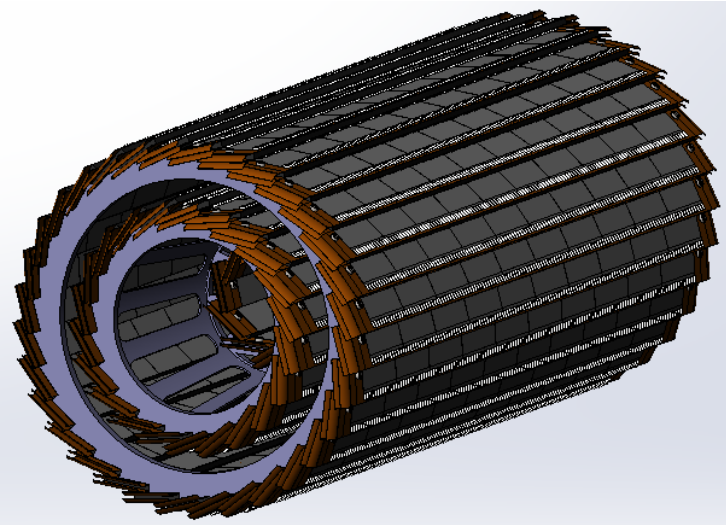
Monolithic active Pixel CMOS (MAPS)




Baseline: curved MAPS




Alternative: ladder based MAPS



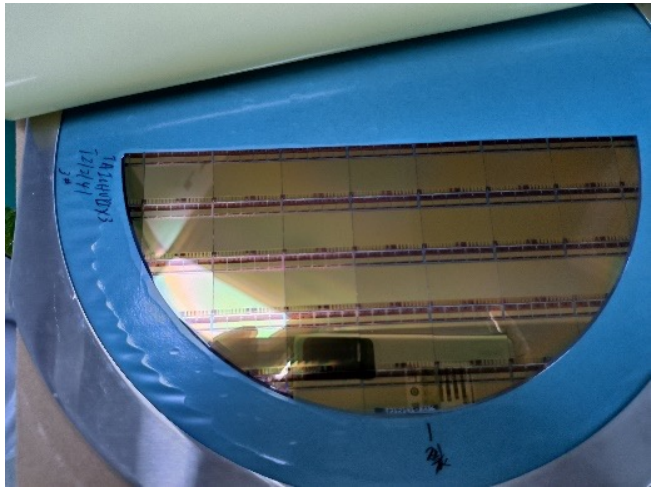
[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

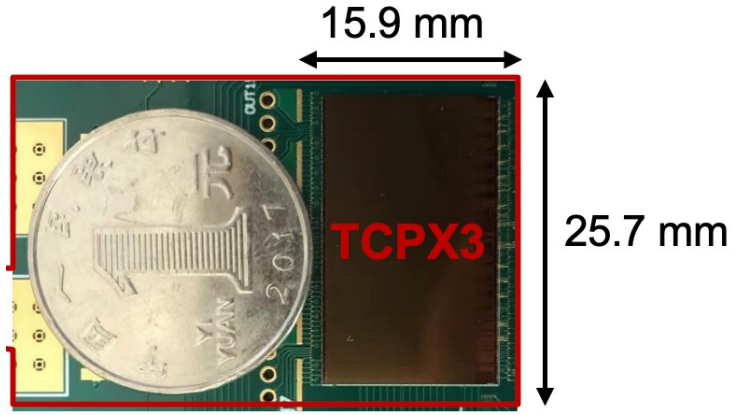
# R&D status and final goal

| Key technology | Status | CEPC Final goal |
|---|---|---|
| CMOS chip technology | Full-size chip with TJ 180nm CIS | 65nm CIS |
| Detector integration | Detector prototype with ladder design | Detector with bent silicon design |
| Spatial resolution | 4.9 μm | 3-5 μm |
| Detector cooling | Air cooling with 1% channels (24 chips) on | Air cooling with full power |
| Bent CMOS silicon | Bent Dummy wafer radius ~12mm | Bent final wafer with radius ~11mm |
| Stitching | 11×11cm stitched chip with Xfab 350nm CIS | 65nm CIS stitched sensor |

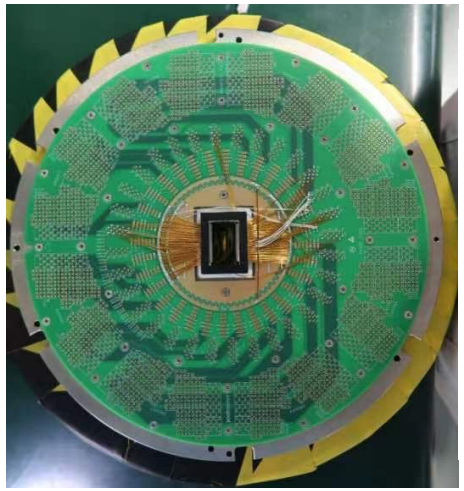
# R&D efforts: Full-size TaichuPix3

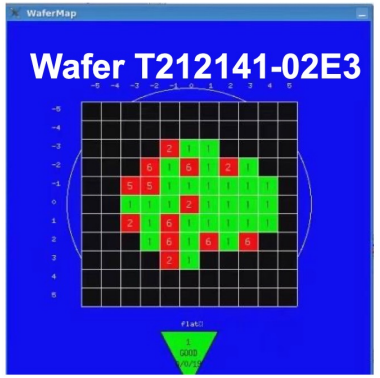
- Full size CMOS chip developed, 1st engineering run
  - 1024×512 Pixel array,  Chip Size：15.9×25.7mm
  - 25μm×25μm pixel size with  high spatial resolution
  - Process: Towerjazz 180nm CIS process
  - Fast digital readout to cope with ZH and Z runs (support 40MHz clock)





TaichuPix-3 chip vs. coin

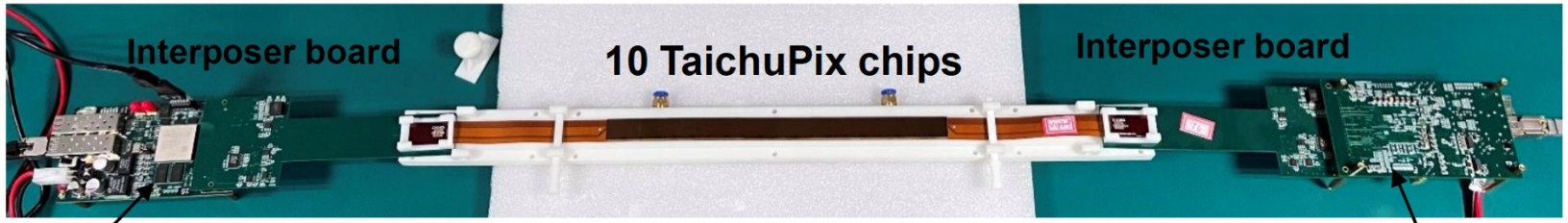




An example of wafer test result

| | Status | CEPC Final goal |
|---|---|---|
| CMOS chip technology | Full-size chip with TJ 180nm CIS | 65nm CIS |

# R&D effort: vertex detector prototype

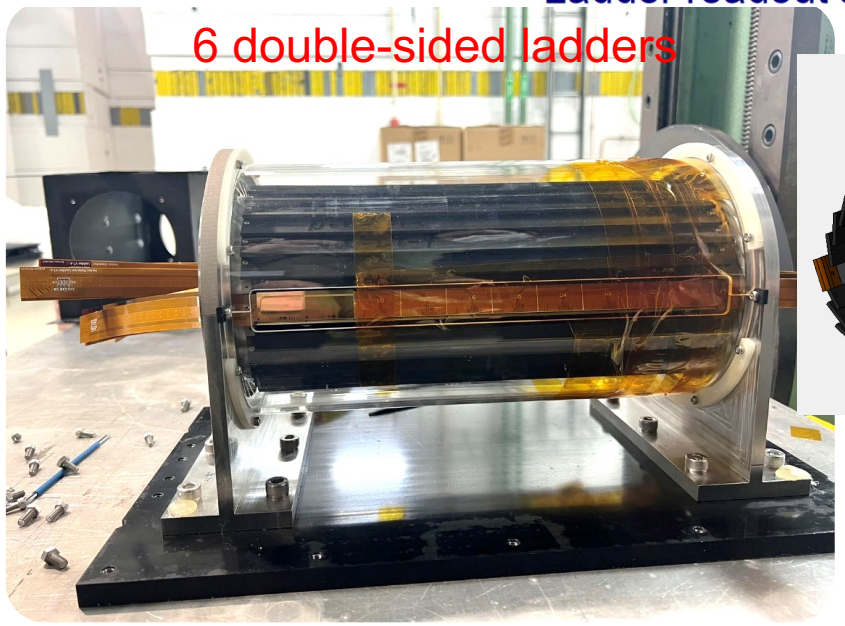


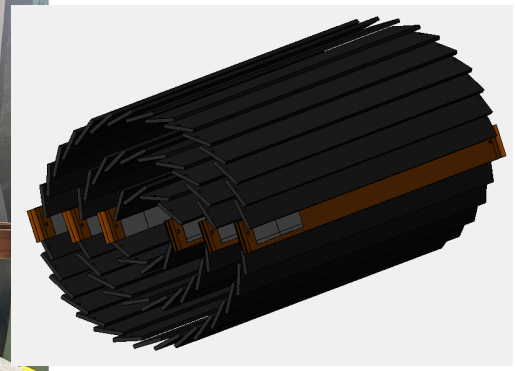

**TaichuPix**-based prototype detector tested at DESY in April 2023

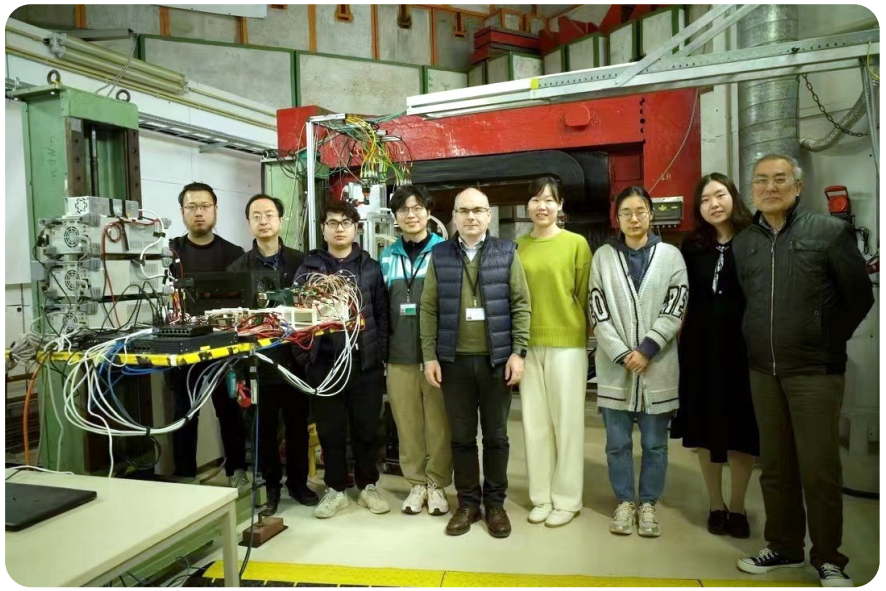
Spatial resolution ~ **4.9 μm**

Ladder readout system

6 double-sided ladders



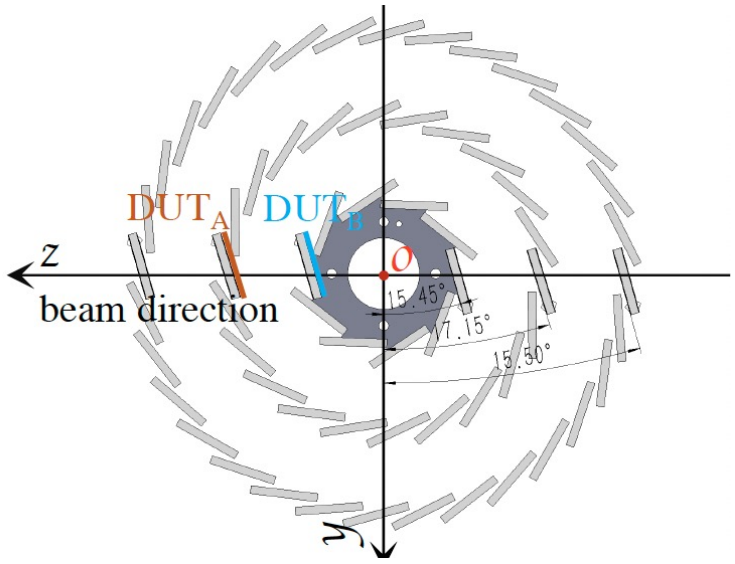


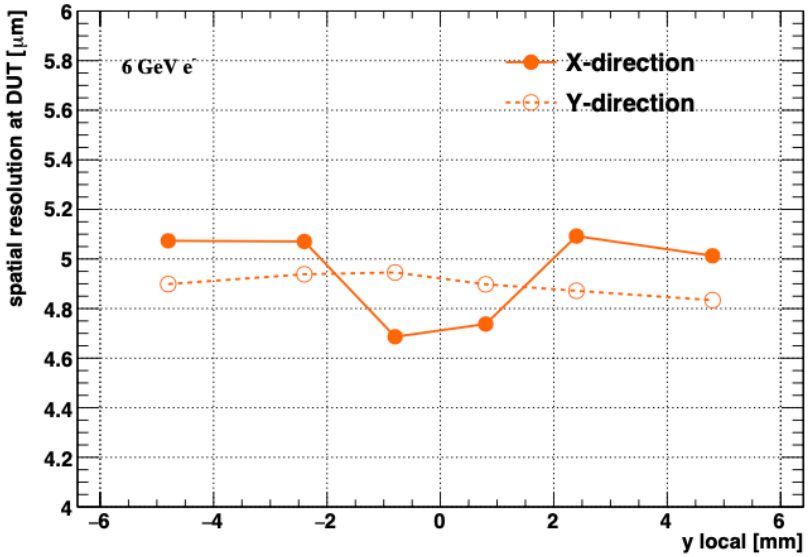


| | Status | CEPC Final goal |
|---|---|---|
| Detector integration | Detector prototype with ladder design | Detector with bent silicon design |

# R&D efforts and results: vertex detector prototype beam test

Spatial resolution ~ **5 μm**

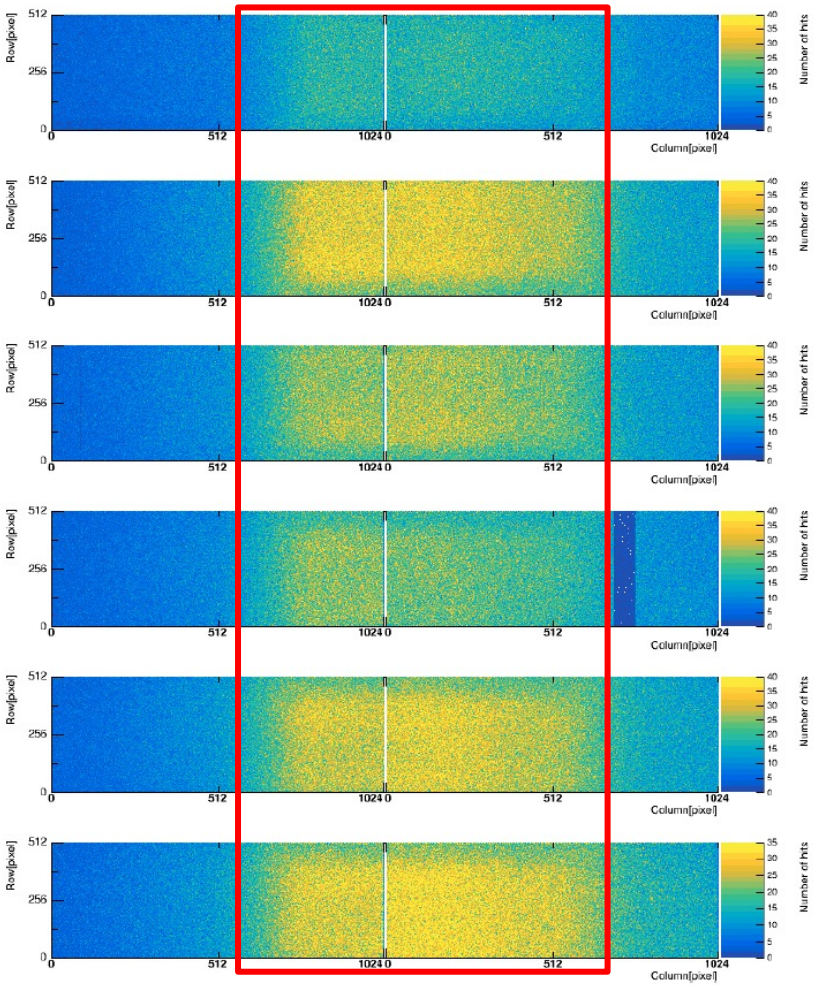



| | Status | CEPC Final goal |
|---|---|---|
| Spatial resolution | 4.9 μm | 3-5 μm |

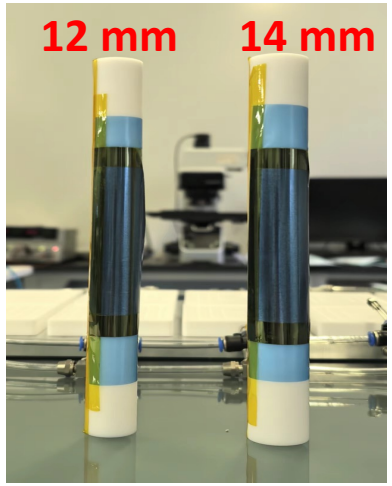
Hit maps of multiple layers of vertex detector

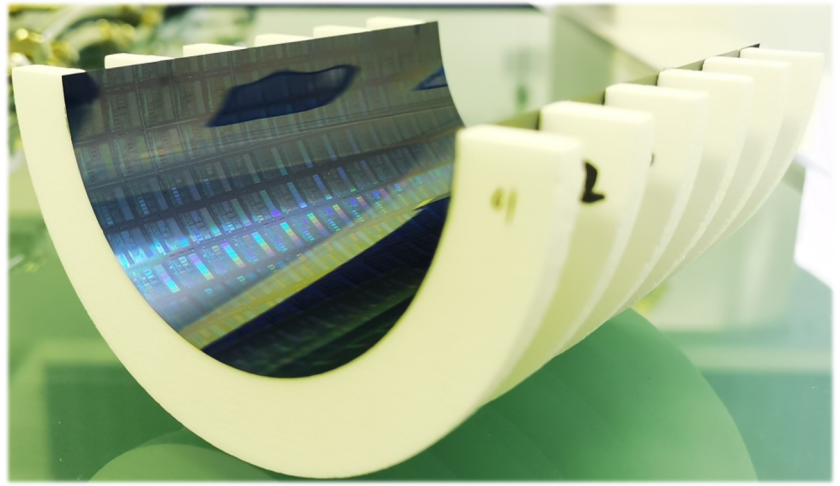
Beam spot



# R&D efforts curved MAPS

- CEPC b-layer radius (11mm) smaller compared with ALICE ITS3 (radius=18mm)
- Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12mm
  - The dummy wafer has been thinned to 40μm

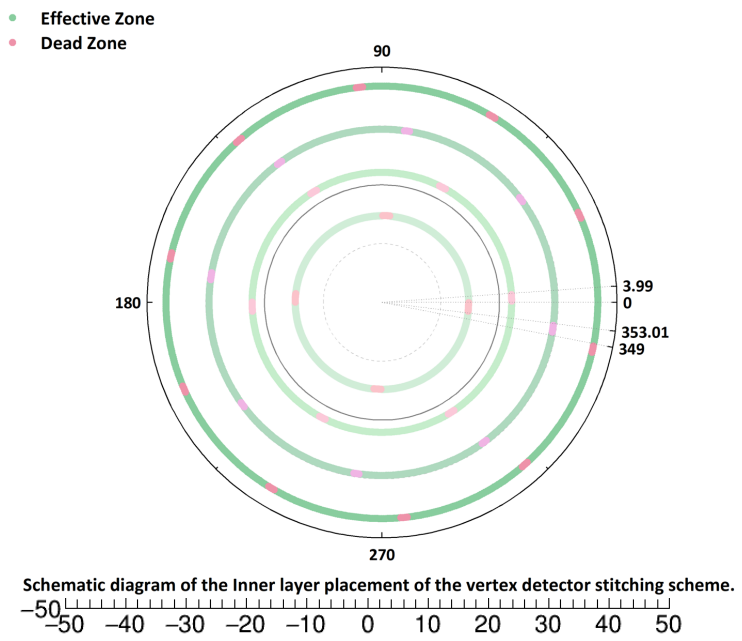


| | Status | CEPC Final goal |
|---|---|---|
| Bent silicon with radius | Bent Dummy wafer radius ~12mm | Bent final wafer with radius ~11mm |

# baseline: bent MAPS

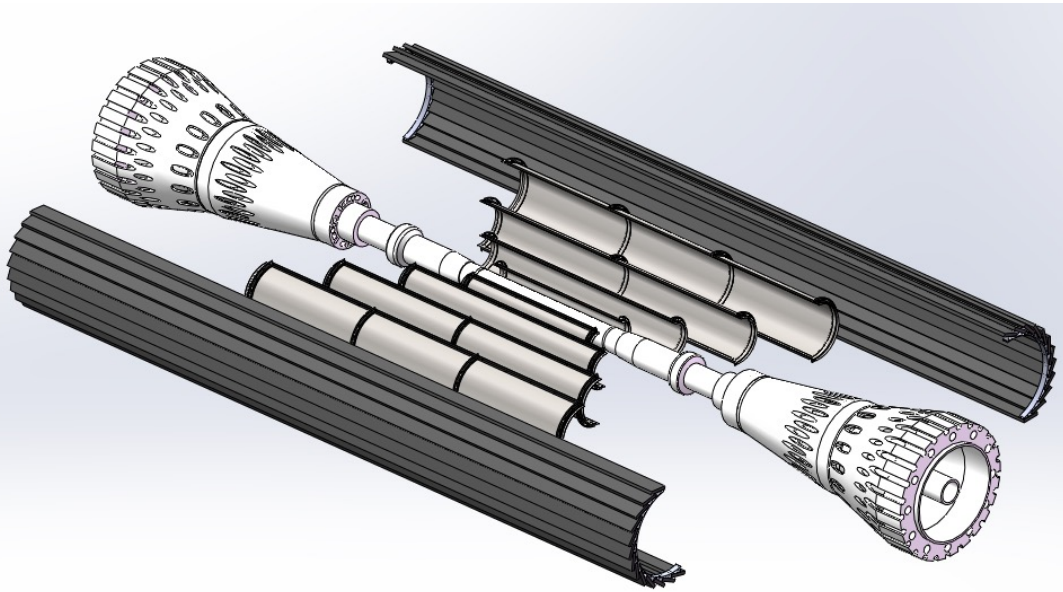
- 4 single layer of bent MAPS + 1 double layer ladder
  - Material budget is much lower than alternative option
- Use single bent MAPS for Inner layer (~0.15m$^2$)
  - Low material budget 0.06%X0 per layer
  - Different rotation angle in each layer to reduce dead area

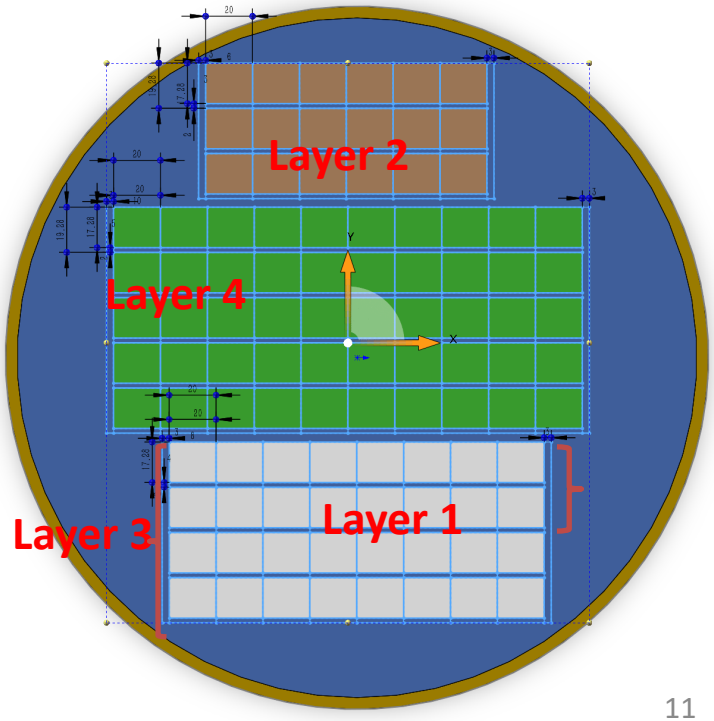


Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.

Long barrel layout (no endcap disk)
to cover cos θ<=0.991

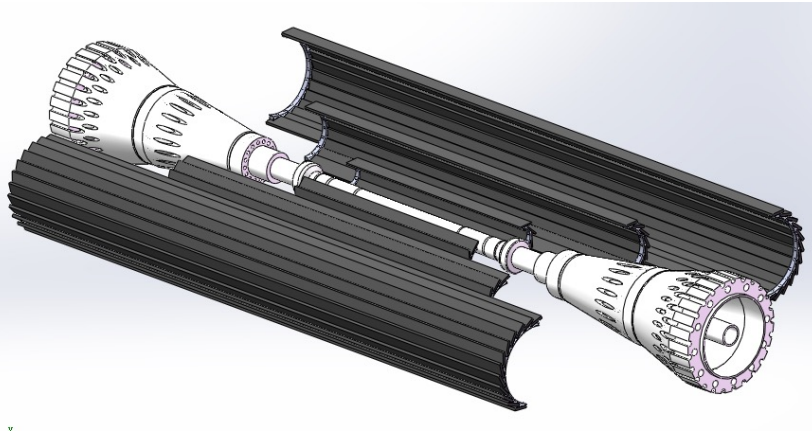
| layer | Radius | Material |
|---|---|---|
| Layer 1 | 11mm | 0.06% X0 |
| Layer 2 | 16.5mm | 0.06% X0 |
| Layer 3 | 22mm | 0.06% X0 |
| Layer 4 | 27.5mm | 0.06% X0 |
| Layer 5/6 (Ladders) | 35-40 mm | 0.33% X0 |
| Total | | 0.57% X0 |



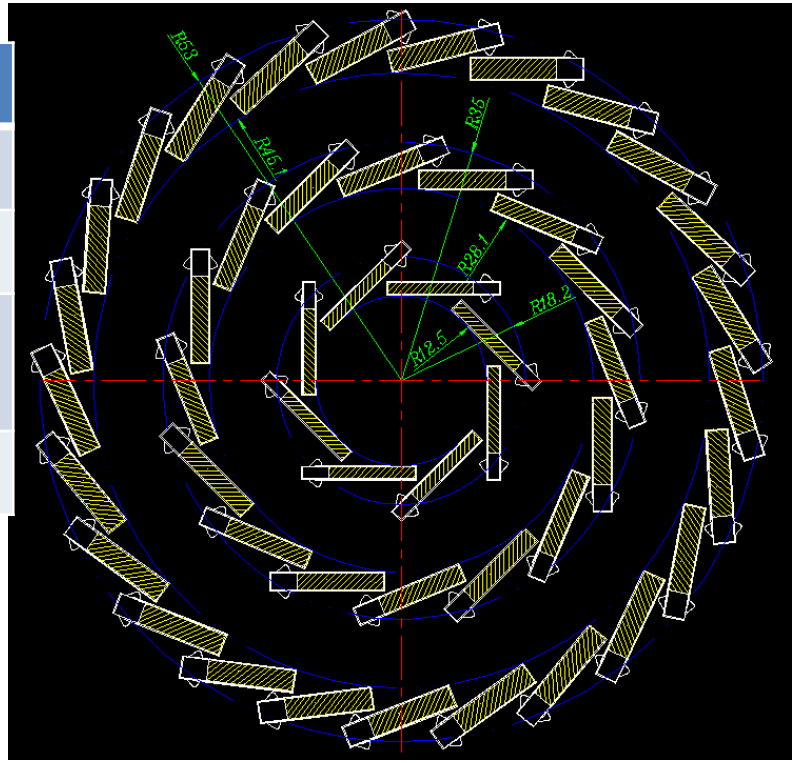


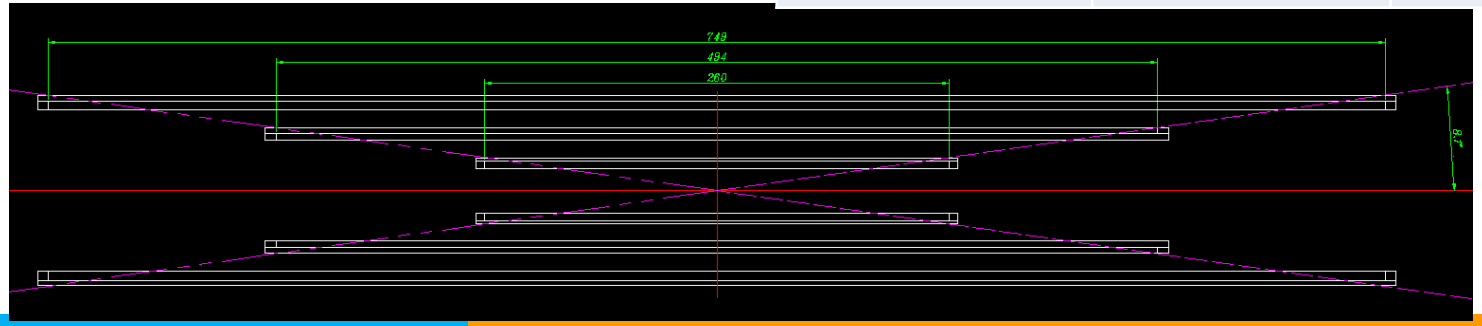
# Alternative： CMOS ladder

- Alternative: CMOS chips with a long ladder layout
  - 3 double-side layer with long ladders design
  - We have built a vertex prototype based on the short ladders design
  - No effective solution for inner layer cooling yet.



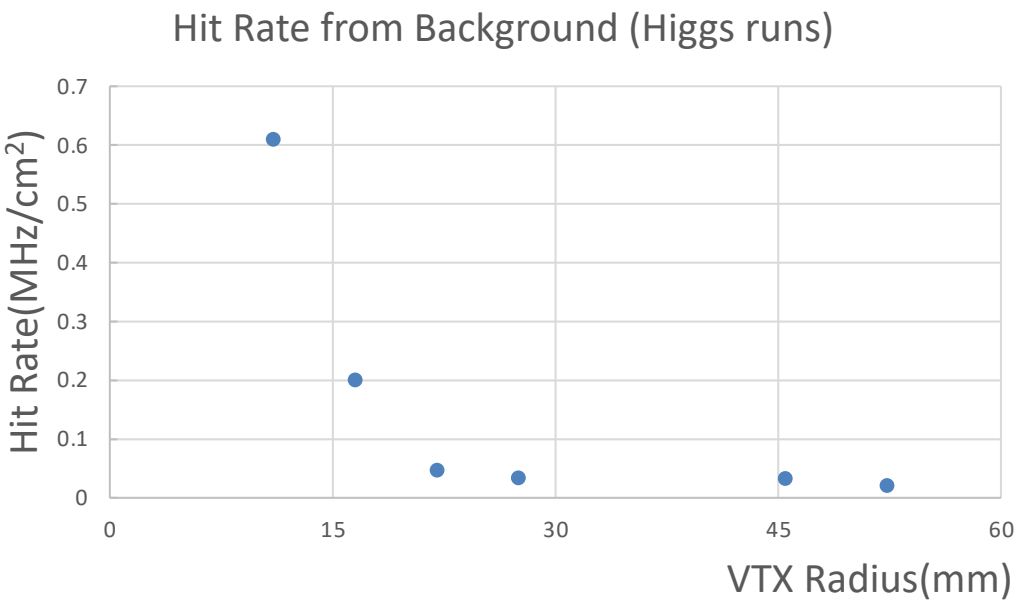
| layer | Radius | Material |
|---|---|---|
| Layer 1/2 | 12.5 -18 mm | ~0.33% X0 |
| Layer 3/4 | 28 - 35mm | ~0.33% X0 |
| Layer 5/6 (Ladders) | 45 - 53mm | ~0.33% X0 |
| Total | | ~1% X0 |



# Data rate estimation of vertex detector

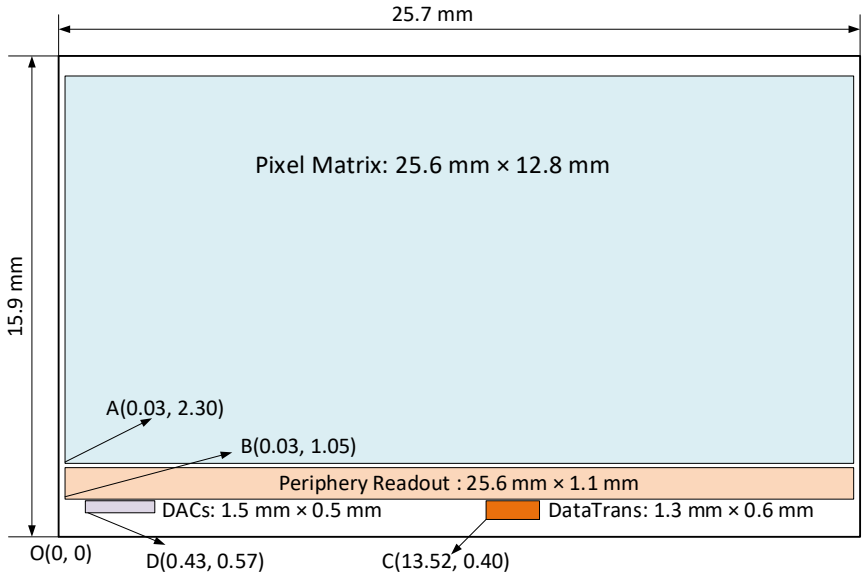
| | Hit rate ($MHz/cm^2$) | Data rate@triggerless (Gbps) | Data rate@trigger (Gbps) |
|---|---|---|---|
| Higgs | 0.61 | 0.18 | <0.01 |
| W | 3.16 | 0.98 | <0.01 |
| Low lumi Z pole | 3.9 | 1.2 | ~0.1 |




- Data rate is dominated by background from pair production
  - Estimated based on old version of software
  - More details in Haoyu's MDI talk this afternoon
- WW runs and low Lumi Z runs (20% of high lumi Z)
- Data rate @1.2Gbps per chip for triggerless readout

# Chip design for ref- TDR and power consumption

- Power consumption
  - **Fast priority digital readout** for 40MHz at Z pole
  - 65/55nm CIS technology
  - Power consumption can reduced to ~40mW/cm$^2$
- Air cooling feasibility study
  - Baseline layout can be cooled down to ~20 ℃
    - Based on 3 m/s air speed, estimated by thermal simulation




| | Matrix | Periphery | DataTrans. | DACs | Total Power | Power density |
|---|---|---|---|---|---|---|
| TaiChu3 180nm chip @ triggerless | 304 mW | 135 mW | 206 mW | 10 mW | 655 mW | 160 mW/cm$^2$ |
| 65nm for TDR @ 1 Gbps/chip (TDR LowLumi Z ) | 60 mW | 80 mW | 36 mW | 10 mW | 186 mW | ~40 mW/cm$^2$ |

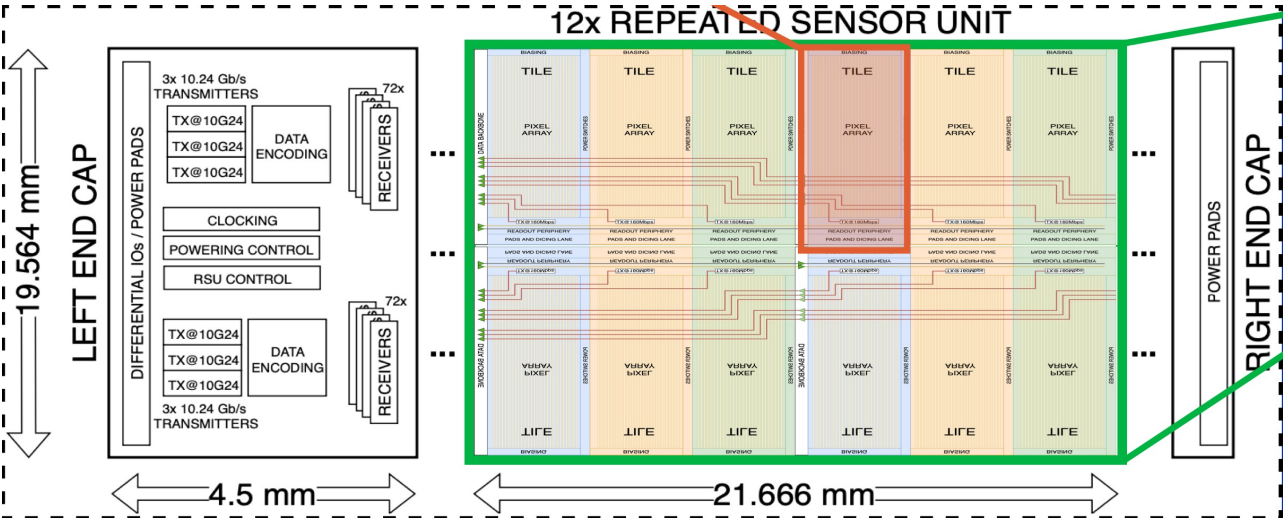
# Ladder Electronics

– Baseline: stitching and RDL metal layer on wafer to replace PCB

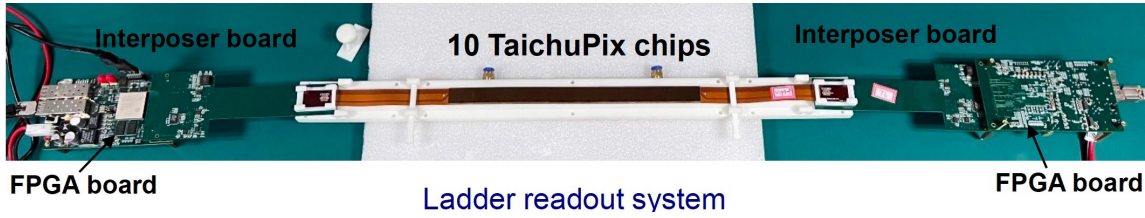
– Alternative: flexible PCB

- Signal, clock, control, power, ground will be handled by control board through flexible PCB

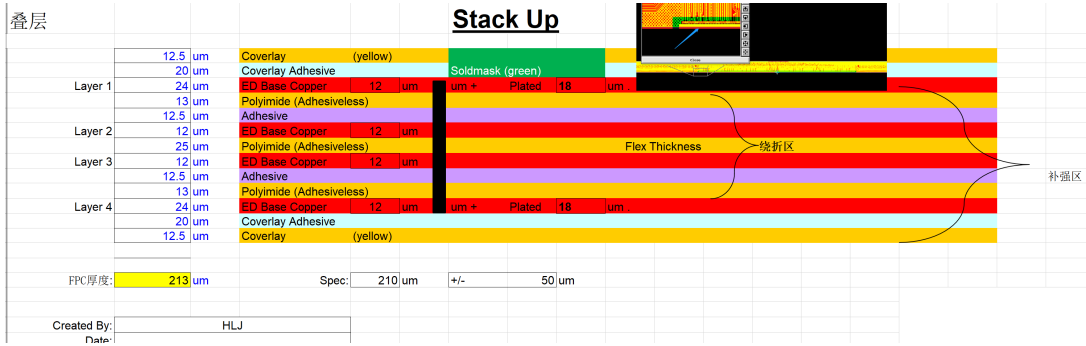
Baseline: ALICE ITS3 like stitching




Alternative: flexible PCB



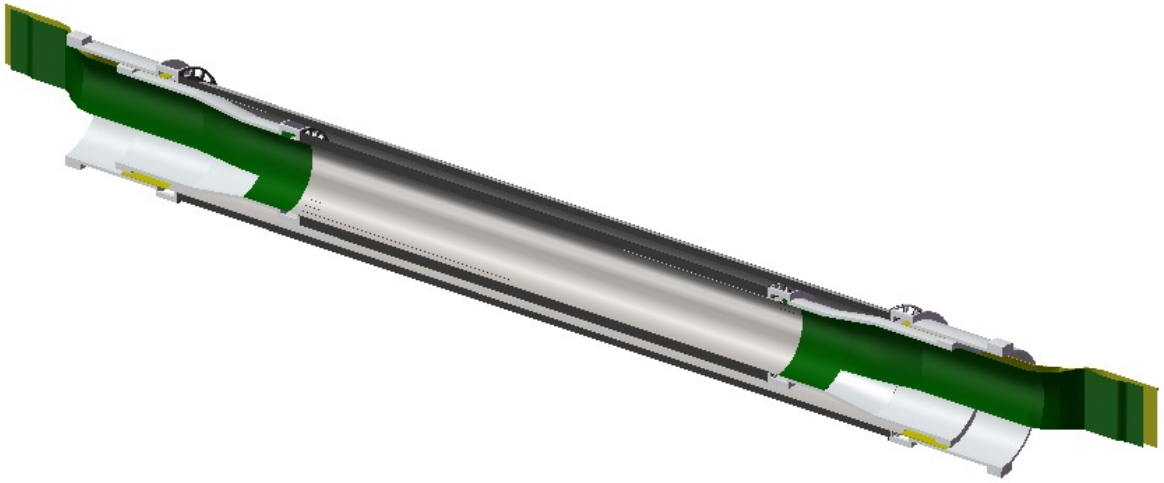

Ladder readout system

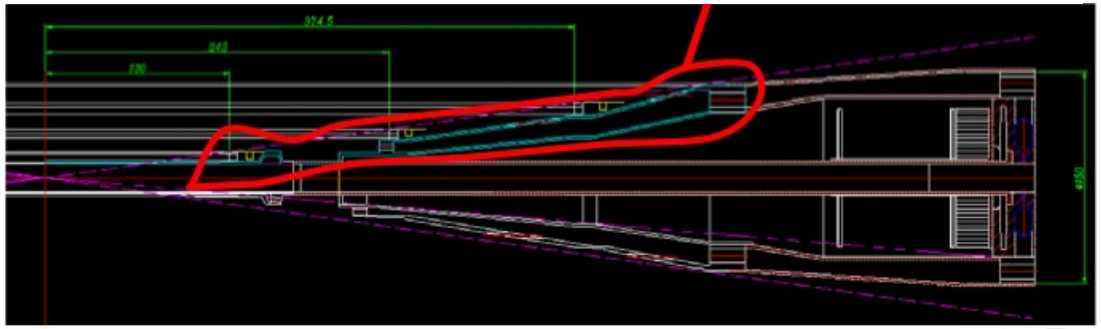


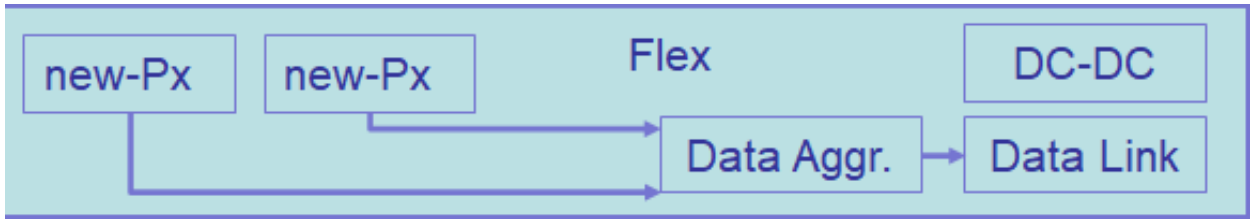

[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

# Vertex technologies: Cables and services

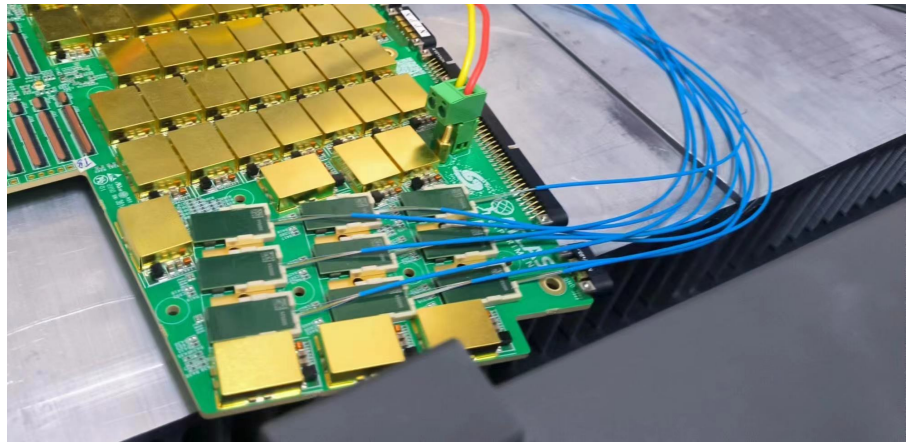
- Limited space in the MDI region for cables and services
  - Utilizes DC-DC powering; MAPS silicon substrate requires a common negative bias
  - Signal are transmitted through a flexible PCB and then converted to optical fiber.







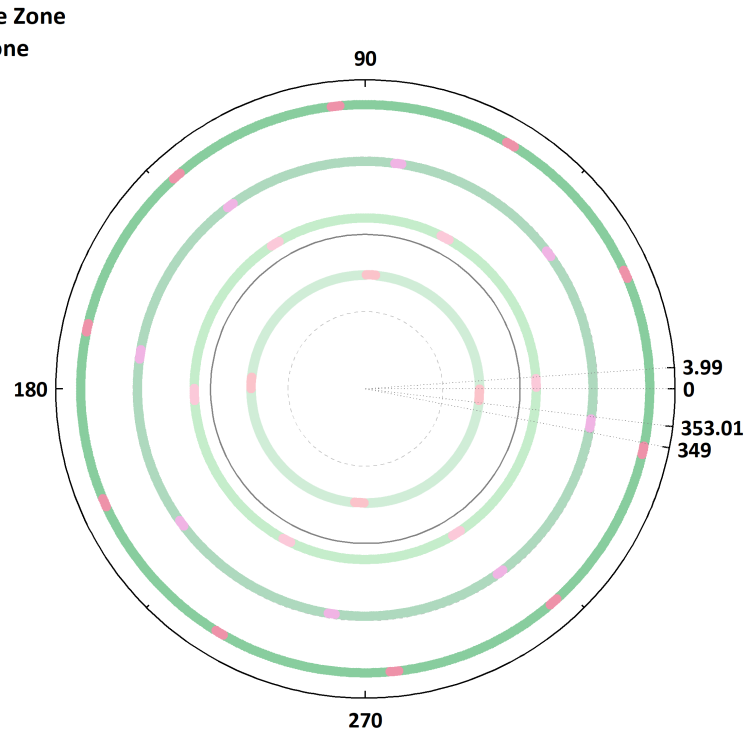

Example from ATLAS HGTD upgrade



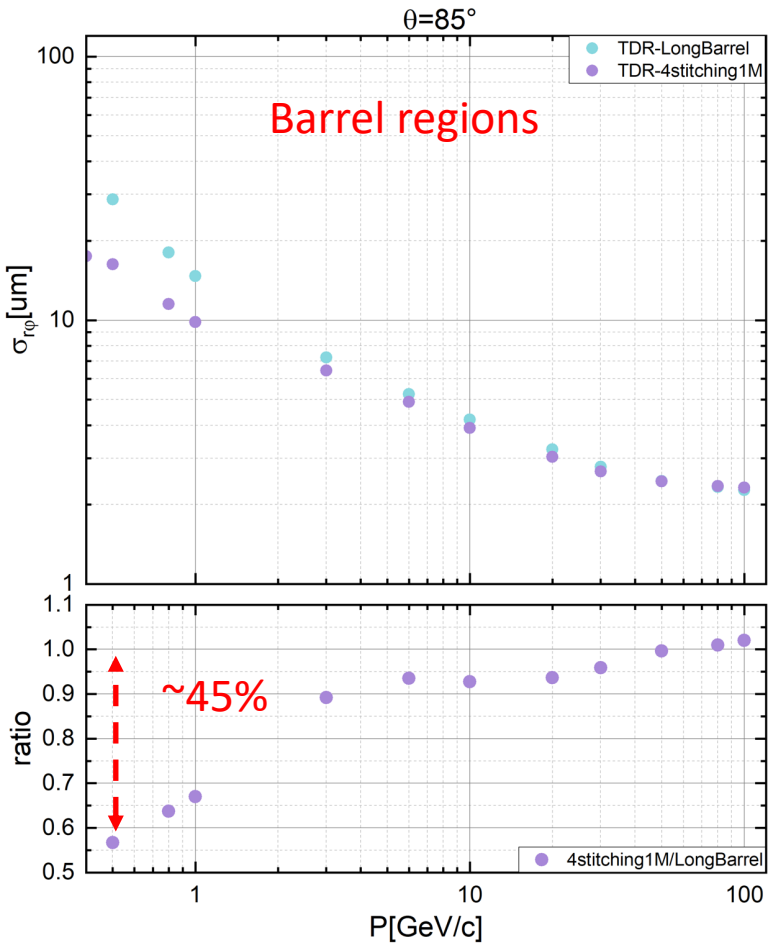
# Performance: impact parameter resolution

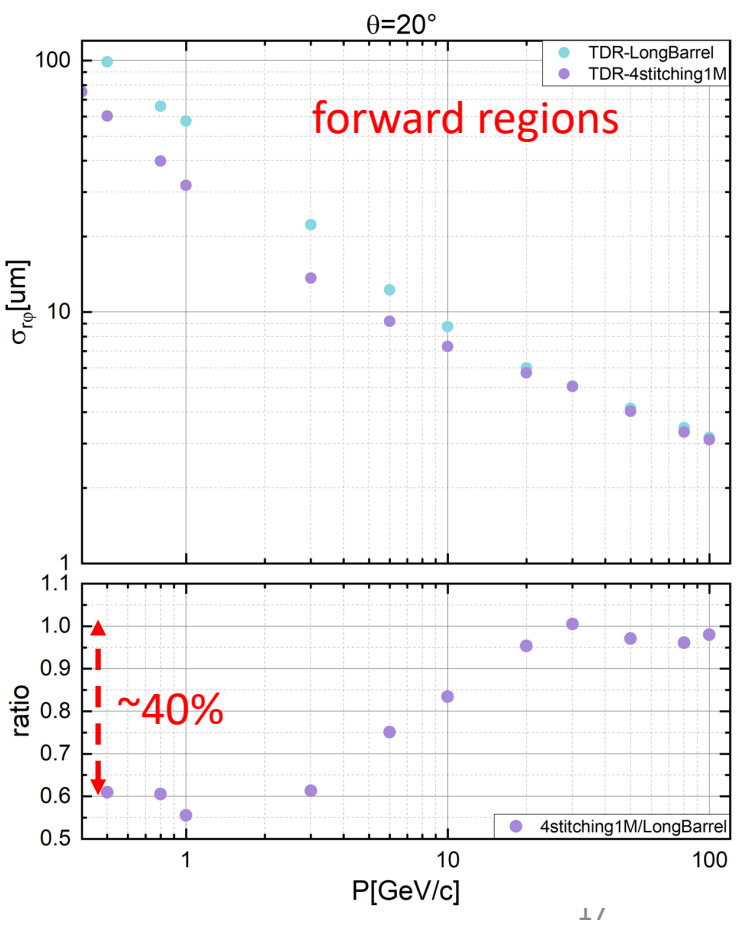
- Compared to alternative (ladder) option
  - baseline (stitching) has significant improvement (~45%) in low momentum case

Different rotation angle in each layer to reduce dead area




Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.



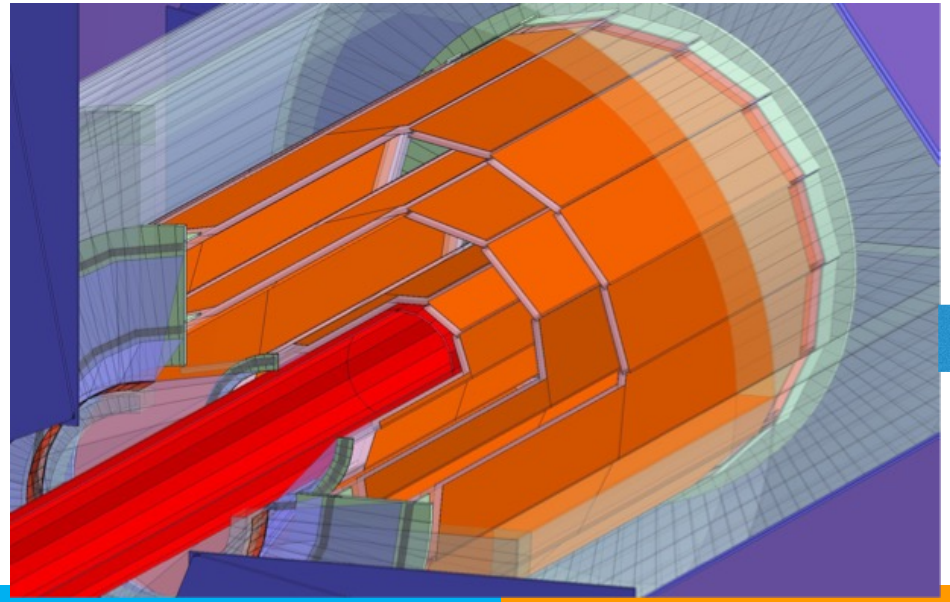
# Research team

- IHEP: Joao Costa, et al, 15 faculty, 5 postdoc, 6 students
  - CEPC vertex prototype, X-ray camera, ATLAS ITK strip and HGTD upgrade
- IPHC/CNRS: Christine Hu et al (3 faculty)
  - CEPC Jadepix design, ALICE ITS3 upgrade (especially on MAPS design, stitching)
- IFAE: Chip design , Sebastian Grinstein et al (2 faculty)
  - CEPC Taichupix chip design, ATLAS ITK pixel and HGTD upgrade
- ShanDong U.: Stitching chip design (3 faculty, 1 postdoc, 3 students )
- CCNU: chip design, ladder assembly (3 faculty, 1 postdoc, 5 students )
- Northwestern Polytechnical U. : Chip design (5 faculty, 2 postdoc, 5 students )
- Nanchang U. : chip design, (1 faculty, 1 students)
- Nanjing: irradiation study, chip design : (2 faculty, 4 students)
- Total : 36 faculty, 9 postdoc, 26 students

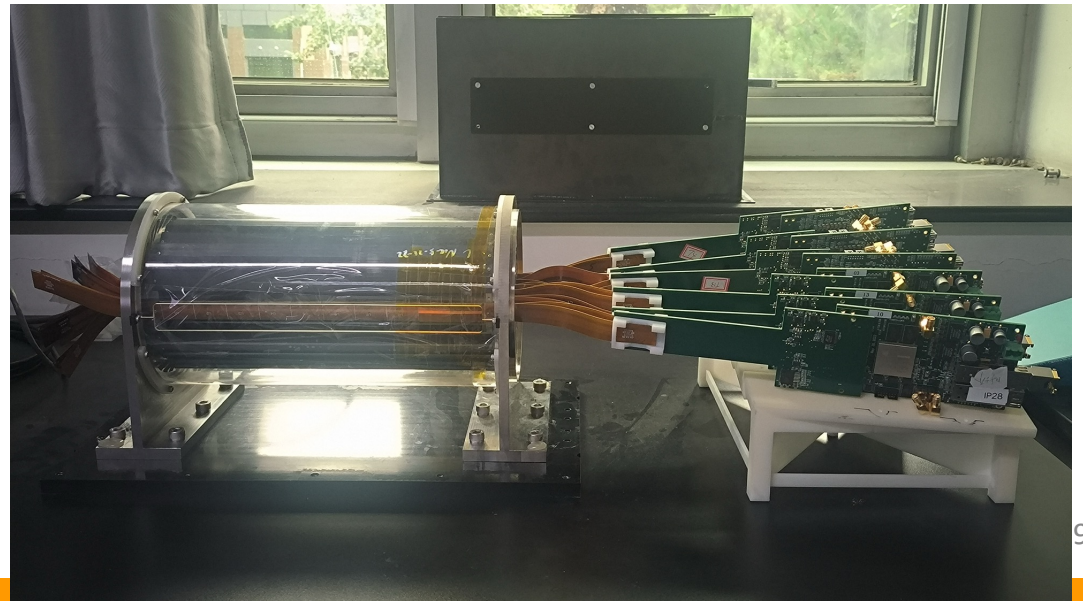
# Summary

- 1st full-size Prototype based the ladder design for CEPC vertex detector has been developed
- The Curved MAPS option has been chosen as baseline for the reference detector TDR.
- We active expanding international collaboration and explore synergies with other projects
  - We are members of ECFA DRD3 collaboration (solid state detectors)

**CEPC vertex conceptional design (2016)**



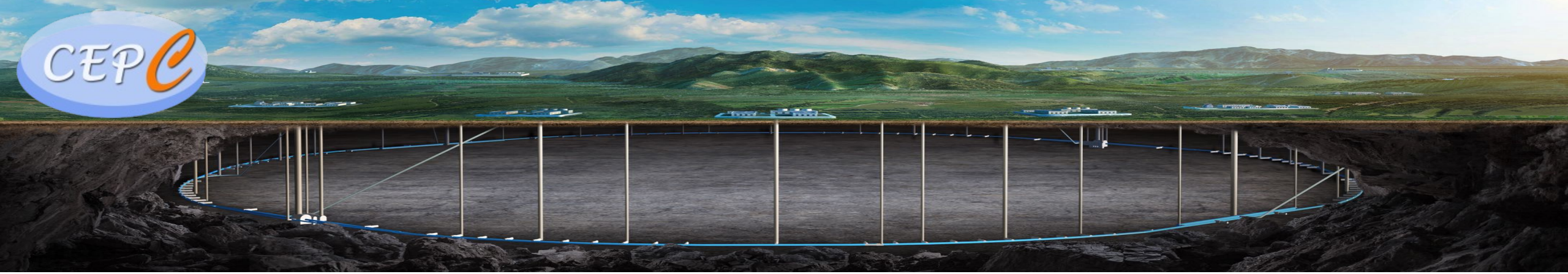
**CEPC vertex prototype (2023)**



# Summary: working plan

- CEPC vertex detector timeline is about 3-4 years after AlICE ITS3 upgrade
  - It will benefit from experience from AlICE ITS3 upgrade

| | CEPC Final goal | CEPC Expected date | AlICE ITS3 schedule |
|---|---|---|---|
| CMOS chip technology | 65nm CIS | 2028<br>Full-size 65nm chip | 2025 |
| Spatial resolution | 3-5 μm with final chip | 2028 | 2025 |
| Stitching | 65nm CIS stitched sensor | 2029 | 2026<br>wafer production |
| Bent silicon with small radius | Bent final wafer with radius ~11mm | 2030 | 2027 |
| Detector cooling | Air cooling with full power | 2027： thermal mockup | 2027 |
| Detector integration | Detector with bent silicon design | 2032 | 2028 |



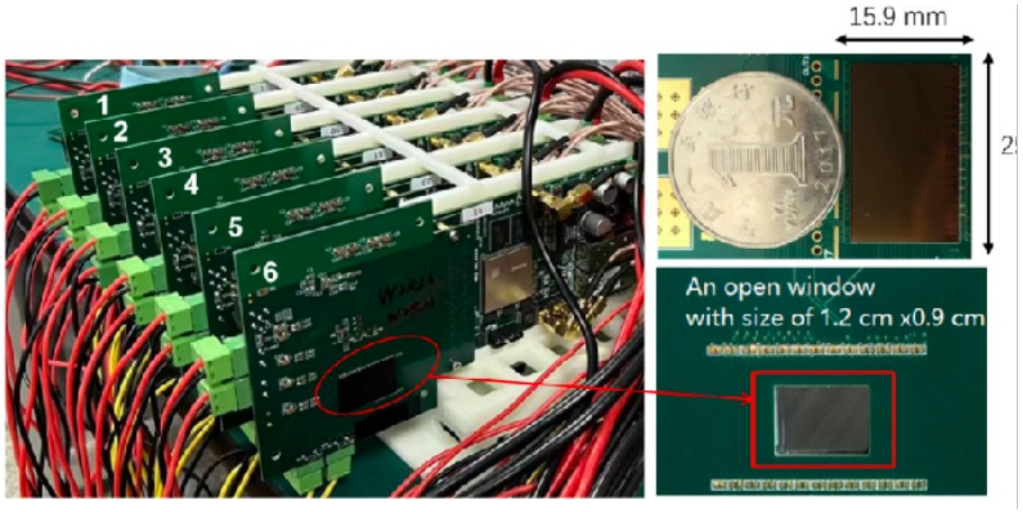

# Thank you for your attention!

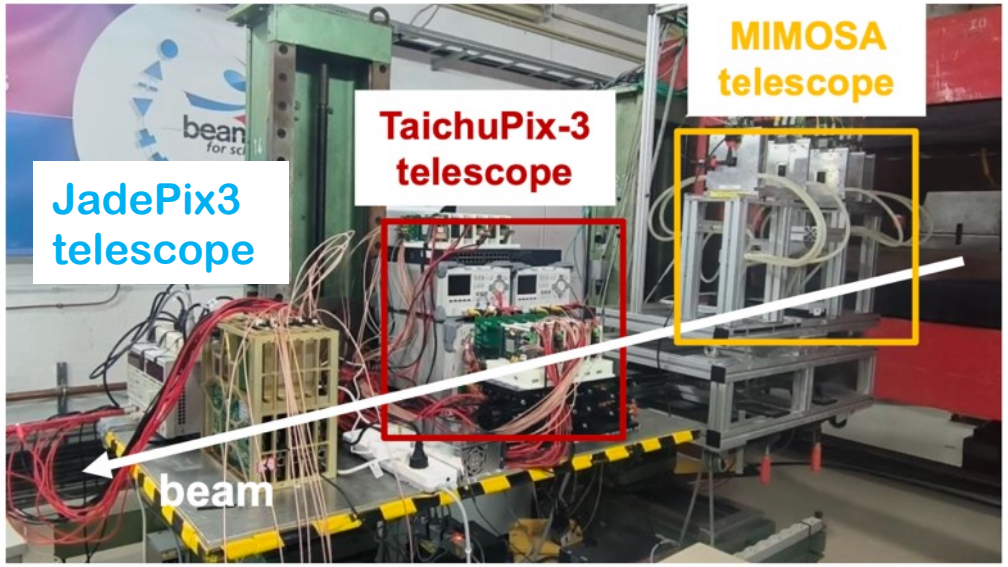
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

# Action item from meeting with IDRC chair

- Total area and Timeline for ALICE ITS3, should compare with CEPC vertex
  - ALICE ITS3 timeline is about 3~4 years earlier
  - Total area of ALICE ITS3 uprade: 0.06 $m^2$,
  - Total area of CEPC curved MAPS layers in vertex detector : 0.15 $m^2$
- Material budget for normal ladders is too conservative ?( especially for carbon fiber )
  - Material for mu3E ladders has 0.1% X0 per layer (we quoted 0.25% X0 per layer in last meeting)
  - Ladder material now reduce from 0.25% to 0.16%X0 per layer
    - Metal layer of flexible PCB now reduced from 6 to 4 layers
  - Carbon fiber thickness in CEPC prototyping can reach 0.12mm,  on the same level as mu3e detector
- Accessibility for 65/55 nm technology in China
  - TowerJazz 65nm CIS can be submitted through TowerJazz agency in China
  - R & D of SMIC 55nm technology is on-going
- Serial powering is widely used in ATLAS/CMS upgrade, should look into it
  - DC-DC powering is preferred , MAPS silicon substrate needed a common negative bias

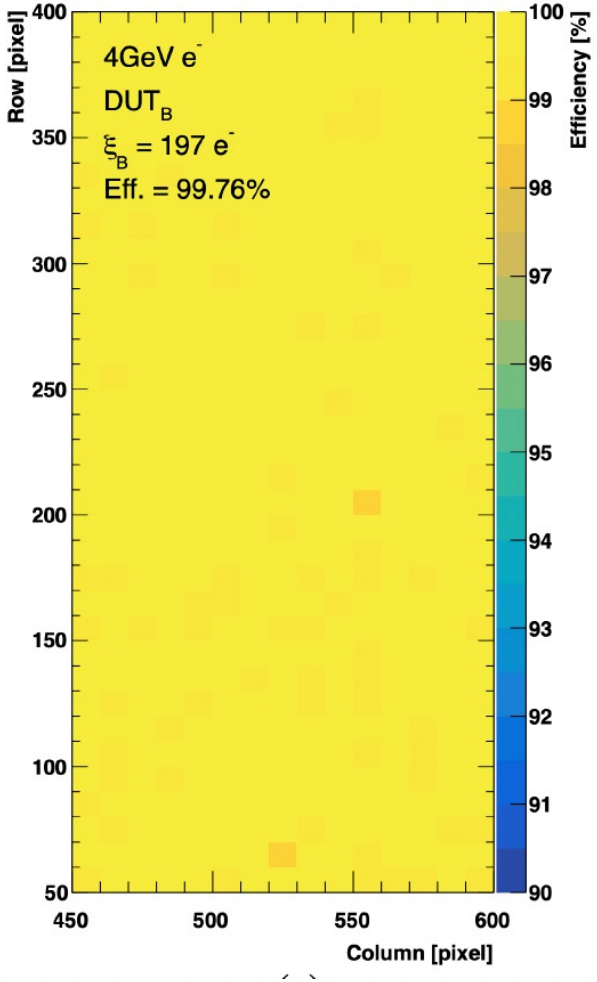
# R&D efforts and results: Jadepix3/TaichuPix3 beam test @ DESY



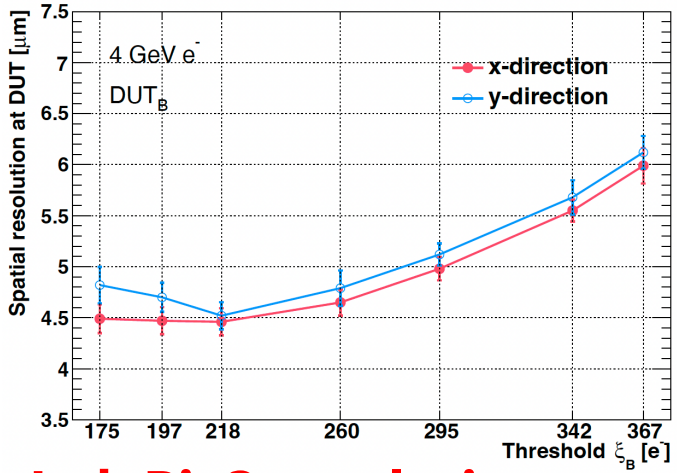




Spatial resolution 4~5um, Efficiency >99%

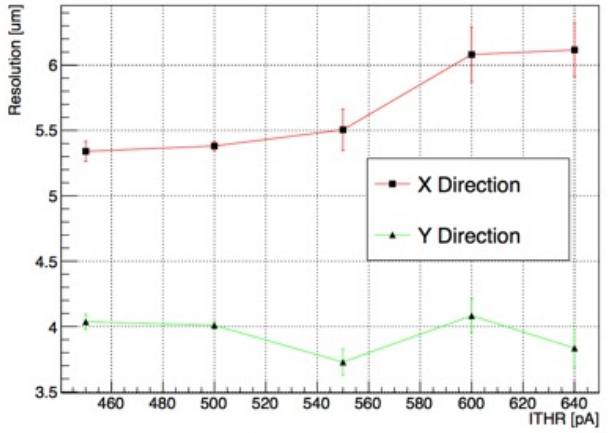
## TaichuPix3 efficiency




## TaichuPix3 resolution



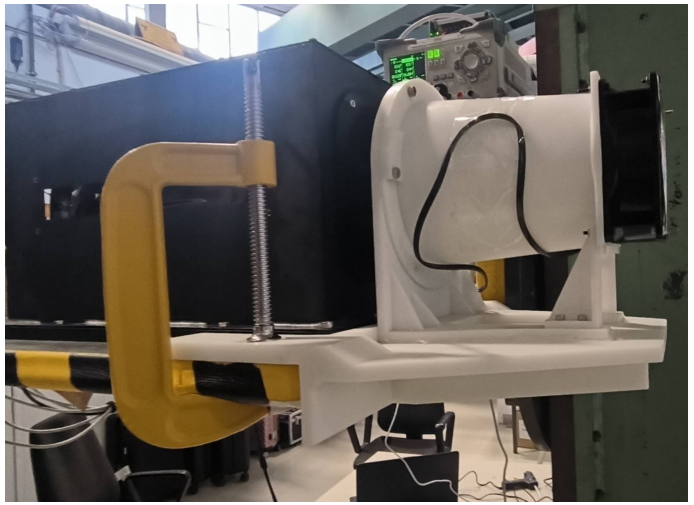

## JadePix3 resolution



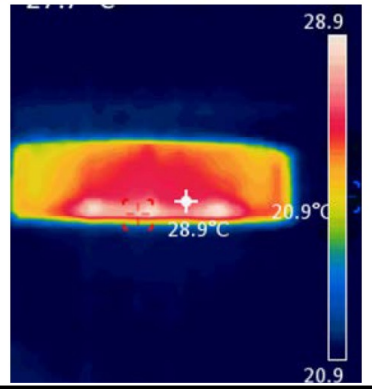

Collaboration with CNRS and IFAE in Jadepix/TaichuPix R & D

# R&D efforts: Air cooling in vertex prototype

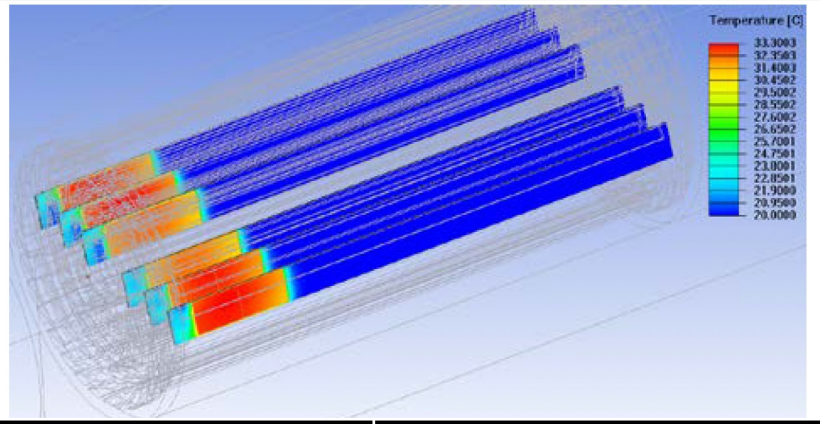
- Dedicated air cooling channel designed in prototype.
  - Measured Power Dissipation of Taichu chip: ~60 mW/cm$^2$ (17.5 MHz in testbeam)
  - Before (after ) turning on the cooling, chip temperature 41 °C (25 °C)
    - In good agreement to our cooling simulation
    - No visible vibration effect in spatial resolution when turning on the fan



Chip temperature under cooling during beam test: Max 28.9 ℃




Prototype cooling simulation： Max 33.3 ℃

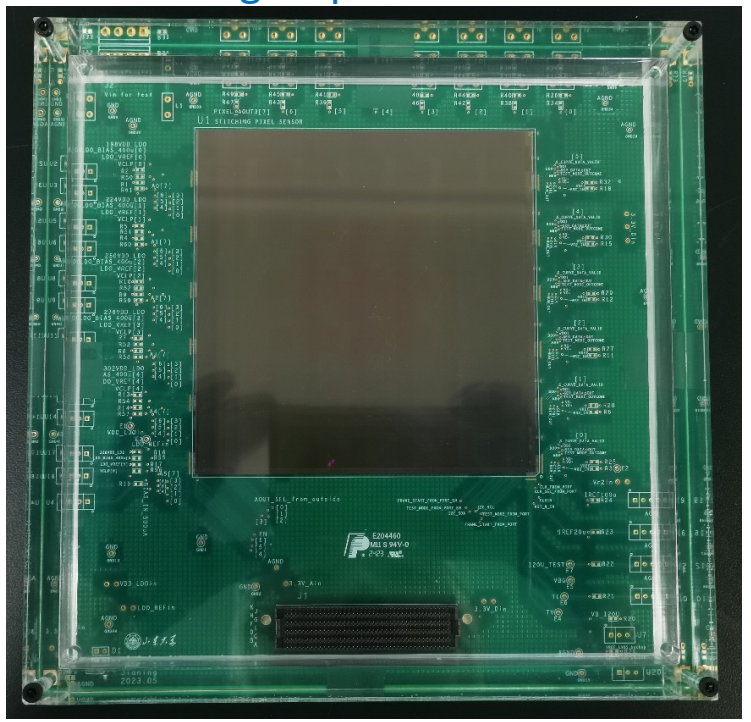


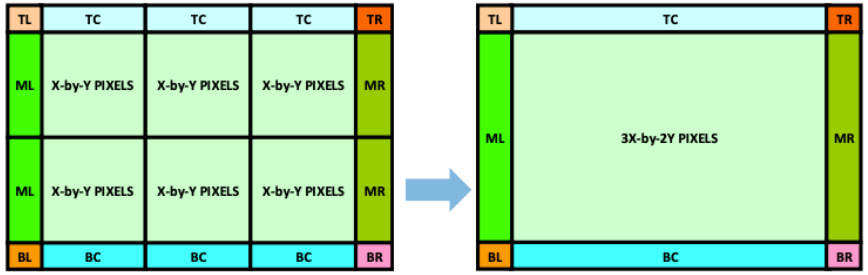

| Key technology | Status | CEPC Final goal |
|---|---|---|
| Detector cooling | Air cooling with 1% channels (24 chips) on | Air cooling with full power |

# R&D efforts and results: R & D for curved MAPS

- Stitching chip design (by ShanDong U.)
  - 350nm CIS technology Xfabs
  - Wafer level size after stitching ~11 ×11 cm$^2$
  - reticle size ~2 ×2 cm$^2$
  - 2D stitching
  - Engineering run, chip under testing

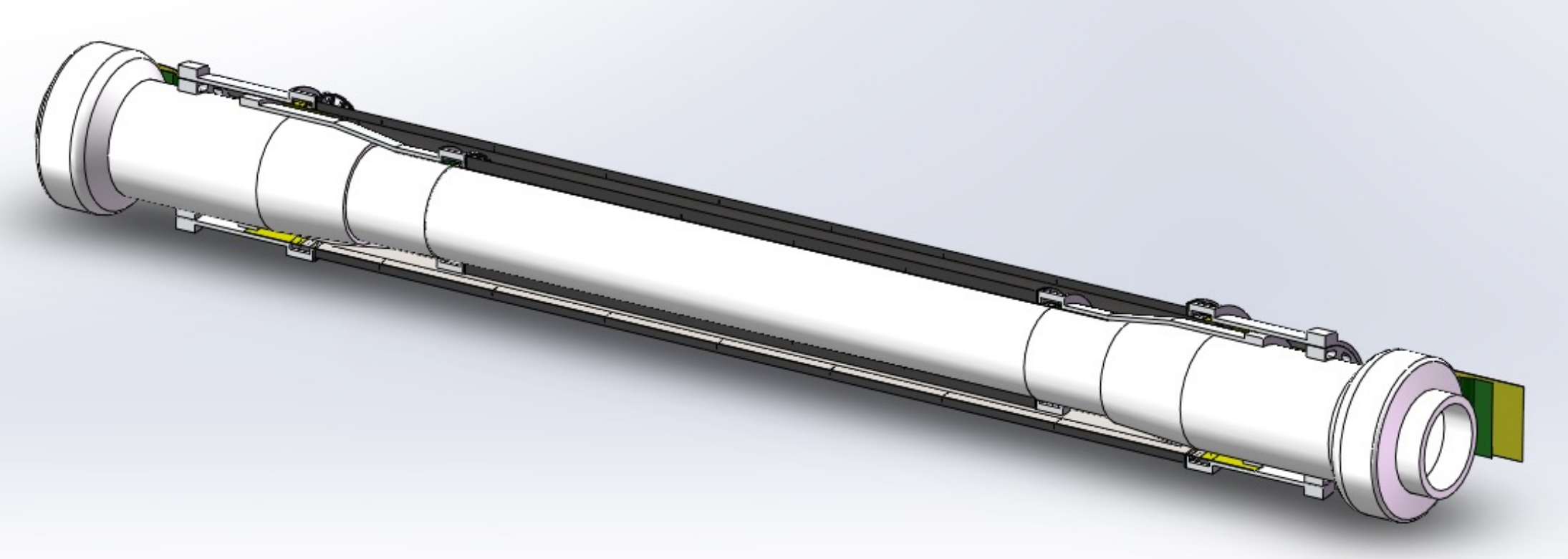
Stitching chip : 11 ×11 cm$^2$





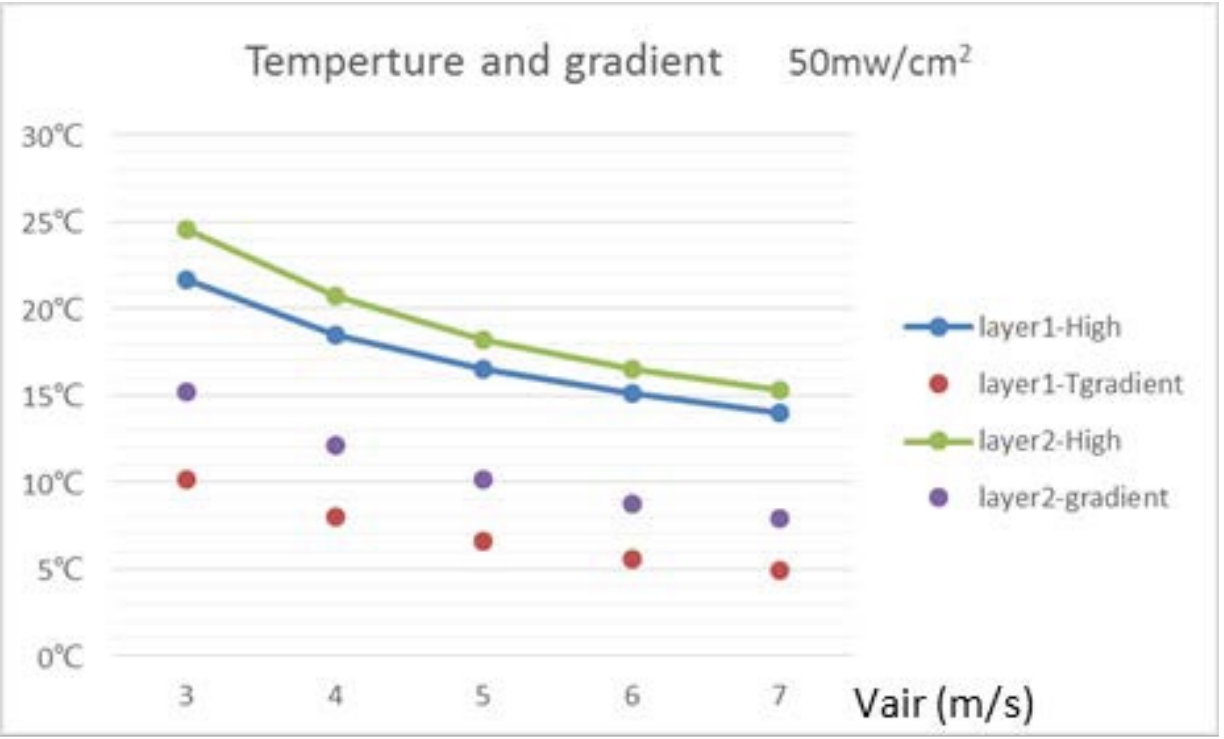

| Key technology | Status | CEPC Final goal |
|---|---|---|
| Stitching | 11*11cm stitched chip with Xfab 350nm CIS | 65nm CIS stitched sensor |

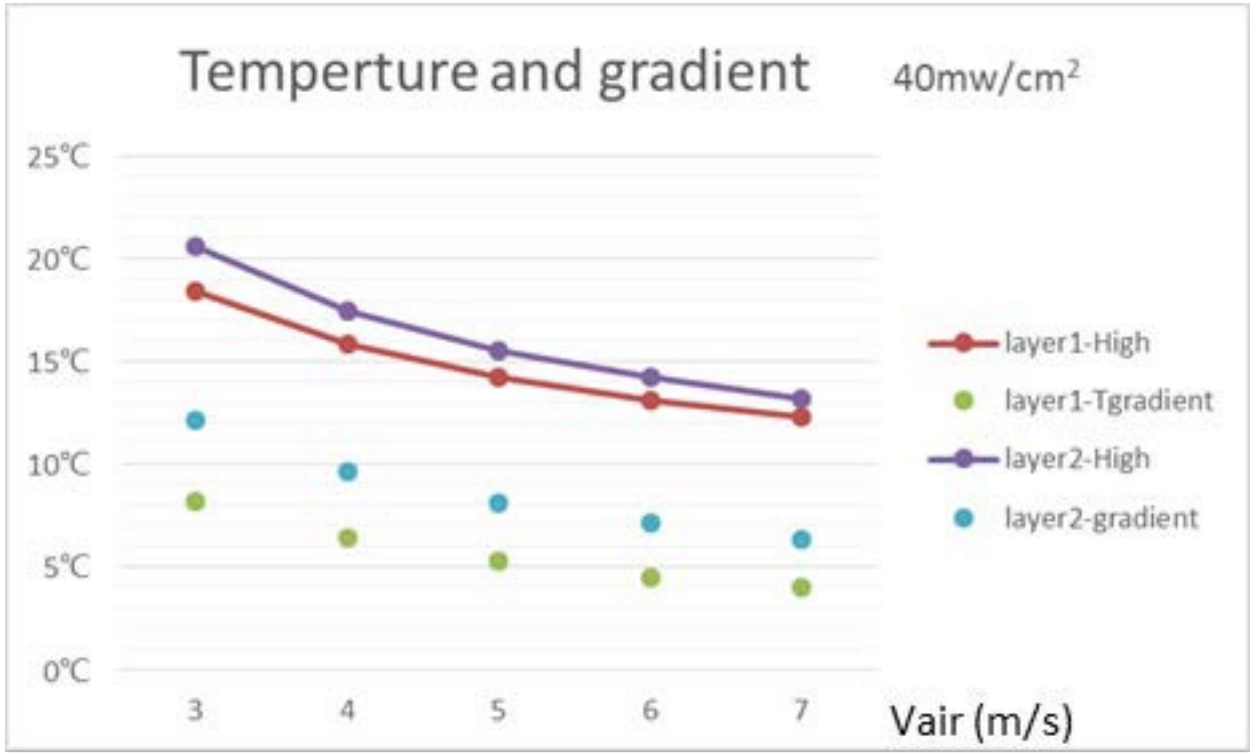
# Backup: Mechanics



# Backup : Cable and service

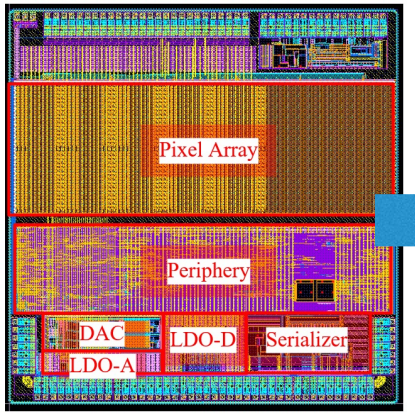
# Backup : air cooling simulation

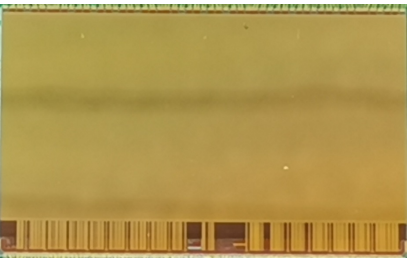


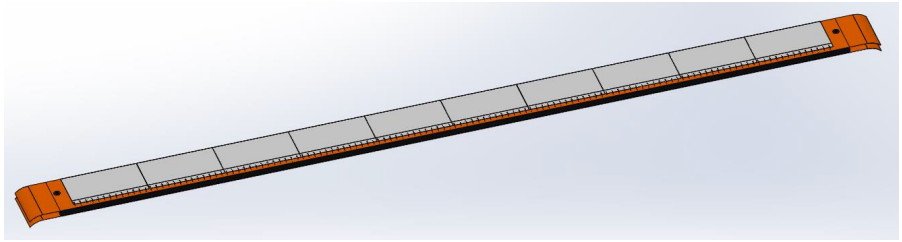
# Overview of CEPC vertex detector prototype R & D

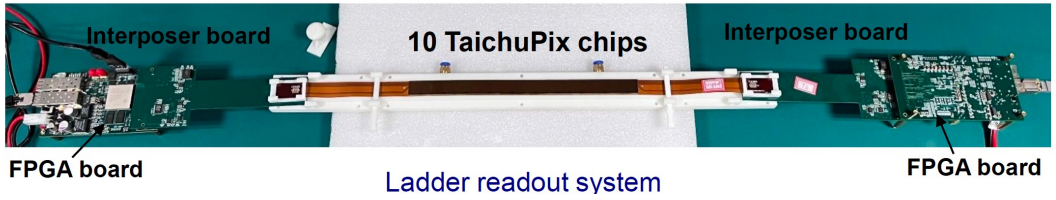
## CMOS Sensor chip development



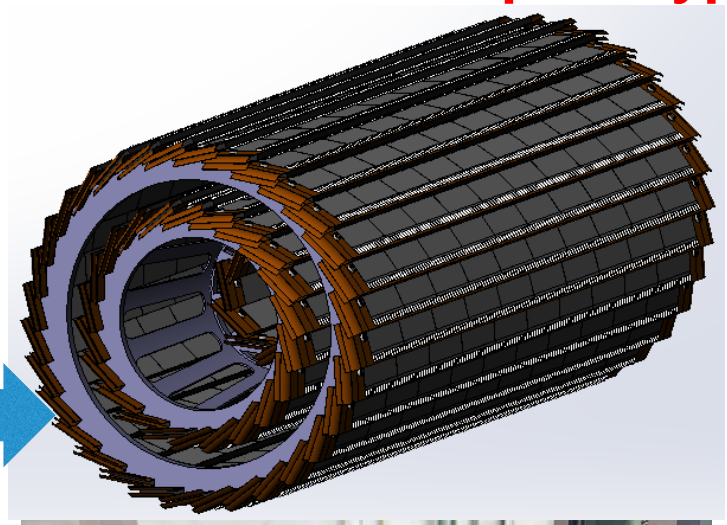
## Detector module (Ladder) Prototyping

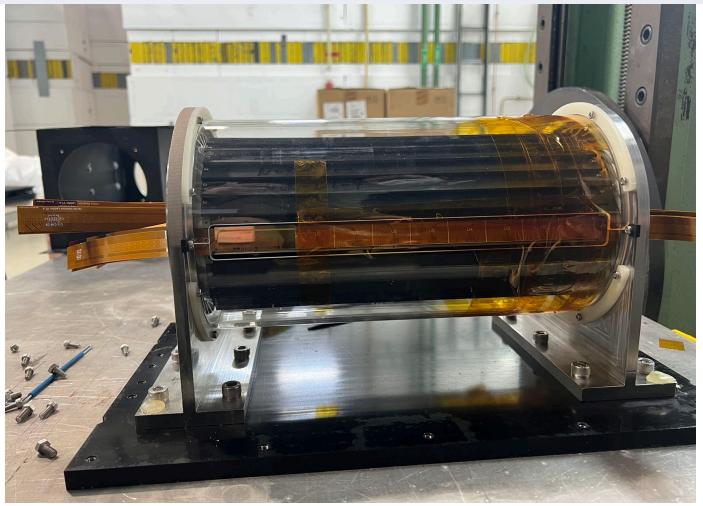





Ladder readout system

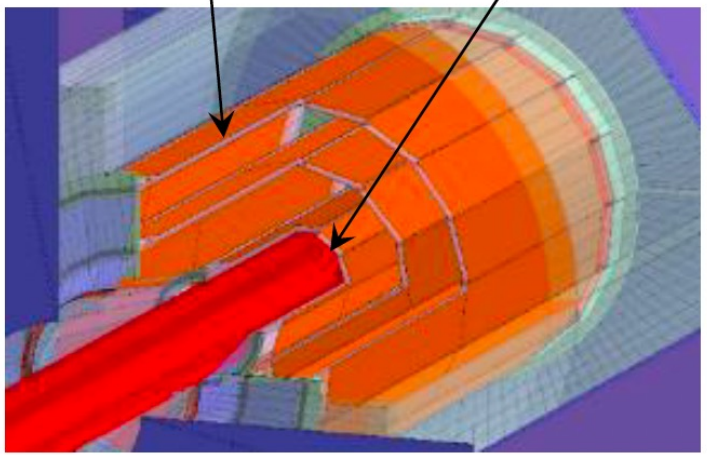
## Vertex detector prototype





# Silicon Pixel Chips for Vertex Detector

2 layers / ladder  $R_{in}$~16 mm



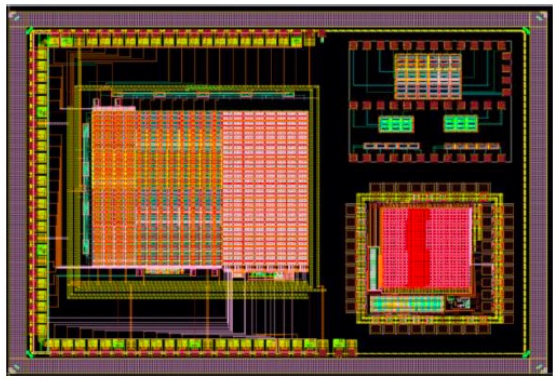
**Goal: σ(IP) ~ 5 μm for high P track**

**CDR design specifications**

- **Single point resolution ~ 3μm**
- **Low material (0.15% $X_0$ / layer)**
- **Low power (< 50 mW/cm²)**
- **Radiation hard (1 Mrad/year)**

**Silicon pixel sensor develops in 5 series: JadePix, TaichuPix, CPV, Arcadia, COFFEE**

Develop **COFFEE** for a CEPC tracker using SMIC 55nm HV-CMOS process

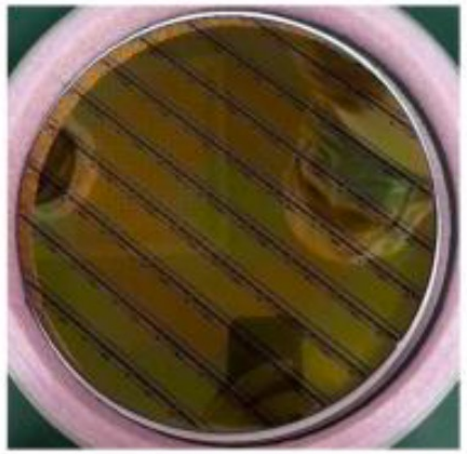


**JadePix**-3 Pixel size ~16×23 μm²

**Tower-Jazz 180nm CiS process**
**Resolution 5 microns, 53mW/cm²**

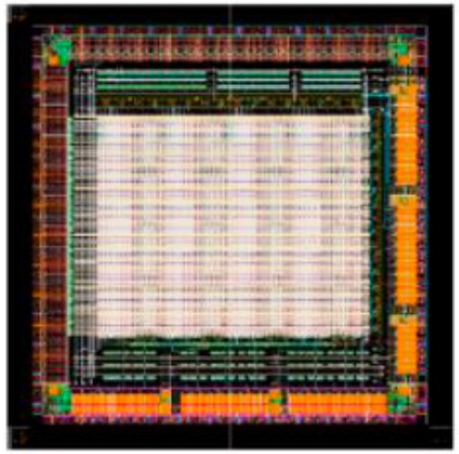
**MOST 1**

**TaichuPix**-3, FS 2.5x1.5 cm²
25×25 μm² pixel size

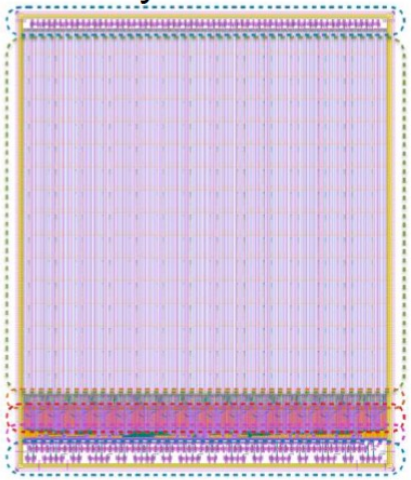


**MOST 2**

**CPV4** (SOI-3D), 64×64 array
~21×17 μm² pixel size

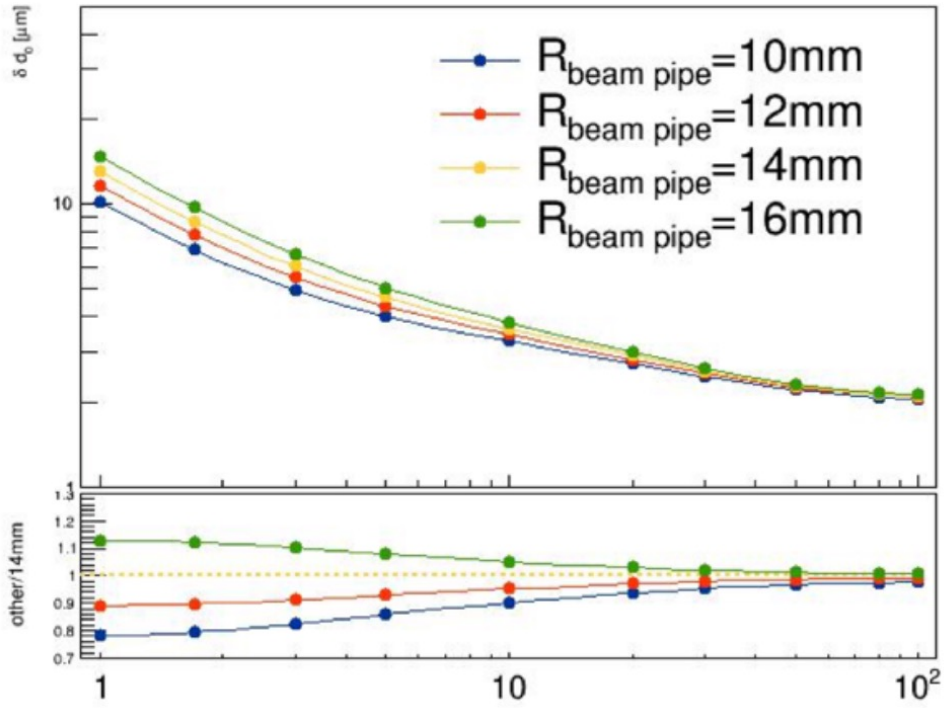


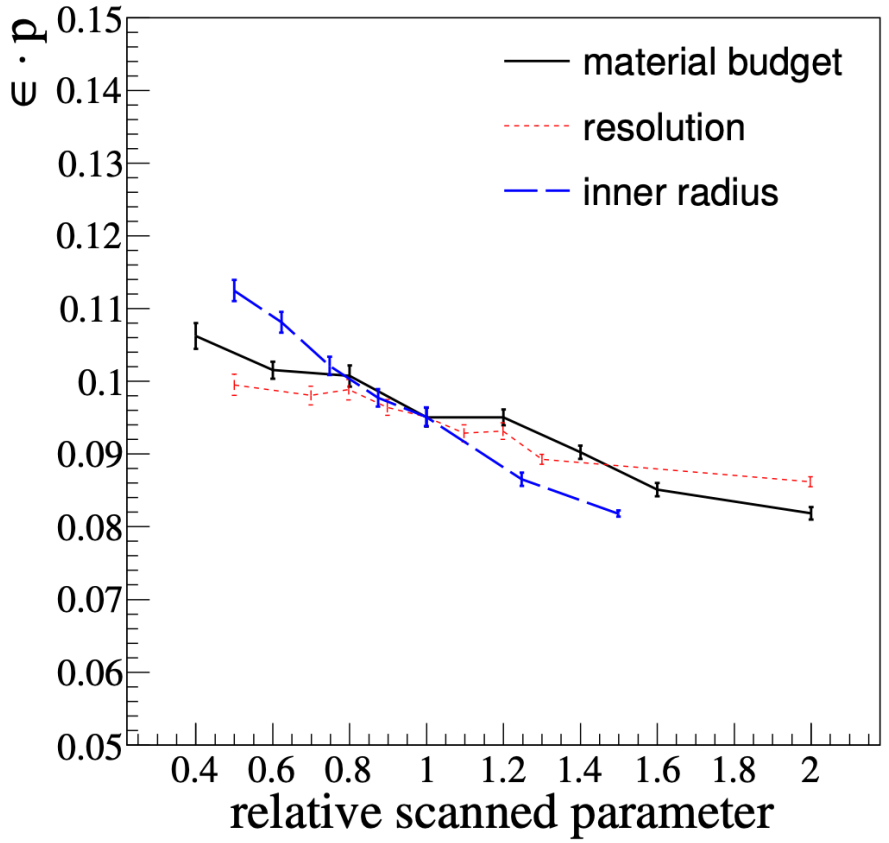
**Arcadia** by Italian groups for IDEA vertex detector
LFoundry 110 nm CMOS



# Vertex Requirement

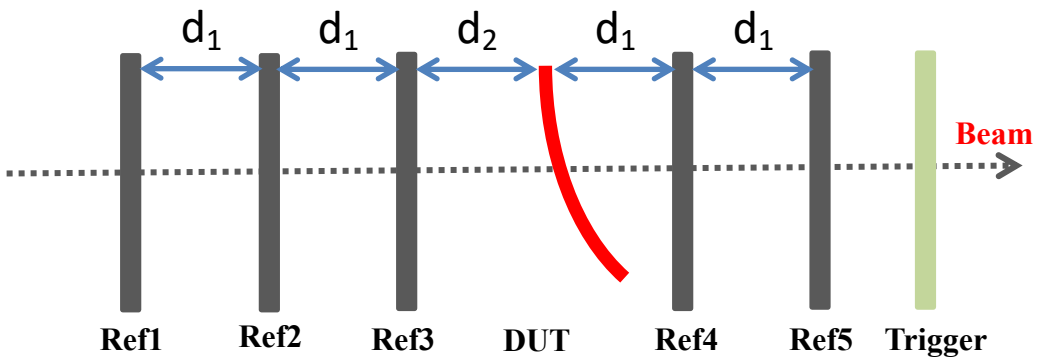
- 1st priority: Small inner radius, close to beam pipe (11mm )
- 2nd priority: Low material budget <0.15% X0 per layer
- 3rd priority: High resolution pixel sensor： 3~5 μm

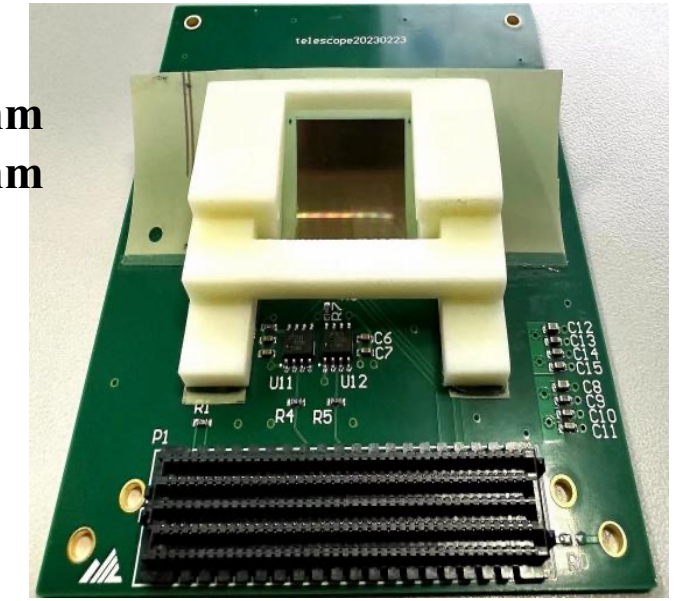


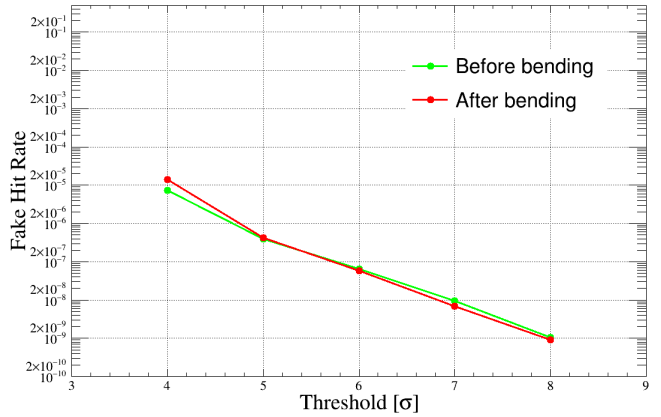



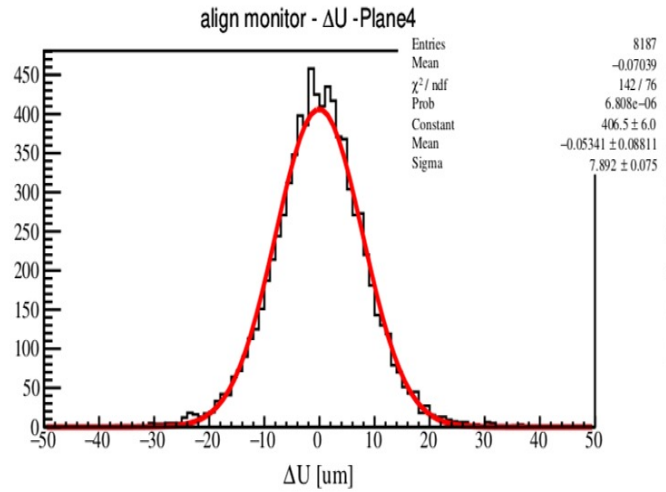
# R&D efforts : Curved MAPS testbeam

- R & D of curved maps with MIMOSA28 chip
  - No visible difference in noise level or spatial resolution before/after bending

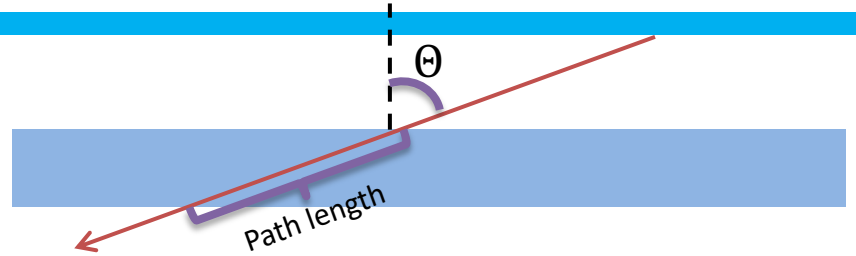


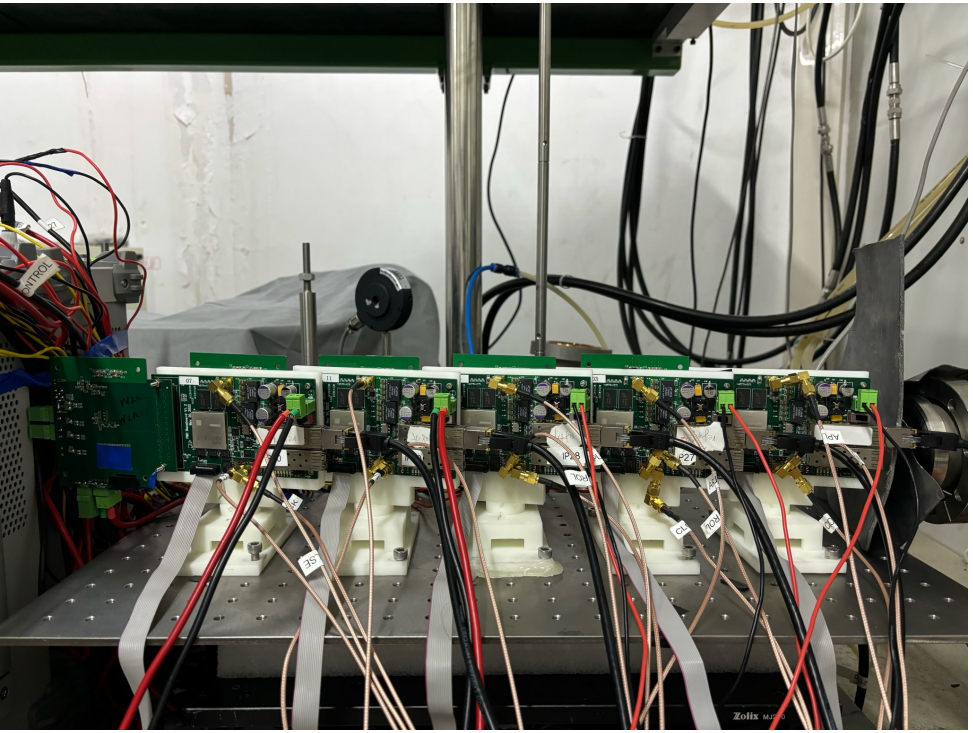



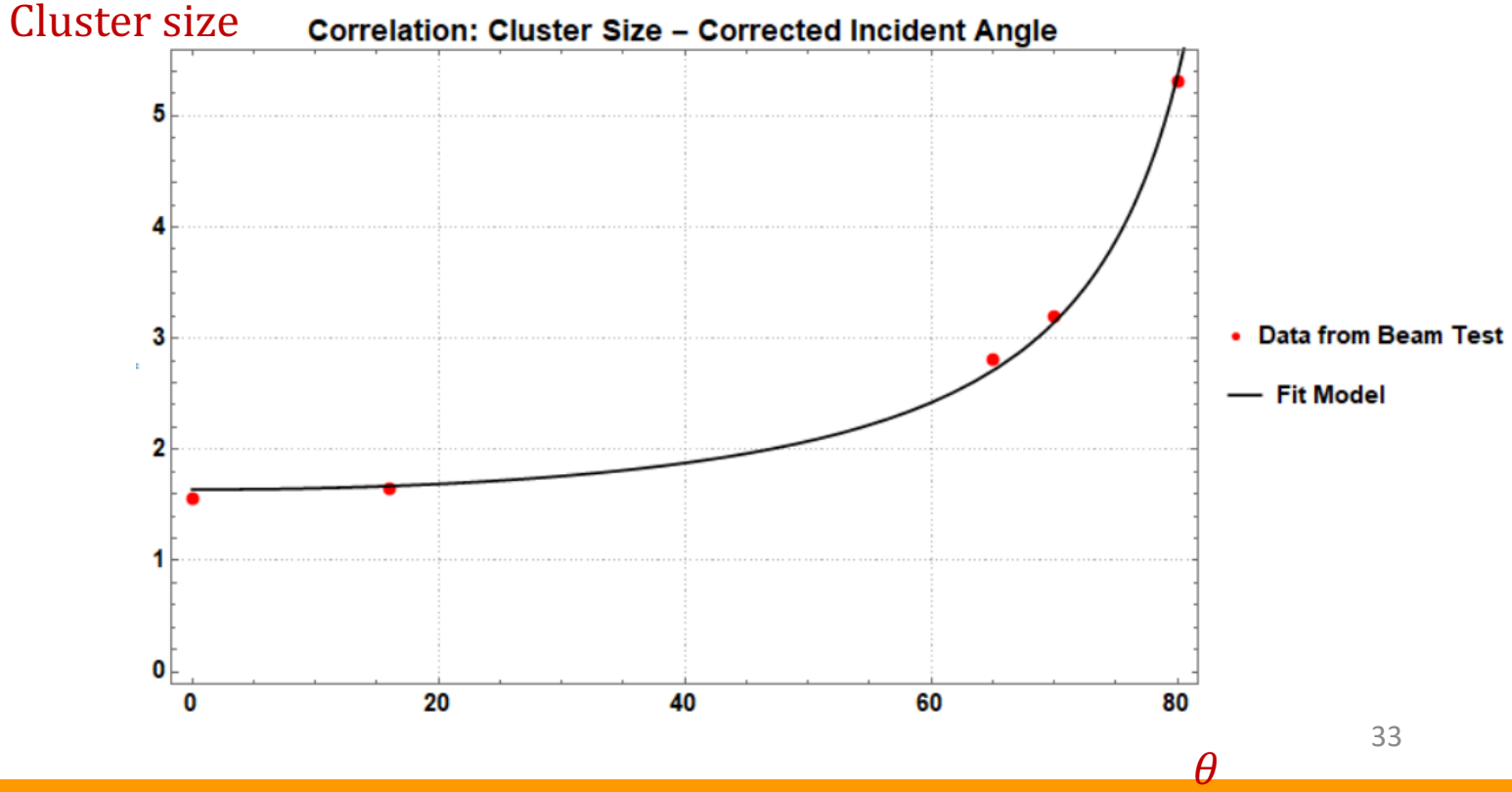



# Long barrel : cluster size vs incident angle



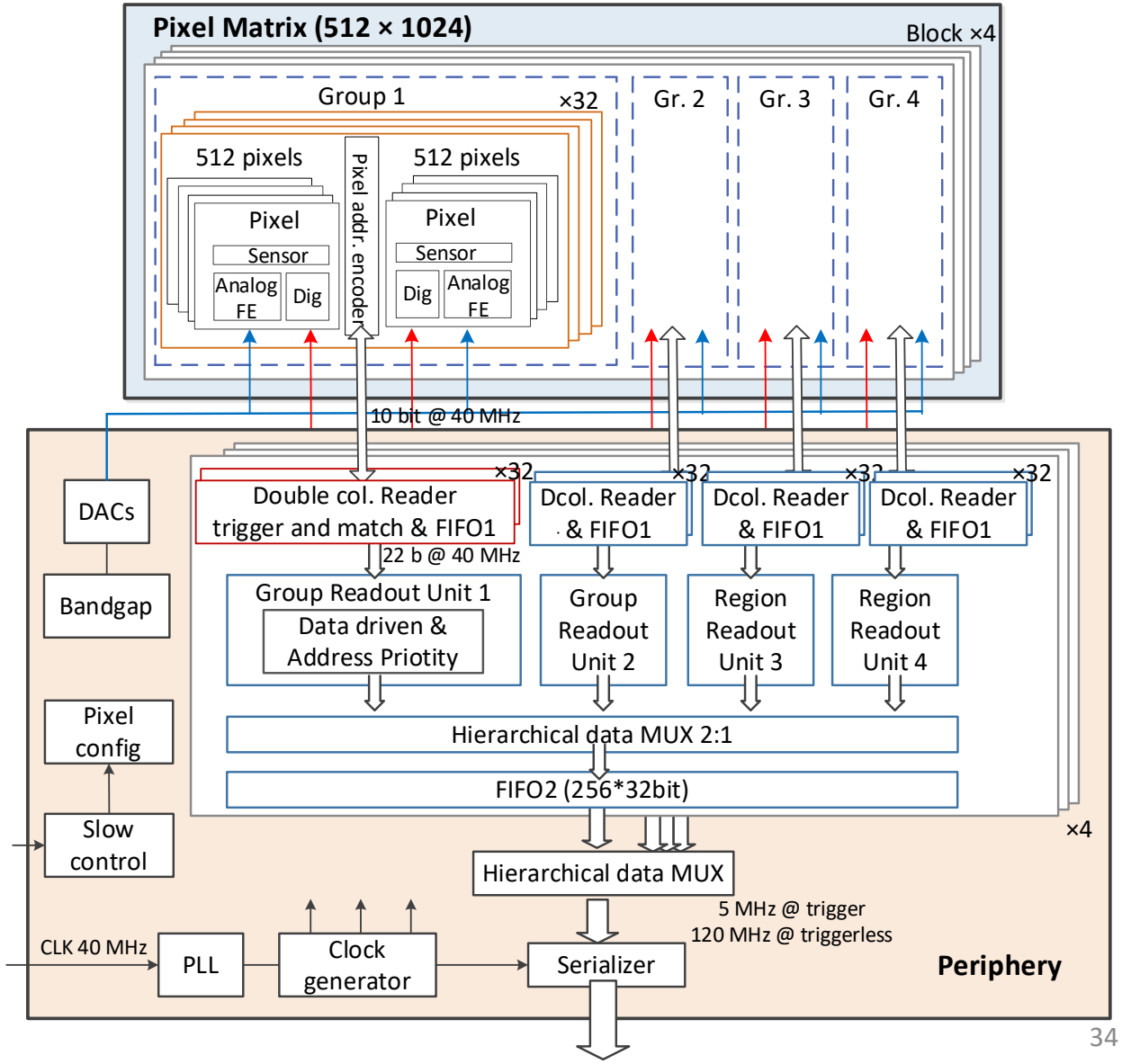

Cluster size $= a \times sec\theta + b$





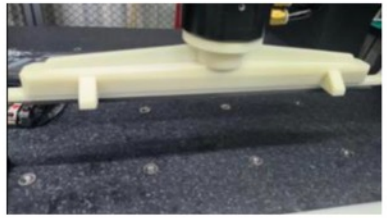
# TaichuPix design

- Pixel 25 μm × 25 μm
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- Column-drain readout for pixel matrix
  - Priority based data-driven readout
  - Readout time: 50-100 ns for each pixel
- 2-level FIFO architecture
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate
  - between core and interface
- Trigger-less & Trigger mode compatible
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp
    only matched event will be readout
- Features standalone operation
  - On-chip bias generation, LDO, slow control, etc

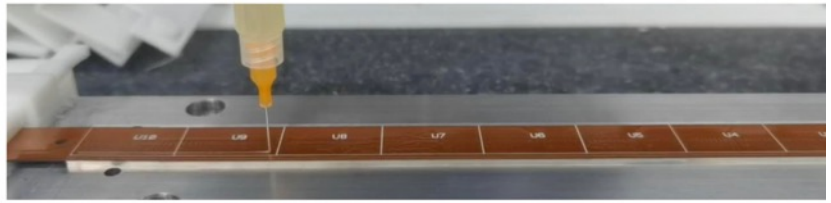


# TaichuPix3 vertex detector prototype

New pickup tools

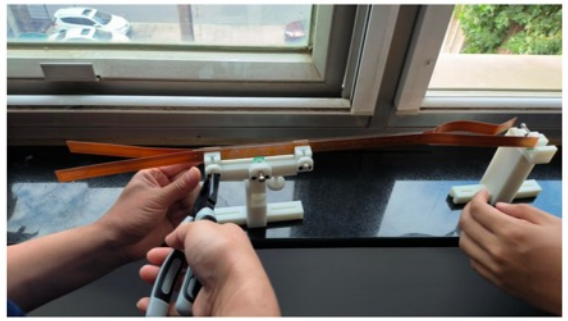


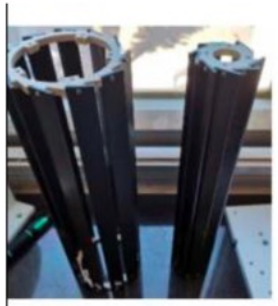
Dummy ladder glue automatic dispensing using gantry

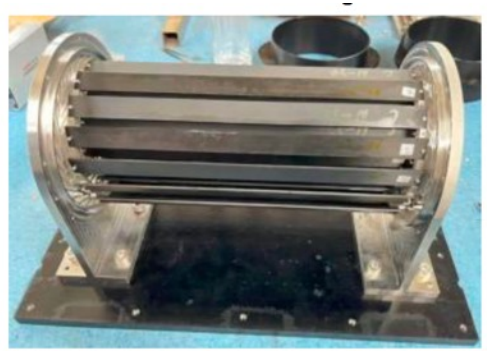


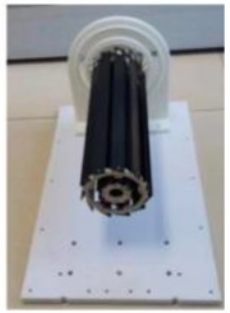
Ladder on wire bonding machine

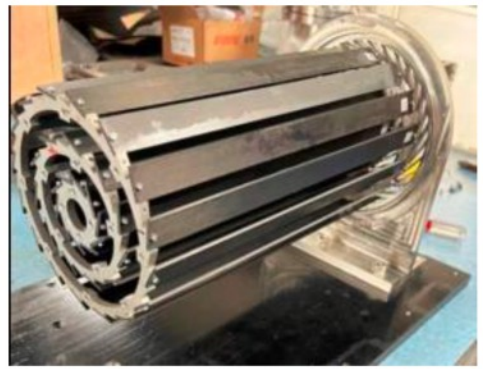
Dummy Ladder on holder



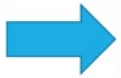








Ladder support tools



Ladder loaded on vertex detector

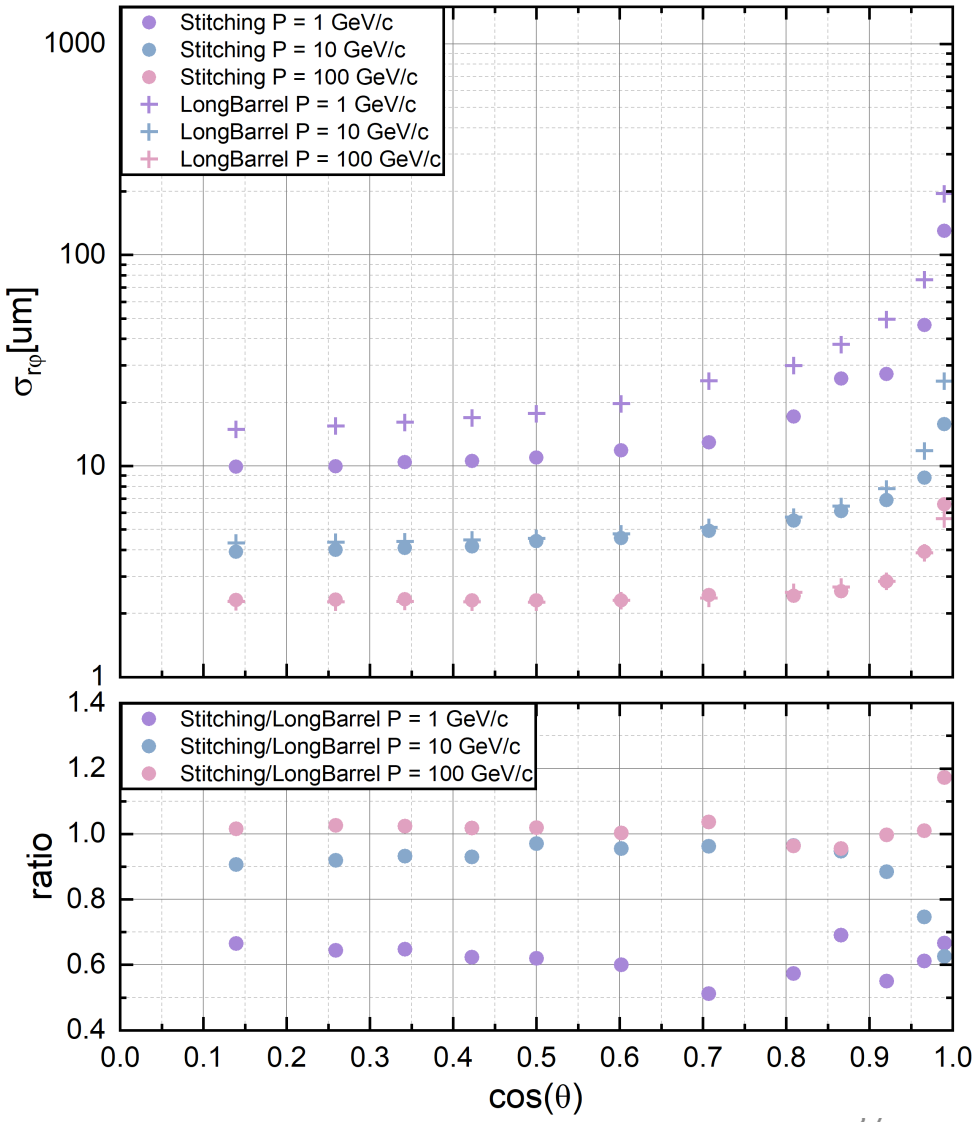
**The first vertex detector (prototype) ever built in China**

# Research team

- IHEP: overall intergration, chip design, detector assembly, electronics, offline
  - Overall : Joao, Zhijun ,Ouyang Qun
  - Mechnical: Jinyu Fu
  - Electronics: Wei wei, Ying Zhang, Jun Hu, Yunpeng Lu , Yang Zhou, Xiaoting Li
  - DAQ: Hongyu Zhang
  - Detector assembly: Mingyi Dong
  - Physics:  Chengdong Fu, linghui Wu, Gang Li
- IFAE: Chip design , Sebastian Grinstein, Raimon Casanova et al
- IPHC/CNRS: chip design , Christine Hu, Yongcai Hu et al
- ShanDong: chip design , Meng Wang, Liang Zhang, Jianing Dong
- CCNU: chip design, ladder assembly, Xiangming Sun, Ping Yang
- North West U. : Chip design Xiaoming Wei, Jia Wang, Yongcai Hu
- Nanchang U. : chip design,  Tianya Wu
- Nanjing: irradation study: Ming Qi , Lei Zhang

# Performance: impact parameter resolution

- Compared to alternative (ladder) option
  - baseline (stitching) has significant improvement in low momentum case



# Vertex detector Operation

- Vertex detector optimized for first 10 year of operation (ZH, low lumi-Z )
  - Low luminosity Z runs is ~20% instant luminosity of high luminosity Z runs

**Table 1.4:** Primary CEPC design objectives (@ 50 MW)

| Parameter | Operation mode | | | |
|---|---|---|---|---|
| | H | Z | W | $t\bar{t}$ |
| Colliding particles | $e^+, e^-$ | | | |
| Center-of-mass energy (GeV) | 240 | 91 | 160 | 360 |
| Luminosity ($10^{34}$ cm$^{-2}$s$^{-1}$) | 8.3 | 192 | 27 | 0.8 |
| No. of interaction points | 2 | | | |