Upgrade Poster Session - CLHCP, 14-17 November 2024

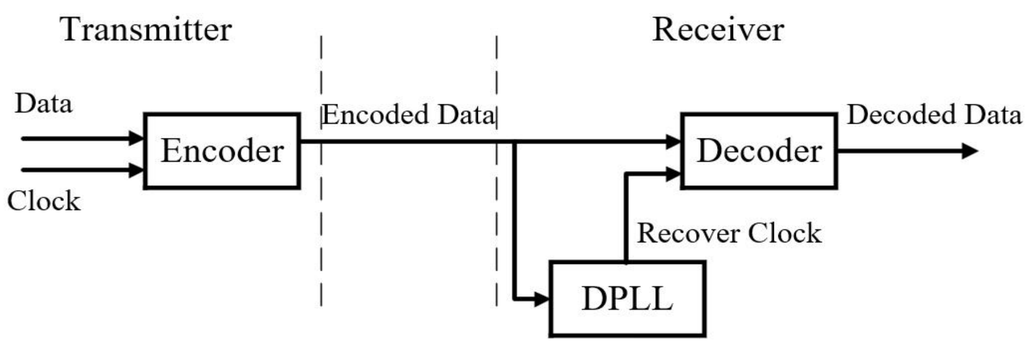
A multi-channel Manchester decoder based on FPGA for ATLAS RPC

INTRODUCTION

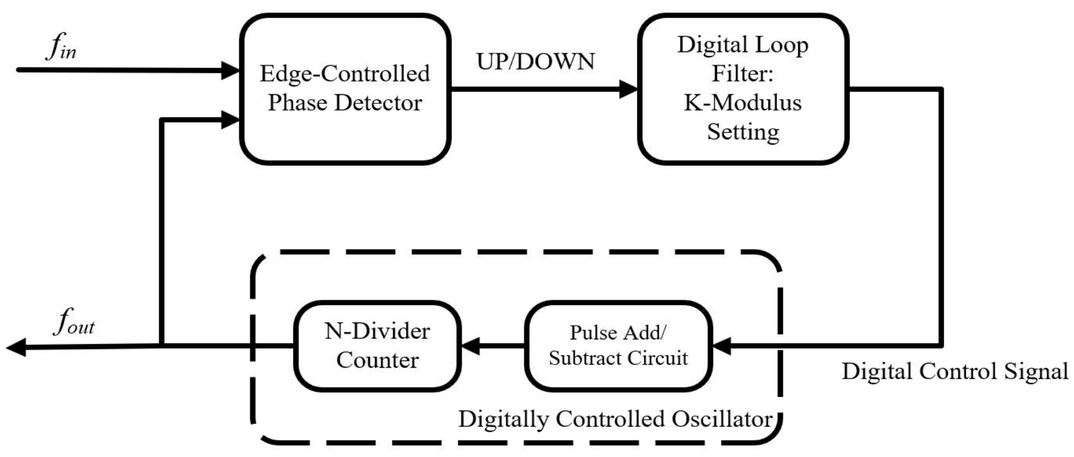
- For the ATLAS Phase II upgrade, a DAQ system with Manchester decoding capability has been designed to enable high-speed reception and decoding of time information output from the front-end boards.
- The decoder is based on the Kintex UltraScale FPGA and is expected to handle decoding for 144 channels, with each channel operating at a transmission frequency of 280 MHz to 320 MHz.

DESIGN OVERVIEW

➢Manchester decoder



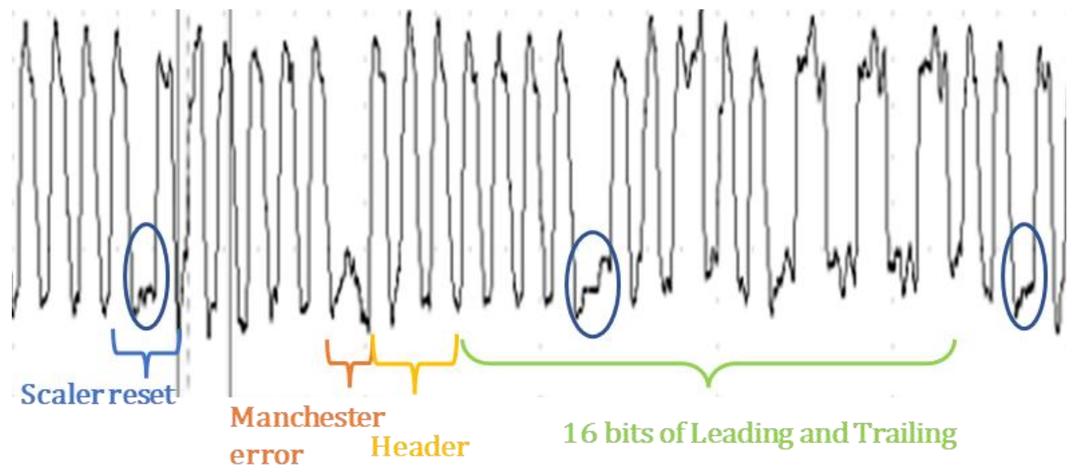
➢Digital Phase-locked Loop



➢Decoding Optimization

- Multi-phase detection is employed to enhance precision of edge capture.
- Adaptive filtering to adjust filter parameters dynamically.
- Low-latency filter decreases the DPLL's locking time.
- Regular self-calibration is a crucial step in preventing cumulative errors during long-term operation.

➢Serial signals output from front-end board



- No signal is injected in the FE, the Manchester output is the data clock.
- The term ‘Manchester error’ refers to the initiation of the transmission, while the term "header" denotes how many BC passed between leading and trailing.
- The reset of the scaler is given every 2 BC, the reset signal creates an occupancy of around 200ps every 2 BC.

➢Theoretical Performance

- In a basic DPLL, the system clock frequency should be at least 4 times that of signals transmission frequency. In a four-phase DPLL, the system clock frequency can be reduced appropriately.
- The decoding process employs a pipelined mode, with a delay of 2 system clock cycles.
- Locking time depends on the filter settings, with a filter depth set to 7 resulting in a locking time of 63 system clock cycles. The combination of filter settings and decoder self-calibration ensures that the dead time of the entire decoder meets the system requirements.

RESULTS

Test with FE

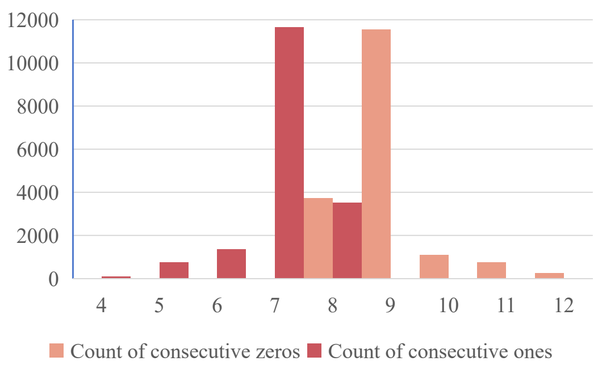
- The pulse signal is configured with a frequency of 1MHz , a duration of 20ns, and an amplitude of -390 mV.
- The required decoding delay is less than 100 ns. Currently, the decoding delay is 3 system clock cycles, which equals 5.36 ns. Even with the addition of serial data processing, the total delay remains well within the 100 ns requirement.

Resource Utilization

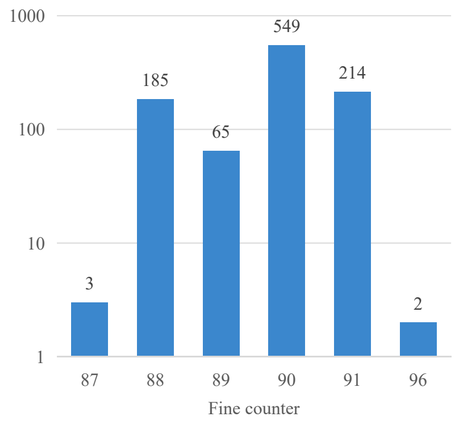
Resource	Utilization	Available	Utilization %
LUT	1323	331680	0.40
LUTRAM	120	146880	0.08
FF	2186	663360	0.33
BRAM	8	1080	0.74

- Half of the resources shown in this table are allocated for ILA (Integrated Logic Analyzer) data sampling.
- The current resource allocation is sufficient to support decoding across 144 channels.

Waveform analysis



- 4.64GHz sampling results (8 times encoding data transmission frequency)
- The count of consecutive zeros is mostly higher than the count of consecutive ones.
- The number of consecutive ones and zeros(34778) small than number of samples(34816), refers to real frequency is small lower than 280 MHz .



Decoded data analysis

- Total events: 1020
- The number of correctly decoded: 1018
- Pulse width calculate function:

$$90 \times \frac{1}{280MHz \times 8 \times 2} = 20.09\ \text{ns}$$

- Data loss: 2
- Decode event error rate: 0.19%

CONCLUSION

➢Single-channel testing demonstrates effective performance, with low error rates and efficient resource utilization.

➢The main challenge going forward is scaling the solution to reliably support 144-channel decoding in preparation for full RPC detector cosmic ray test.

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