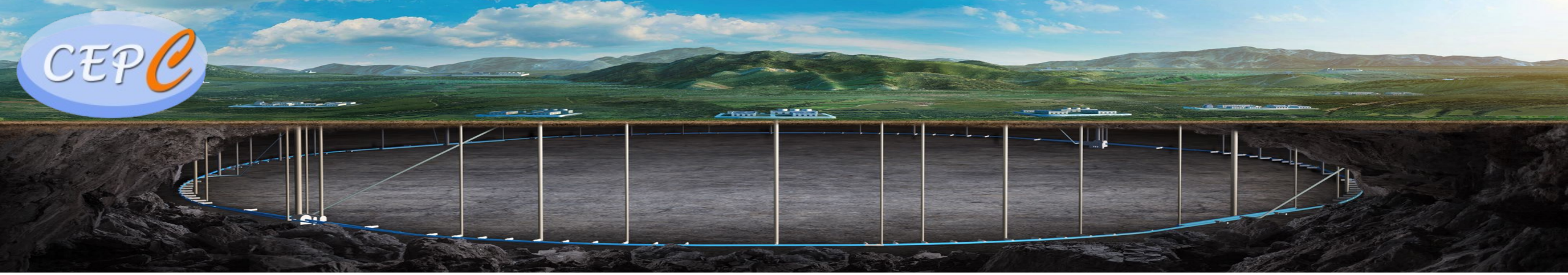


CEPC Silicon Tracker Detector

Qi Yan

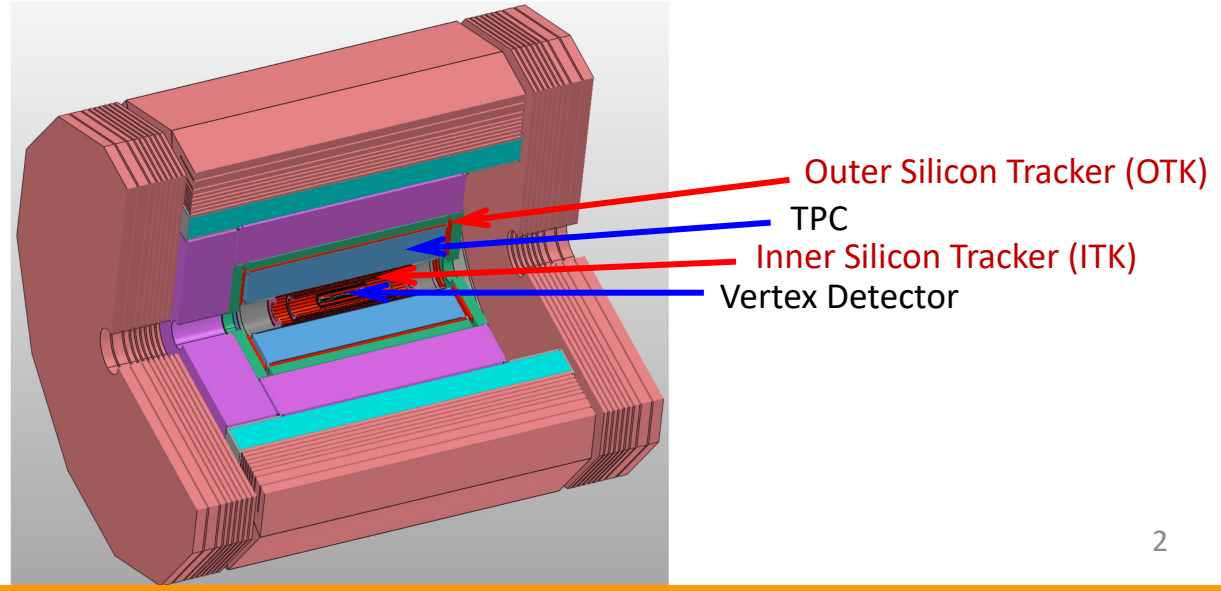
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Introduction

- The CEPC tracker system includes several detectors: the Vertex Detector, Inner Silicon Tracker, Time Projection Chamber (TPC), and Outer Silicon Tracker. This presentation will focus on the Inner Silicon Tracker (ITK) and Outer Silicon Tracker (OTK).

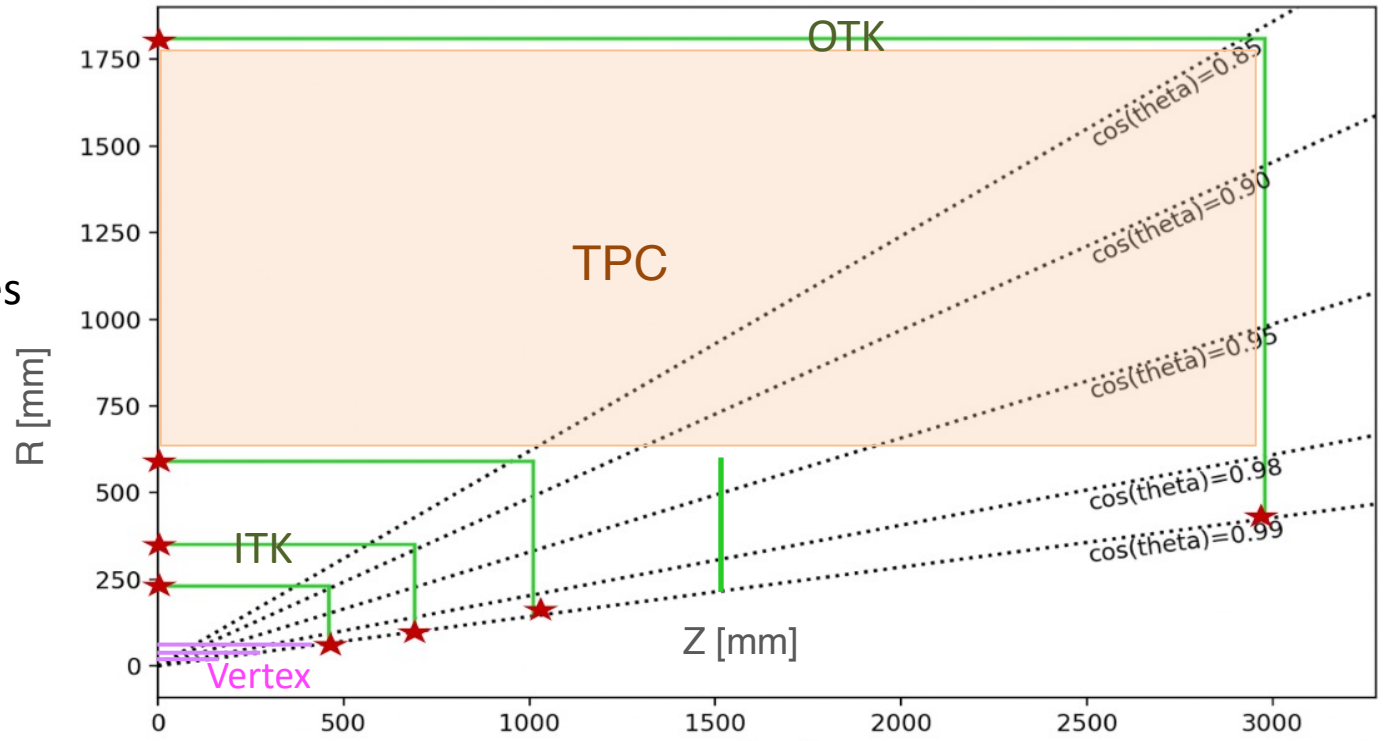
- The ITK employs advanced sensor technologies, including HV-CMOS pixels and CMOS strips, to achieve precise position measurements for accurate particle trajectory determination.

- Both the ITK and OTK measure particle ionizations. Additionally, the OTK incorporates the AC-LGAD semiconductor detector for precision time measurement of charged particles, significantly enhancing particle identification capabilities.



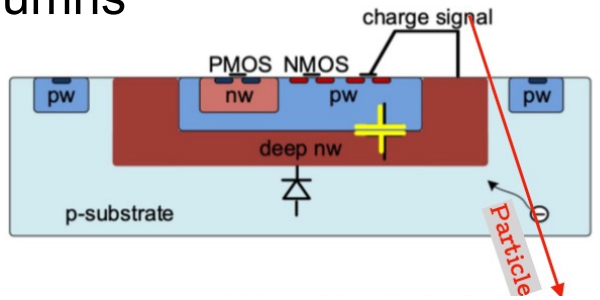
Requirement

- Inner silicon tracker (ITK)
  - Spatial resolution:
    Barrel: $\sigma_\phi < 10\ \mu m$, $\sigma_z < 50\ \mu m$
    Endcap: $\sigma_\phi < 10\ \mu m$, $\sigma_r < 100\ \mu m$
  - Material budget:
    <0.7% X_0 per layer
  - Luminosity ~$115\times10^{34}\ s^{-1}cm^{-2}$ (Z-pole):
    A few ns timing resolution to tag 23ns bunches
    Hit rate ~$2\times10^{6}\ s^{-1}cm^{-2}$
    Radiation hard: TID >800 kGy
  - Cost effectiveness:
    >20 m^2 area
- Outer silicon tracker (OTK)
  - Spatial resolution:
    $\sigma_\phi < 10\ \mu m$
  - Timing resolution:
    σ_t<100 ps
  - Cost effectiveness:
    ~100 m^2 area

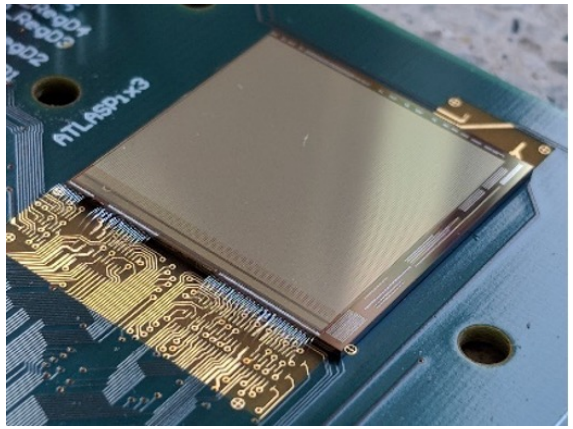


Technology Survey and our Choices for ITK Barrel

- CMOS sensor technology:
  - Cost-effective due to widespread use in the semiconductor industry
  - Combine the active detection layer and the readout electronics into a single device
- HVCMOS pixels:
  - Large depletion depth (can achieve full depletion), large signal
  - Radiation hard
  - Relatively large capacitance, leading to increased noise and power consumption
- New COFFEE (HVMOS) pixels R&D for CEPC:
  - Utilizes 55nm process instead of the 180 nm used in ATLASPix3
    More functionality and less power consumption
  - Pixel size: $34 \times 150\ \mu m^2$
  - Array size: 512 rows × 128 columns
  - Wafer resistivity: 1k-2k Ω·cm
  - Power consumption: ~200 mW/cm^2



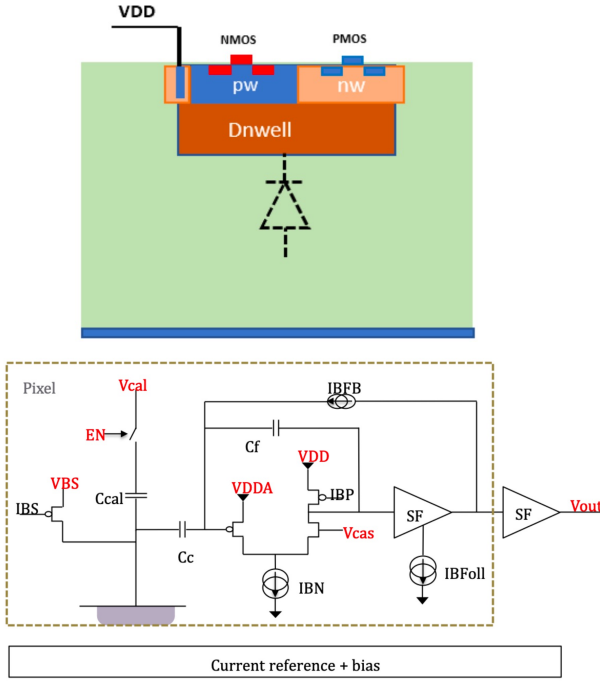
- ATLASPix3
  - TSI 180nm HVCMOS on 200 Ωcm substrate
  - Pixel size 50 × 150 μm^2
  - 372 rows × 132 columns
  - 20.2 × 21 mm^2 reticle size
  - Each pixel has 7-bit TOT + 10-bit timestamp
  - Continuous / triggered readout with 8b10b / 64b66b coding
  - Power consumption ~160 mW/cm^2.

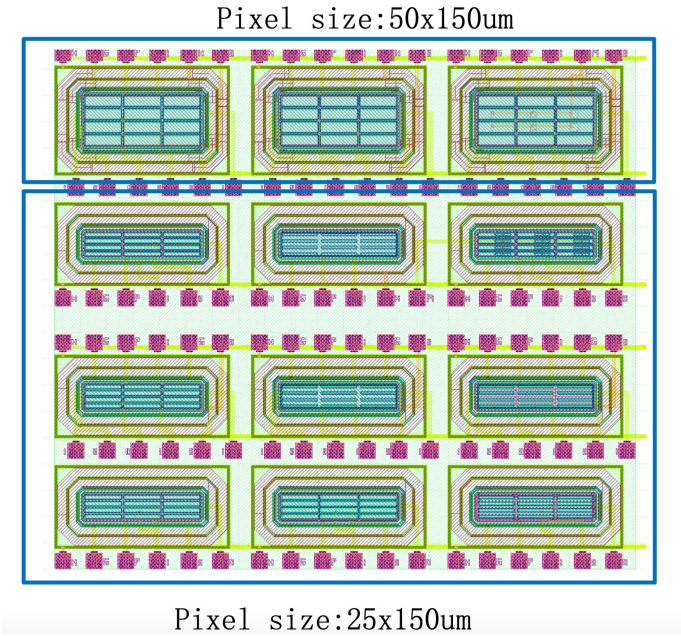


R&D: COFFEE1 (HVCMOS) Pixels Development

- COFFEE1: SMIC 55nm Low-Leakage process

1) Submitted in Oct 2022, received in Apr 2023
   - Low resistivity wafer. Not HV process, but with a similar deep n-well structure
2) Pixel size: 25×150 μm² or 50×150 μm²



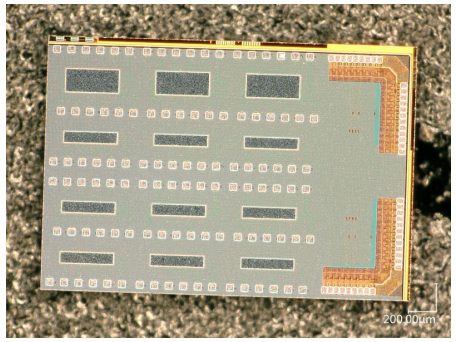


COFFEE

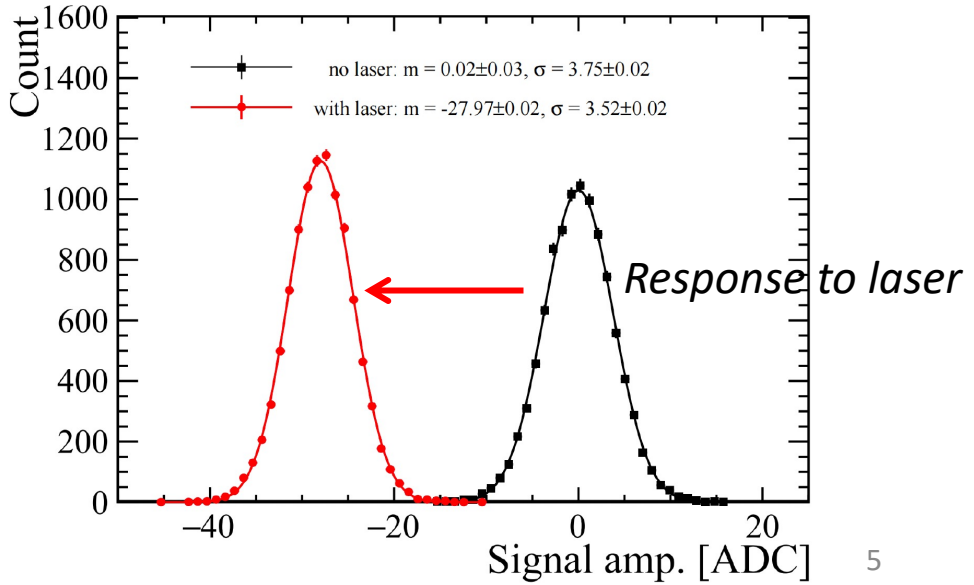
CMOS SENSOR IN FIFTY-FIVE NM PROCESS

KIT Karlsruher Institut für Technologie

COFFEE1



3) Capacitance of a single pixel (25×150 μm²): 150~200 fF
4) Clear signal response to laser: charge of ~2400 e-



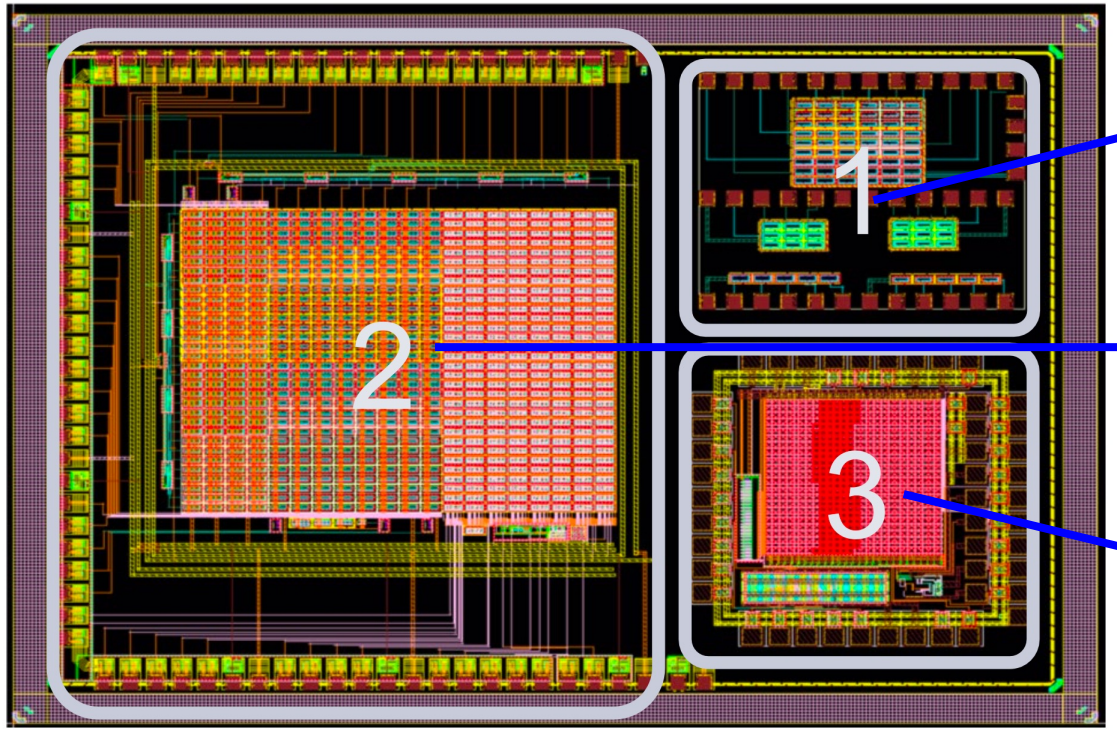
R&D: COFFEE2 (HVCMOS) Pixels Development

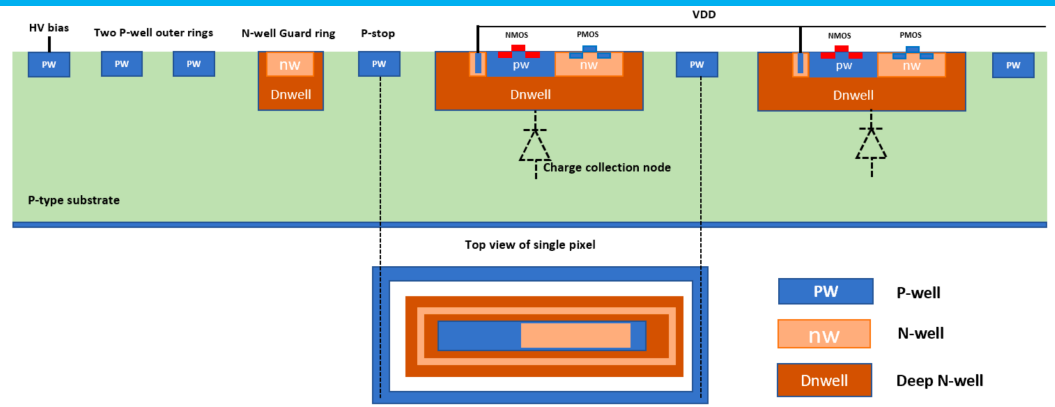
COFFEE2: SMIC 55nm HVCMOS process

Submitted in Aug 2023, received in Dec 2023

- HVCMOS process, with 1k Ω·cm wafer, without deep p-well structure

Chip performance test in on going





Three sections in the chip:

1: Passive diode arrays:

- Including 6 different signal collection structures for studying diodes and charge sharing.
- pixel size: 40 × 80 μm^2

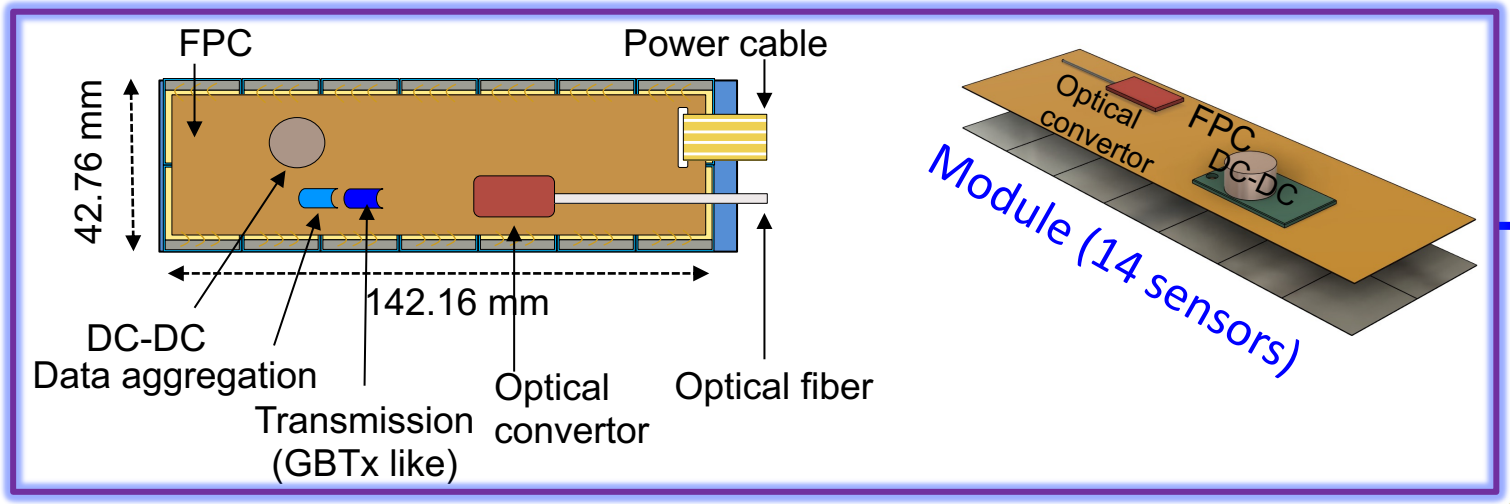
2. Pixel arrays with diodes and in-pixel electronics:

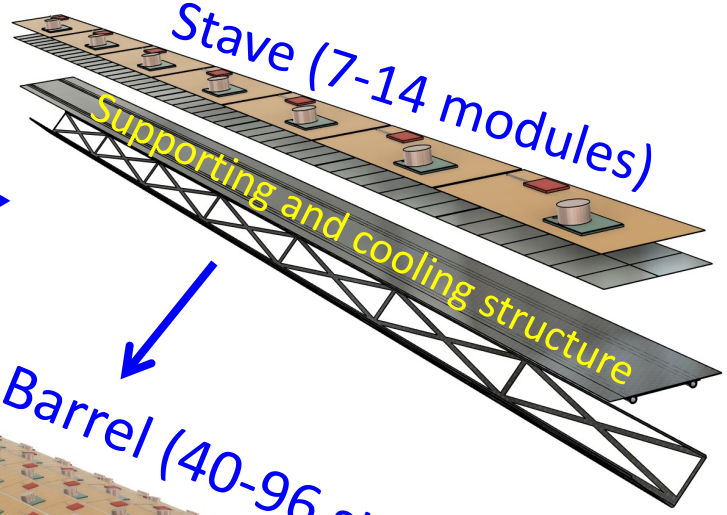
- Features 6 types of diodes and 3 types of in-pixel electronics.
- pixel size: 40 × 80 μm^2

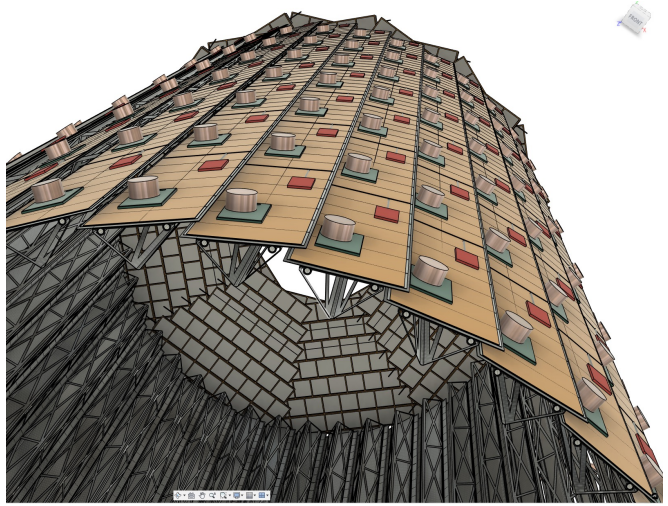
3. Pixel arrays with peripheral digital readout

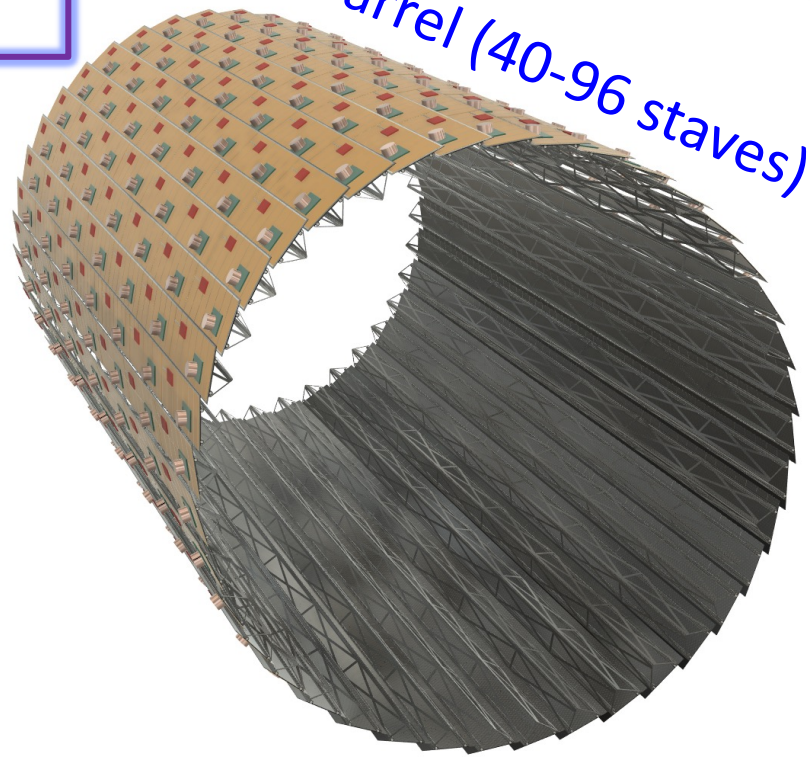
- Used for validating readout strategies.
- pixel size: 25 × 25 μm^2

CEPC ITK Barrel Baseline Design with HVCMOS Pixel Sensor, Modules and Staves

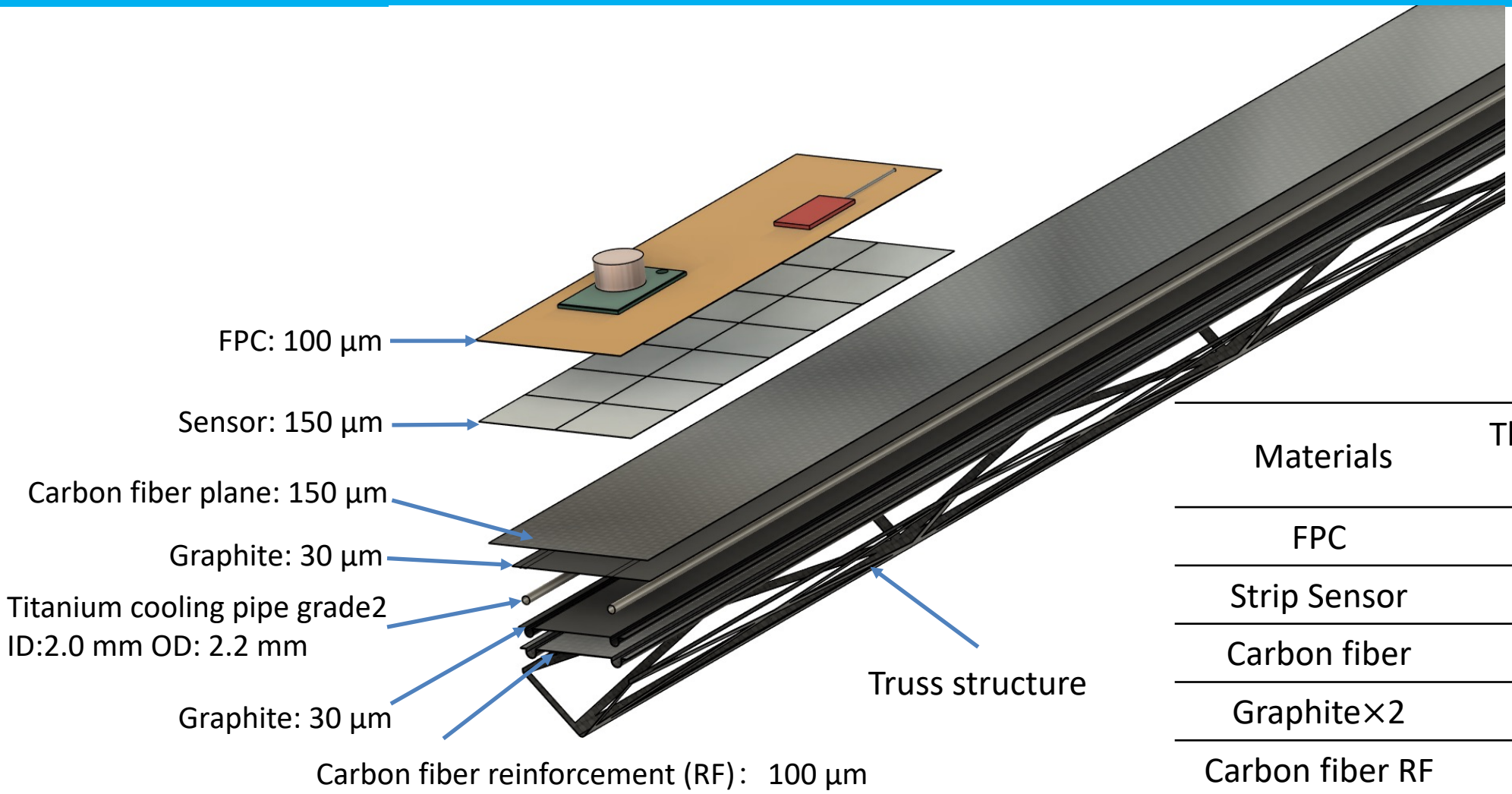








Mechanical and Cooling Design for ITK Barrel

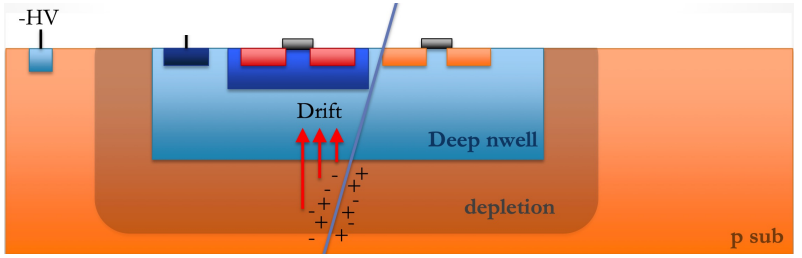


Materials	Thickness (mm)	Radiation Length [% X_0]
FPC	0.10	0.14
Strip Sensor	0.15	0.18
Carbon fiber	0.15	0.06
Graphite×2	0.06	0.03
Carbon fiber RF	0.10	0.04
Total		0.45

Technology Survey and our Choices for ITK Endcap

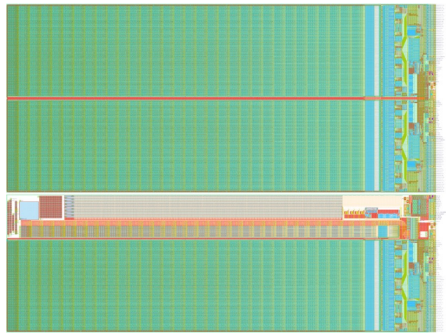
- CMOS sensor technology：
  - Cost-effective due to widespread use in the semiconductor industry
  - Combine the active detection layer and the readout electronics into a single device
- CMOS strips compared with CMOS pixels:
  - Less expensive and relatively lower power consumption
  - Simpler readout with fewer technical barriers
  - Comparable or even better spatial resolution
  - Negligible track ambiguity using specific design detector layout:

    For example: the CEPC ITK endcap is designed with strip sensors with a 22.5° cross angle between 2 half-layers
- CSC (CMOS) strip R&D for CEPC:
  - Based on CHESS for ATLAS ITK strips
  - Utilizes 150-180 nm process
  - Strip pitch size: 20 μm
  - Wafer resistivity: >1k Ω·cm
  - Power consumption: <200 mW/cm^2

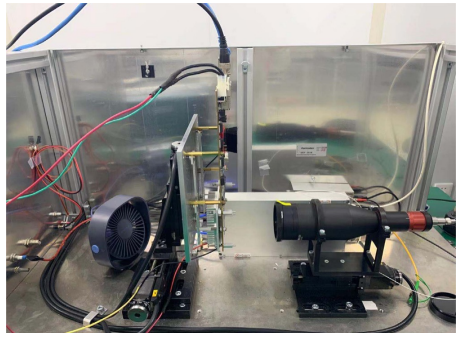


CMOS Strip R&D Efforts and Results

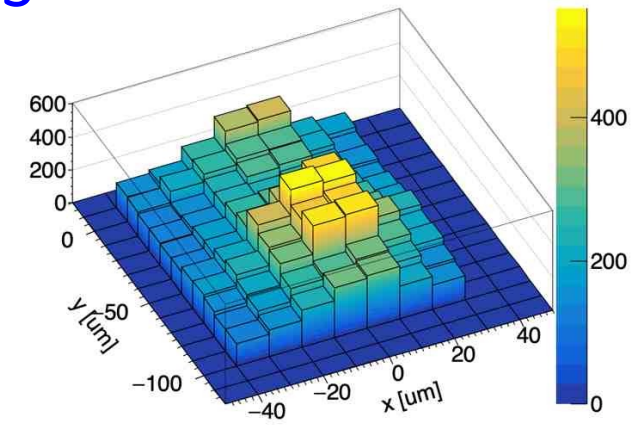
- CMOS strip layout and test - CHESS



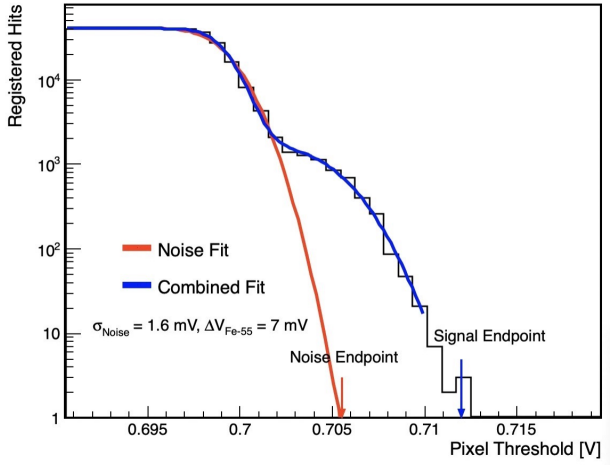
layout



Laser test system



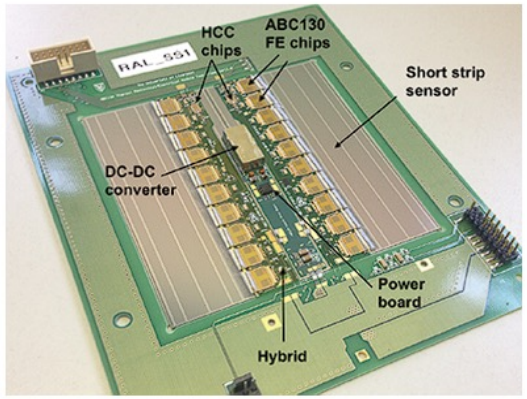
Contact and strip match design



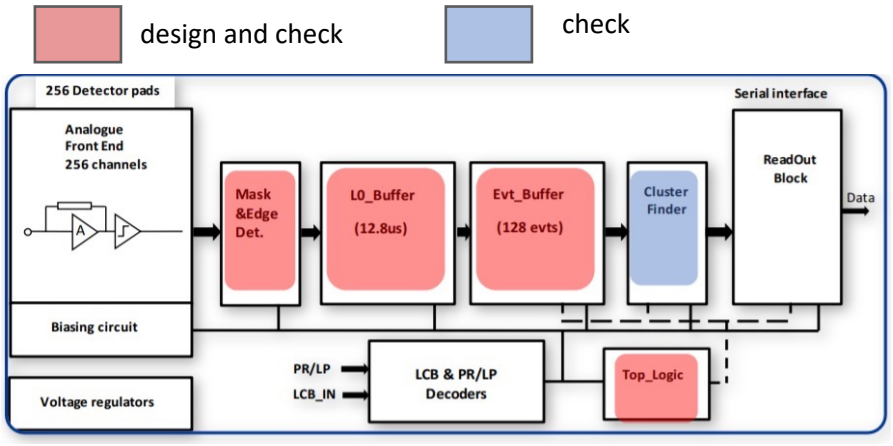
S/N~3 when detected X-ray from Fe-55

H. Zhu DOI 10.1016/j.nima.2020.164520

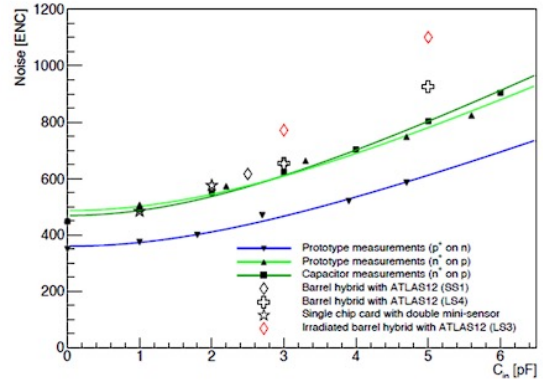
- ATLAS ITK ABCStar Chip design



real chip



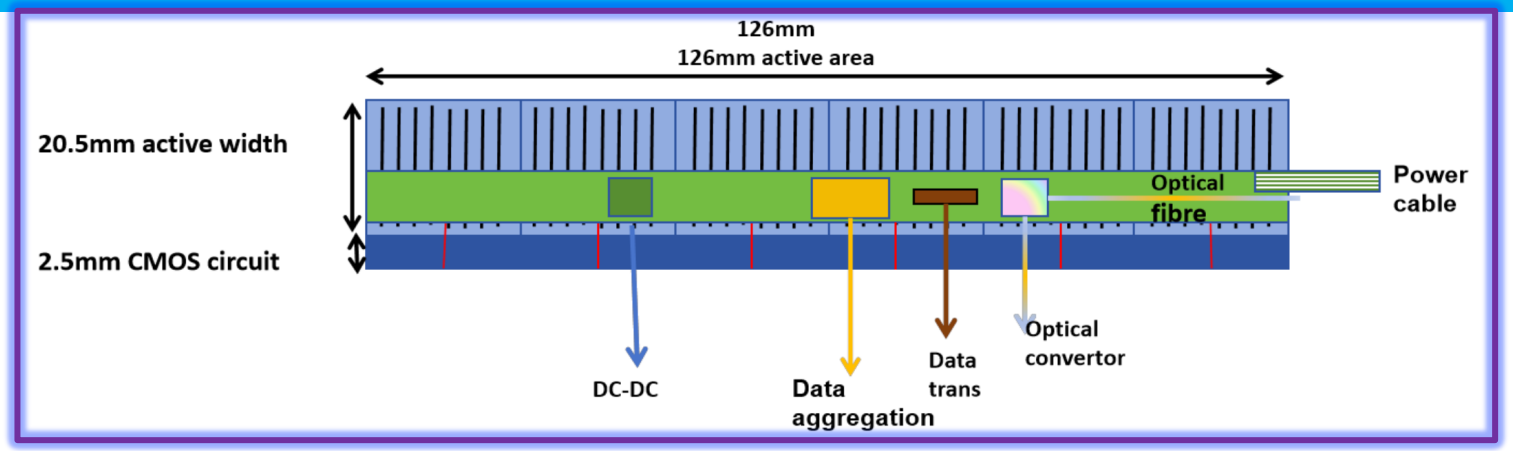
Block diagram of current ABCStar.

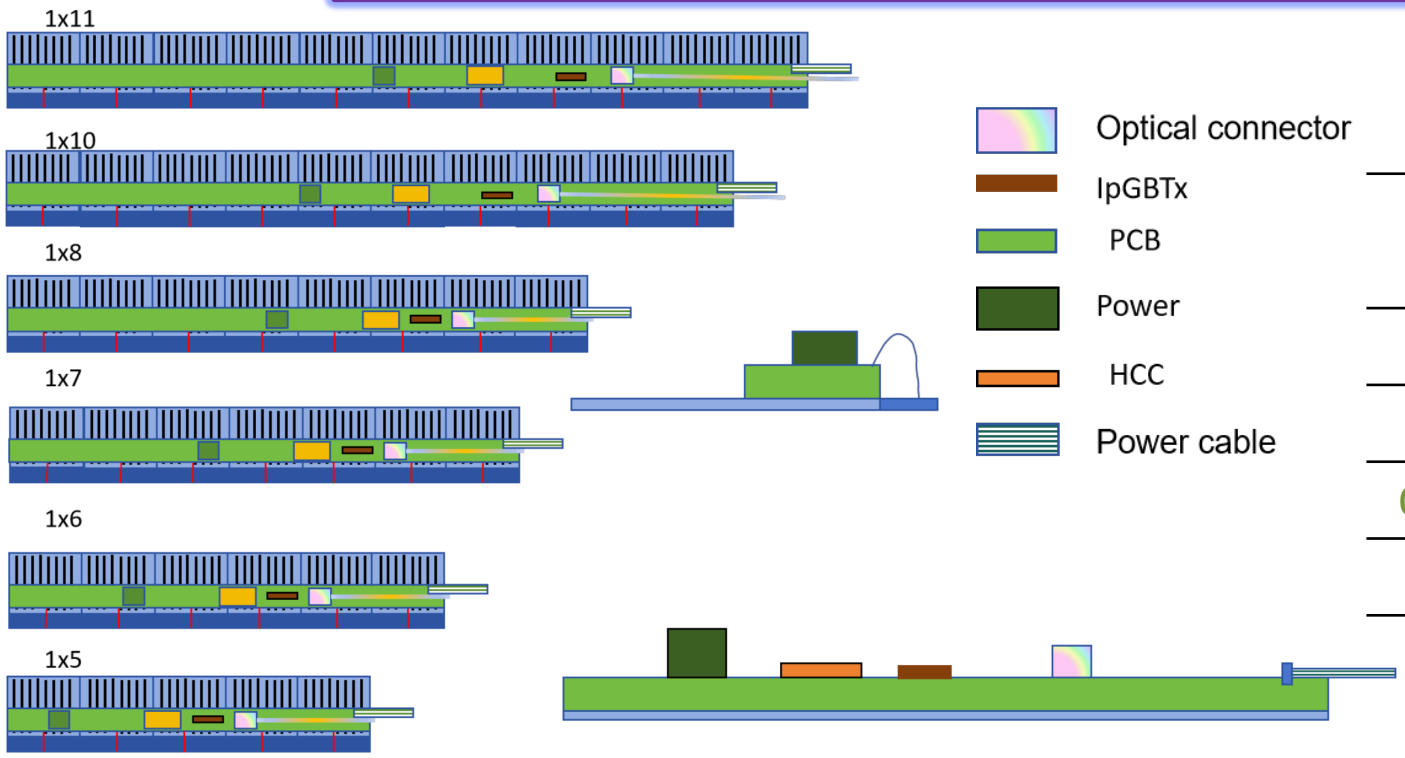


W. Lu DOI 10.1088/1748-0221/12/04/C04017
Measured noise as a function of input capacitance

Strip Sensor and Module Design for ITK Endcap

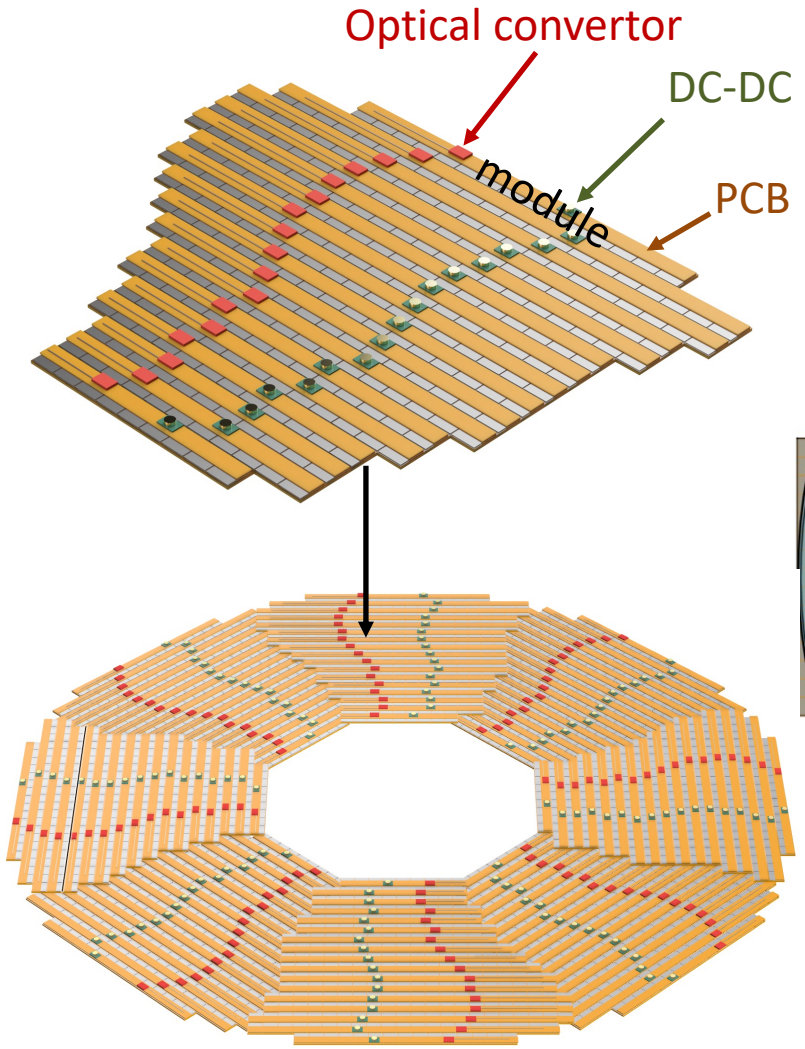
- Module

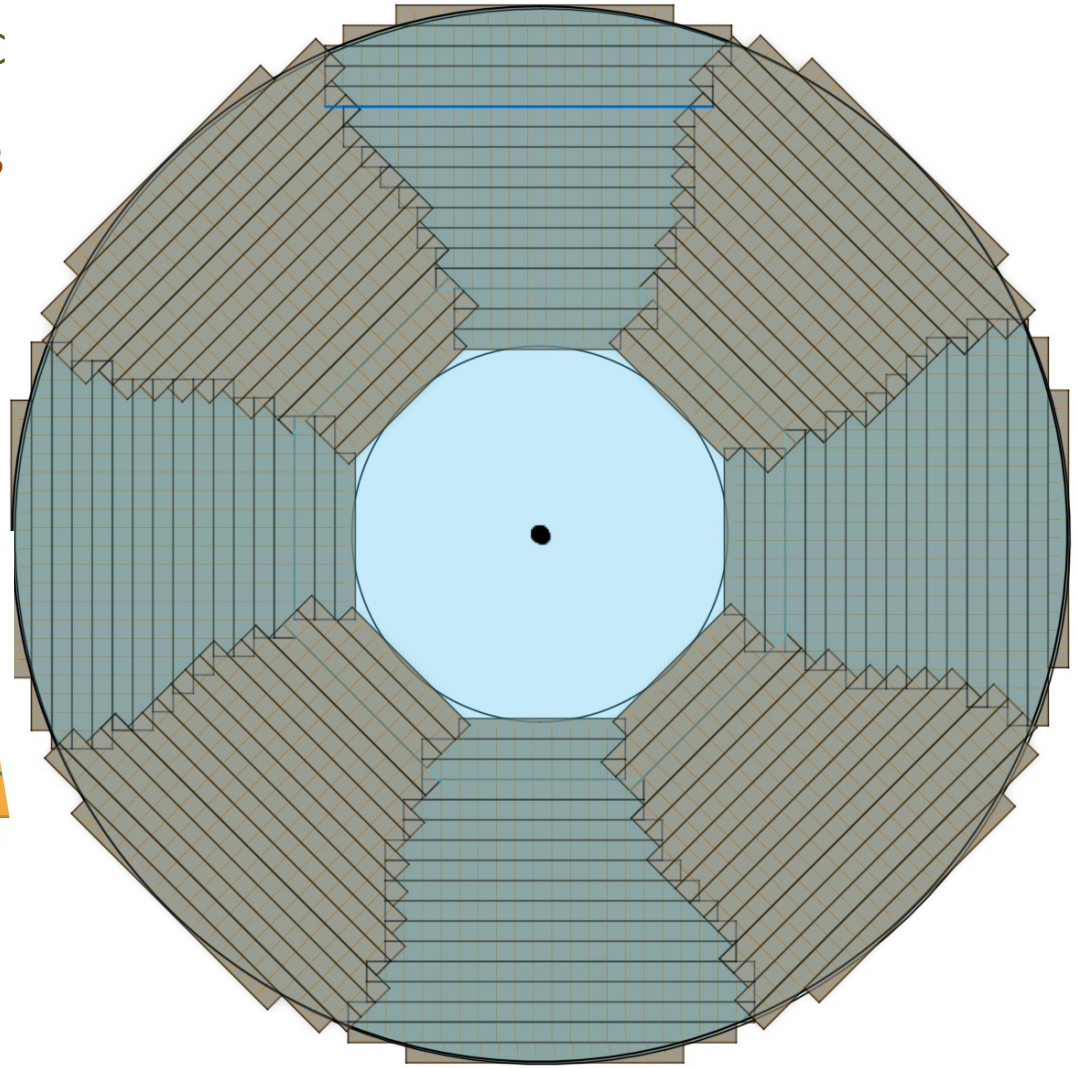




Materials	Thickness (mm)	Radiation Length [% X_0]
Strip Sensor	0.15	0.18
FPC	0.10	0.14
Optical Connector	1.25	0.13
IpGBTx	4.00	0.07

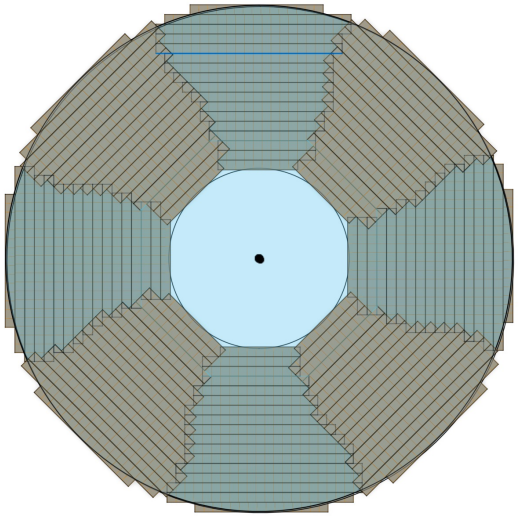
CEPC ITK Half-Endcap Design



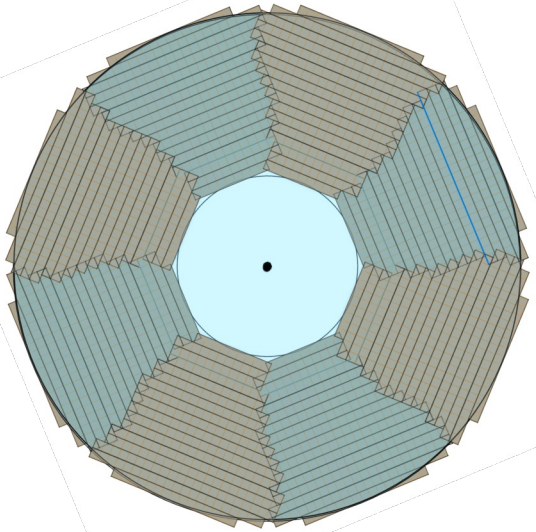


Each half endcap is divided into 8 sectors: Each sector is entirely composed of rectangular modules, with minimal overlapping between sectors.

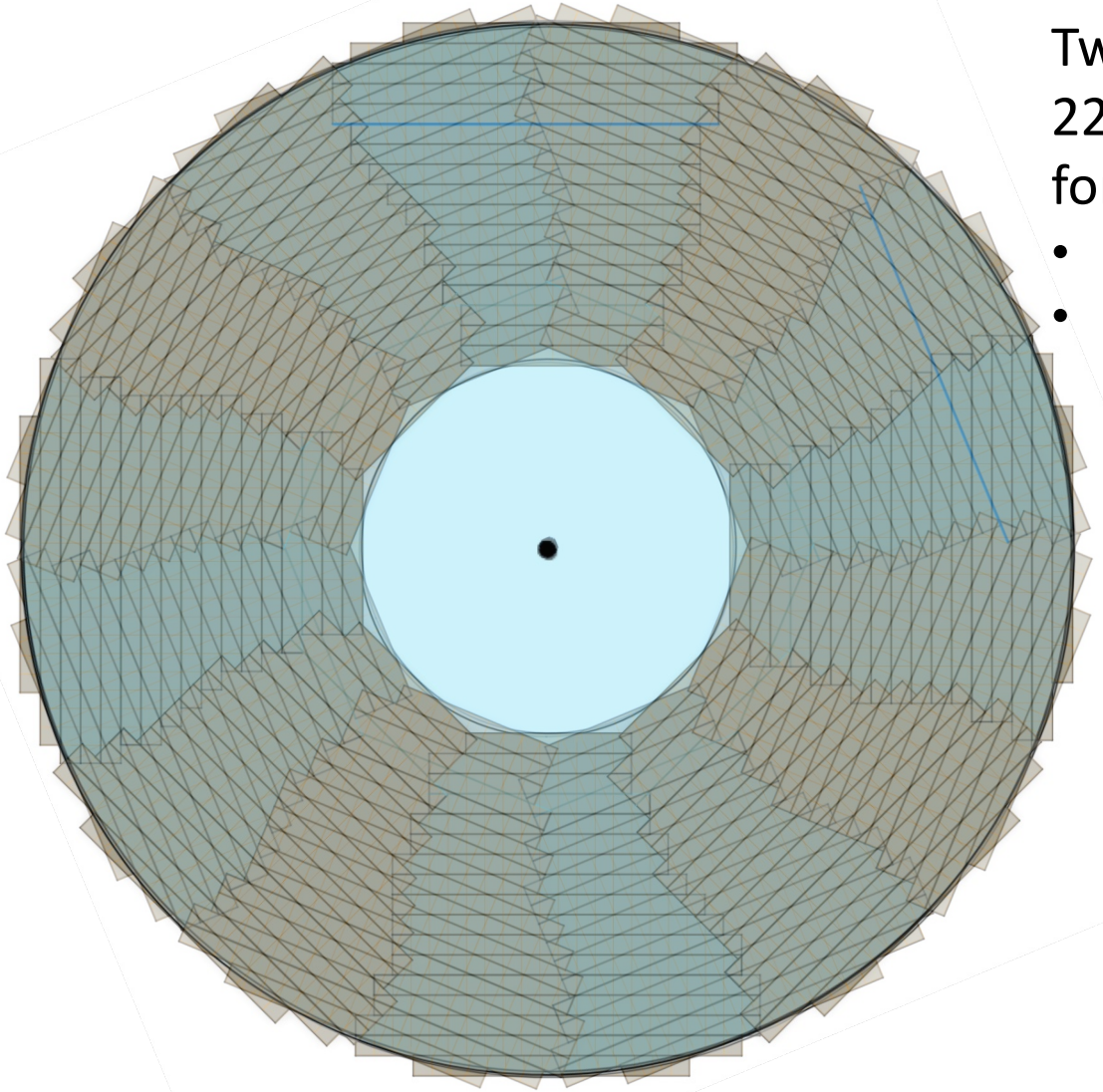
CEPC ITK Complete Endcap Design



Normal half endcap

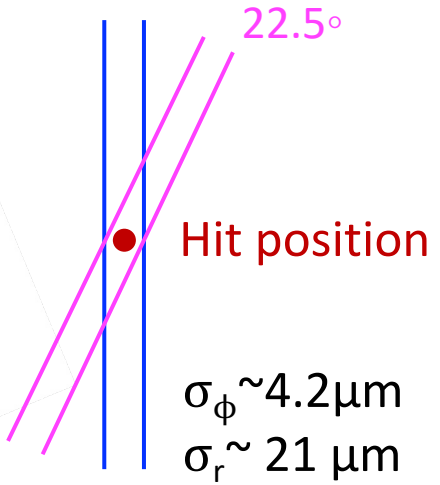


22.5◦ half endcap



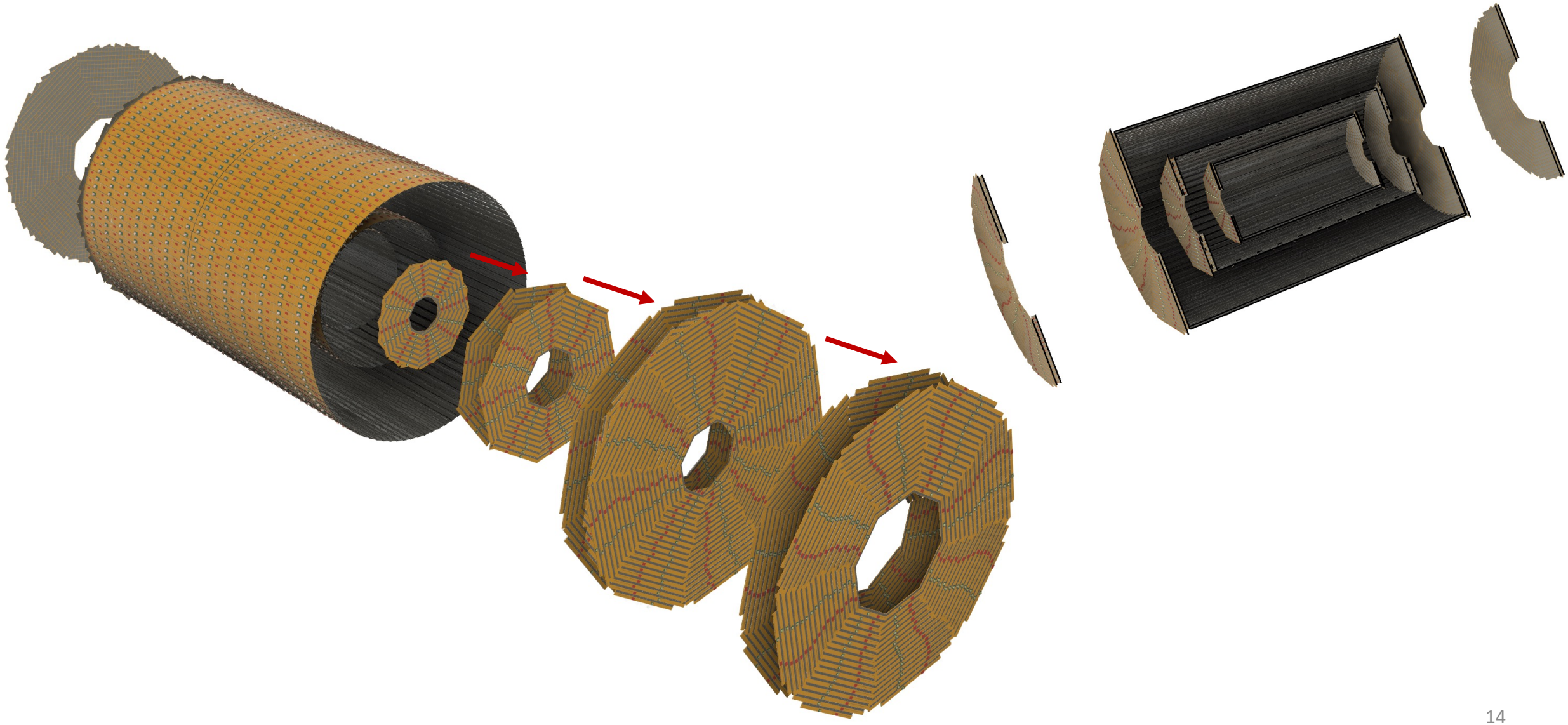
Two half endcaps are rotated 22.5° relative to each other to form one complete endcap:

- Minimize track ambiguity
- Maximize track resolution in bending direction ϕ

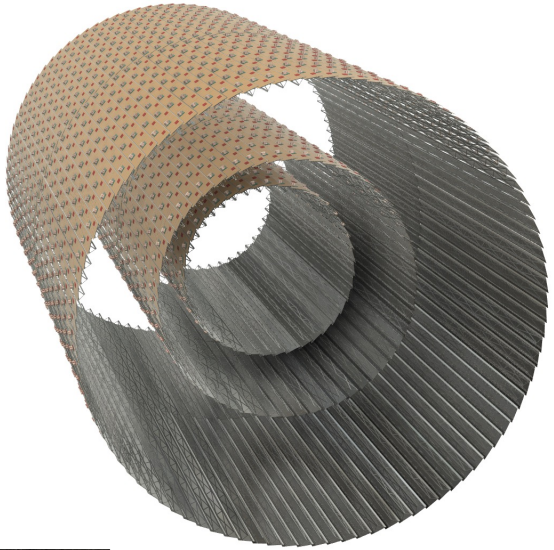


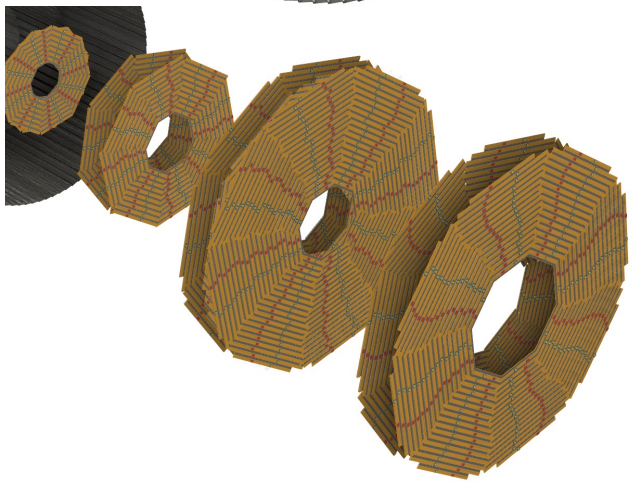
Basic detect concept

Full ITK with 3 Barrels and 8 Endcaps



ITK Barrel and Endcap Detector Components





Barrels	Modules/Stave	Staves	Modules	Sensors	Sensor area
ITKB1	7	40	280	3920	1.6 m^2
ITKB2	10	58	580	8120	3.2 m^2
ITKB3	14	96	1344	18816	7.5 m^2
Total		194	2204	30856	12.3 m^2

Endcaps	Module Types	Sensors	Sensor area
ITKE1	5	1568	0.76 m^2
ITKE2	7	3168	1.53 m^2
ITKE3	15	9568	4.62 m^2
ITKE4	12	8416	4.06 m^2
Total	18	22720	10.97 m^2

The total power consumption of the chips (excluding other electronic components) is 24.6 kW for barrels and 21.9 kW for endcaps (200 mW/cm^2).

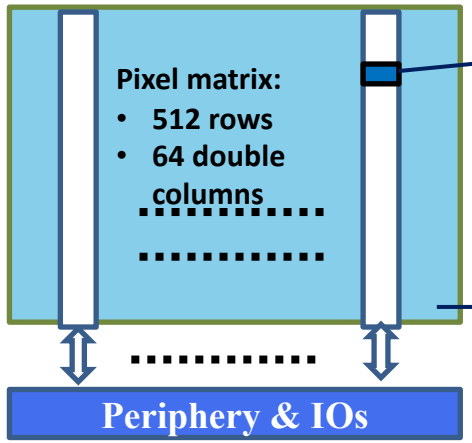
CMOS Chip Parameters Summary

	HVCMOS Pixels (Barrel)	CMOS Strips (Endcap)
Pixel Size (Strip Pitch Size)	$34 \times 150\ \mu m^2$	20 µm
Chip size	$2 \times 2\ cm^2$ (active area: 1.92x1.74 cm^2)	2.1×2.3 cm^2 (active area: 2.05x2.05 cm^2)
Array size (Strip number)	512 rows × 128 columns	1,024
Spatial resolution	σ_φ ~8 µm, σ_z~40 µm	σ_φ~4.2 µm, σ_r~21 µm
Timing resolution	~3-5 ns	~3-5 ns
Data size per hit	42 bit (14b BXID*, 7b+9b address, 6b TOT, 5b fine TDC, 1 polarity*)	32 bits (10b BXID, 10b address, 6b TOT, other 6 bits)
Event rate / chip	??? (background?) up to 1.28 Gbps	Maximum~0.25Gbps (pair production)
LV / HV	1.2V / 150 V	1.5V / 150 V

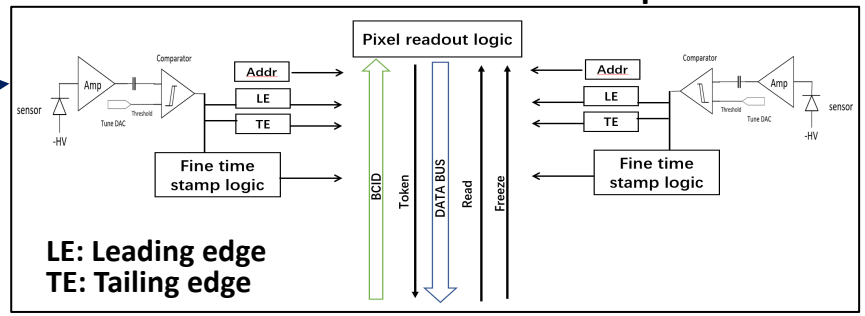
* To be reduced

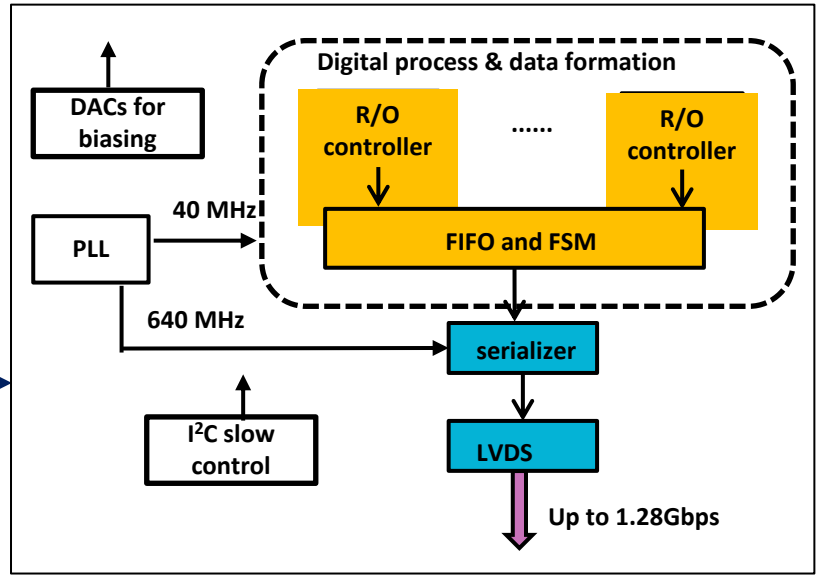
CMOS Chip Front-End Electronics

Pixels

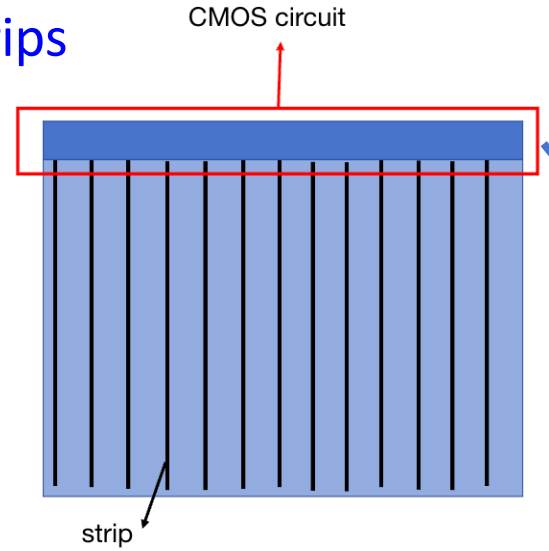


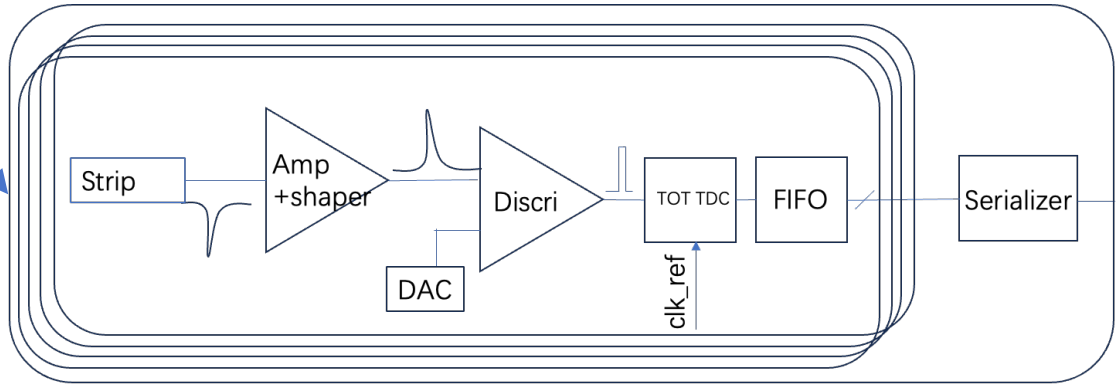
Schematic of a HV pixel sensor



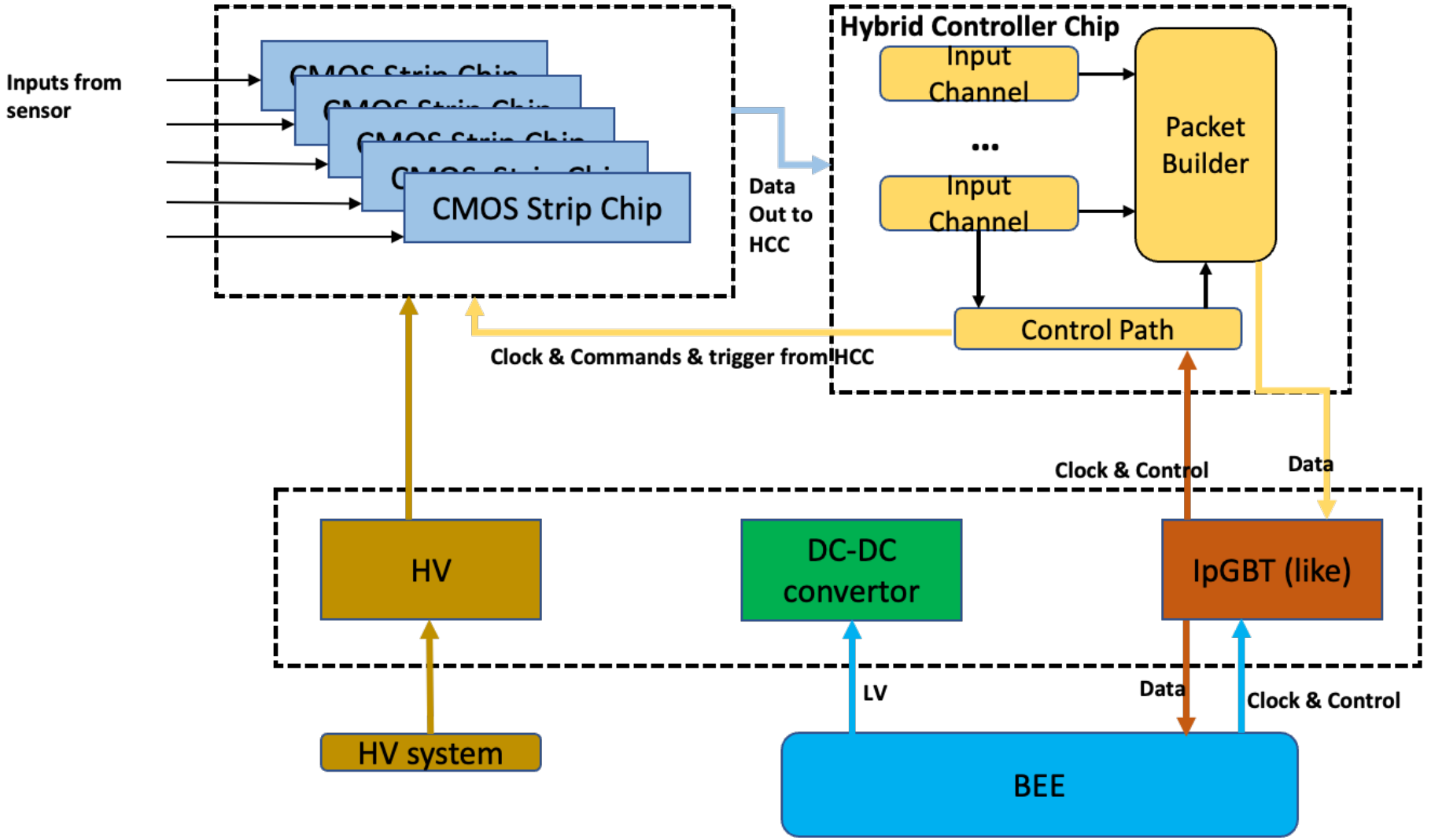


Strips





ITK Electronics Design

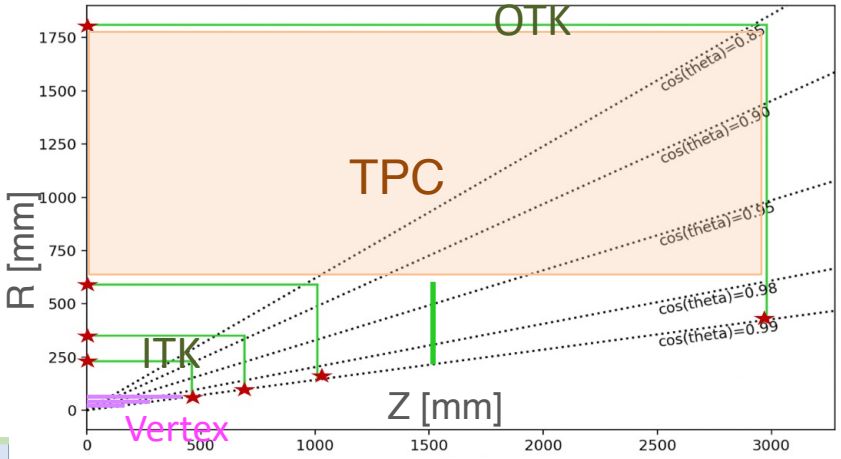


Cost Estimation

Category	Item	Total (10k CNY)	Unit cost (CNY)	Unit	Quantity	Note
Barrels (HVCMOS Pixels): 12.3 m^2 sensor area						
Sensor chip	Sensor chip	1278	18,000	Wafer	710	assume 50% yield
Common electronics	Hybrid PCB	154	700	Piece	2204	
	Optical fibre	44	200	20m	2204	
	Optical connector	441	2,000	Piece	2204	
	PCB connector	22	100	Piece	2204	
	Power cable	88	400	20m	2204	
Total		**2027**				
Endcaps (CMOS Stirps): 10.97 m^2 sensor area						
CMOS Strip Chip	Sensor chip	851.2	8000	Wafer	1064	assume 50% yield
Common electronics	Hybrid Flex	118.72	700	Piece	1696	
	Optical fibre	0.2	200	20m	10	
	Optical connector	339.2	2,000	Piece	1696	
	Hybrid connector	16.96	100	Piece	1696	
	Power cable	0.4	400	20m	10	
Total		**1326.68**				

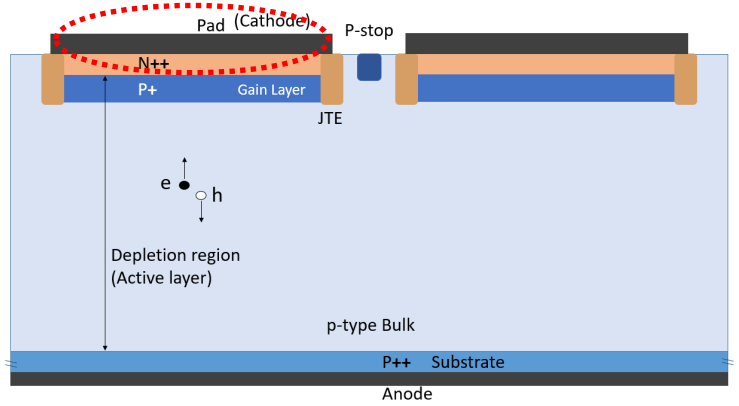
Technology Survey and Our Choices for OTK

- Outer silicon tracker (+TOF)



LGAD (Low-Gain Avalanche Diode)

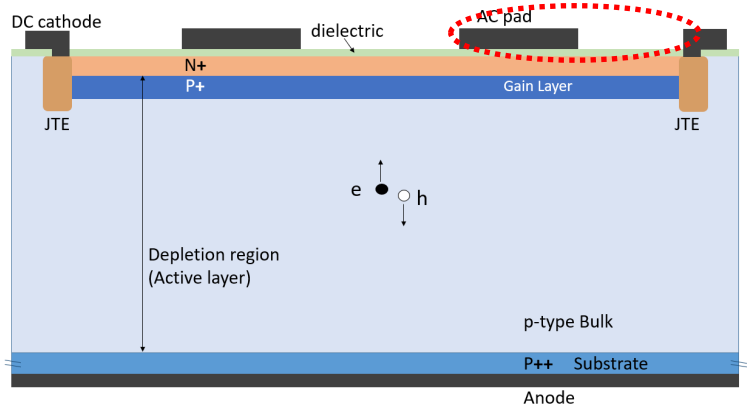
Segmented gain layer



- The read-out electronics is connected to the N++ layer
- Time resolution ~ 30ps
- Position resolution: pixel size/$\sqrt{12}$

AC-LGAD (AC-coupled LGAD)

Continuous gain layer



- Metal AC-pads separated from the N+ layer by a thin dielectric (Si_3N_4, SiO_2)
- Time resolution ~ 30ps
- Position resolution: 5~10 um

– AC-LGAD strip sensor:
  - Strip pitch size: 100 µm
  - Long strip length: 70 mm
  - sector sensor for endcap
– High time precision ASIC:
  - 40-48 bit TDC
  - Low power consumption
  - Fast timing

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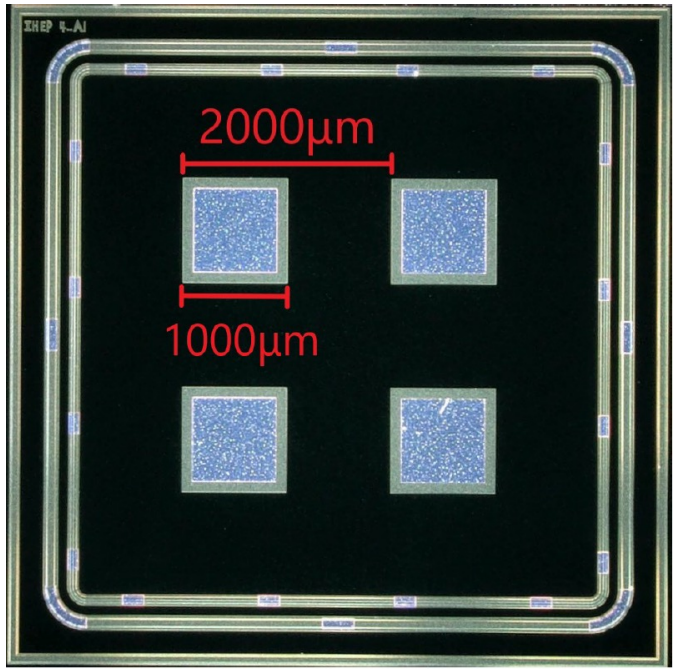
R&D：AC-LGAD Sensors Development at IHEP

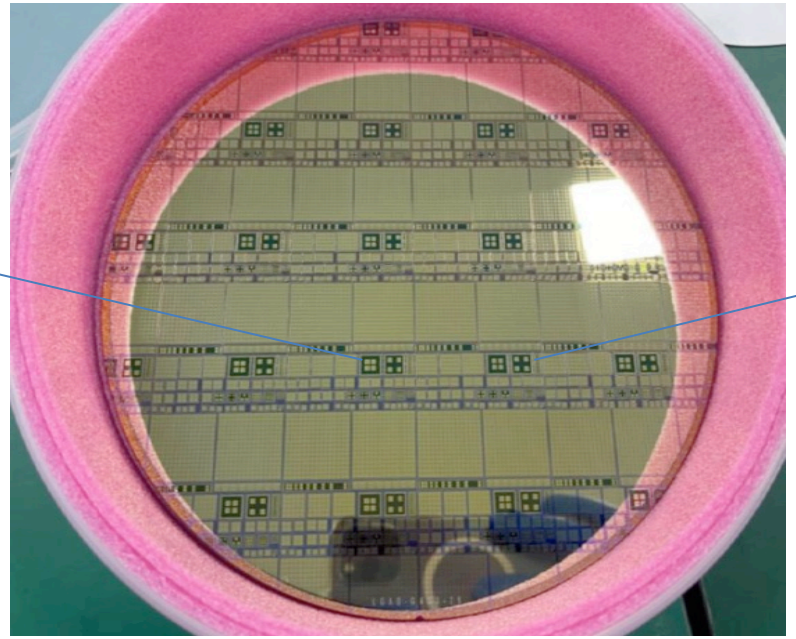
Pixels AC-LGAD：

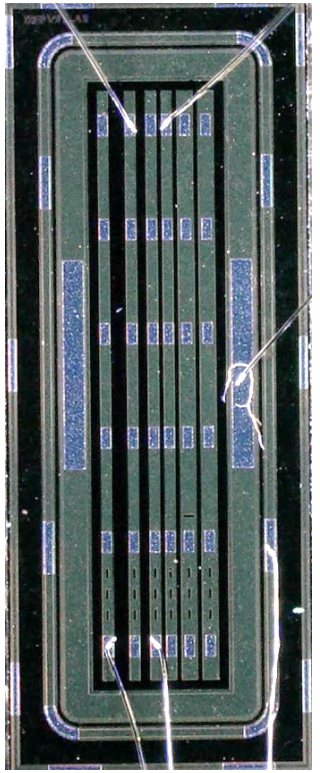
- Position information： 1 layer
- Pitch size 2000 μm, pad size 1000 μm
- Different N+ dose ：
  - **10P， 5P， 1P， 0.5P， and 0.2P**

Strips AC-LGAD：

- Position information： 2 layer
- Strip length 5.6mm, width 100 μm
- Different pitch size：
  - **150 μm, 200 μm, and 250 μm**







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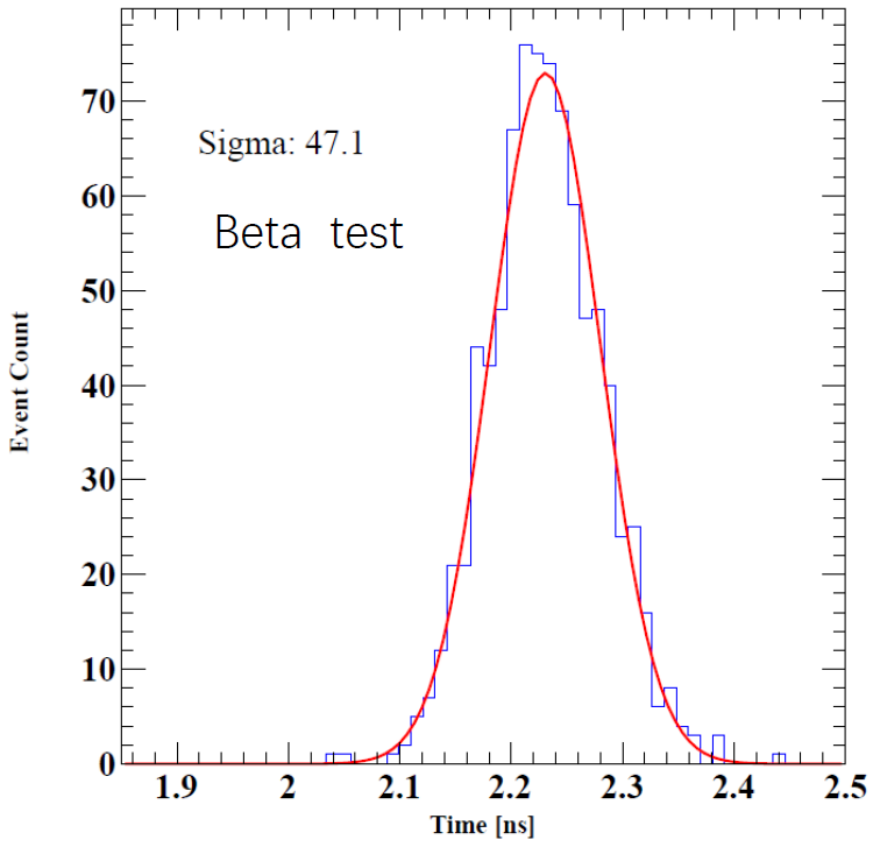
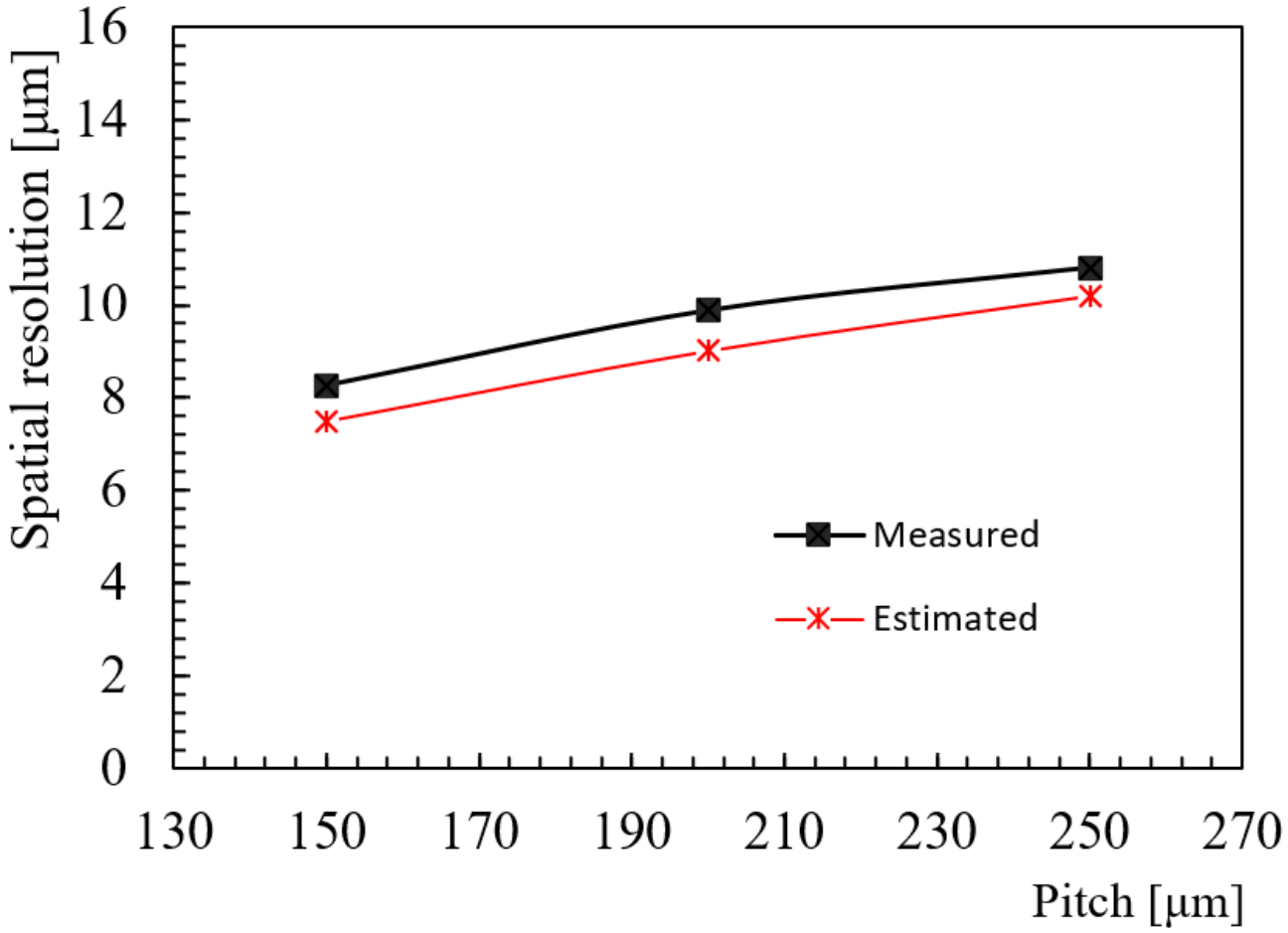
AC-LGAD Performance: Time and Spatial Resolution



Time residual sigma: 47.1 ps

Time resolution: 37.5 ps



Spatial resolution: 8 μm for 150 μm strip pitch size

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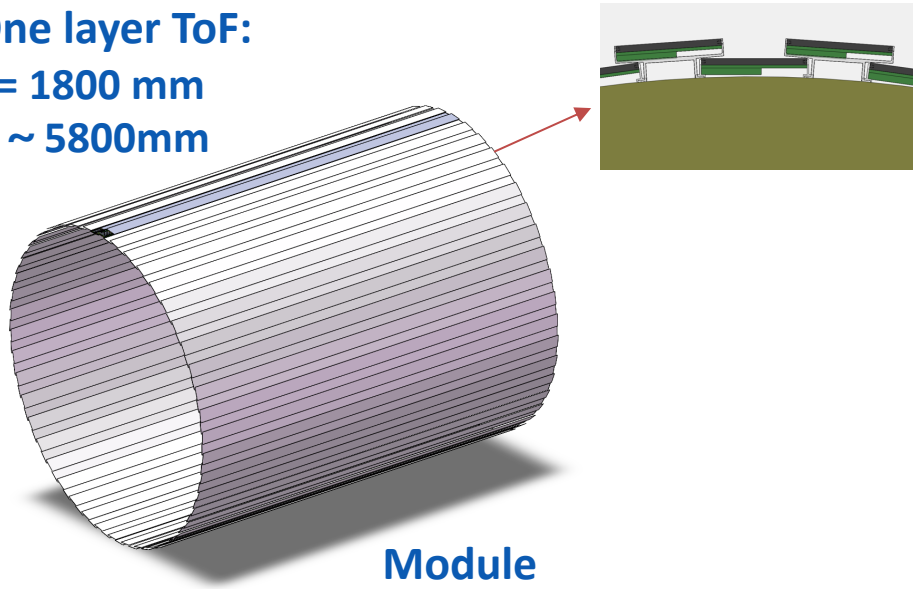
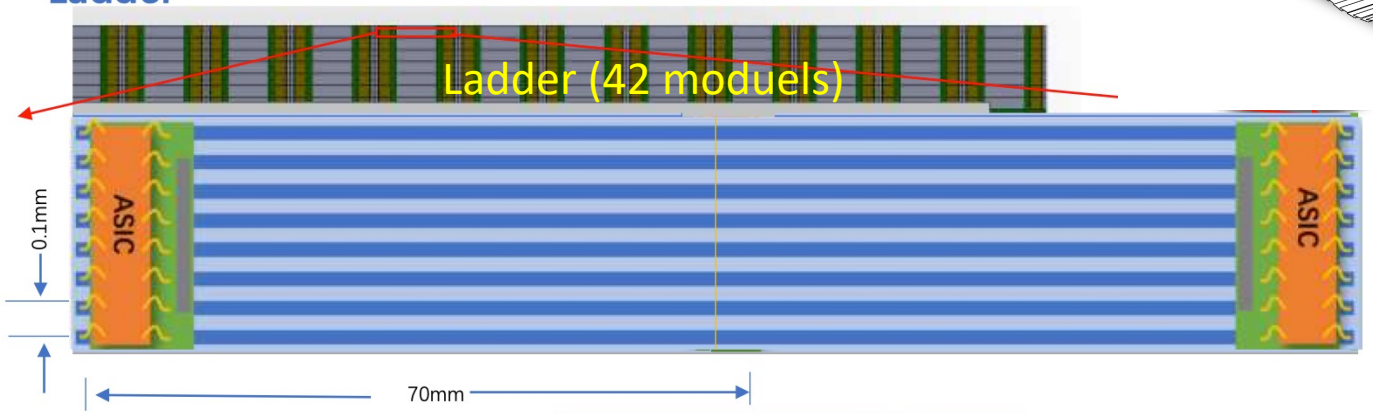
OTK Barrel Design

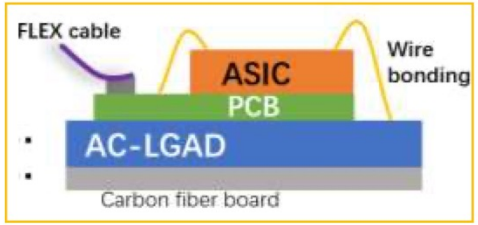
- 90 ladders (total area: 70 m²)
- Each ladder has 42 modules
- Each module has 28 ASICs
- Each ASIC has 128 channels

One layer ToF:
R= 1800 mm
H ~ 5800mm

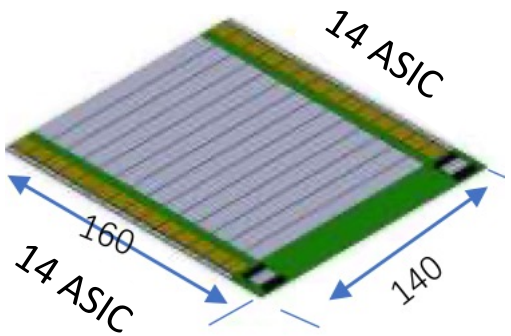


Ladder



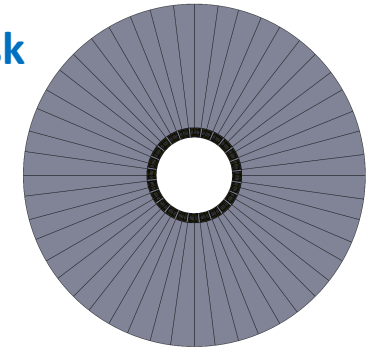


Module
140mm x 160mm

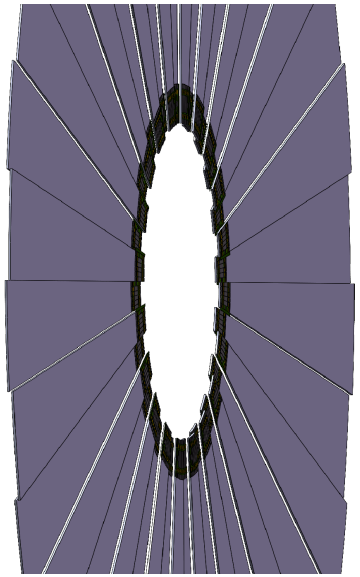


OTK Endcap Design

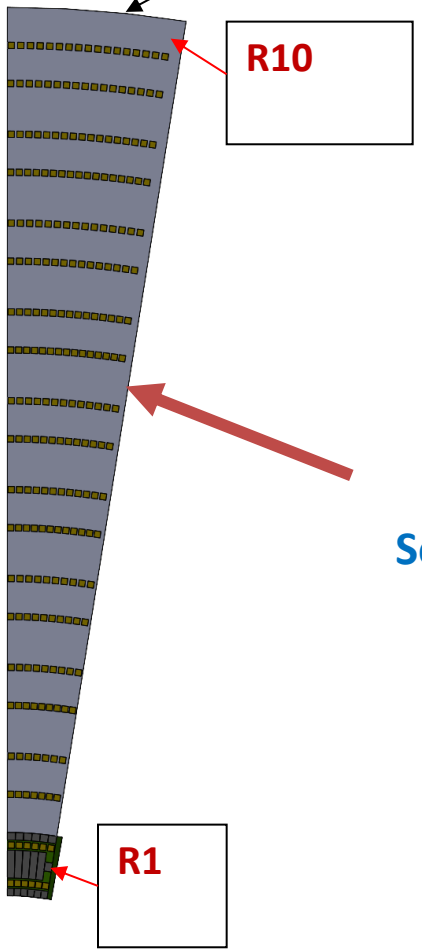
Disk



overlap arrangement

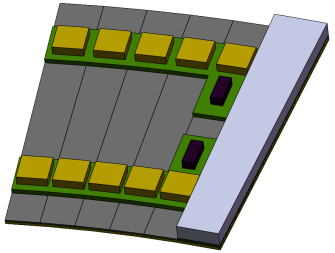


Petal

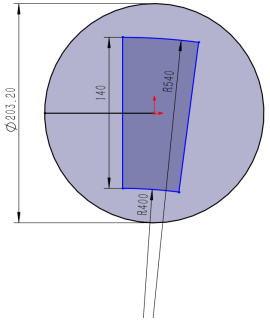


- Total area: 19.4 m^2
- Double layers to reduce the dead area
  - ✓ 24 petals/layer
  - ✓ 10 rows/petal,
  - ✓ 7.5° per row,
  - ✓ Overlap 0.5°/petal
- 140 mm / row at R direction

Sector Module per row

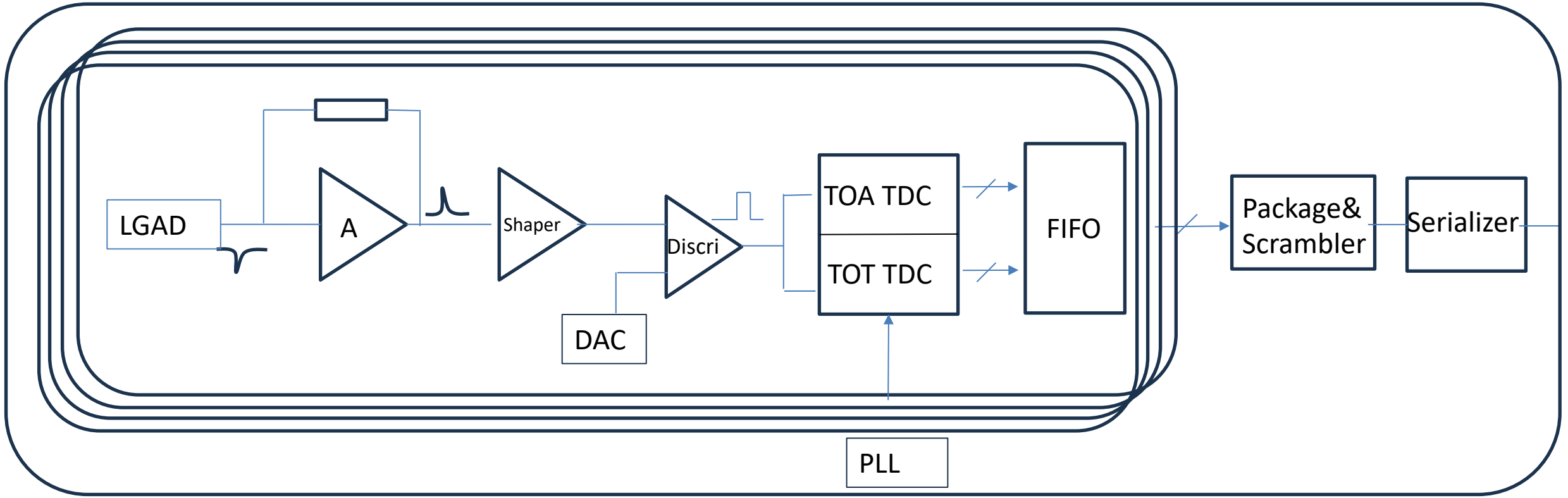


Sector/wedge shape sensor in the 8 inch wafer



R1: 52.36 mm-70.69 mm

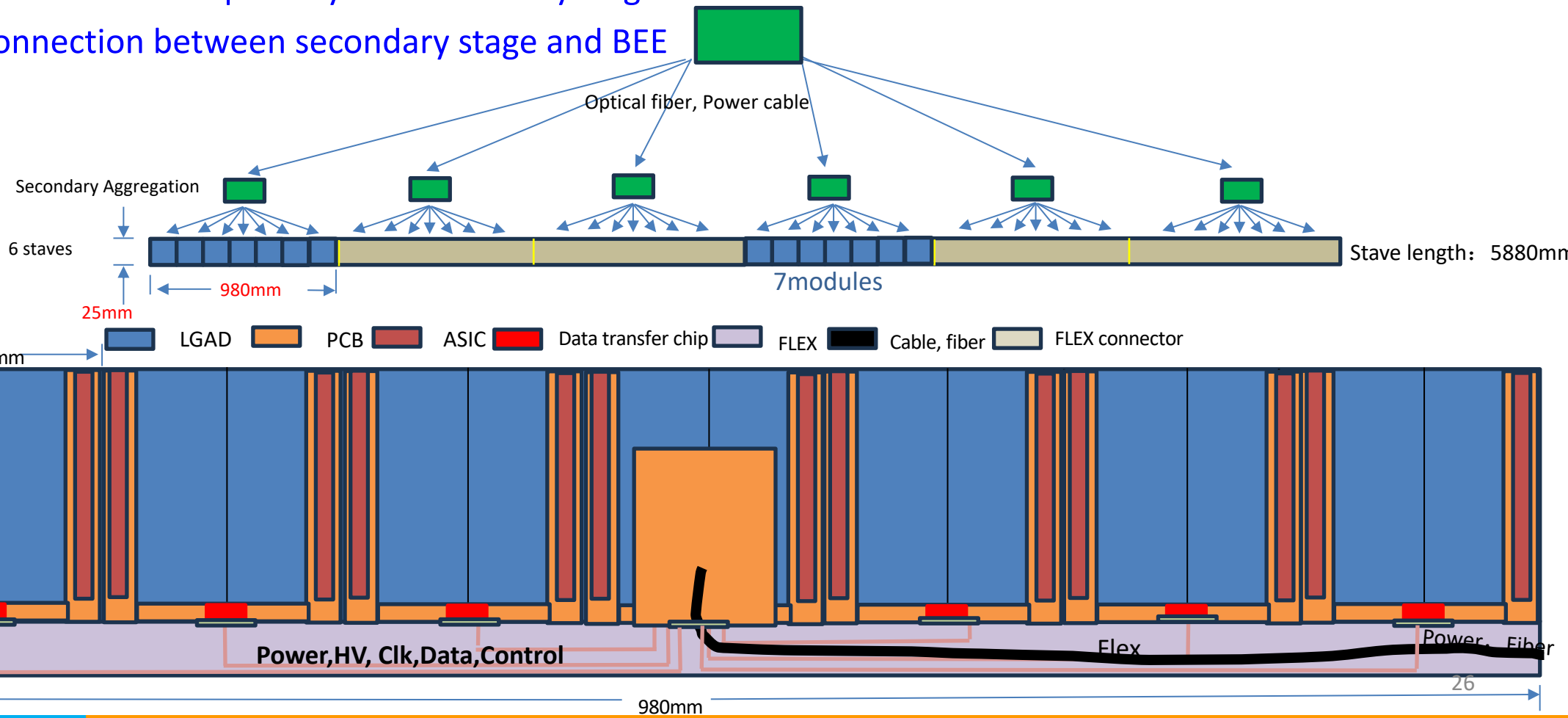
OTK Front End Electronics



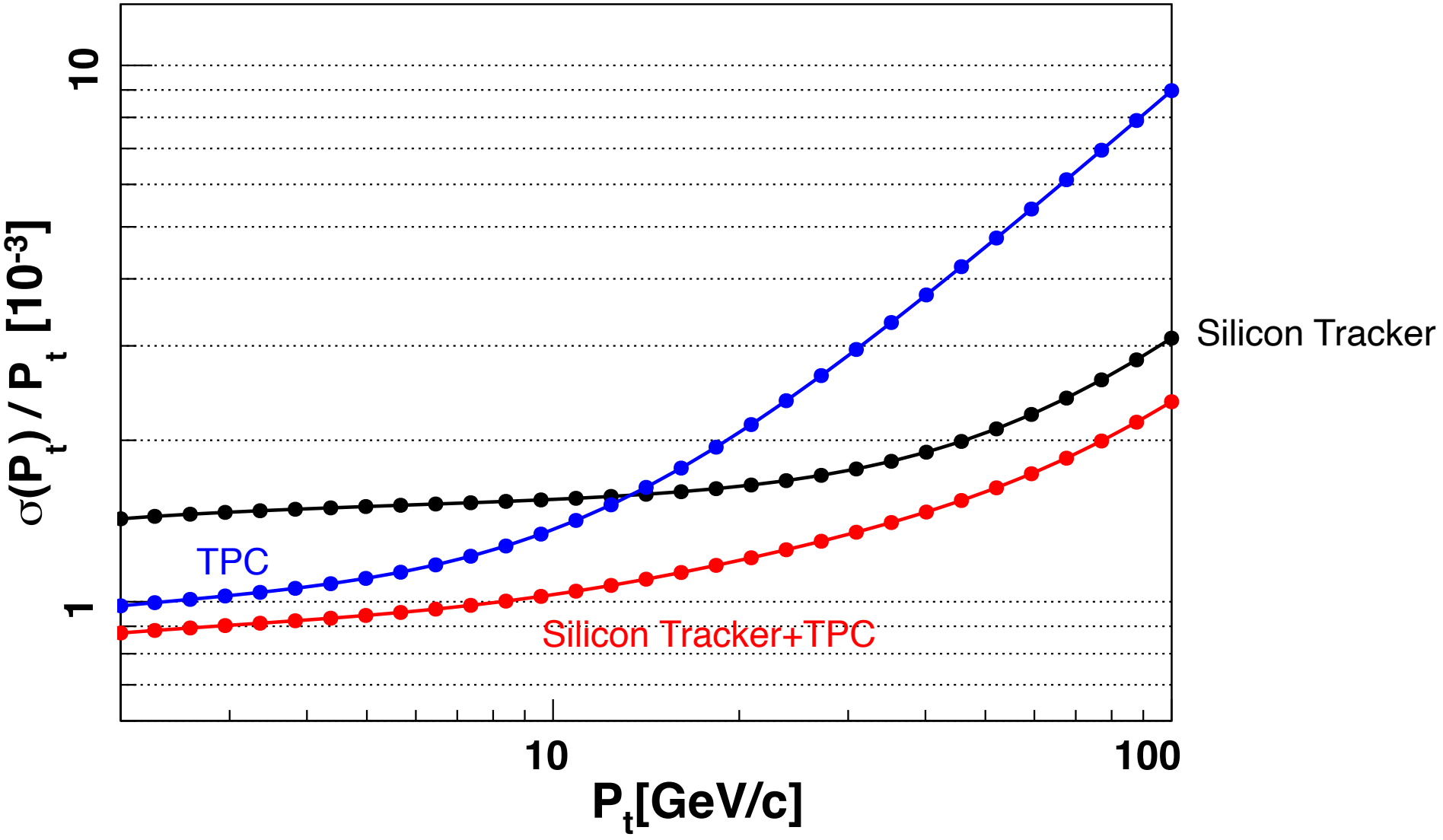
TOA for arrival time
TOT for charge measurement and time walk correction

OTK Electronics Design

- Provide LV and HV for module independently
- Primary aggregation adapts the data rate between the ASIC and LpGBT_like interface
- Flexible connection between primary and secondary stages
- Optical fiber connection between secondary stage and BEE



Full Tracker Performance from Simulation: Momentum Resolution



HVCMOS Pixels Research Team in China

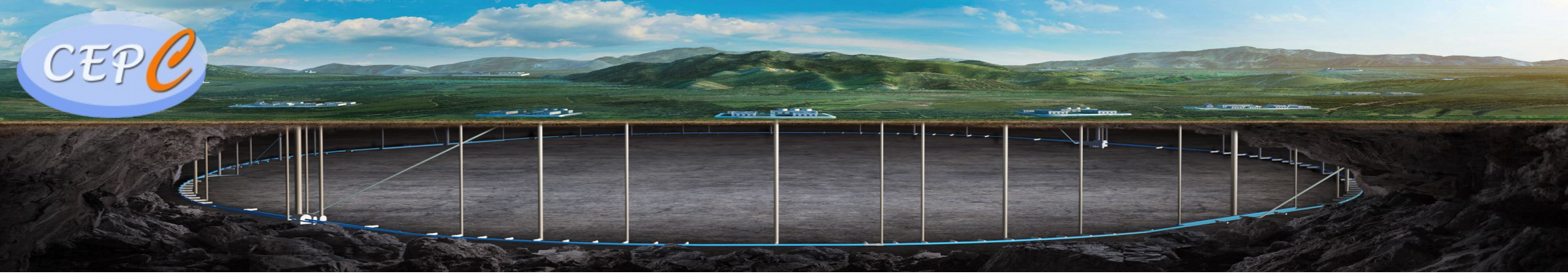
- IHEP
  - Jianchun Wang, Yiming Li, Yang Zhou, Weiguo Lu, Mei Zhao, Zijun Xu, Xiongbo Yan, Jinyu Fu (Postdoc & Students) Zhiyu Xiang, Kunyu Xie, Xiaojie Jiang, Shuqi Sheng, …
- Shandong U
  - Meng Wang, (Students) Leyi Li, Qinglin Geng
- Zhejiang U
  - Hongbo Zhu, (Students) Jianpeng Deng, Pengxu Li
- Hunan U
  - Zhuojun Chen, Jiesheng Yu
- Northwestern Polytechnical University
  - Xiaomin Wei, (Students) Yinghua He …
- Dalian Minzu
  - Zhan Shi, (Students)Yang Chen, Yujie Wang
- Nanjing U
  - Lei Zhang, (Student) Xiaoxu Zhang

CMOS Strips Research Team in China

- IHEP
  - Staff: Xin Shi, Qi Yan, Weiguo Lu, Mei Zhao, Xiongbo Yan, Jinyu Fu
  - Postdoc & Students: Chengwei Wang, Yuxing Cui, Zhan Li, Sen Zhao, Chenxi Fu, Kaibo Xie, Yihan Zhang, Shoudong Luo
- Zhejiang U
  - Shoudong Luo

Working Plan

- HVCMOS Pixel Chip - R&D
  - COFFEE3: Key module validation, small chip like COFFEE2
  - COFFEE4: Quarter chip, to validate full column readout
  - COFFEE5: Full size and full function chip
- CMOS Strip Chip - R&D
  - CSC1: Passive CMOS strip sensor and seperate front-end electronics CMOS circuit
  - CSC2: Small size and large pitch prototype
  - CSC3: Full size and full function chip
- Module Assembly - R&D
  - Assembly
  - Electrical Testing



Thank you for your attention!

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