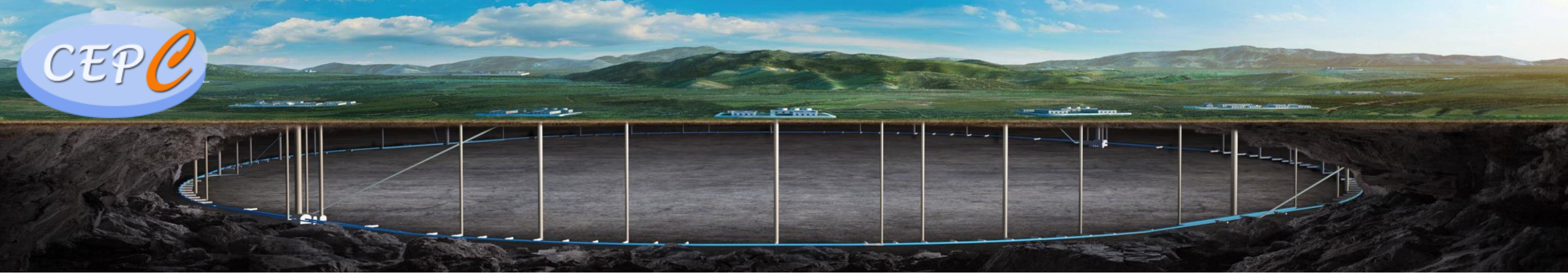

# CEPC Electronics System

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# Content

- Introduction
- Requirements
- Technology survey and our choices
- Technical challenges
- R&D efforts and results
- Global framework of the electronics system
- Detailed design for common electronics
- Research team and working plan
- Summary

# Introduction

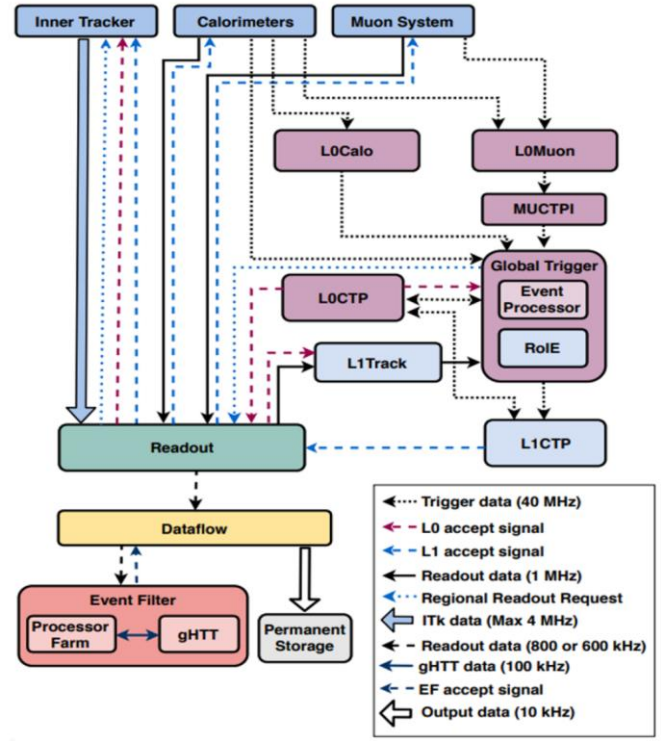
- This talk is about the consideration of the general framework of the electronics system for the Ref-TDR of CEPC.
- The general or common electronics blocks, including the consideration of data aggregation, data transmission, powering, and common backend electronics board, will also be introduced.
- Some considerations on backup schemes, including the innovative scheme based on wireless communication, and the conventional schemes based on traditional trigger, will also be discussed.
- This talk relates to the Ref-TDR Ch 11.

# Requirement

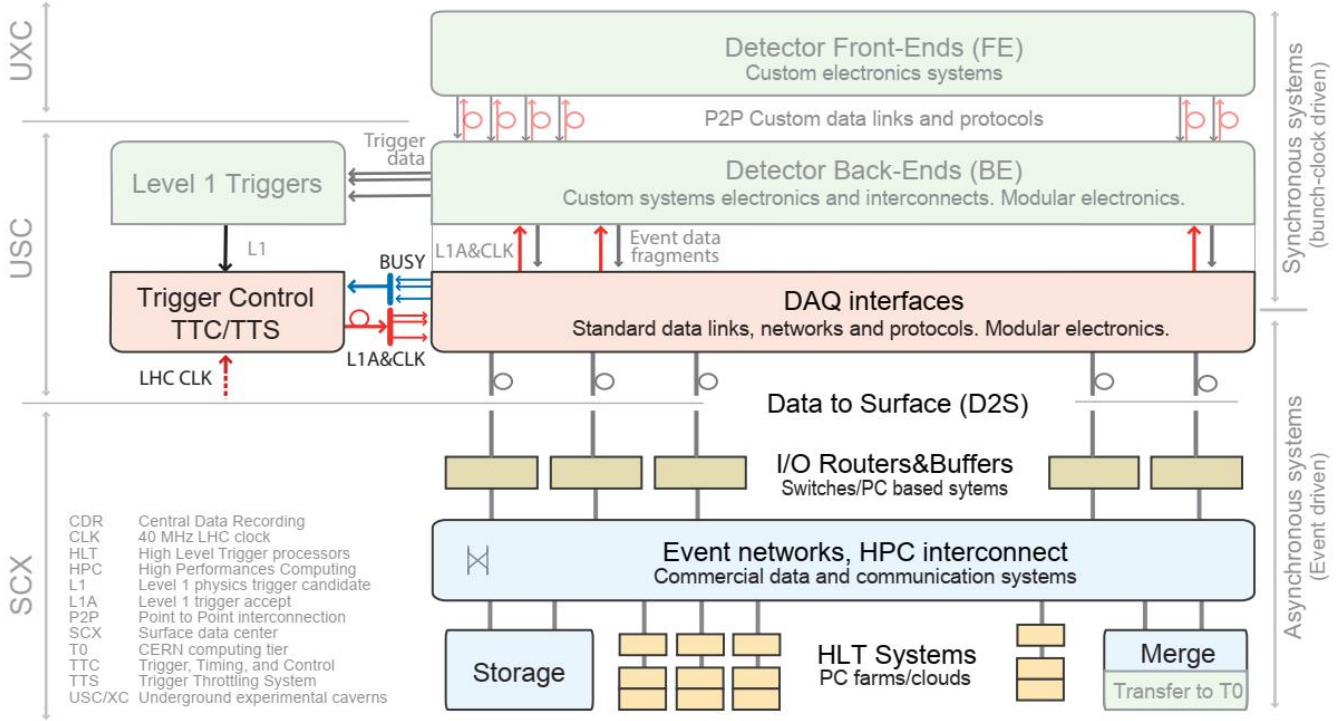
| | Vertex | Pix(ITKB) | Strip (ITKE) | TOF (OTK) | TPC | ECAL | HCAL |
|---|---|---|---|---|---|---|---|
| Channels per chip | 512*1024 Pixelized | 512*128 (2cm*2cm@34um*150um) | 512 | 128 | 128 | 8~16 | 8~16 |
| Ref. Signal processing | XY addr + BX ID | XY addr + timing | Hit + TOT + timing | ADC+TDC/TOT+TOA | ADC + BX ID | TOT + TOA/ ADC + TDC | TOT + TOA/ ADC + TDC |
| Data Width /hit | 32bit (10b X+ 9b Y + 8b BX + 5b chip ID) | 48bit （9b X+7b Y +14b BX + 6b TOT + 5TOA + 4b chip ID） | 32bit (10b chn ID + 8b BX + 6b TOT + 5b chip ID) | 40~48bit （7b chn ID + 8b BX + 9b TOT + 7b TOA+5b chip ID ) | 48bit (7b chn ID + 8b BX + 11b chip ID + 12b ADC + 10b TOA) | 48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID) | 48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID) |
| Data rate / chip | 1Gbps/chip@Triggerless@Low LumiZ Innermost | 640Mbps/chip Innermost | Avg. 1.01MHz/chip Max. 100MHz/chip | Avg：26kHz/chip @ z pole Max：210kHz/chip @z pole | ~70Mbps/modu Inmost | <4.8Gbps/module | <4.8Gbps/module |
| Data aggregation | 10~20:1, @1Gbps | 1. 1-2:1 @Gbps； 2. 10:1@O(10Gbps) | 1. 10:1 @Gbps 2. 10:1 @O(10Gbps) | 1. 10:1 @1Mbps 2. 10:1 @O(10Mbps) | 1. 279:1 FEE-0 2. 4:1 Module | 1. 4~5:1 side brd 2. 7*4 / 14*4 back brd @ O(10Mbps) | < 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC) |
| Detector Channel/module | 2218 chips @long barrel | 30,856 chips 2204 modules | 22720 chips 1696 modules | 41580 chips 1890 modules | 258 Module | 1.1M chn | 6.7M chn |
| Data Volume before trigger | 2.2Tbps | 2Tbps | 22.4Gbps | 1Gbps | 18Gbps | 164.8Gbps | 14.4Gbps |

- The first requirement from detector is to readout all the FEE data to the BEE, while keeping all necessary information for trigger
- Data volume at the module level, data format, and the module data organization were summarized in the table

# Technology survey on global framework




ATLAS Trigger framework

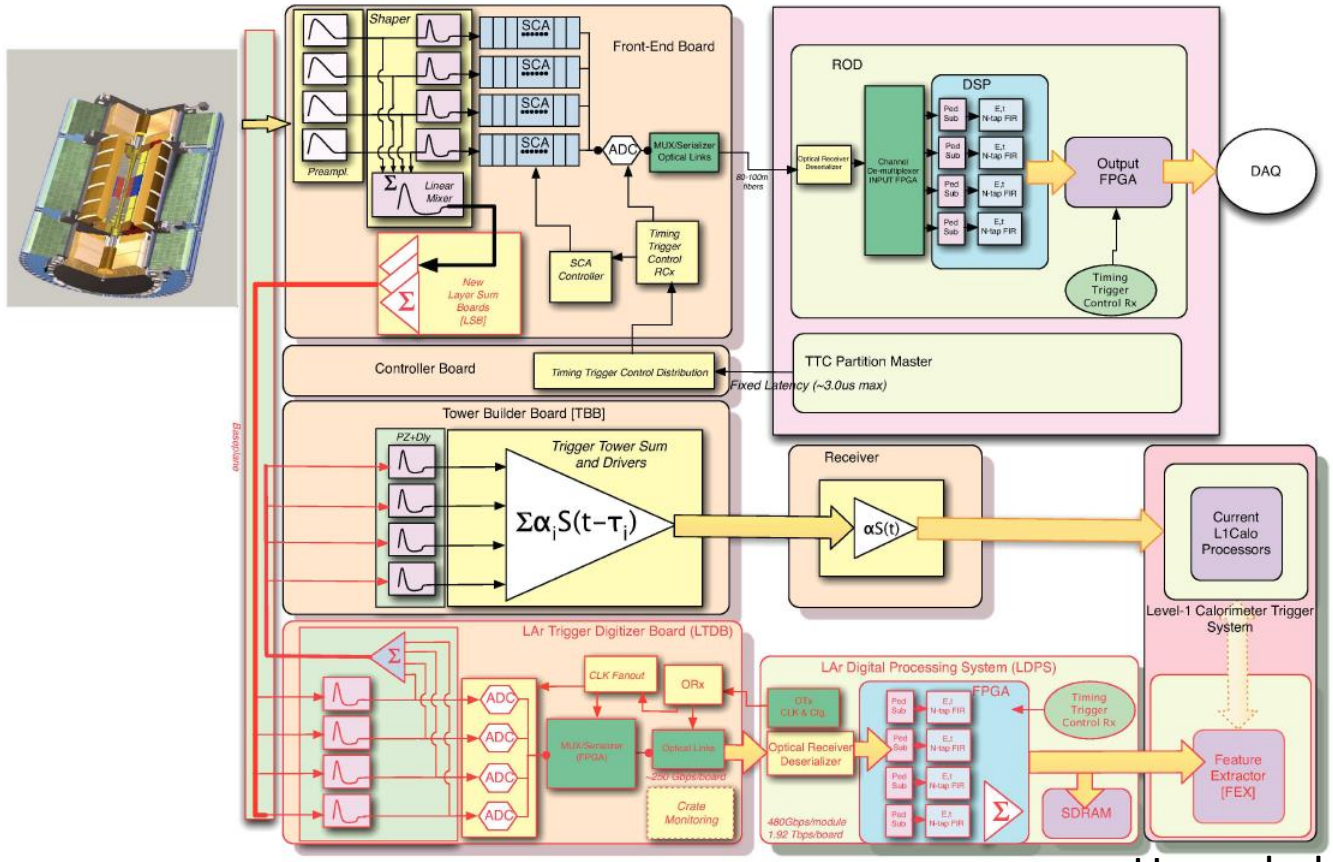



CMS Trigger framework

- Two main reference frameworks of Electronics-TDAQ system are ATLAS & CMS Trigger system.
- While ATLAS is more like “Frontend trigger” that FEE provides the trigger information, the CMS is more like “Backend trigger” that trigger system communicates only with BEE.

# Technology survey on global framework

ATL-CAL-PROC-2017-001

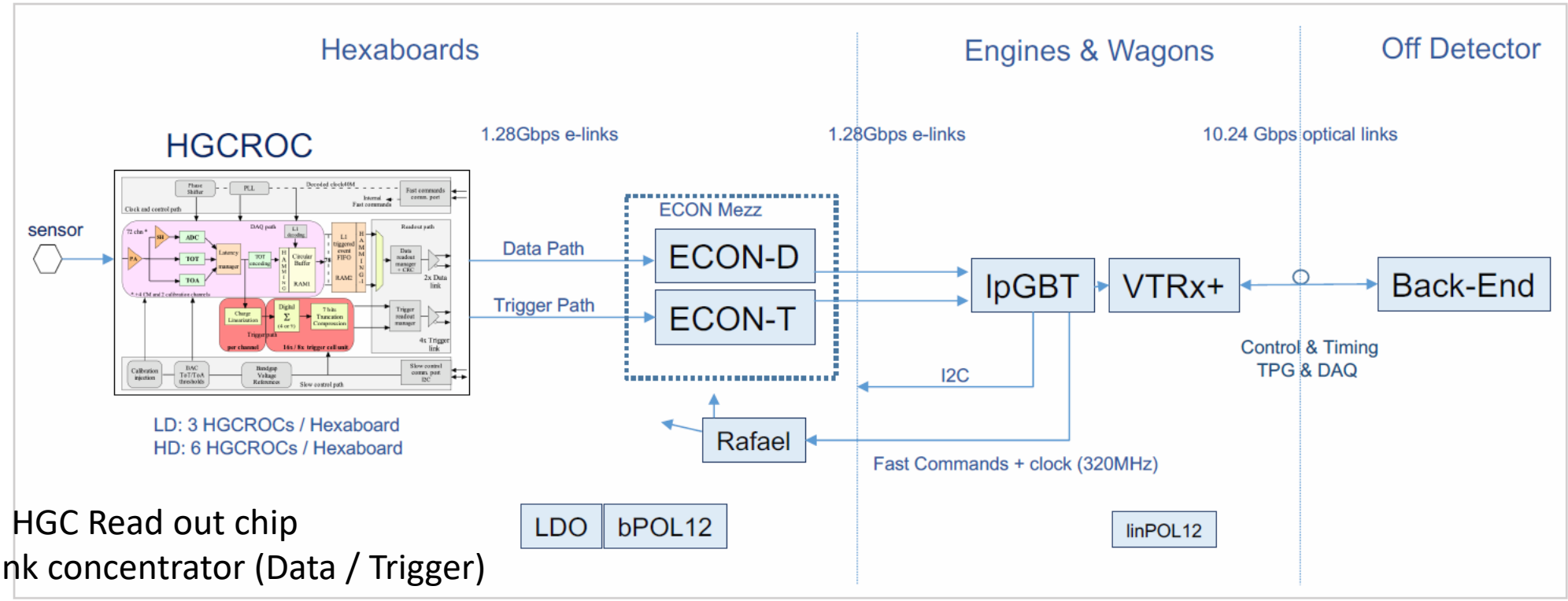



Upgraded LAr readout schemes for Phase-I

- A typical readout framework can be referred to ATLAS detector system(e.g. LAr CAL)
- It can be noted the FEE not only has to generate and send out trigger info.(e.g. SUM), but also store data for trigger latency and accept the trigger decision.

# Technology survey on global framework

From Paul Aspell, CMS HGCAL An Electronics Perspective




HGCROC: HGC Read out chip
ECON: elink concentrator (Data / Trigger)

- The electronics readout framework can also be inspired by CMS detector system(e.g. HGCAL).
- It can be observed that the data stream is mostly in a single direction to the BEE, and the electronics system architecture is relatively compact.

# Our choice on global framework

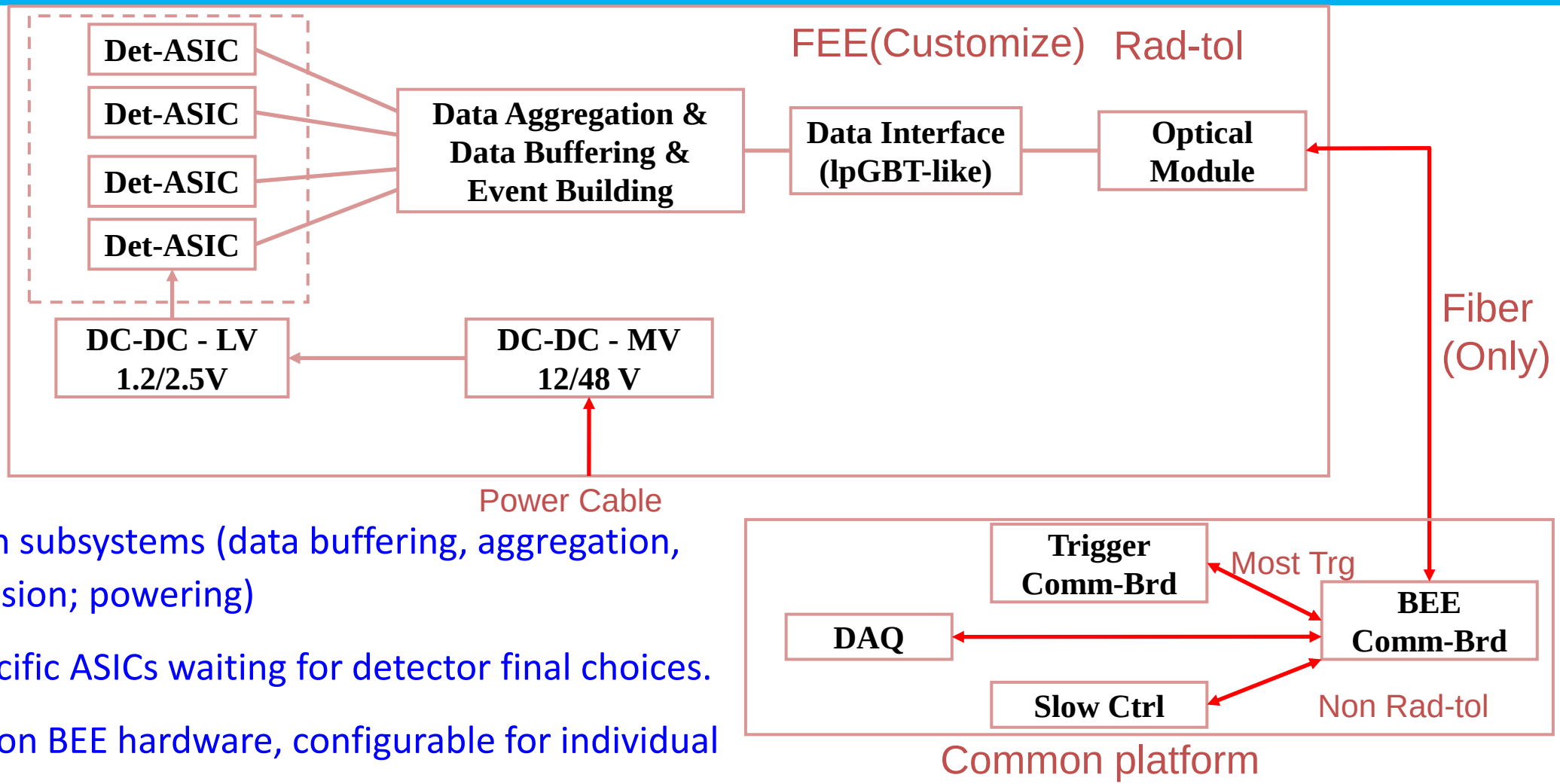
- We choose FEE-triggerless readout as our baseline global framework for the electronics and TDAQ system, for the following reasons:

1. Keep the max possibility for new physics, by readout all the information w/o pre-assumed trigger condition.
2. Sufficient headroom @ 10Gbps per link(module) kept for the data transmission, concerning the current background rate, also preserving possibility of future upgrade.
3. Speed-up the FEE-ASIC iteration & finalization process, w/o the need to consider the undefined trigger algorithm, esp. regarding the potential tight schedule.
4. Reading out all the raw data seems more convenient than storing and triggering them based on current knowledge, concerning the background, uncertain trigger latency, and dead area
5. Except the FEE-ASIC, the rest part will be designed in a unified style common to all sub-detectors, and scalable based on the detector volume.

# Main Technical Challenges

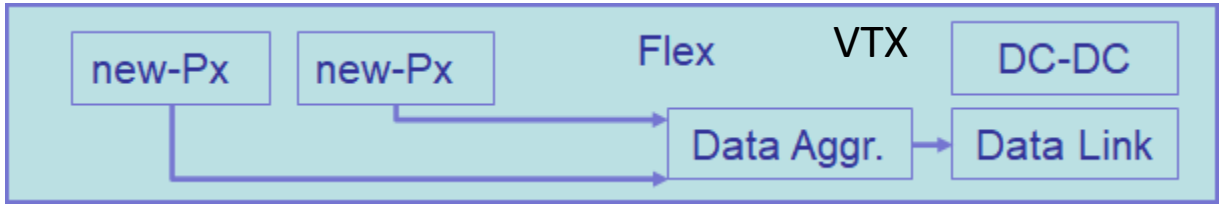
- Background rate from MDI is under optimization, the beam-induced background varies widely at the current stage, which may impact the final readout framework and scheme
- A high performance, reliable data link & optical module is the key part of the framework. It is the only path for not only data, but also high precision clocking system.

# Global framework of the Elec system

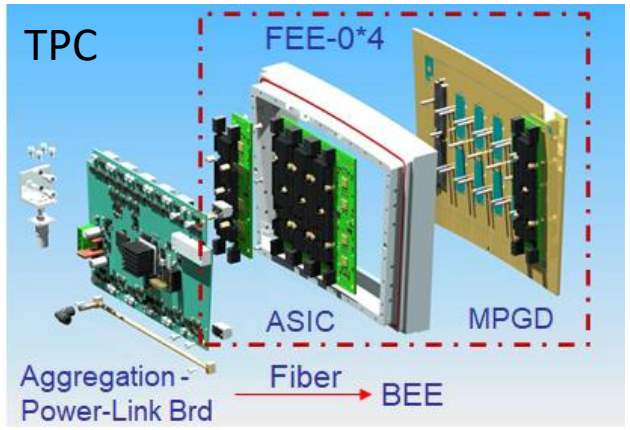


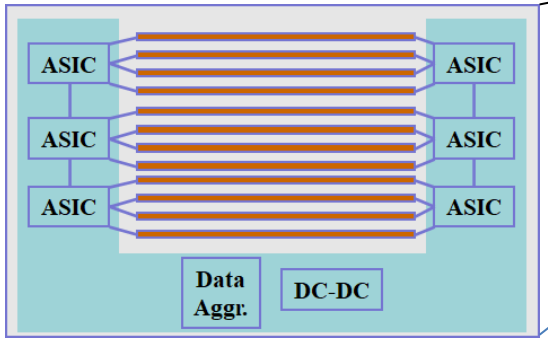

- Common subsystems (data buffering, aggregation, transmission; powering)
- Det. specific ASICs waiting for detector final choices.
- A common BEE hardware, configurable for individual subsystems.
- TDAQ interface is (probably) only on BEE

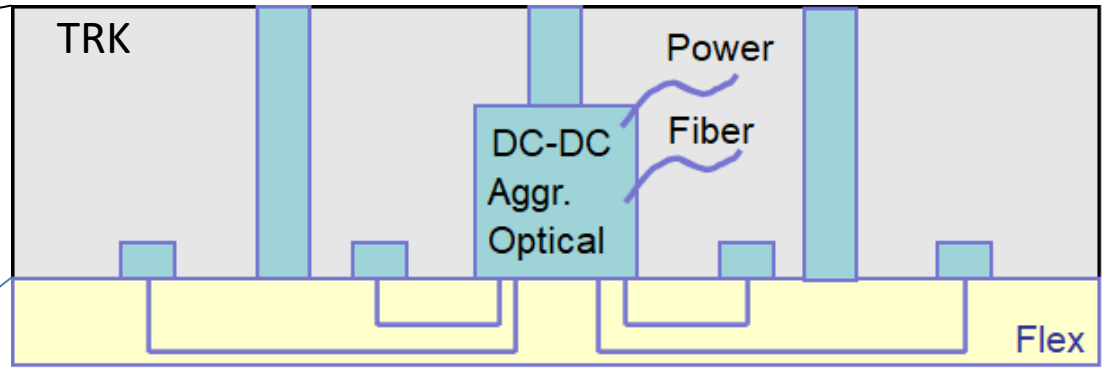
# An overview of the Sub-Det readout Elec.

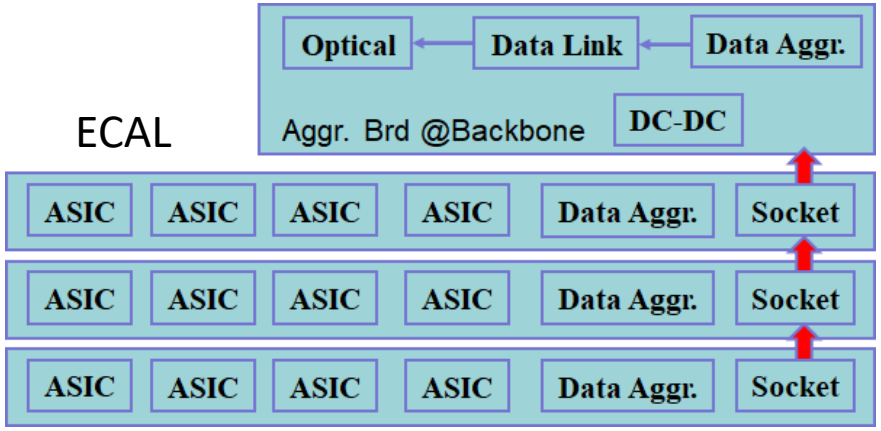


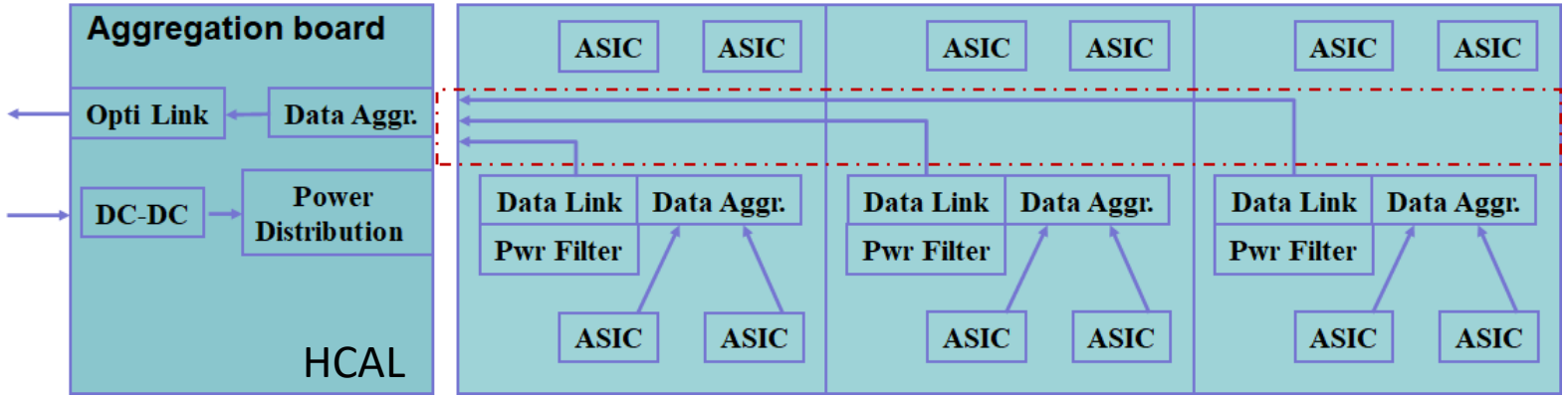

- All sub-det readout electronics were proposed based on this unified framework, maximizing possibility of common design usage.



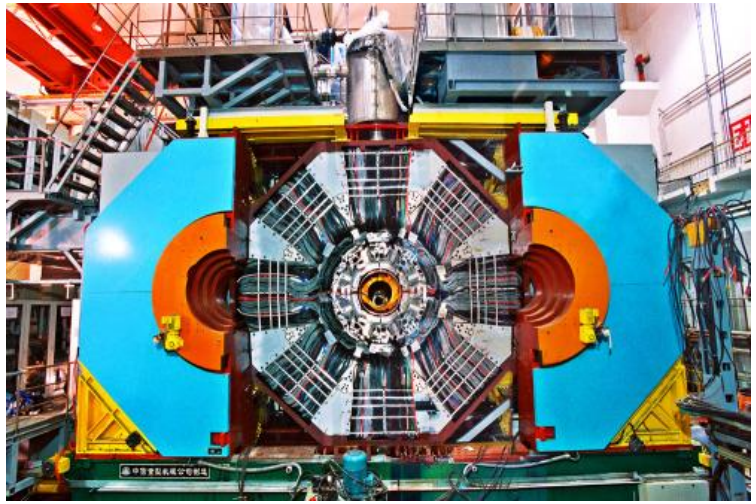



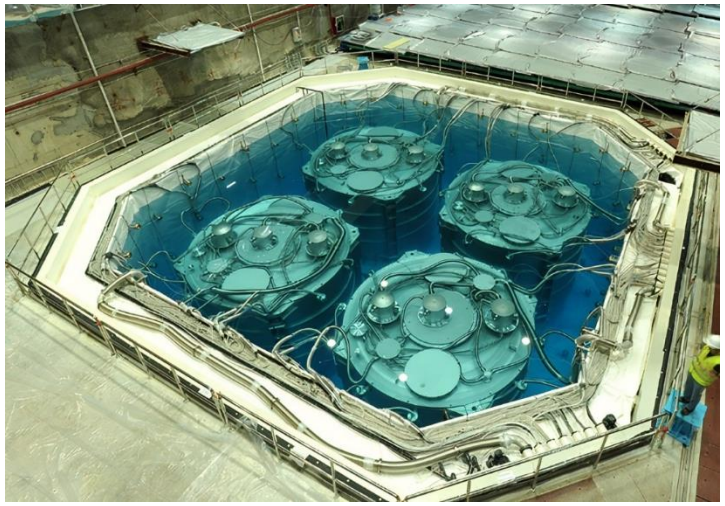



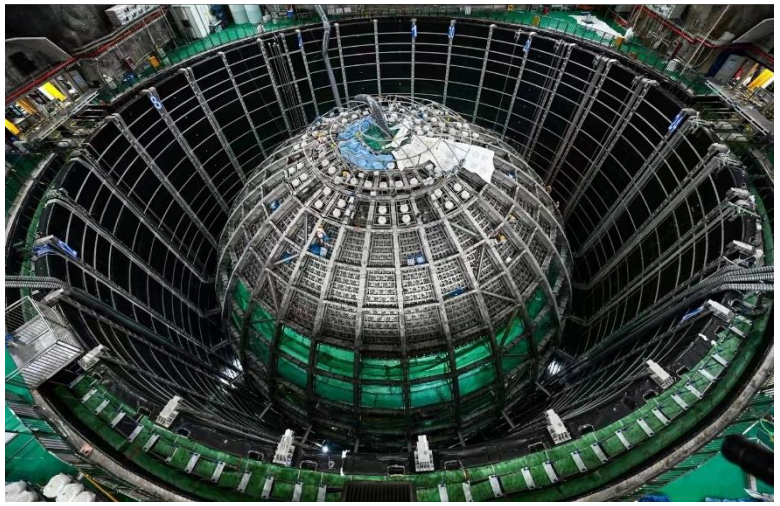
# Previous experience on electronics system



BESIII

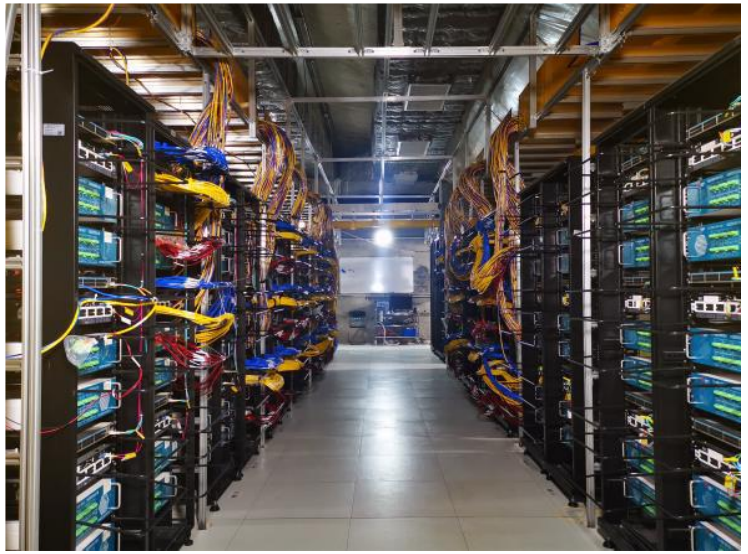


Dayabay experiment



JUNO experiment

- Our team have developed the electronics systems of most of the major particle physics experiments in China, including BESIII, Dayabay, JUNO, LHAASO…
- We have extensive experience in typical electronics system design from the FEE to BEE

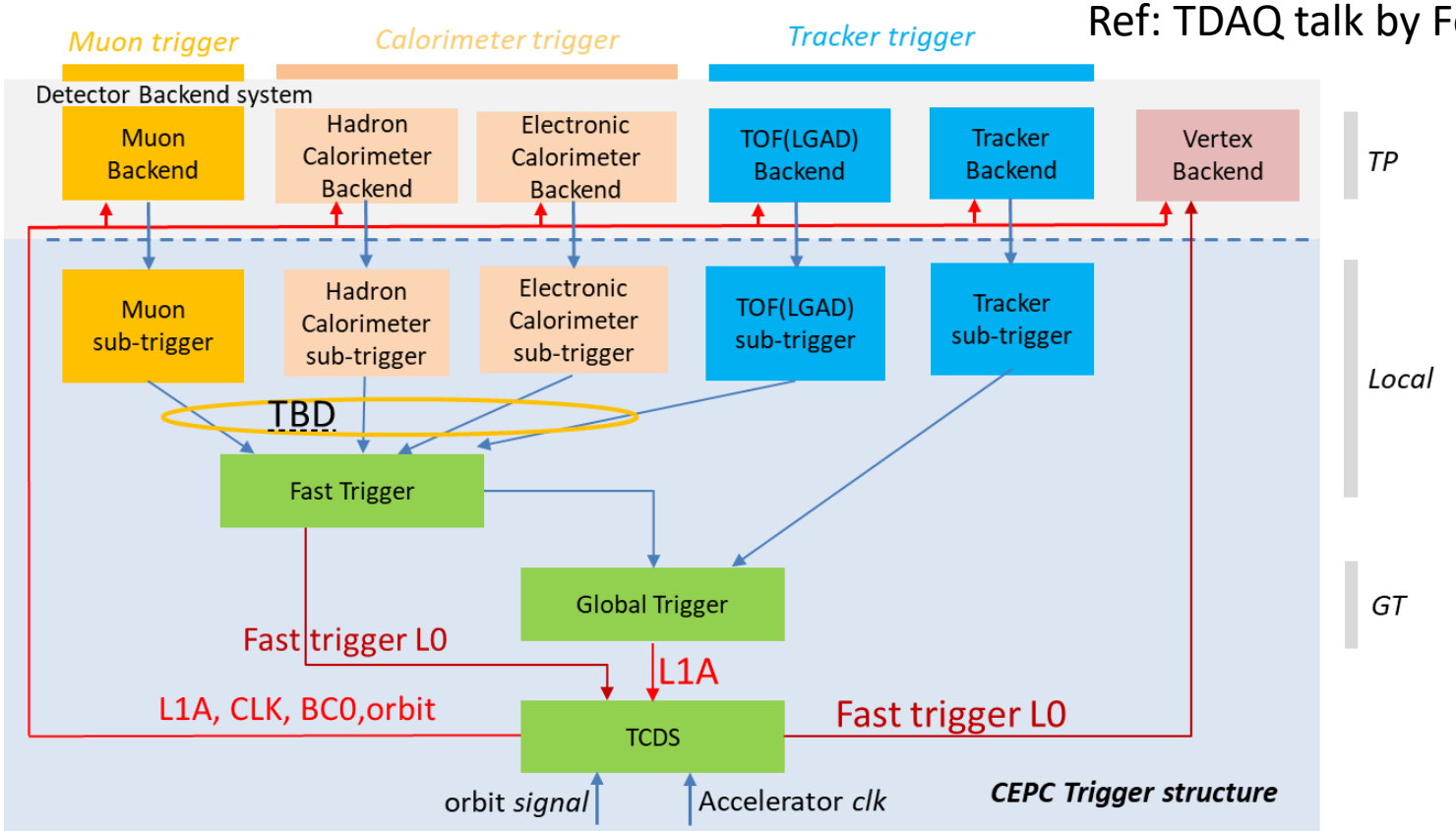


# Backup scheme of the framework

- The proposed framework was based on the estimated background rate of all sub-det.
- In case of under-estimation or unexpected condition:

1. Additional optical links can be allocated to the hottest module.
2. In case the background rate is too high for FEE-ASIC to process, Intelligent Data Compression algorithm can be integrated on-chip, for the initial data rate reduction.

Ref: TDAQ talk by Fei Li



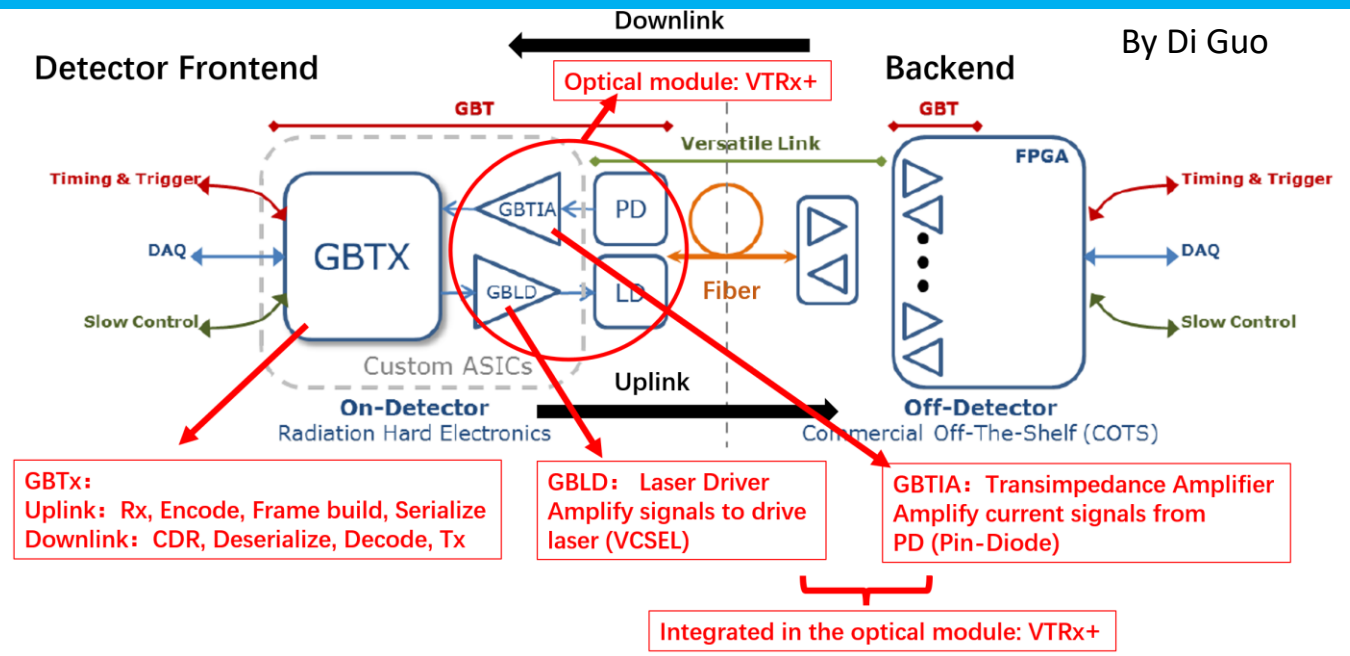

The conventional trigger scheme can always serve as a backup plan, with sufficient on-detector data buffering and reasonable trigger latency, the overall data transmission rate can be controlled.

# Common Electronics Components

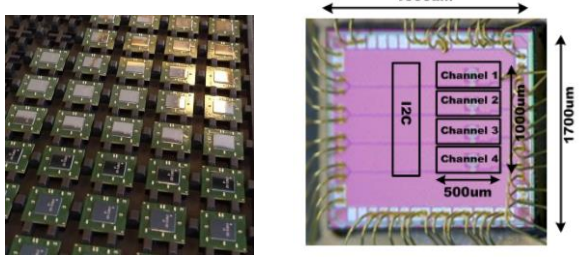
- Common Data Link
- Common Powering
- Common Backend Electronics
- Backup Scheme based on Wireless Communication

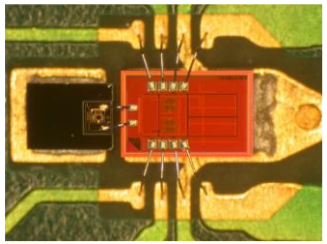
# Technical Survey on Data Transmission System

- GBT Project:
  - Aims to build an high-speed, bidirectional optical data transmission system between the detector front-end and the back-end, developed by CERN
  - Core components:
    - GBTx: Bidirectional Serdes ASIC
    - GBLD: Laser driver
    - GBTIA: Transimpedance amplifier
    - Customized Optical Module
- Our choice:
  - Build a similar universal bidirectional data transmission system that can be used by different front-end detectors.




**GBT Architecture Developed by CERN**



lpGBTx
Uplink: 10.24Gbps
Downlink: 2.56 Gbps

GBLD (LDQ10)
10.24 Gbps x 4ch

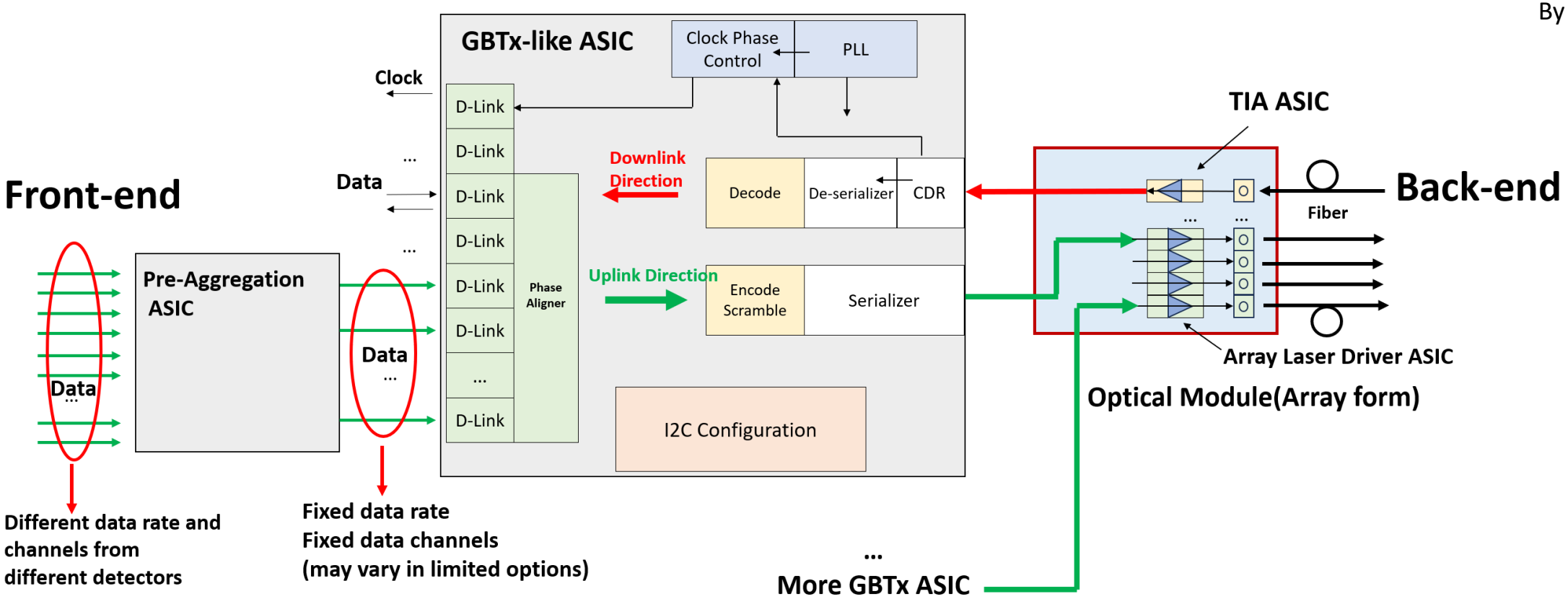
GBTIA
2.56 Gbps

VTRx+
4Tx + 1Rx
Array Optical Module

**GBT Series ASICs and optical module**

# Detailed design on Data Transmission Structure

By Di Guo

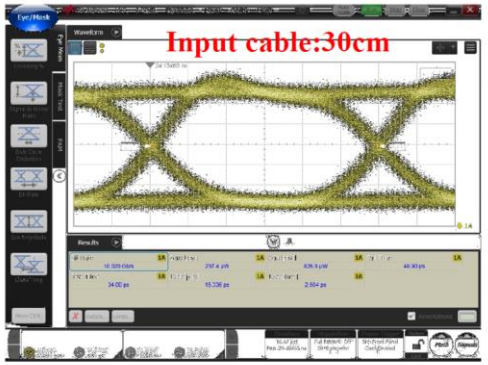



- Pre-Aggregation ASIC: Intend to fit with different front-end detector (different data rates/channels)
- GBTx-like ASIC: Bidirectional serdes ASIC including ser/des, PLL, CDR, code/decode …
- Array Laser Driver ASIC + TIA ASIC + Customized Optical module

# R&D efforts and results on Data Link

By Di Guo

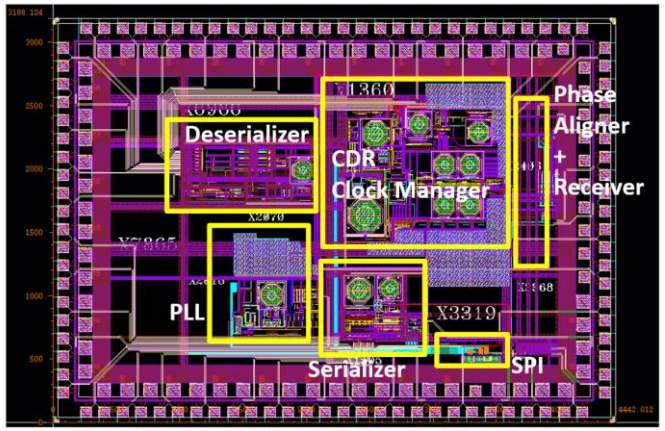
- GBT-like ASIC prototype:
  - 5.12 GHz PLL + 10.24 Gbps Serializer verified√
  - 2.56 Gbps CDR + 2.56 Gbps Deserializer verified√
  - Phase aligner under test
- 10 Gbps Laser Driver Verified √
- Customized optical module prototype Done √
- the rad-tol fiber will be investigated together with the accelerator clocking system



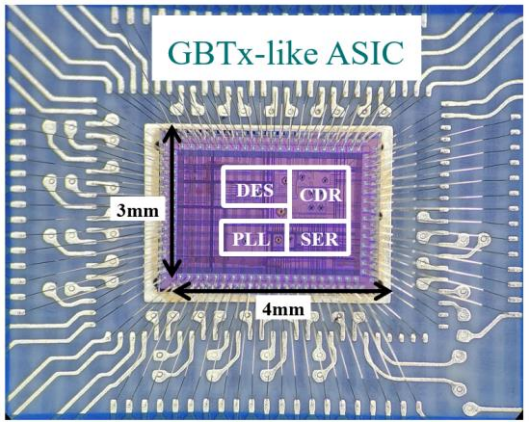

10 Gbps optical eye

| Bit Rate | 10Gbps | RMSJ | 2.6ps |
|---|---|---|---|
| Rise Time | 34.0ps | PPJ | 15.3ps |
| Fall Time | 48.9ps | Amp | 589.4μW |

**10 Gbps optical eye diagram**

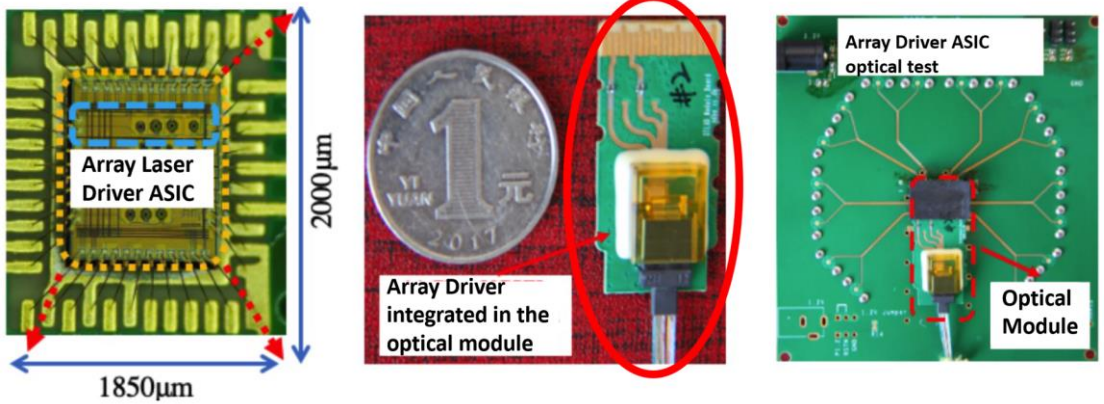



**GBT-like ASIC prototype layout**



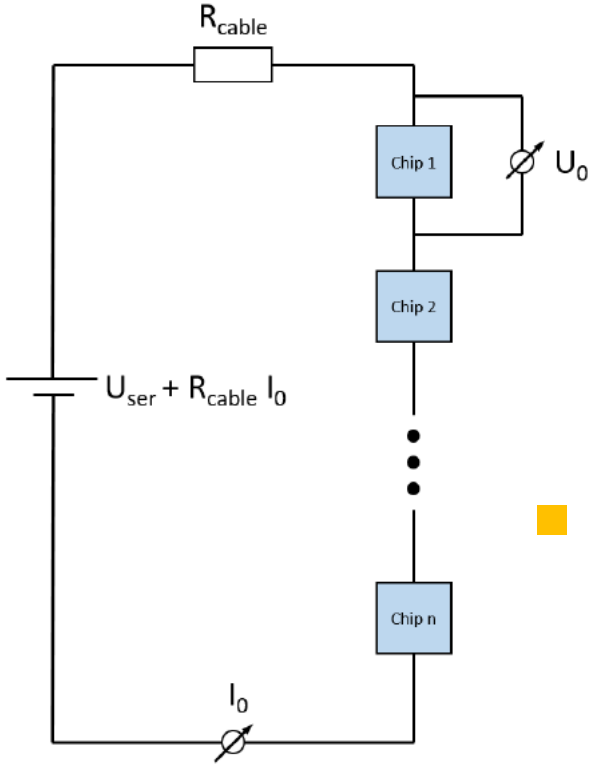

**GBT-like ASIC wire-bonding picture**

Customized Optical module

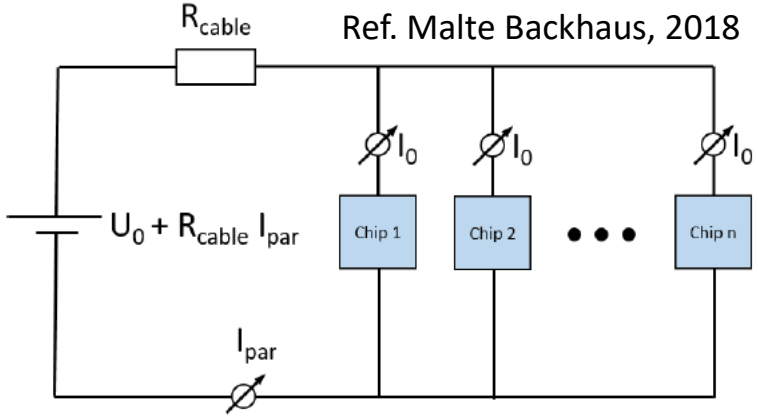



**4 x 10 Gbps/ch VCSEL Array Driver with customized optical module**

# Technology survey and our choice on Powering

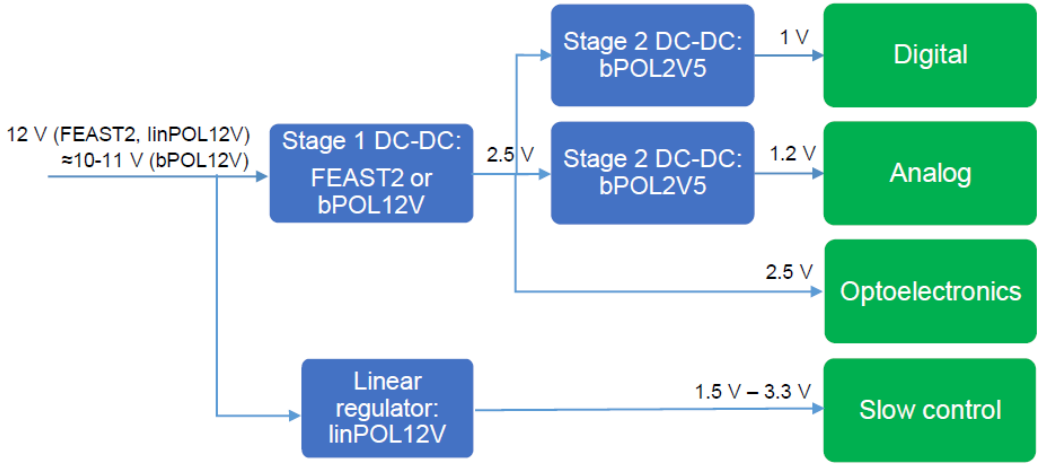



Serial Powering




Ref. Malte Backhaus, 2018

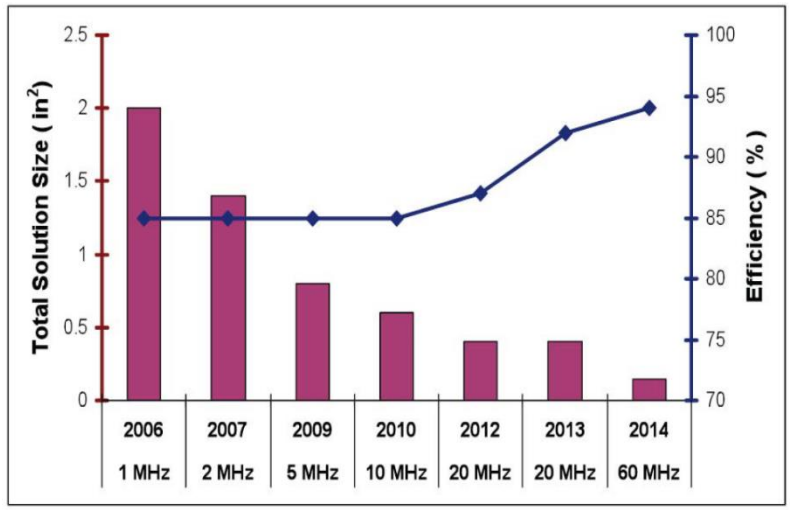
Parallel Powering



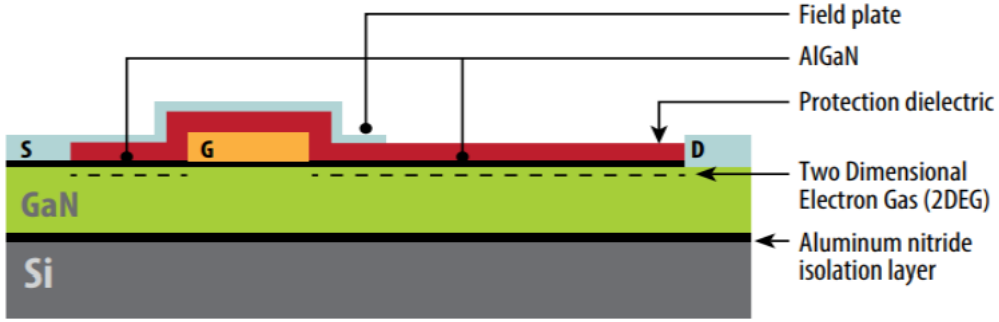

Ref. F. Faccio, FEAST and bPOL status and plans, 2020

- On powering distribution
  - Major solutions, esp. Serial Powering and Parallel Powering were investigated
  - While the superior advantages of Serial Powering on material, cable cross section were noted, the reliability and system complexity issues were also worth a serious concern
- Our choice
  - We chose (conventional) Parallel Powering as the baseline scheme, while continuing to monitor the R&D progress on Serial Powering

# Technology survey and our choice on Powering

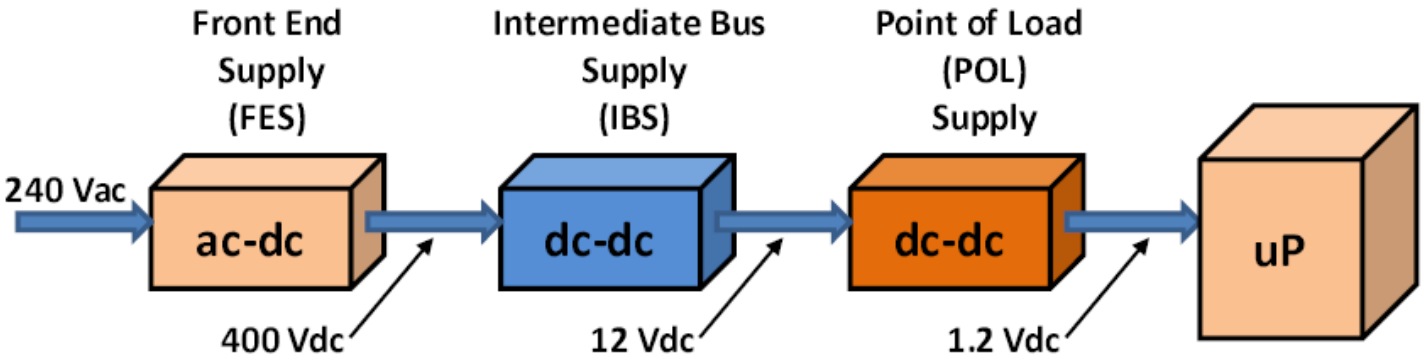



Higher switching Freq, smaller size,
higher efficiency, lower on-resistance




Increased radiation hardness (no SiO2, responsible for most TID effects in Si MOSFETs, in contact with the channel)

Ref. Satish K Dhawan, 2010
Ref. S. Michelis, Prospects on the Power and readout efficiency



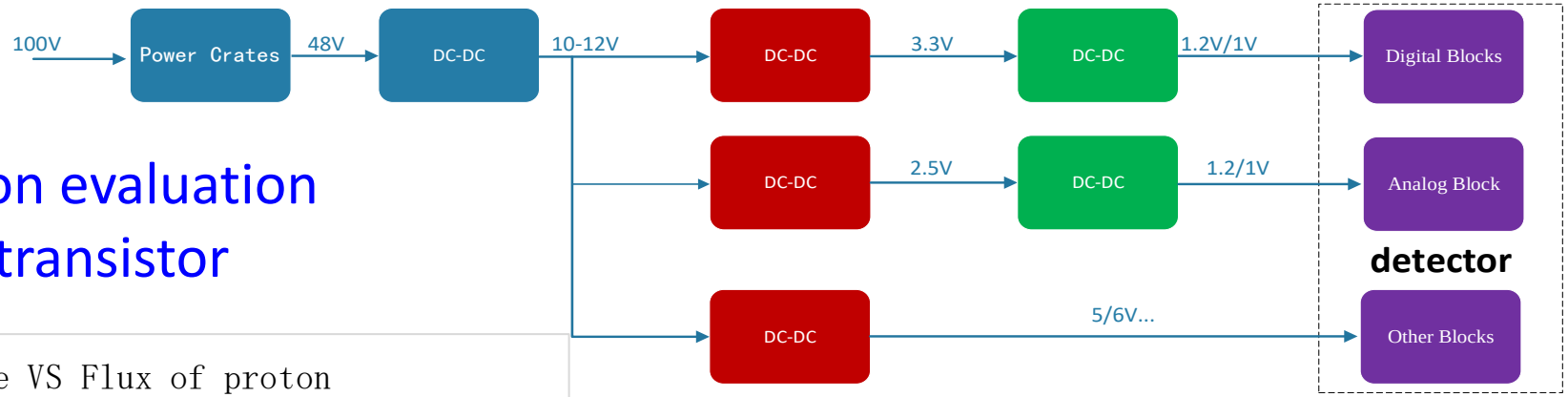

A 400V to 1.2V chain, lower power loss on cable

- Investigation was also conducted to compare the key component schemes of the power module, esp on LDO & DC-DC convertor.
- The GaN transistor has been a game changer in recent years, enabling DC-DC converters to achieve ultra-high efficiency, high radiation tolerance, and noise performance comparable to LDO.
- We choose a GaN-based DC-DC as the baseline power module shceme. This also enables high voltage power distribution, for low cable material and low power loss.

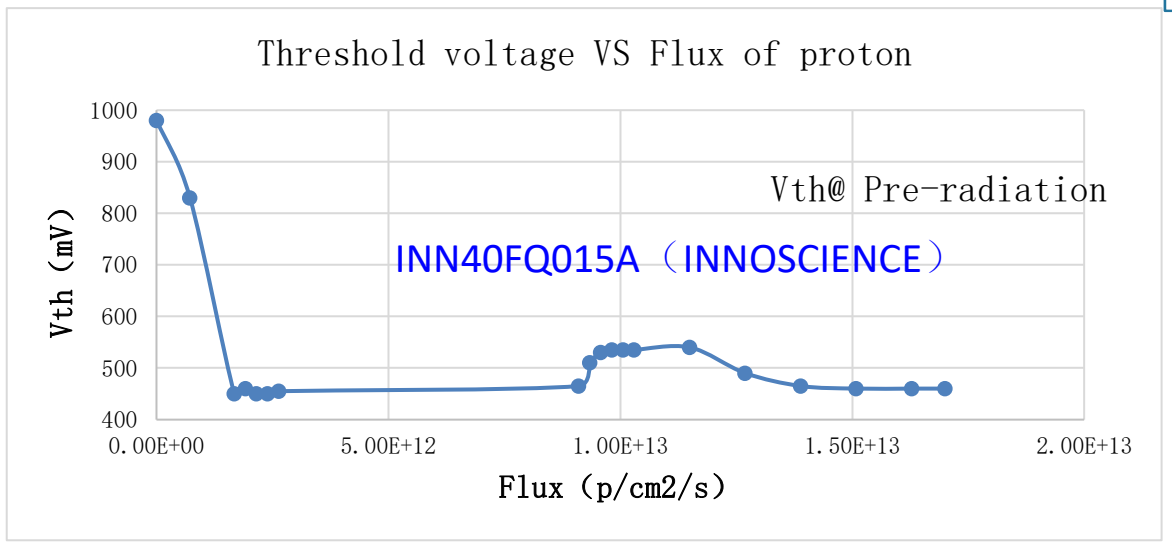
# R&D efforts preliminary design on powering

- Structure of power distribution systems

By Jia Wang

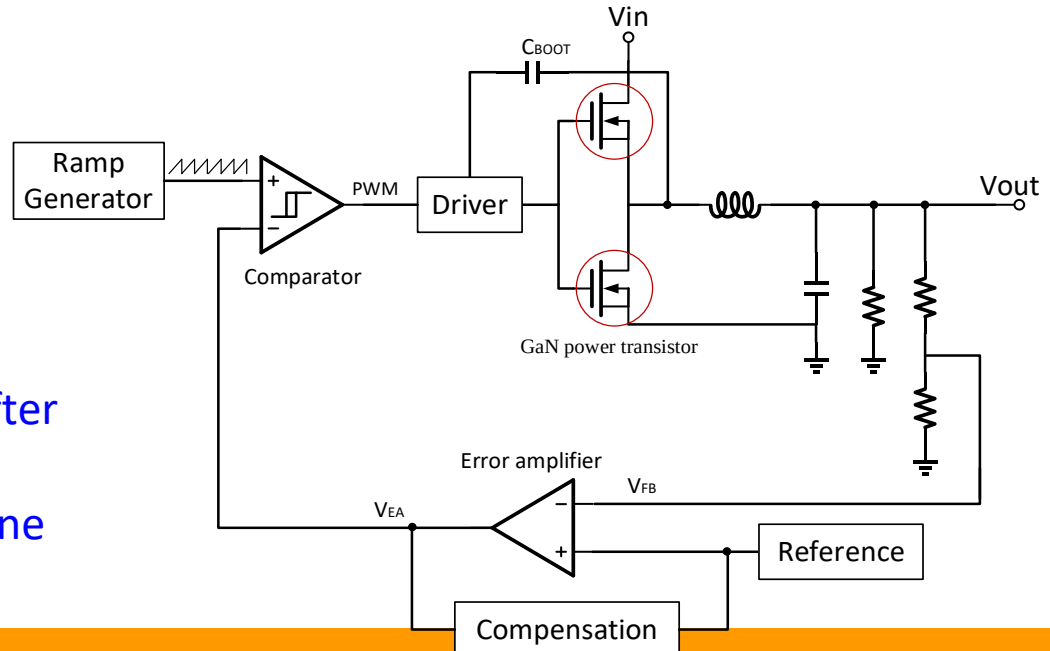



- Preliminary radiation evaluation results of GaN power transistor



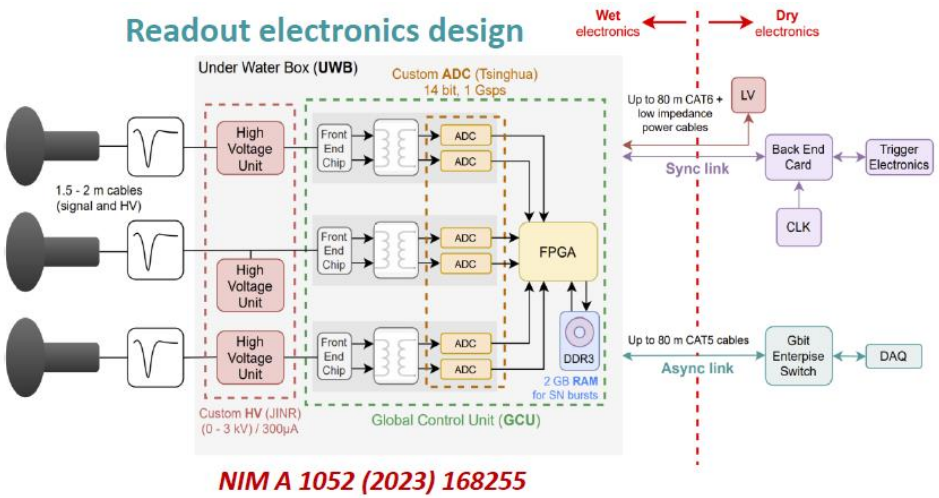

The threshold of the tested GaN was relatively stable, after irradiated for 1.2 h @80MeV proton (flux @ $1.7\times10^{13}$ p/cm$^2$)
Preliminarily verified its radiation tolerance. More test to be done

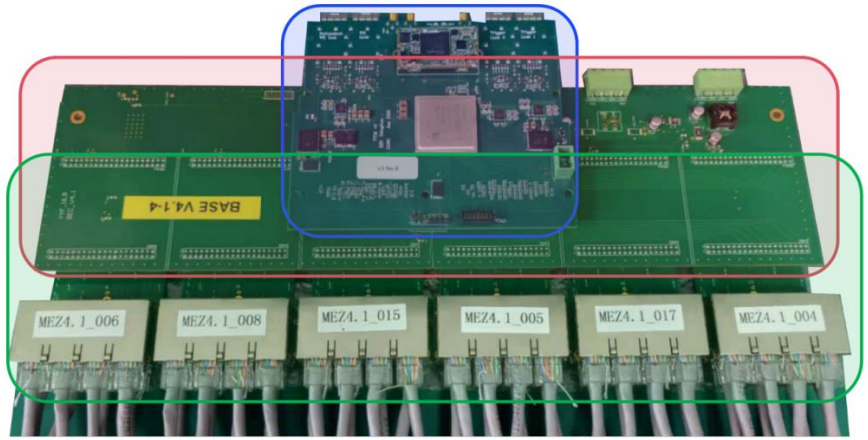
- Proposed design of BUCK DC-DC converter



# Related R&D and experience on BEE

By Jun Hu



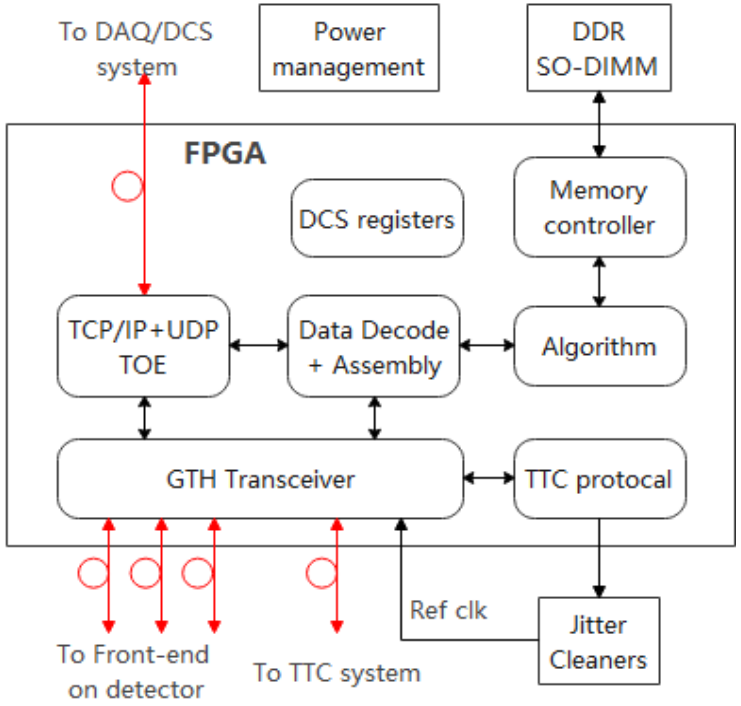




The back-end box for the JUNO experiment

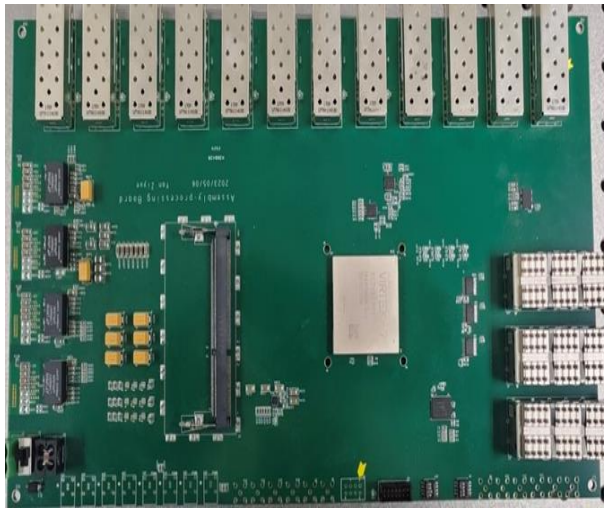
- located between trigger system and front-end electronics,
- Collects the incoming trigger request for trigger system,
- Fanout the synchronized clock and the trigger decisions to front-end electronics.

- Red box: The base board provides the power supply,
- Blue box: Trigger and Time Interface Mezzanine (TTIM) with WR node,
- Green box: The extenders interface with ethernet cables coming from underwater front-end boxes.

# Detailed design on common BEE




By Jun Hu



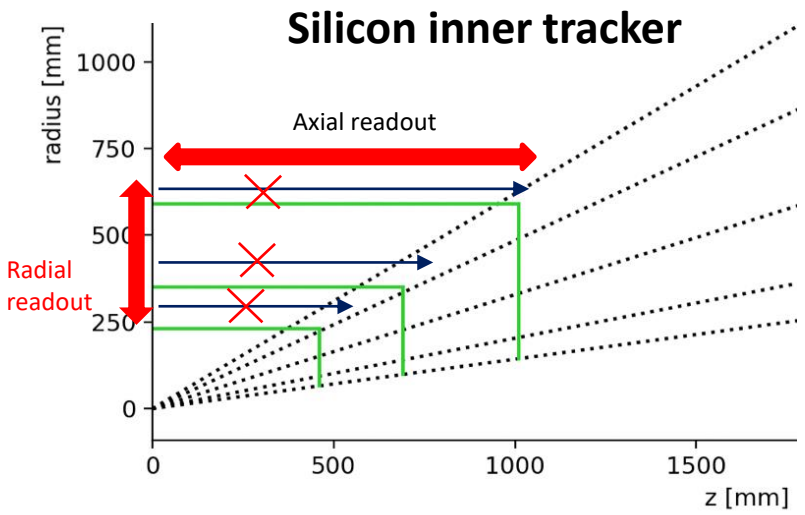
Data aggregation and processing board Prototype for Vertex detector

| | KC705 (XC7K325T-2FFG900C) | KCU105 (XCKU040-2FFVA1156E) | VC709 (XC7VX690T-2FFG1761C) | VCU108 (XCVU095-2FFVA2104E) | XCKU115 |
|---|---|---|---|---|---|
| Logic Cells(k) | 326 | 530 | 693 | 1,176 | 1451 |
| DSP Slices | 840 | 1920 | 3,600 | 768 | 5520 |
| Memory (Kbits) | 16,020 | 21,100 | 52,920 | 60,800 | 75,900 |
| Transceivers | 16(12.5Gb/s) | 20(16.3Gb/s) | 80(13.1Gb/s) | 32(16.3Gb/s) and 32(30.5Gb/s) | 64(16.3Gb/s) |
| I/O Pins | 500 | 520 | 1,000 | 832 | 832 |
| Cost | 2748 (650) | 3882(1500) | 8094 | 7770 | |

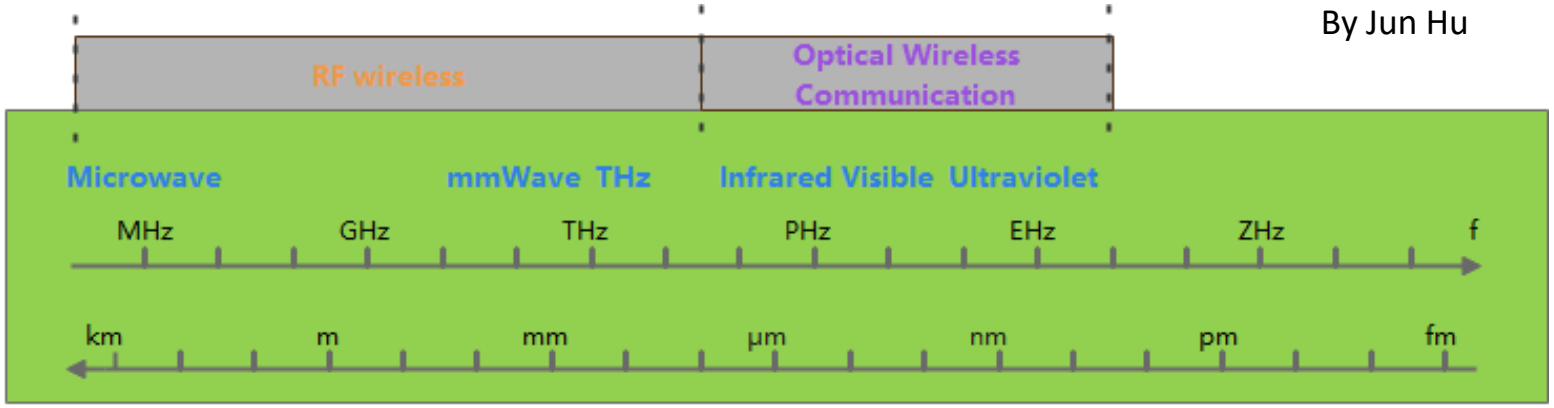
- Routing data between optical link of front-end and the highspeed network of DAQ system.
- Connect to TTC and obtain synchronized clock, global control, and fanout high performance clock for front-end.
- Real-time data processing, such as trigger algorithm and data assembly.
- On-board large data storage for buffering.
- Preference for Xilinx Kintex UltraScale series due to its cost-effectiveness and availability.

- FPGA： XC7VX690T
- Interface： SFP+ 10Gbps X12 + QSFP 40Gbps X3
- Implement real time FPGA based machine learning for clustering, hit point searching, and tracking algorithms

# Backup scheme based on wireless communication




By Jun Hu




- Radial readout with mm-wave
  - 12- 24 cm transmission distance
  - Data rate : < 30Mbps
- Axial readout to endcap
  - Only at the outermost layer or dedicated aggregation layer.

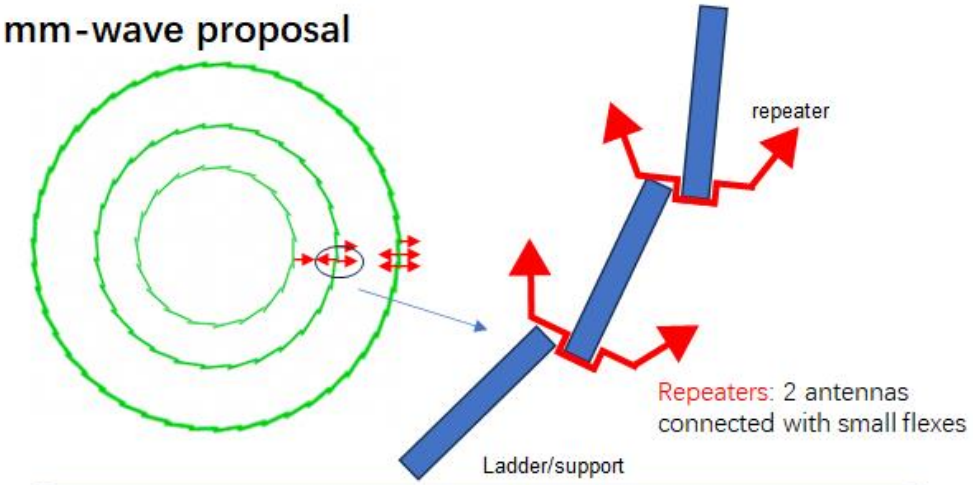
- WiFi (2.4GHz, 5GHz)
  - large antenna volume, high power consumption, narrow frequency band, and high interference
- Millimeter Wave (24GHz，45GHz，60GHz，77GHz)
- Optical wireless communication (OWC) / Free Space Optical (FSO)

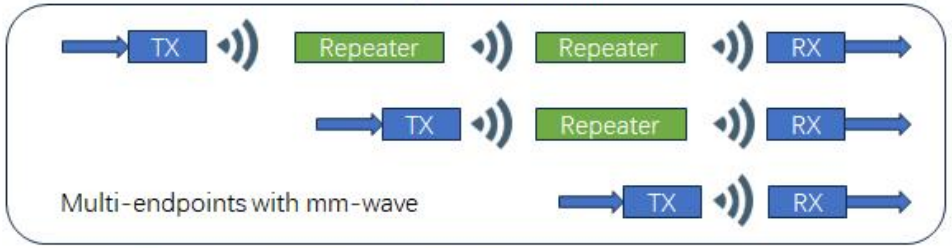
- Wireless communication based readout scheme was proposed to mitigate the cabling problem, as a backup scheme
- Three major solutions were investigated through R&D, two were selected with corresponding schemes

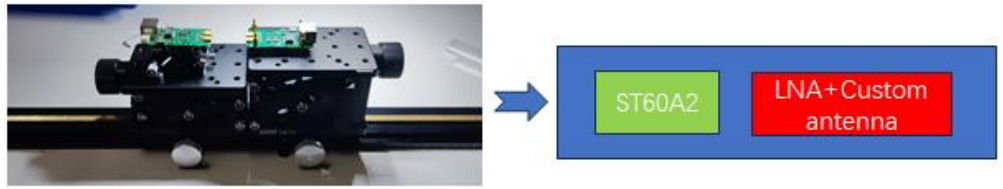
# R&D efforts and results on WLess Comm

By Jun Hu

## mm-wave proposal




Test with evaluation boards – SK202

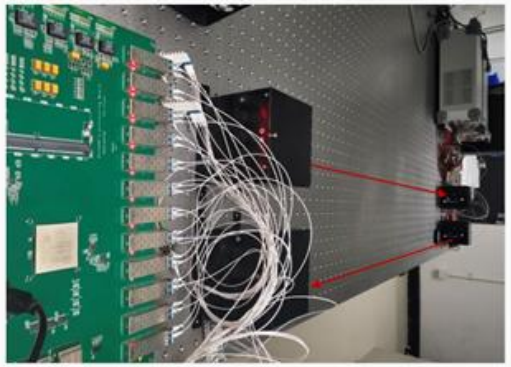
- Based on the commercial 60GHz RF chip ST60A2 transceiver from ST Microelectronics company.
- The transmission speed can exceed 900Mbps when the distance is less than 6 cm.

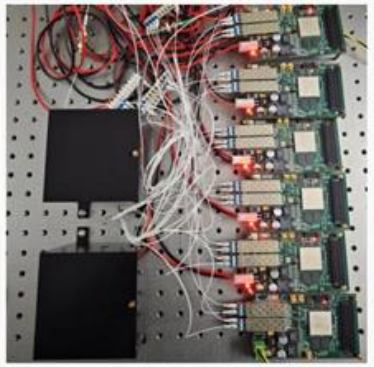
- Design a small PCB module with ST60A2. LNA and custom antenna.
- Higher bandwidth and longer distance
- Evaluate the interference with detector
- Under design, cheap and easy
- → custom transceiver + antenna +AIP

## Optical wireless proposal

Transceiver with alignment mechanics



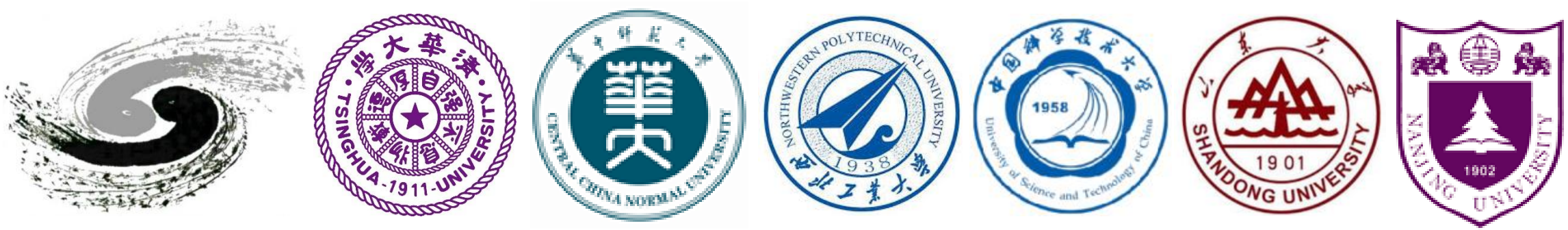


DWDM transceivers +AWG + lens

- Up to 6-meter free space optical transmission distance
- 10Gbps X 12 channels bandwidth
- PRBS 31bits error rate < BER-15 @ 10Gbps under 1.6m distance

# Research Team

- A wide collaboration was built involving most of the affiliations in the HEP field in China.
- We are working to expand the collaboration, including attracting international colleagues.

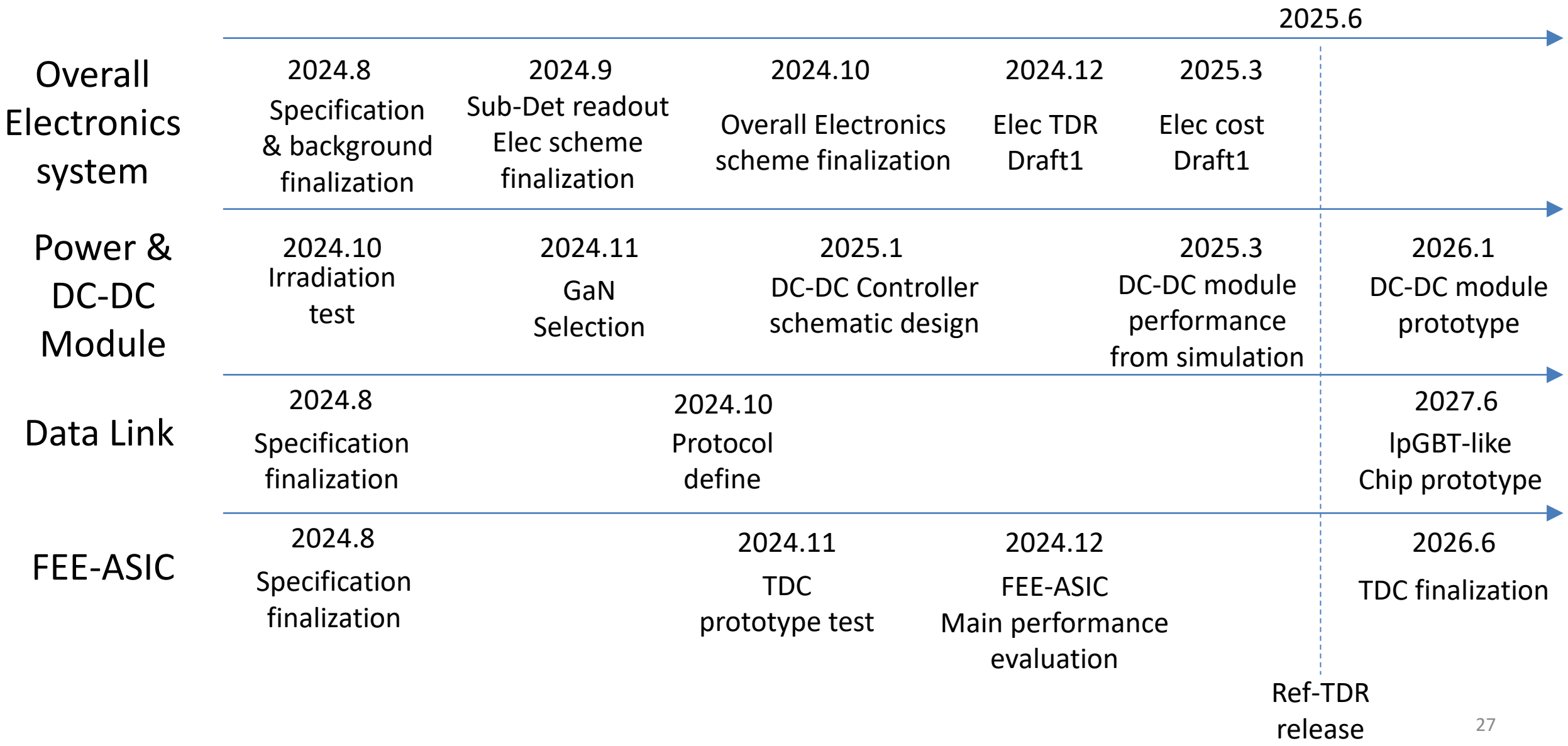



- Overall electronics and BEE: IHEP
- Sub-detector readout electronics: IHEP, Tsinghua, CCNU, NPU, SDU, NJU
- Data link: CCNU, IHEP, USTC
- Powering: NPU, IHEP, USTC

# Working plan on key R&Ds

- Key R&D left to do towards & beyond the Ref-TDR
  - An lpGBT-like chip series should be developed as the common data link platform
    - Transmission protocol, including up(typically 8b10b) and down(typically I2C & fast commander), is a key component according the current tech stage
  - GaN based DC-DC module is also critical for FEE modules in high radiation environment
    - Further radiation tests should be performed, including TID, SEE, and NIEL
  - A prototype based on wireless communication scheme will be demonstrated to show the feasibility
    - Customized antennas, adapters, and repeaters are being coordinated with the industrial sector in China for a more compact design

# Working plan on schedule for the Ref-TDR



# Summary

- We proposed a global framework for the CEPC electronics system and prepared a readout scheme for each sub-detector according to the framework.
- Previous R&D has shown promising technical feasibility for key components, including data links, common BEEs, and powering.
- Backup schemes based on conventional triggers and innovative schemes based on wireless communication were also considered for more conservative and aggressive approaches, respectively.
- Future R&D is scheduled beyond Ref-TDR, and prototypes of each key technology will be demonstrated soon.

# Thank you for your attention!

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

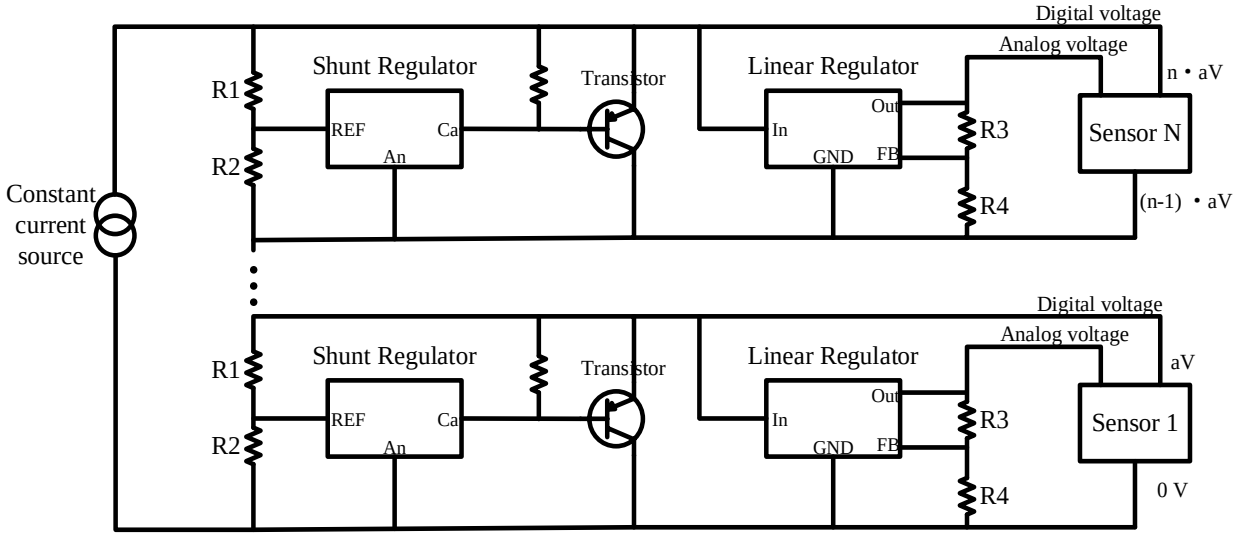
# Requirement of the powering system

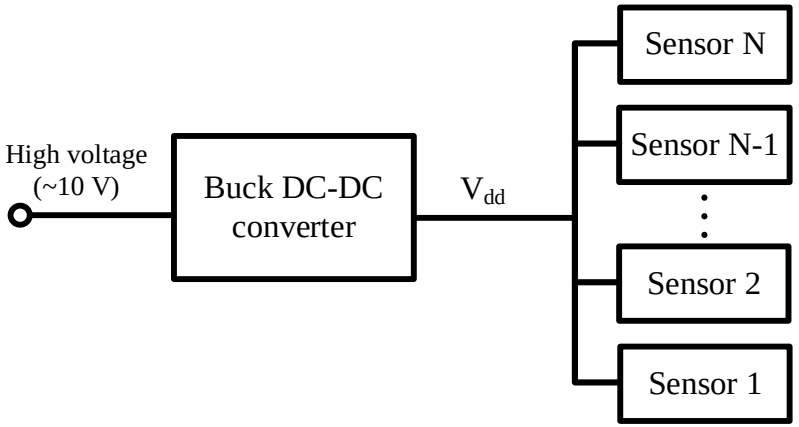
| | Vertex | Pix Tracker | TOF | Si Strip | TPC | DC | ECAL | HCAL |
|---|---|---|---|---|---|---|---|---|
| Detector for readout | CMOS Sensor | HVCMOS | Strip-LGAD | Si Strip | Pixel PAD | Drift Chamber | SiPM | SiPM |
| Main Func for FEE | X+Y | XY + nsT | X + 50psT | X | E + nsT | Analog Samp. | E + 400psT | E + 400psT |
| Channels per chip | 512*1024 Pixelized | 768*128 (2cm*2cm @25um*150um) | 128 | 128 | 128 | - | 16 | 16 |
| Voltage@chip | 1.8V@180nm (1.2V@65nm future) | 1.2V@55nm (HVCMOS Pixel) | 1.2V@55nm (TDC) | 1.2V@130nm | 1.2V@65nm | ±3.3V →1.2V@GaAs? | 1.2V@55nm (TDC) | 1.2V@55nm (TDC) |
| Power@chip | <200mW/cm2 <0.8W/chip | <200mW/cm2 <0.8W/chip | <40mW/ch <5W/chip | 5mW/ch 640mW/chip | 35mW/chip | ? | 20mW/chn 160~320mW/chip | 20mW/chn 160~320mW/chip |
| chips@module | 10~20:1 | <14:1 | 10:1 | 10:1 | 279:4:1 | 1.2V@FPGA | 112~280:1 | ~10:1 |
| Power@module | 8~16W @1.8V 4.4~8.9A | 8~16W @1.8V 4.4~8.9A | 50W @1.2V 41.7A | 6.4W @1.2V 0.53A | 40W @1.2V 33.3A | | 44.8W @1.2V 37.3A | 3.2W @1.2V 2.6A |
| Other | TID 7.3Mrad/y @ HLumi Z | | | | | On FPGA | May use 60V for SiPM | May use 60V for SiPM |

- Requirement for the powering system is to power all the FEE modules with high efficiency.
- The power module should also be rad-tolerant, and small size for assembly.
- Power requirements and module organization were collected from the proposed FEE schemes of sub-det. and summarized in the table.

# Technology survey and our choices on Powering

- Serial powering VS Parallel powering with DC-DC converter

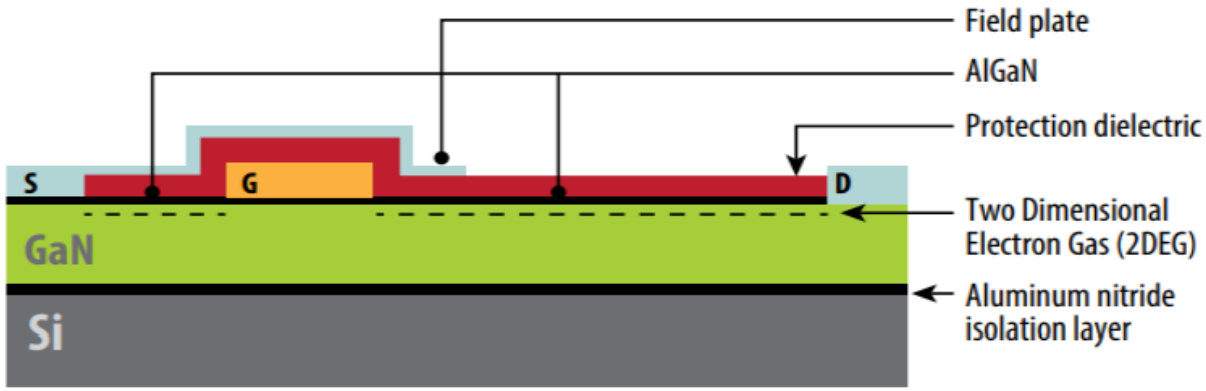



Performance comparasion of the two power distribution system

| | Serial powering | Parallel powering (DC-DC converter) |
|---|---|---|
| **Power efficiency** | 60-80% | 60-80% |
| **Power cable number** | Reduction by factor 2n | Reduction by factor 2n |
| **System ground potential** | Different for every module | One ground level |
| **Noise** | Noiseless, even better | More noise due to the switching. |
| **Compatibility with the old power system** | Many changes are needed due to the virtual ground. | A few changes |
| **Reliability** | Not good. Bypass circuits are required for the faulty modules. | Good |

# Stage1: Why GaN?




GaN power FETs offer superior performance compared to Silicon devices:

- Smaller size and increased breakdown voltage for the same on-resistance
- Faster switching (which leads to reduced losses and smaller passive components)
- Increased radiation hardness (no SiO2, responsible for most TID effects in Si MOSFETs, in contact with the channel).

# Update on common Power module

| | Vertex | Pix Tracker | TOF | Si Strip | TPC | DC | ECAL | HCAL |
|---|---|---|---|---|---|---|---|---|
| Detector for readout | CMOS Sensor | HVCMOS | Strip-LGAD | Si Strip | Pixel PAD | Drift Chamber | SiPM | SiPM |
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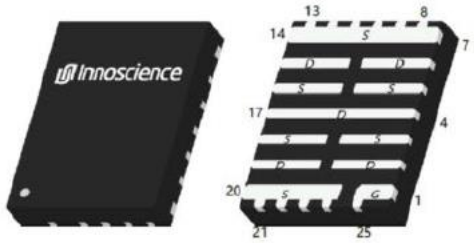
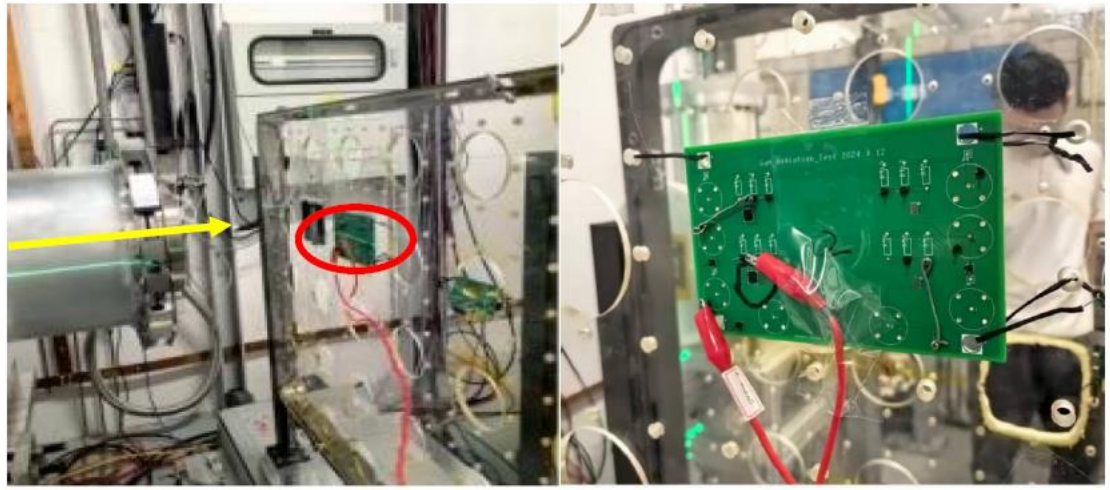
| Power@chip | <200mW/cm2 <0.8W/chip | <200mW/cm2 <0.8W/chip 尚无设计 | <40mW/ch <5W/chip | 5mW/ch 640mW/chip | 35mW/chip | ? | 20mW/chn 160~320mW/chip | 20mW/chn 160~320mW/chip |
| chips@module | 10~20:1 | <10:1 尚无设计 | 10:1 | 10:1 | 279:4:1 | 需FPGA、ADC供电，可统一1.2V？ | 112~280:1 侧板无DCDC 仅电容 | ~10:1 |
| Power@module | 8~16W @1.8V 4.4~8.9A | 8~16W @1.8V 4.4~8.9A | 50W (???) @1.2V 41.7A | 6.4W @1.2V 0.53A | 40W @1.2V 33.3A | | 44.8W @1.2V 37.3A | 3.2W @1.2V 2.6A |
| Other | 辐照TID 7.3Mrad/y @ HLumi Z | | 需进一步优化 | | | On FPGA | 可能SiPM可共用60V中压电源 | 可能SiPM可共用60V中压电源 |




测试仪器：源表、电源、万用表

- Power requirements summarized according to the current readout schemes of each SubD
- Rad-test of COTS samples initiated, preliminary proved the GaN transistor can survive in the CEPC rad environment
- Recent plan:
  - Key component evaluation



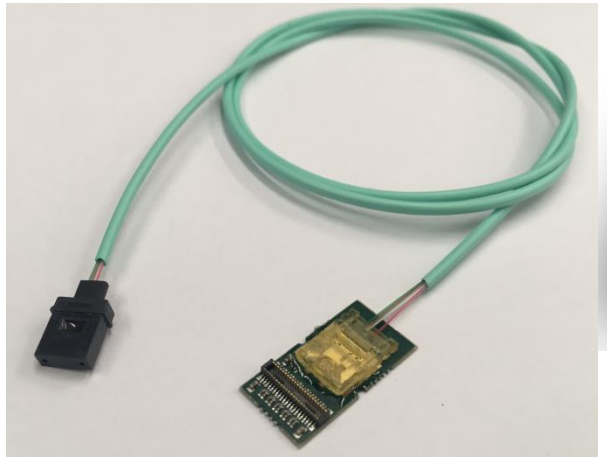
测试PCB固定到样品台上的实物照片(左图中黄色箭头为束流方向)

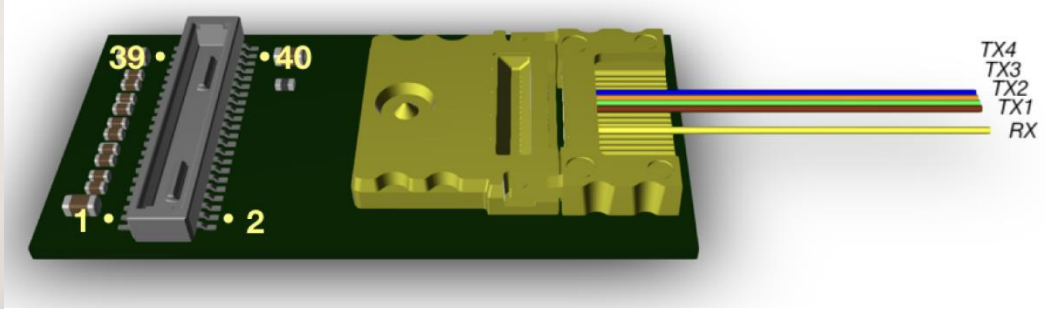
# Preliminary consideration on common BEE

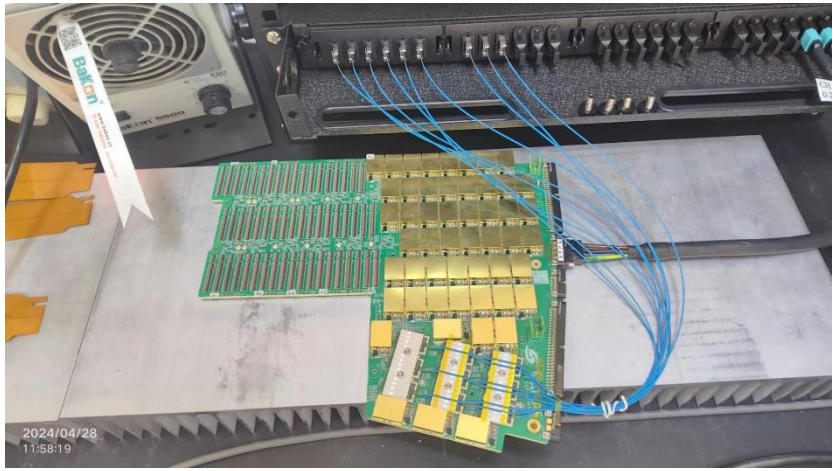
| | KC705 (XC7K325T-2FFG900C) | KCU105 (XCKU040-2FFVA1156E) | VC709 (XC7VX690T-2FFG1761C) | VCU108 (XCVU095-2FFVA2104E) | XCKU115 |
|---|---|---|---|---|---|
| Logic Cells(k) | 326 | 530 | 693 | 1,176 | 1451 |
| DSP Slices | 840 | 1920 | 3,600 | 768 | 5520 |
| Memory(Kbits) | 16,020 | 21,100 | 52,920 | 60,800 | 75,900 |
| Transceivers | 16(12.5Gb/s) | 20(16.3Gb/s) | 80(13.1Gb/s) | 32(16.3Gb/s) and 32(30.5Gb/s) | 64(16.3Gb/s) |
| I/O Pins | 500 | 520 | 1,000 | 832 | 832 |
| Cost | 2748 (650) | 3882(1500) | 8094 | 7770 | |

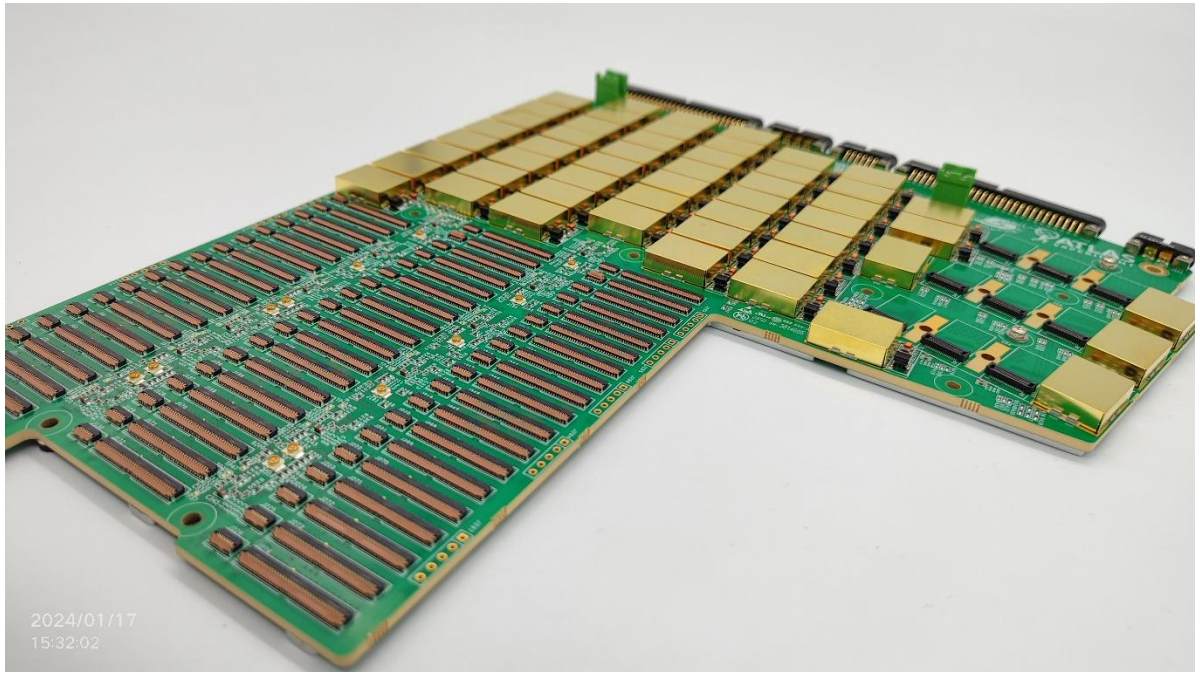
- A common station for fibers from FEE
- Providing data buffers till trigger comes
- Possible calculation resource needed for trigger algorithm
- Number of IOs, port rate & the cost are the major concerns

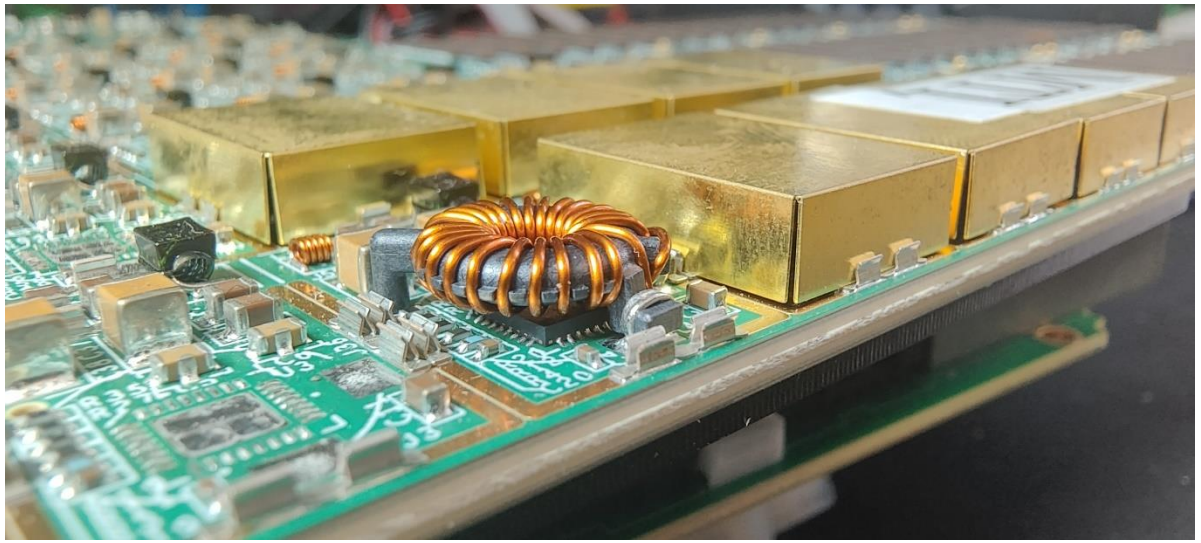
# Size of bPol & GBT



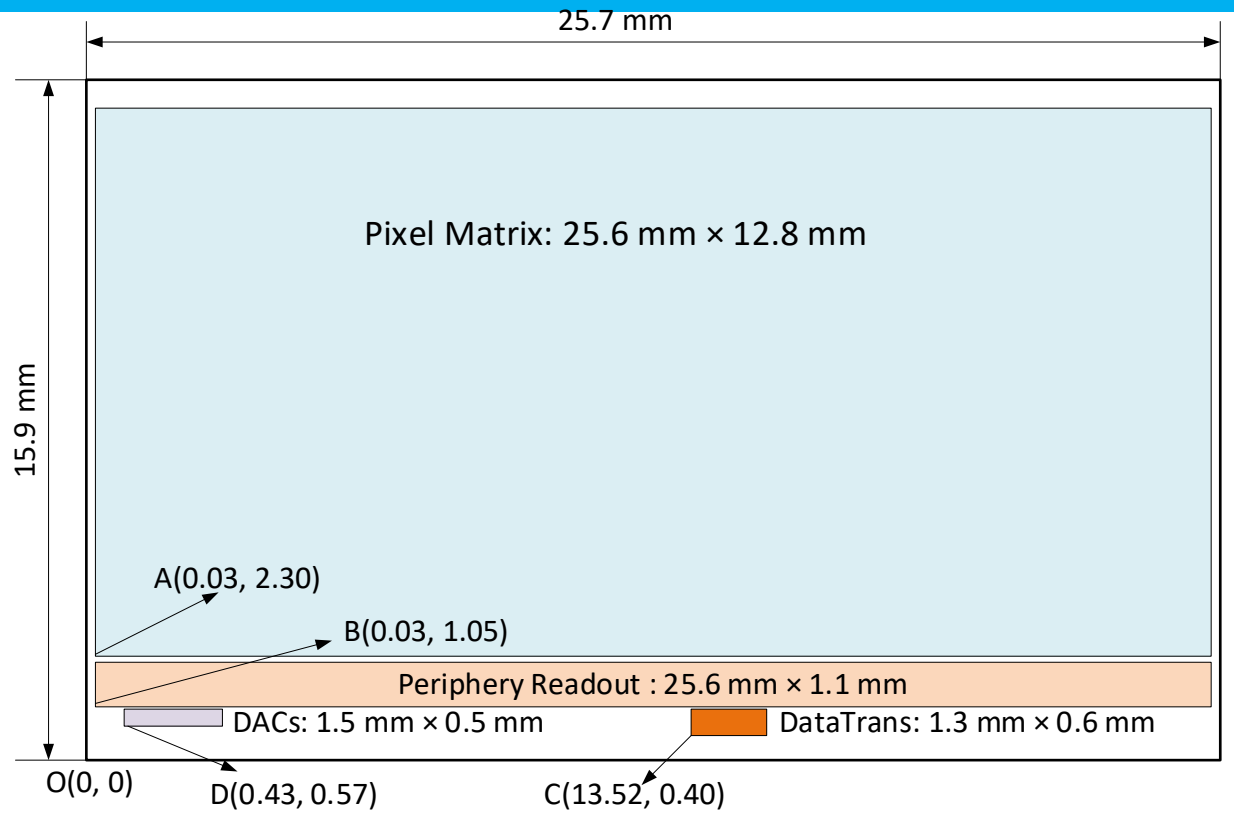


# VTX像素芯片功耗分布估算




估算说明：

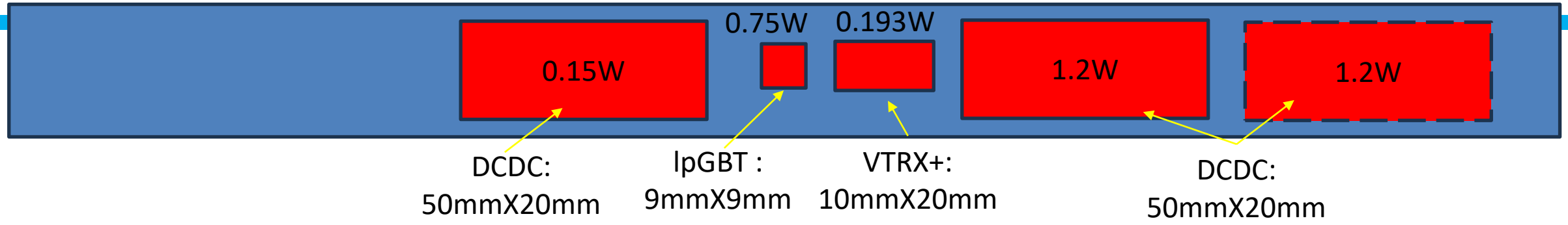
- 太初芯片：180 nm工艺，电源1.8 V;
- 65 nm芯片：电源1.2 V;
- Data rate @Triggless-CDR: 4.48 Gbps /chip

  bunch spacing (min.): 25 ns需要快前沿前端
- Data rate @Triggless-TDR (Low Lumi):

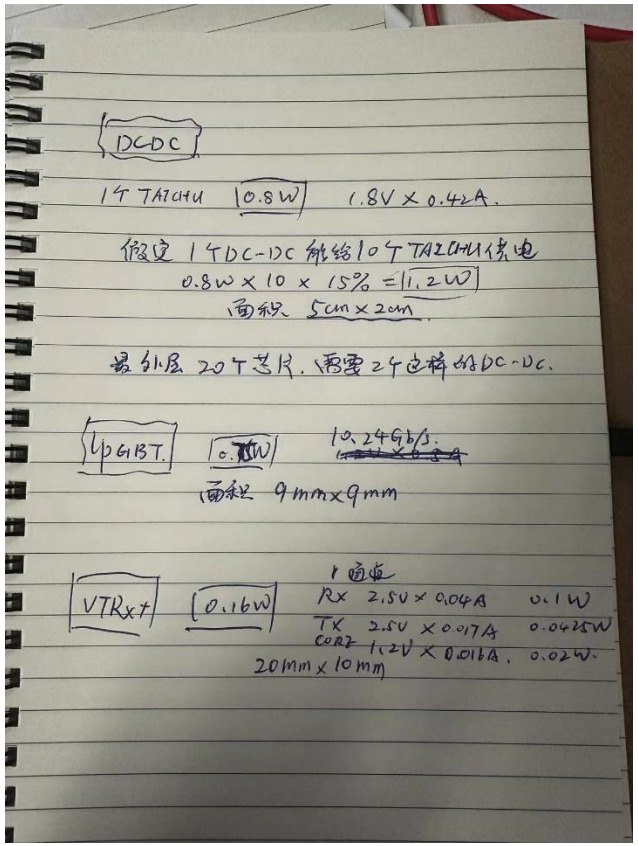
  1 Gbps/chip
- Low Lumi@TDR: bunch spacing ~几百ns，像素前端不需要快前沿，Matrix功耗可降低
- 图中芯片坐下角标为坐标原点，标注4个功耗模块的左下角坐标(X,Y)，单位为毫米

| | Matrix | Periphery | DataTrans. | DACs | Total Power |
|---|---|---|---|---|---|
| 太初芯片<br>@ triggerless (CDR) | 304 mW | 135 mW | 206 mW | 10 mW | 655 mW |
| 65nm 芯片<br>@ 1 Gbps/chip<br>(TDR LowLumi) | 60 mW | 80 mW | 36 mW | 10 mW | 186 mW |

# Ladder端部热功耗分布



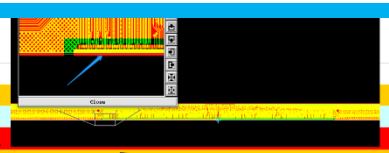

- **DCDC：电源管理芯片**
  - **TAICHU功耗0.8W（1.8V*0.42A）**
  - **单个DCDC最多为10个TAICHU提供电源，效率按85%计算**
  - **DCDC功耗为0.8*10*15% = 1.2W**
  - **如果最外层需要20个芯片则需要2个DCDC**
  - **lpGBT和VTRX+需要其他种类电源（1.2V，2.5V），总体功耗不高，~1W，则DCDC功耗为0.15W**
- **lpGBT：数据汇总芯片**
  - **0.75W@10.24Gb/s**
- **VTRX+：光电转化芯片**
  - **1发1收：0.193W（RX：2.5V*0.05A，TX：2.5V*0.02A，core：1.2V*0.015A）**
- **说明：1：图中仅展示ladder一端一面，底面及ladder另一端有同样的配置**
- **2：lpGBT及VTRX+的参数为CERN对应芯片手册得到，CEPC最终参数可能有所不同。**
- **Ladder长度及端部器件位置，需结合机械及安装设计来调整**



# Flex厚度和物质分布

叠层

**Stack Up**



| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 12.5 | um | Coverlay | (yellow) | | | | |
| | 20 | um | Coverlay Adhesive | | Soldmask (green) | | | |
| Layer 1 | 24 | um | ED Base Copper | 12 um | um + | Plated | 18 | um . |
| | 13 | um | Polyimide (Adhesiveless) | | | | | |
| | 12.5 | um | Adhesive | | | | | |
| Layer 2 | 12 | um | ED Base Copper | 12 um | | | | |
| | 25 | um | Polyimide (Adhesiveless) | | Flex Thickness | | | |
| Layer 3 | 12 | um | ED Base Copper | 12 um | | | | |
| | 12.5 | um | Adhesive | | | | | |
| | 13 | um | Polyimide (Adhesiveless) | | | | | |
| Layer 4 | 24 | um | ED Base Copper | 12 um | um + | Plated | 18 | um . |
| | 20 | um | Coverlay Adhesive | | | | | |
| | 12.5 | um | Coverlay | (yellow) | | | | |

绕折区

补强区

FPC厚度: 213 um Spec: 210 um +/- 50 um

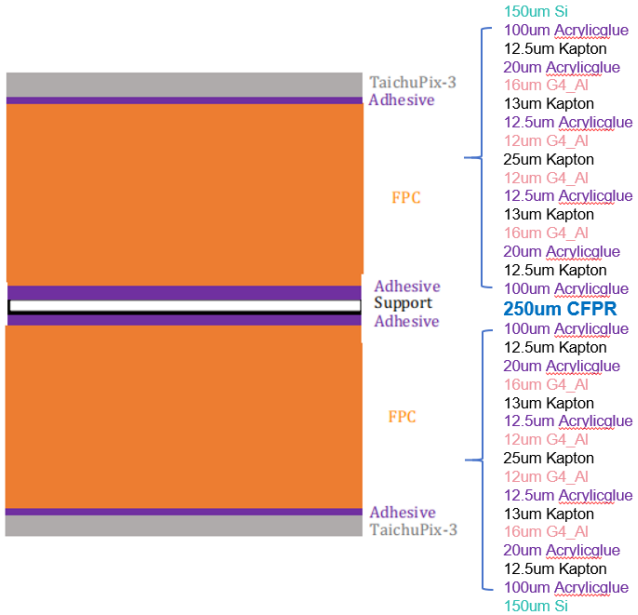
Created By: HLJ

Date:

4层柔性板基于国内Cu工艺（当前阶段）

| | | | |
|---|---|---|---|
| | 12.5 | um | Coverlay |
| | 20 | um | Coverlay adhesive |
| layer1 | 24 | um | ED Base Copper |
| | 13 | um | Polymide(Adhesiveless) |
| | 12.5 | um | Adhesive |
| layer2 | 12 | um | ED Base Copper |
| | 13 | um | Polymide(Adhesiveless) |
| | 12.5 | um | Adhesive |
| layer3 | 12 | um | ED Base Copper |
| | 25 | um | Polymide(Adhesiveless) |
| layer4 | 12 | um | ED Base Copper |
| | 12.5 | um | Adhesive |
| | 13 | um | Polymide(Adhesiveless) |
| layer5 | 12 | um | ED Base Copper |
| | 12.5 | um | Adhesive |
| | 13 | um | Polymide(Adhesiveless) |
| layer6 | 24 | um | ED Base Copper |
| | 20 | um | Coverlay adhesive |
| | 12.5 | um | Coverlay |
| | | | |
| 厚度 | 288 | um | |

6层柔性板基于国内Cu工艺（当前阶段）




- 国内工艺当前只能实现基于铜的PCB，如需采用铝材料，需要委托CERN进行加工（accessibility？）
- Long barrel方案，同ladder芯片更多，需要更多层的PCB
  - For Innermost：4层Flex（now：Cu based，proposed：Al based）
  - For Middle & Outer：6层Flex（now：Cu based，proposed：Al based）



Proposed Double-sided ladder based on 铝

# Backup

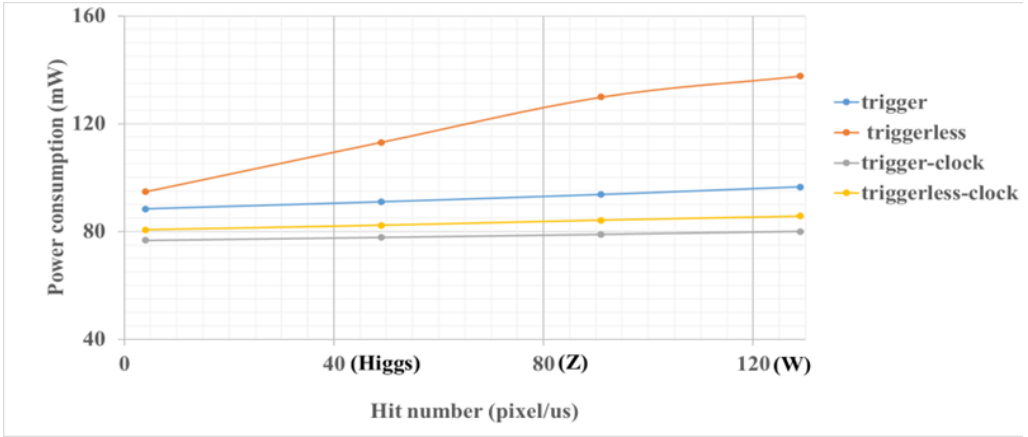
## Specification calculation- from hit density

| | | Hit density (Hits/cm²/BX) | Bunch spacing (ns) | Hit rate (M Hits/cm²) | Hit Pix rate (M Px/cm²) | Hit rate/chip (MHz) | Data rate@trigerless (Gbps) | Pixel/bunch | FIFO Depth @3us rg latency | Data rate@trigger (Mbps) |
|---|---|---|---|---|---|---|---|---|---|---|
| CDR | Higgs | 2.4 | 680 | 3.53 | 10.59 | 34.62 | 1.1 | 23.5 | 103.9 | 105.28 |
| | W | 2.3 | 210 | 10.95 | 32.86 | 107.44 | 3.4 | 22.6 | 322.3 | 101.248 |
| | Z | 0.25 | 25 | 10 | 30 | 98.1 | 3.1 | 2.4 | 294.3 | 53.76 |
| | | | | | | | | | | |
| TDR | Higgs | 0.81 | 591 | 1.37 | 4.11 | 13.44 | 0.43 | 7.96 | 40.4 | 213.9? |
| | W | 0.81 | 257 | 3.16 | 9.45 | 30.90 | 0.98 | 7.96 | 92.8 | 213.9? |
| | Z | 0.45 | 23 | 19.6 | 58.7 | 191.9 | 5.9 | 4.4 | 575 | 118 |

- TDR raw hit density: Higgs 0.54，Z 0.3；Safety factor: TDR 1.5, CDR 10;
- Cluster size: 3pixels/hit (@Twjz 180nm, EPI 18~25um)
- Area: 1.28cm*2.56cm=3.27cm² (@pixel size 25um*25um)
- Word length: 32bit/event (@Taichu's scale, 512*1024 array)
- Trigger rate：20kHz@CDR，120kHz@TDR estimated
  - Trigger latency: 3us(very likely not enough), Error window: 7 bins
  - FIFO depth: @3us * hit rate/chip
  - Data rate=pixel/bunch*trigger rate*32bit*error window

2

Rate for Low LumiZ still missing




仅外围电路功耗vs计数率

| | 能力 | | |
|---|---|---|---|
| | 160Mbps | 2.56Gbps | 4.48Gbps |
| PLL | 20 | 34 | 34 |
| MUX | 8 | 27.8 | 44.2 |
| CMLdriver | | 36.5 | 36.5 |
| LVDS_TX | 5 | 7.5 | 10 |
| | 33 | 98.3 | 114.7 |

数据接口功耗vs数据率

# Backup scheme of the framework

- The proposed framework was based on the estimated background rate of all sub-det.
- In case of under-estimation or unexpected condition, some backup schemes were also considered to guarantee the overall feasibility:

1. Additional optical links can be allocated to the hottest module as compensation for the local high background.
2. In case the background rate is too high for FEE-ASIC to process, Intelligent Data Compression algorithm can be integrated on-chip, for the initial data rate reduction.
3. The conventional trigger scheme can always serve as a backup plan, with sufficient on-detector data buffering and reasonable trigger latency, the overall data transmission rate can be controlled in a reasonable range.

# R&D efforts and results

- VTX
- TPC
- Muon
- GBTx & Optical module
- BEE
- Power
- Wireless communication
- Drift Chamber

# Related R&D efforts

- HGTD
- PARISROC for CAL
- BESIII，JUNO