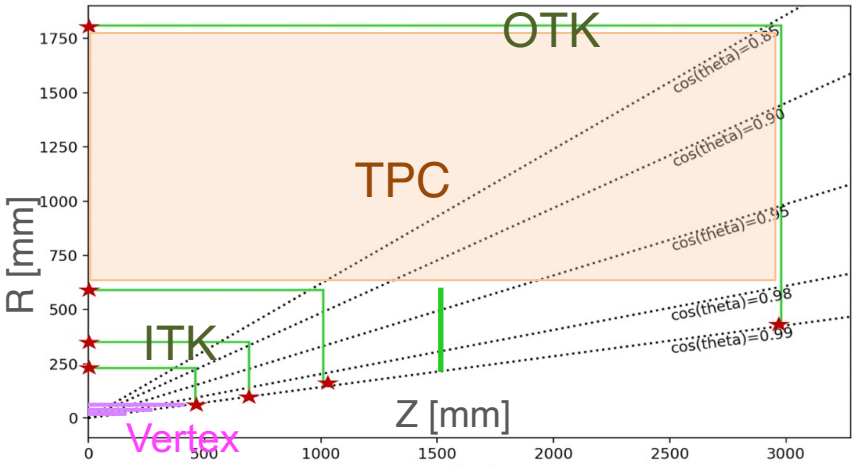
Tracker ITK TDR 的工作进度报告（3）

严琪

2024年7月26日

Tracker探测器Baseline不同层的排布



端盖	ITKE1	ITKE2	ITKE3	ITKE4	OTKE
|Z|[mm]	500.5	715	1001	1500	2903
R-I [mm]	75	101.9	142.6	214	405.7
R-O[mm]	240	350	600	600	1801

桶部	VTX1	VTX2	VTX3	VTX4	VTX5	VTX6	ITKB1	ITKB2	ITKB3	OTKB
R [mm]	12.46		27.89		43.79		240	350	600	1800
Half-Z [mm]	130	130	247	247	374.5	374.5	500.5	715	1001	2900

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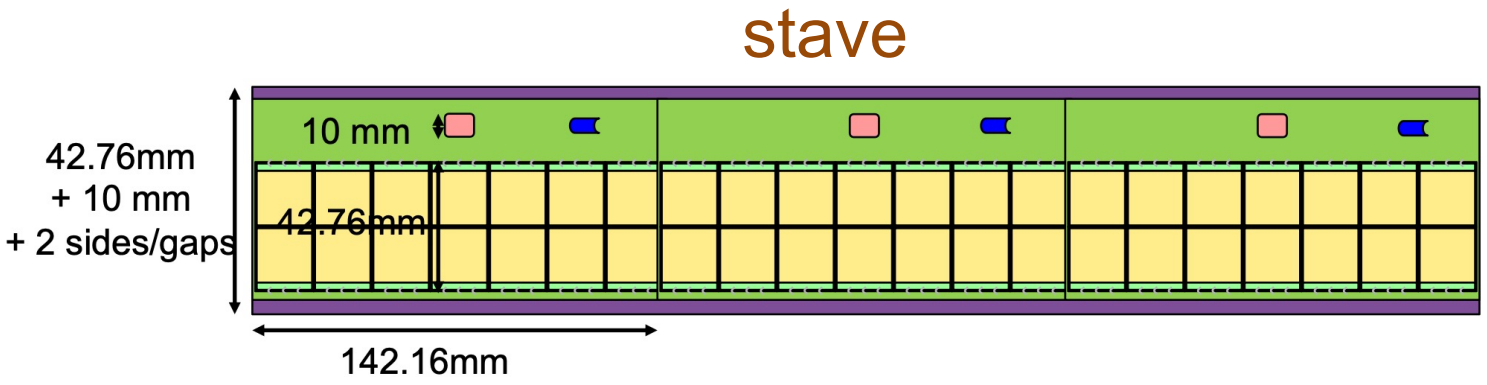
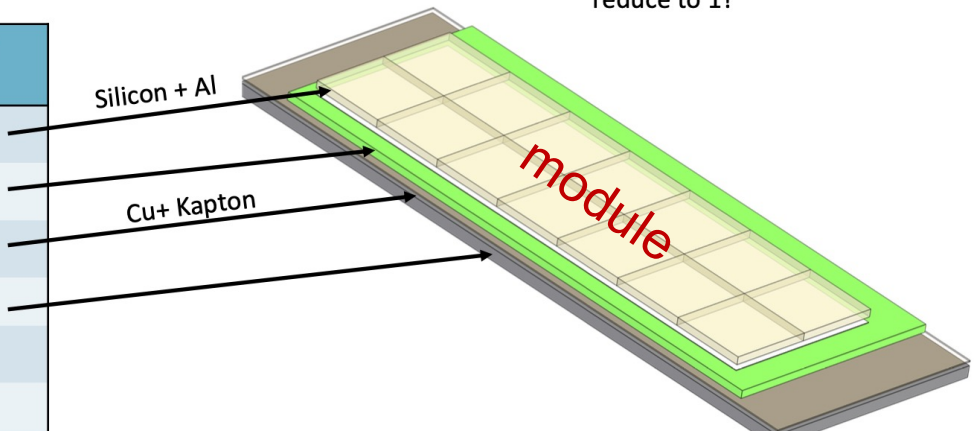
桶部Sensor、Module、和Stave模块的旧方案



lpGBTx: W=9, L=9
Optical connector: W=10, L=20

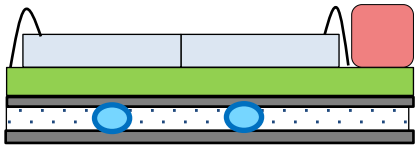
1 lpGBT provides 28×0.32, 14×0.64, or 7×1.28 Gbps **DATA** links
=> 2 lpGBT needed for current bkg rate; may reduce to 1?

	Thickness (mm)	Radiation Length [%X0]
Pixel Sensor	0.150	0.18
HybridFlex	0.200	0.28
Kapton Tape	0.100	0.14
BareStave	4.000	0.21
Optical connector	1.250	0.13
lpGBTx	4.000	0.07

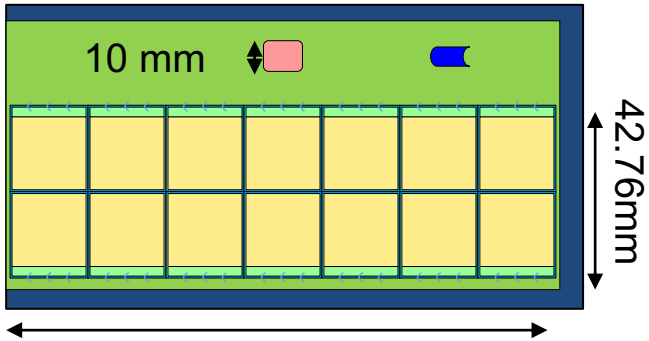


李一鸣(2024.07.10) @ ITK+OTK meeting

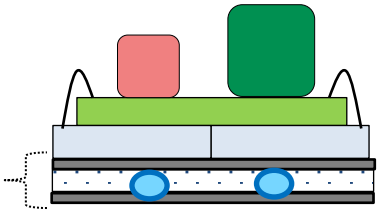
桶部Module的最新方案



42.76mm
+ 10 mm
+ 2 sides/gaps

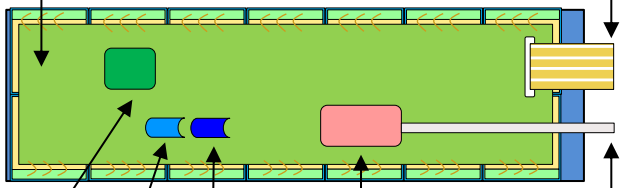


李一鸣(2024.07.23) et al. 最新更新



Supporting & cooling to
be optimized seperately

42.76mm
~~+ 10 mm~~
~~+ 2 sides/gaps~~



DC-DC
Data aggregation

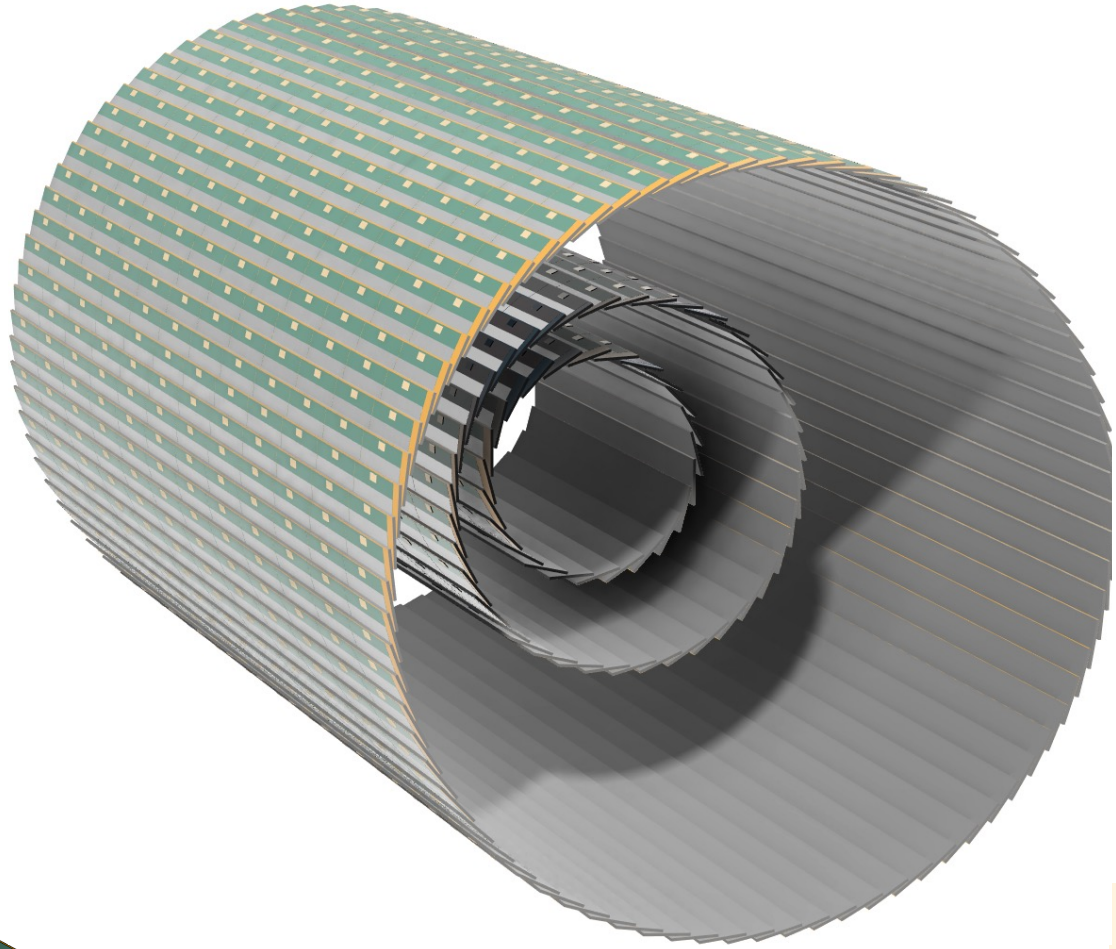
Transmission
(GBTx like)

Optical
convertor

Optical fiber

新方案提高了探测效率，并有助于优化散热和机械结构的设计。

桶部排布的3维几何排布（旧图需要更新）



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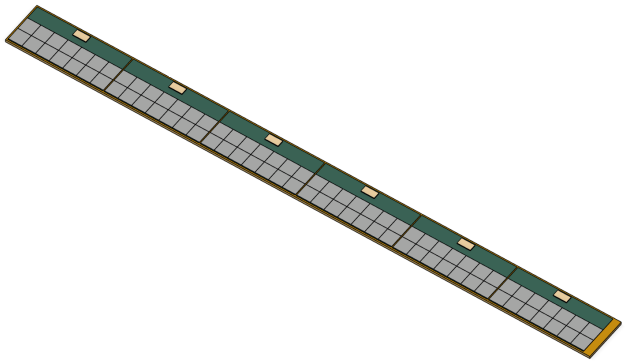

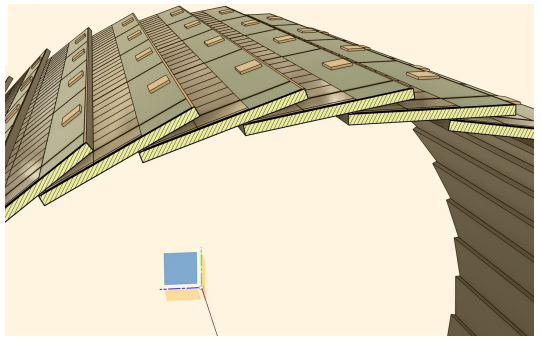

桶部探测元件统计

	Modules/Stave	Staves	Modules	Sensors	Sensor area
ITKB1	7	40	280	3920	1.6 m^2
ITKB2	10	58	580	8120	3.2 m^2
ITKB3	14	96	1344	18816	7.5 m^2
Total		194	2204	30856	12.3 m^2

芯片的总功耗（不包括其他电子学元件）：24.6 KW (200 mW/cm^2)

桶部Stave的机械和散热设计和分析

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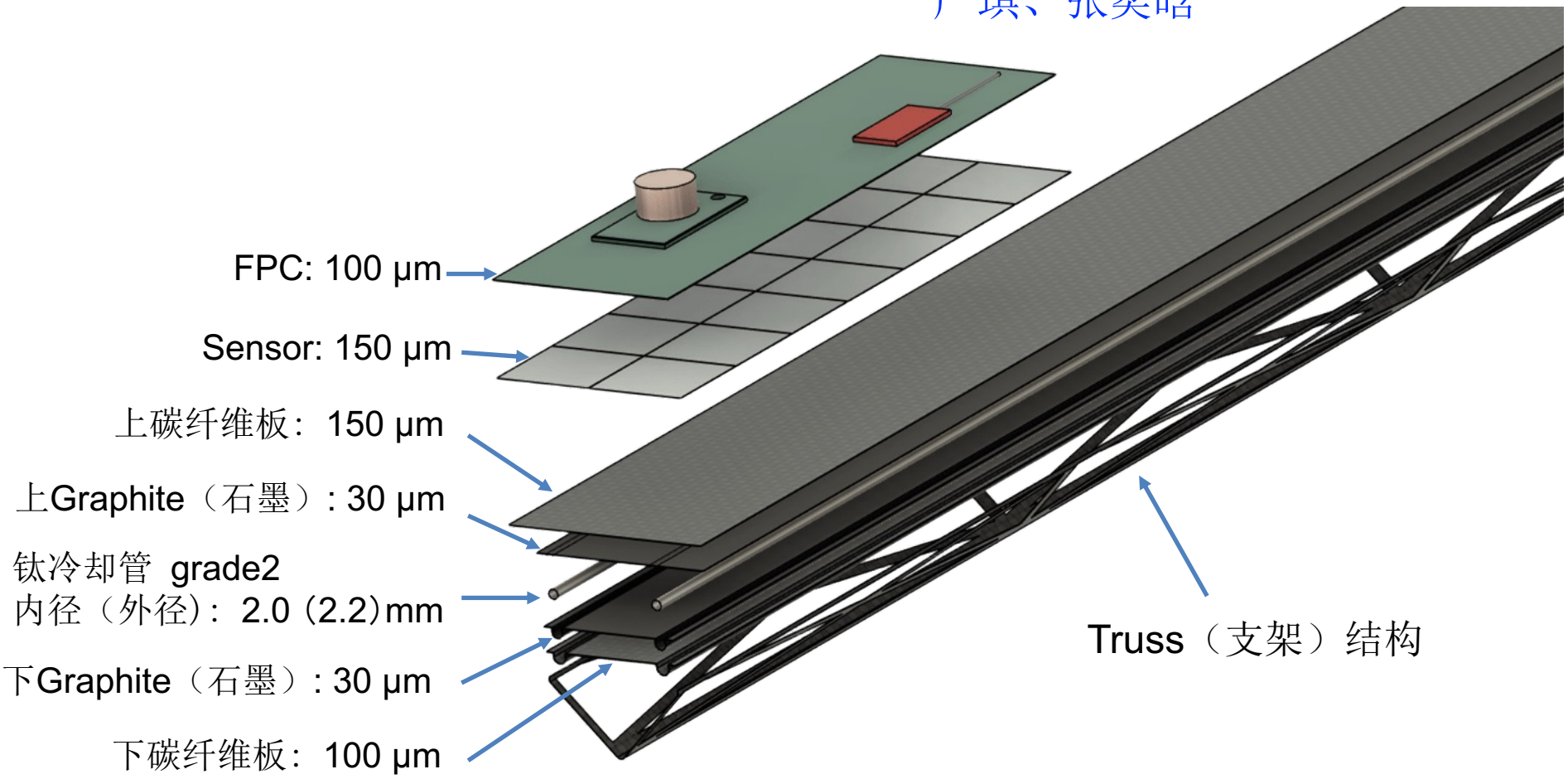

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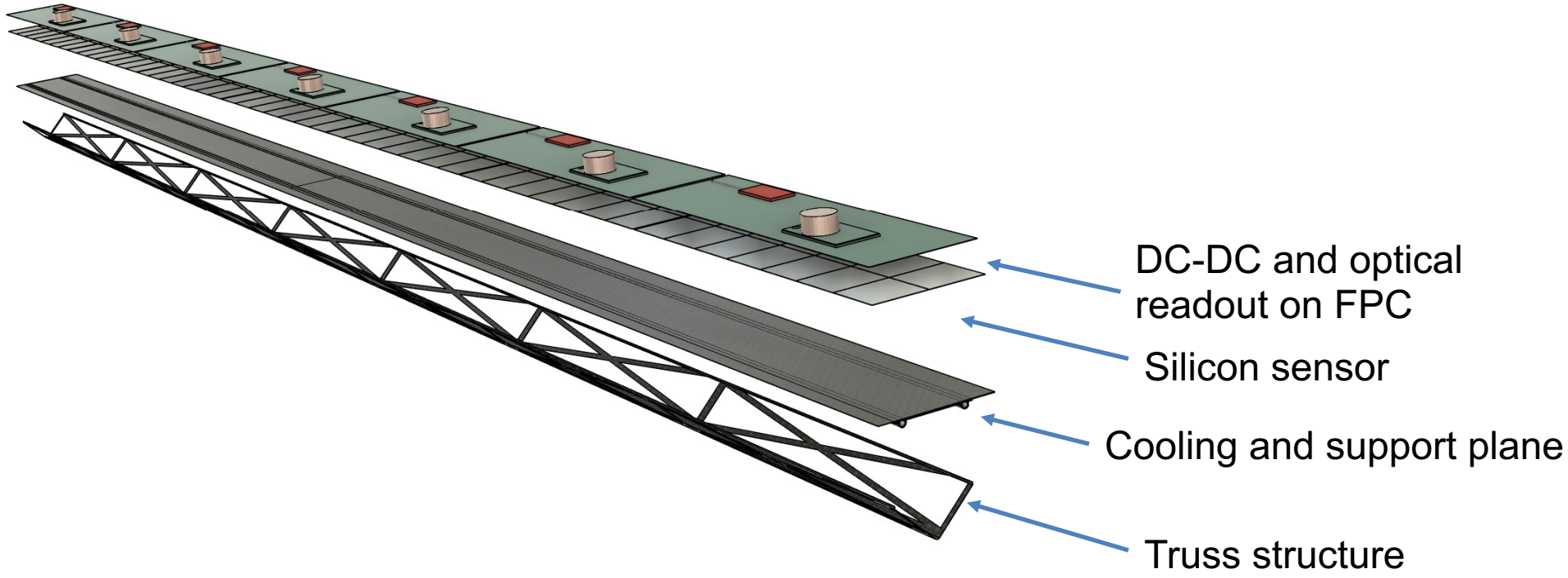
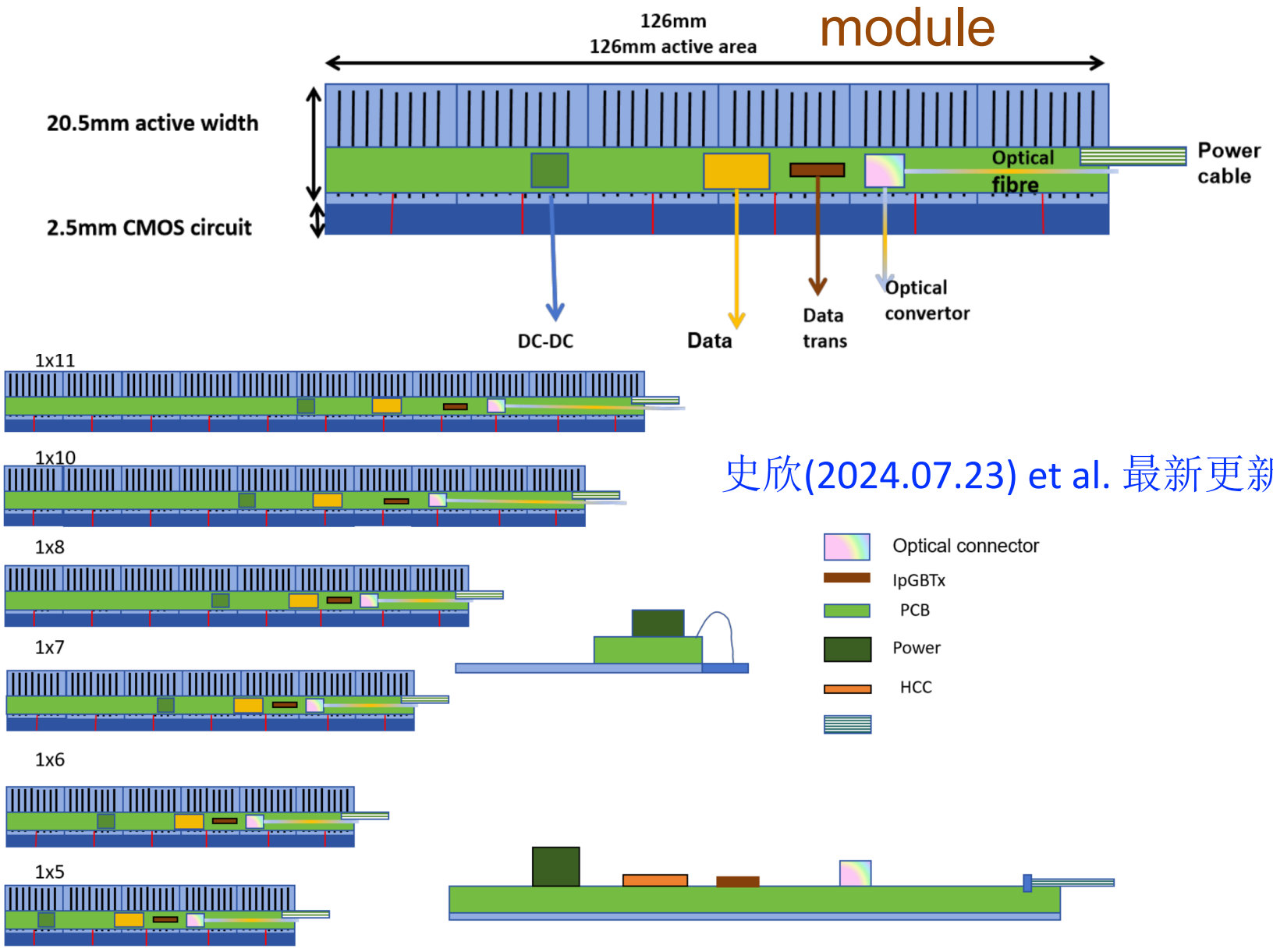


机械和热分析的工作还在进行中.....

端盖Sensor和Module的方案



端盖的最新排布方案 （第一个端盖ITKE1）

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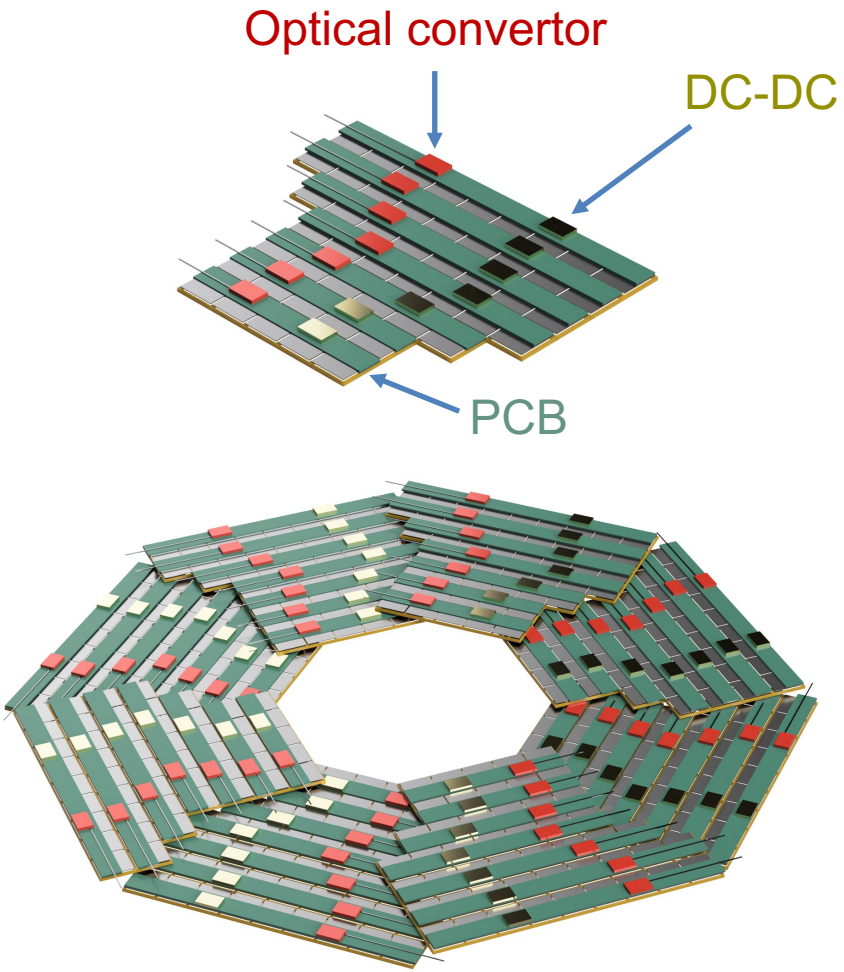
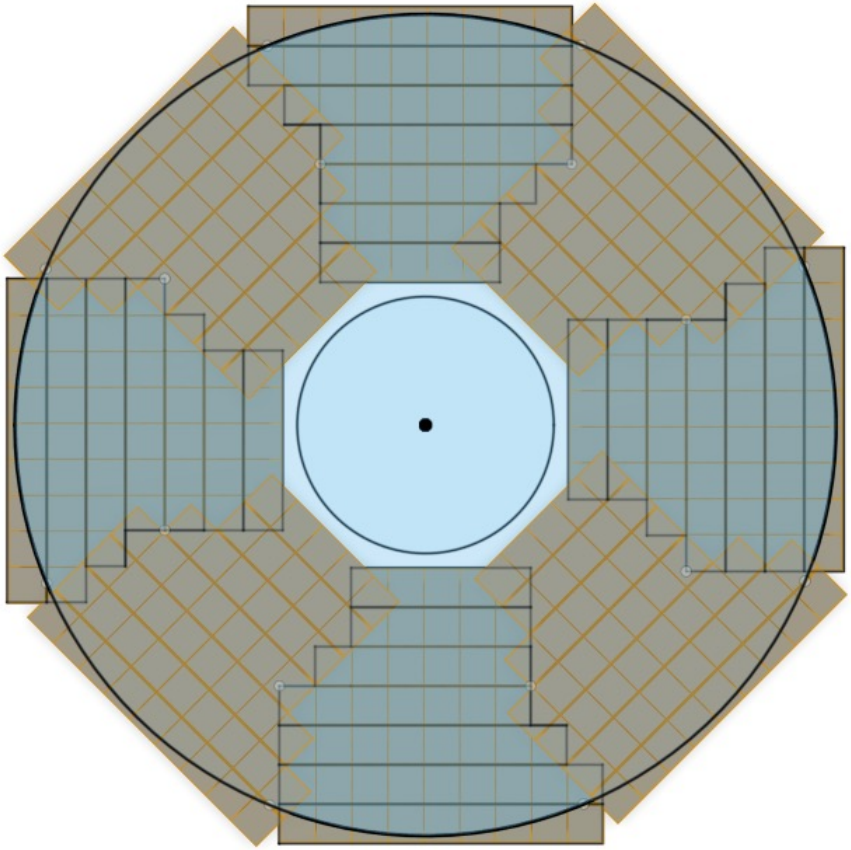
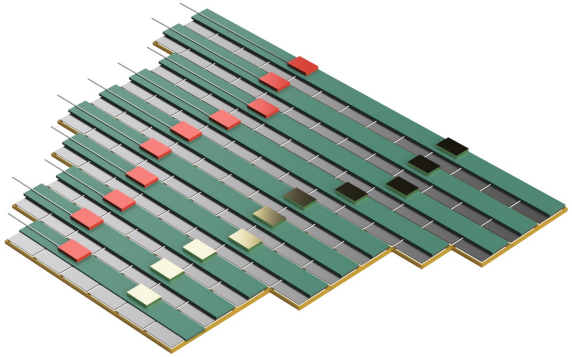
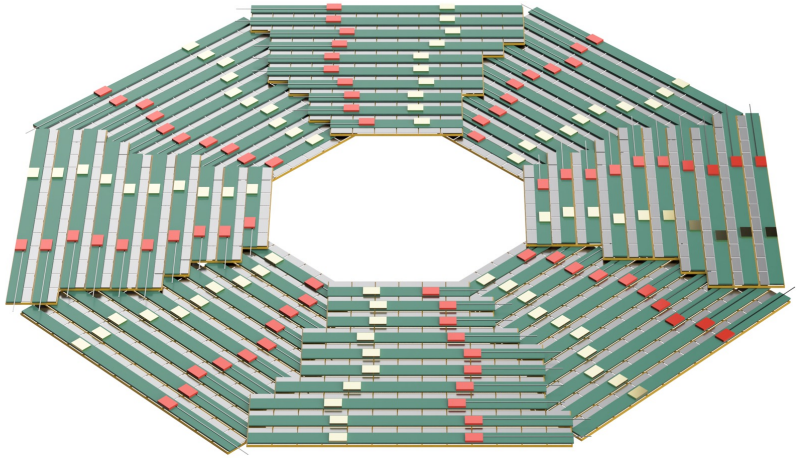


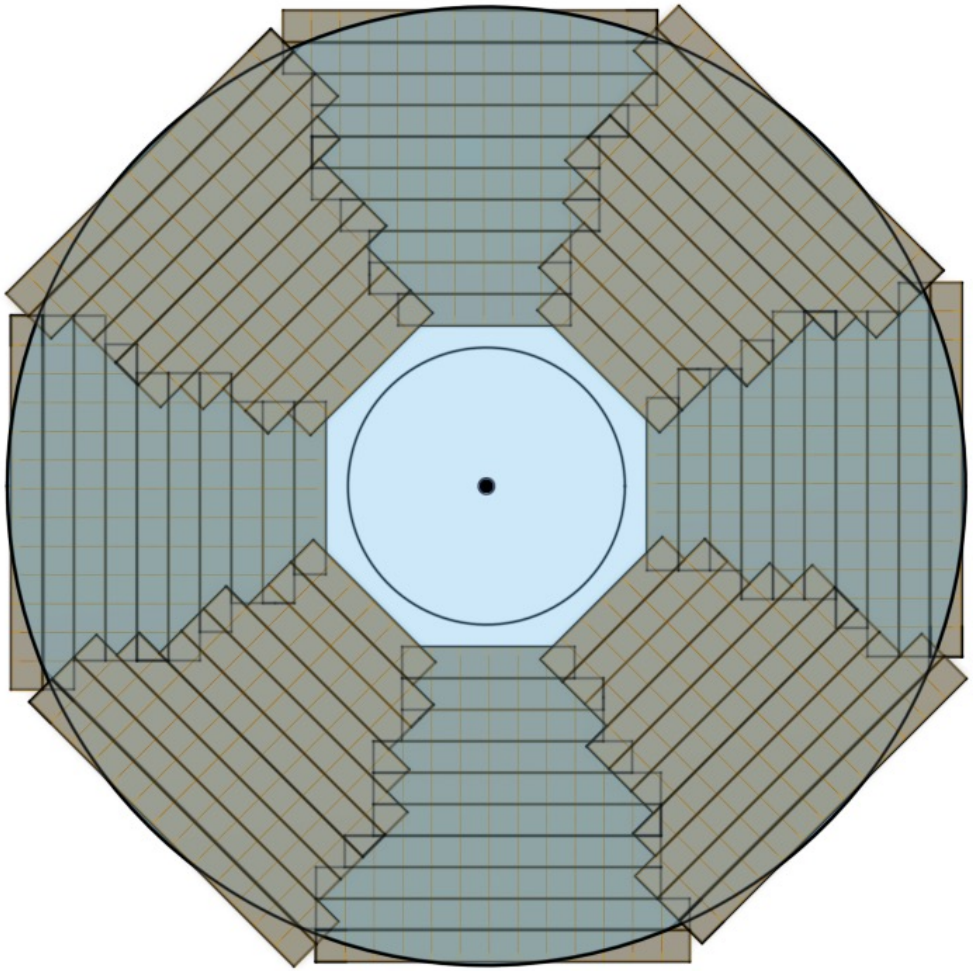


端盖的最新排布方案 （第二个端盖ITKE2）

严琪、骆首栋、史欣

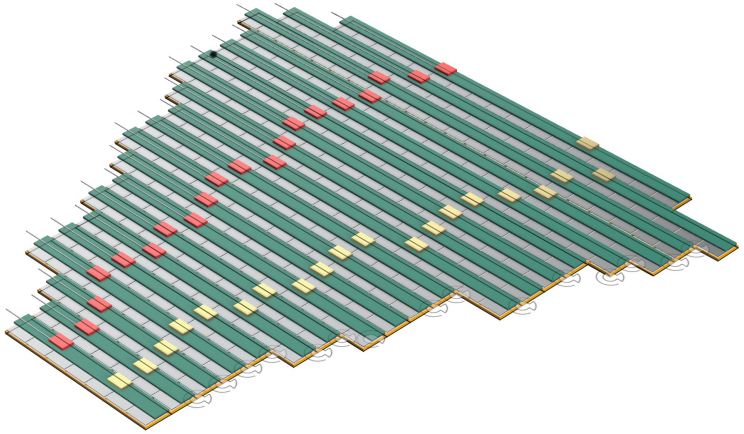


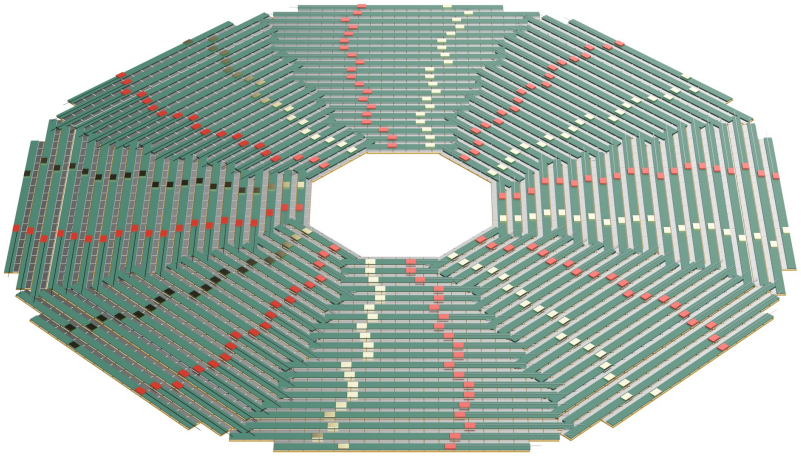


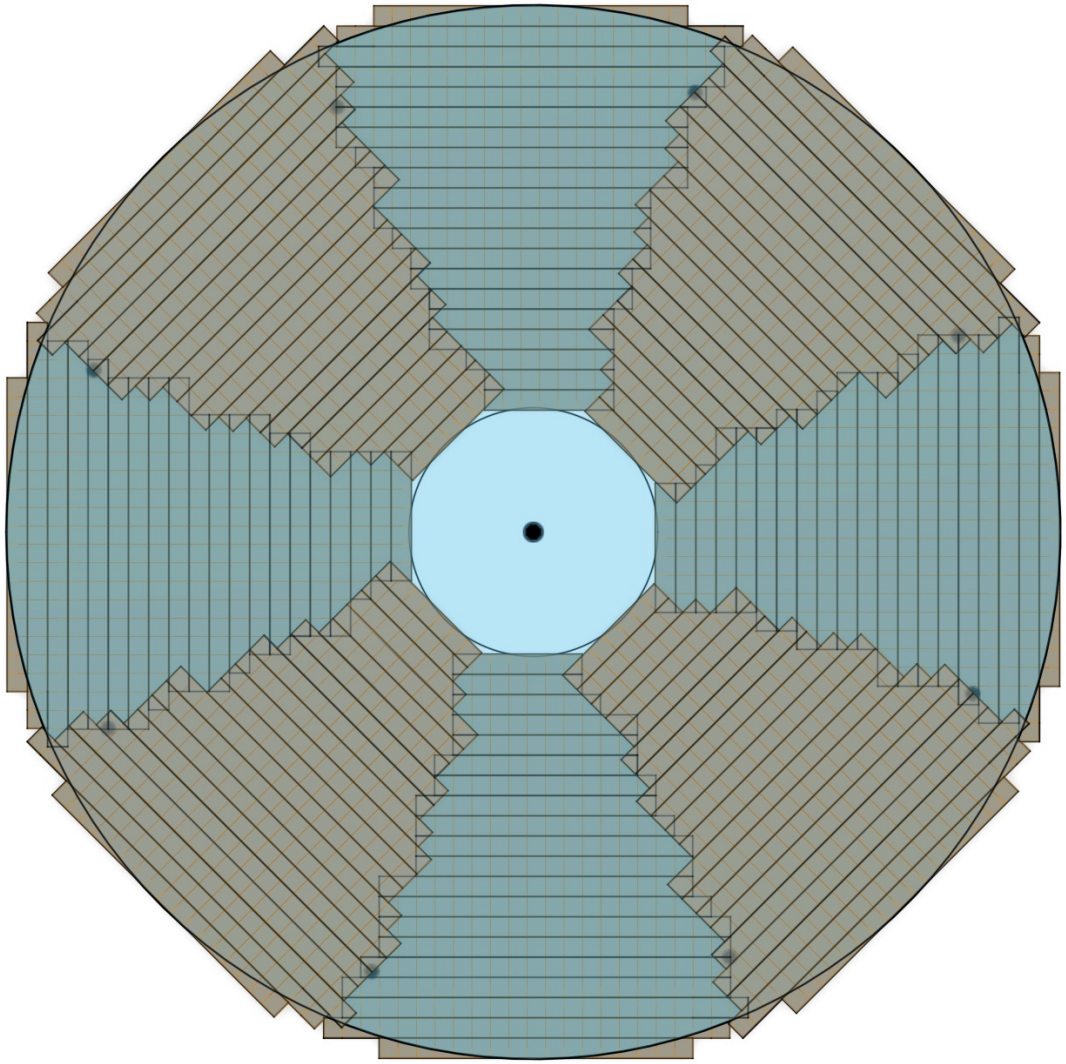


端盖的最新排布方案 （第三个端盖ITKE3）

严琪、骆首栋、史欣







端盖的最新排布方案 （第四个端盖ITKE4）

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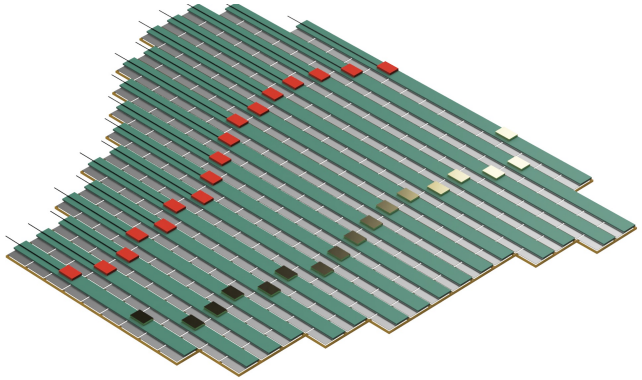

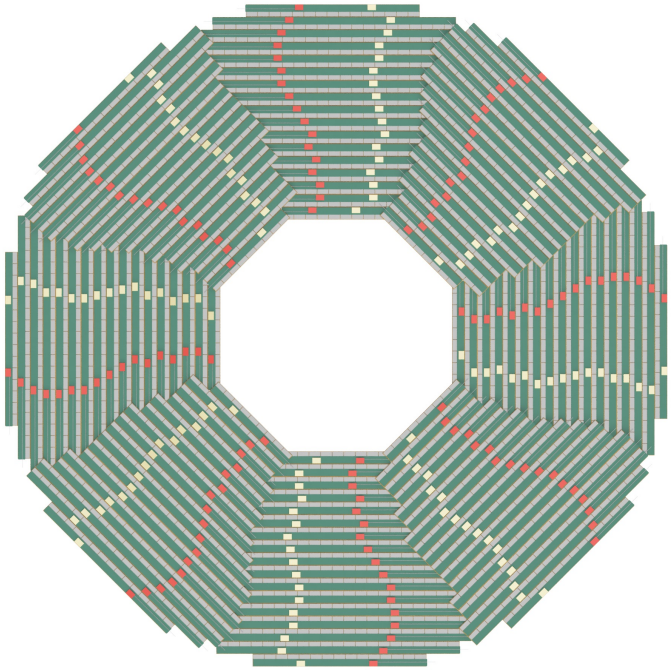

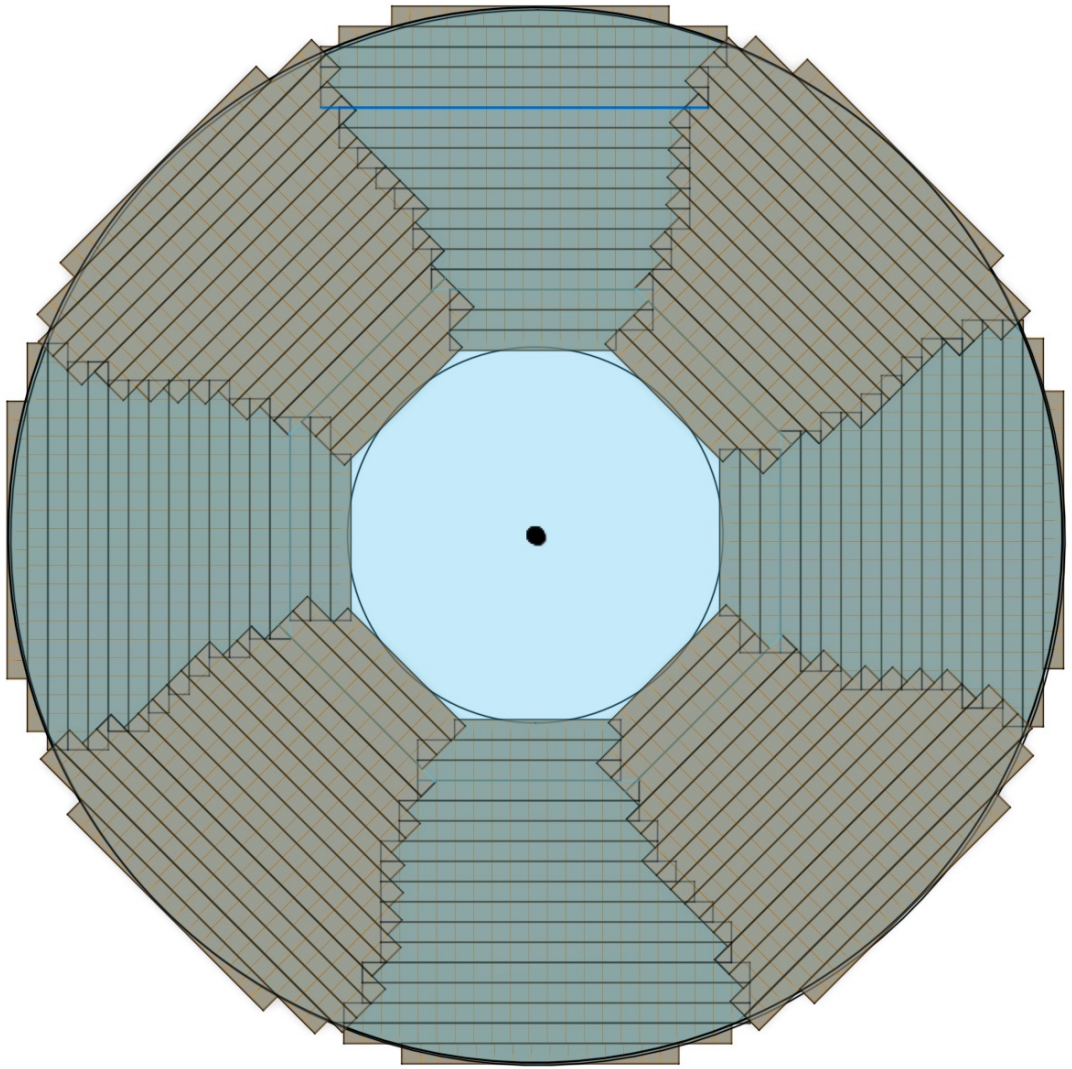

单面Strip Detector端盖的最新排布方案

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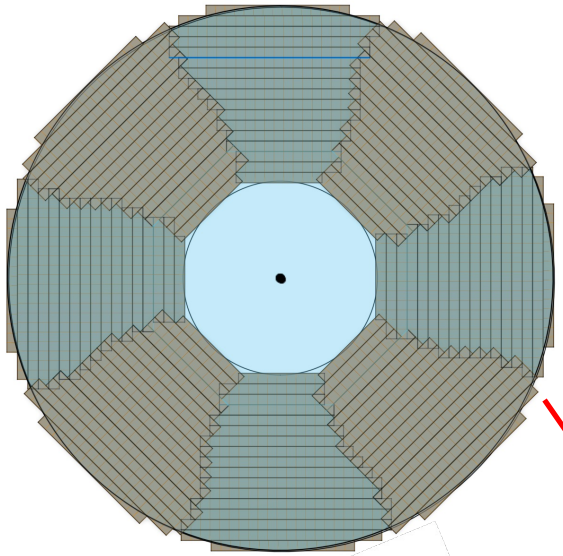
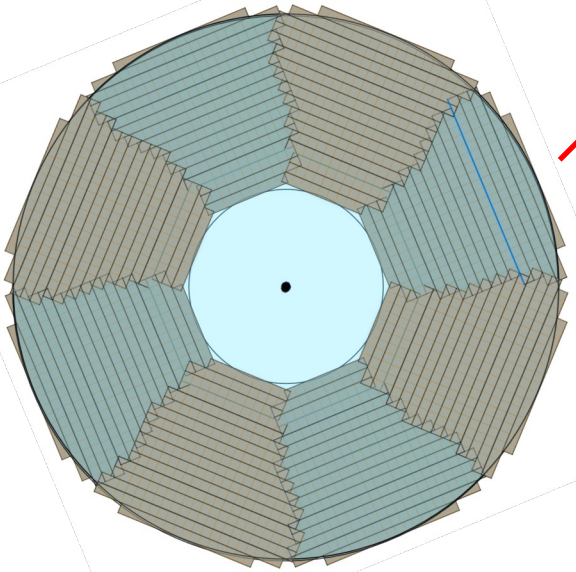
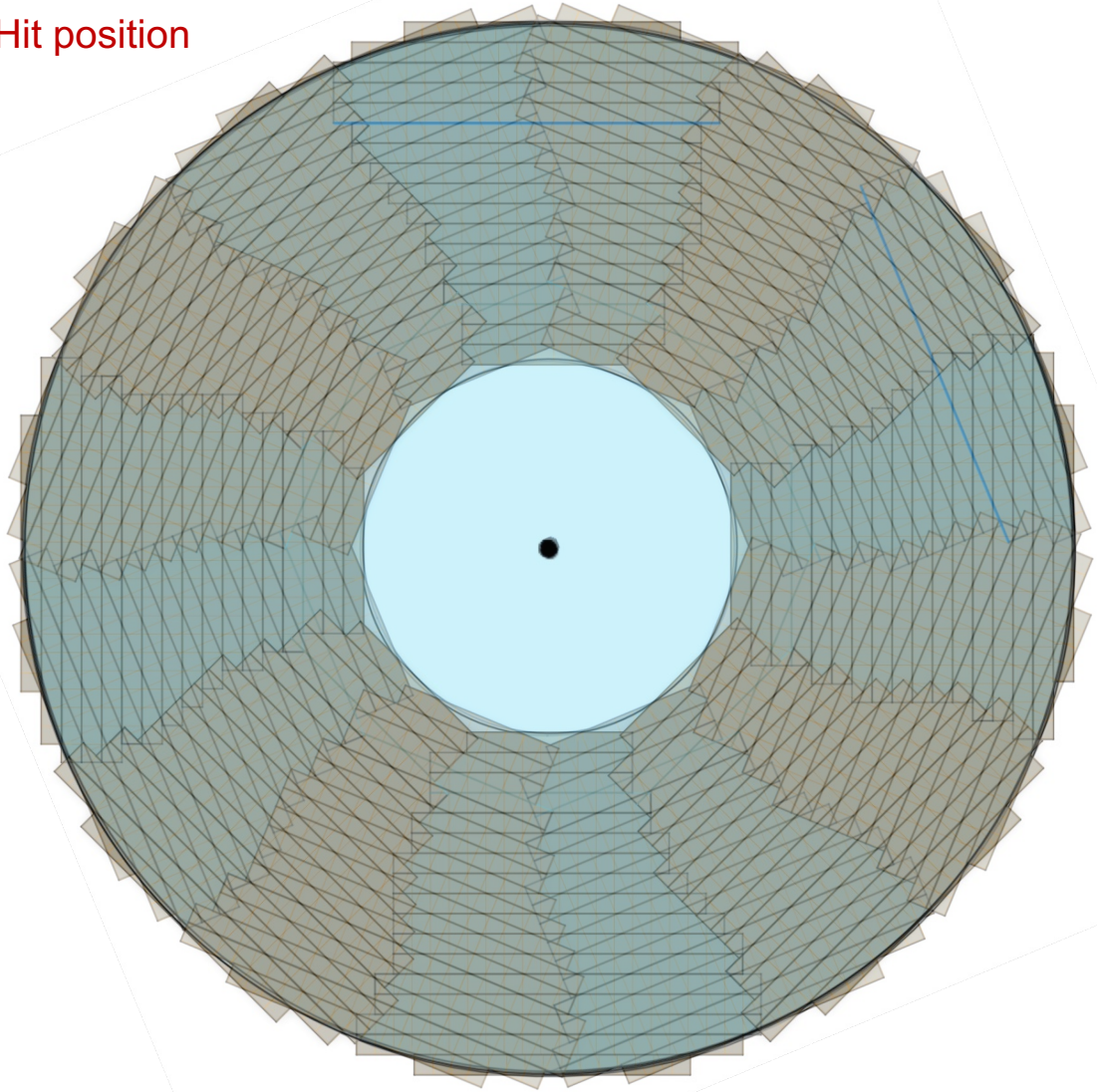


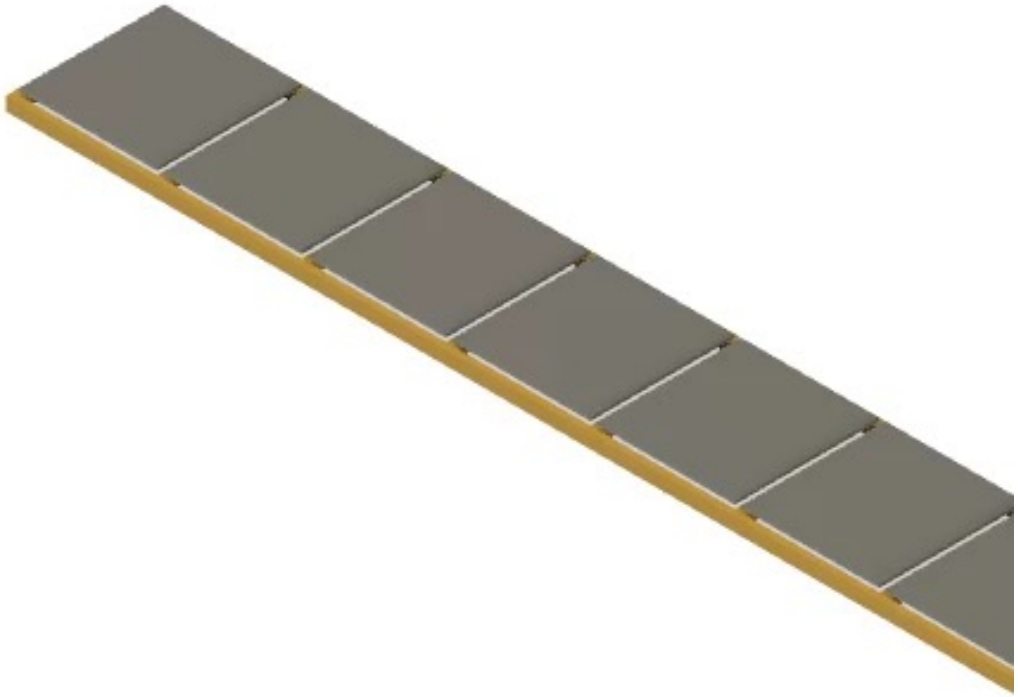
端盖正常半层



端盖22.5°半层



端盖一层



端盖探测元件统计

	Module Types	Sensors	Sensor area	Overlap area Fraction
ITKE1	5	784*2=1568	0.76 m^2	0.138
ITKE2	7	1584*2=3168	1.53 m^2	0.105
ITKE3	15	4784*2=9568	4.62 m^2	0.07
ITKE4	12	4208*2=8416	4.06 m^2	0.029
Total	18	22720	10.97 m^2	

芯片的总功耗（不包括其他电子学元件）：21.9 KW (200 mW/cm^2)

端盖的机械和散热设计和分析

CMOS Chip Parameters

	HVCMOS Pixels (Barrel)	CMOS Strips (Endcap)
Pixel Size/Strip Size	$34 \times 150\ \mu m^2$	20 µm
Chip size	~ $2 \times 2\ cm^2$	2.1×2.3 cm^2 (active area: 2.05x2.05 cm^2)
Array size/Strip number	512 rows × 128 columns	1,024
Spatial resolution	σ_φ ~8 µm, σ_z~40 µm	σ_φ~4.2 µm, σ_r~21 µm
Timing resolution	~3-5 ns	~3-5 ns
Data size per hit	42 bit (14b BXID*, 7b+9b address, 6b TOT, 5b fine TDC, 1 polarity*)	32 bits (10b BXID, 10b address, 6b TOT, other 6 bits)
Event rate / chip	??? (background?) up to 1.28 Gbps	Maximum~0.25Gbps (pair production)
LV / HV	1.2V / >50 V	1.5V / >50V

* To be reduced