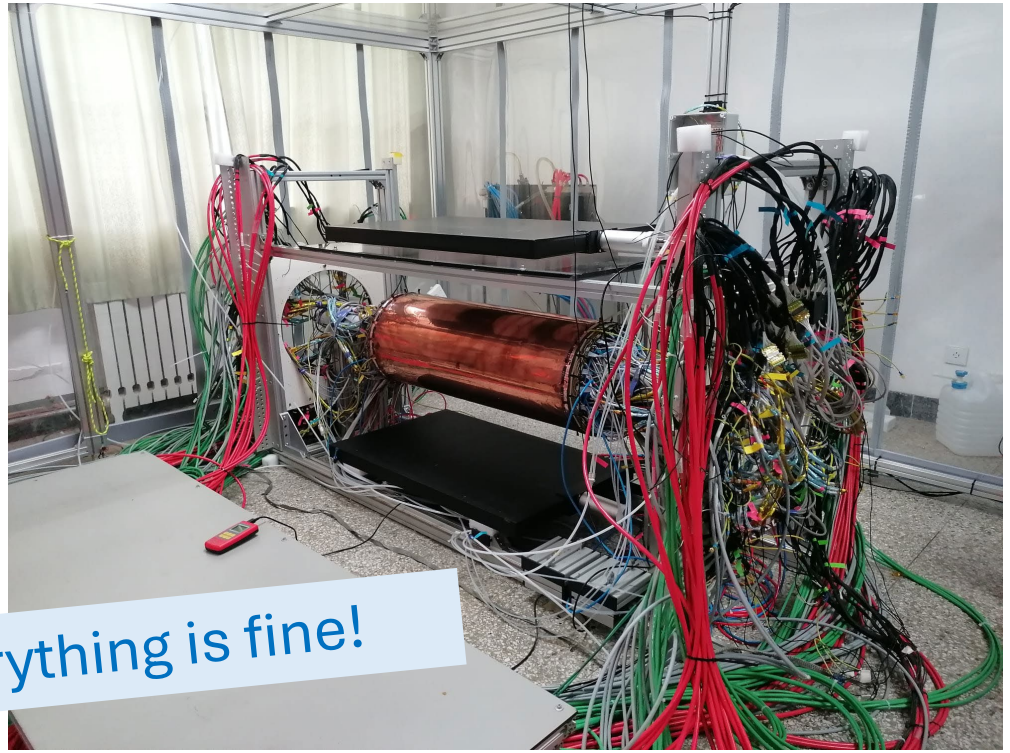
# CGEM operations
# Week 5-12 August

Michela for the WG

# CGEM detector:

- Powered on at operation values
- H from 35% to 70%  ( also depending on the weather outside)
- Ar bottle changed



# CGEM-DAQ

- I had an online meeting with Pawel and Angelo on Thursday, 10.
- Angelo and Pawel agreed on next steps:
  - Pawel is working on changing the firmware of the upper FPGA in the DC BOARD to fulfill the IRQ requirements, i.e. an IRQ is generated every time an event is ready in the data buffer.

  Proposed Changes to Upper FPGA (CGEM_DIAG) in Event Building FSM
  - Angelo is currently on vacation.

  As Gianluigi said at the last meeting, he will not be able to come to Beijing in the next few months due to health problems, but he will work and help us remotely.

They have read Tingxuan's emails and slides, they will comment when possible.

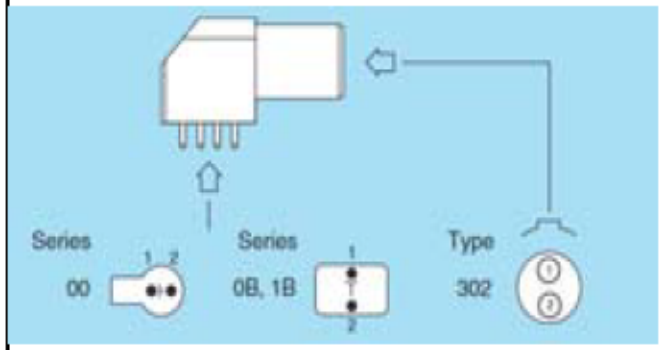
I will organize another meeting and more details will be presented on August 26.

# DAQ : trigger signal test/ first phase


CONN RCPT 5x2

acr 2017-04-20: PLACEMENT NOTE:
place at the front edge of the FCS
"daughter card"

Same logic level



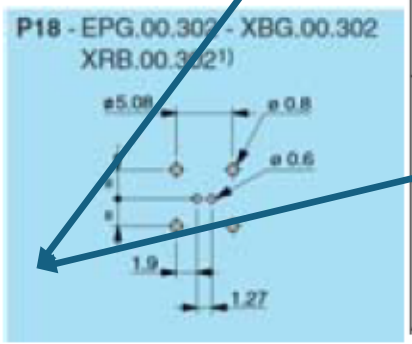




Table 1 Trigger related signals

| Name | Direction | Level | Definition | Comment |
|---|---|---|---|---|
| L1 | To ZDD | +3.3V LVPECL | Level 1 trigger | Width of 8 clock cycles, high effective |
| CHK | To ZDD | +3.3V LVPECL | Check of trigger number | Width of 8 clock cycles, high effective |
| CLK | To ZDD | +3.3V LVPECL | System clock | 41.65MHz |
| FULL | From ZDD | +3.3V LVPECL | Readout memory **almost** full | High effective |

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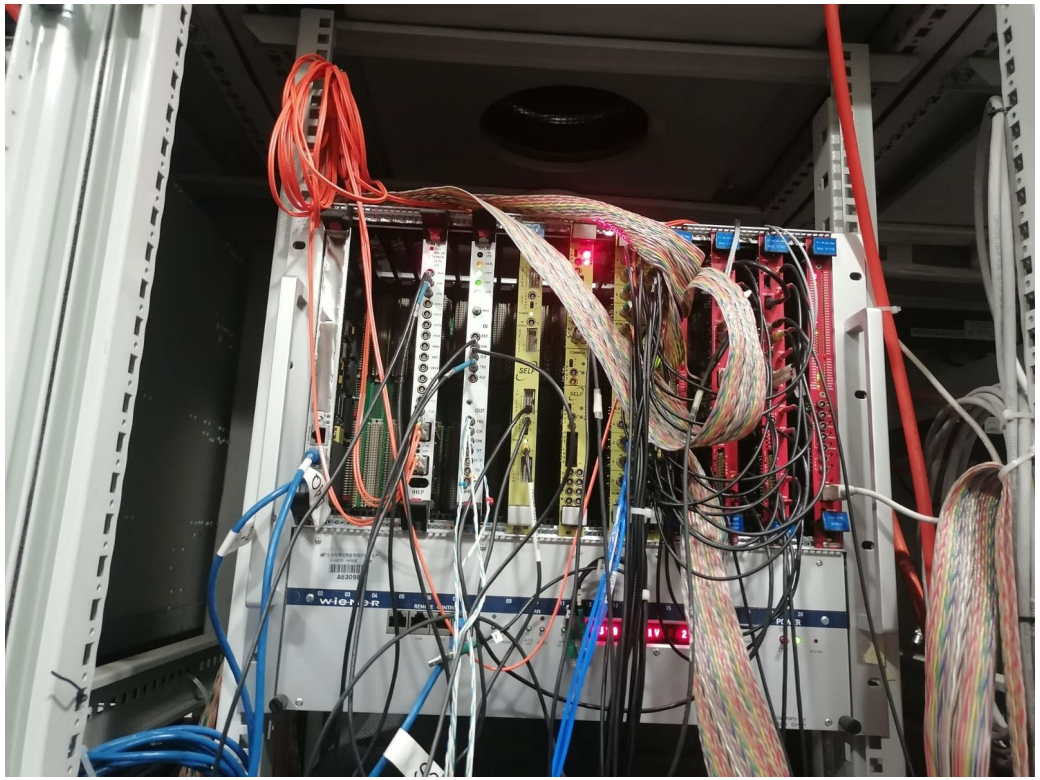
# DAQ : started trigger signal test/ first phase

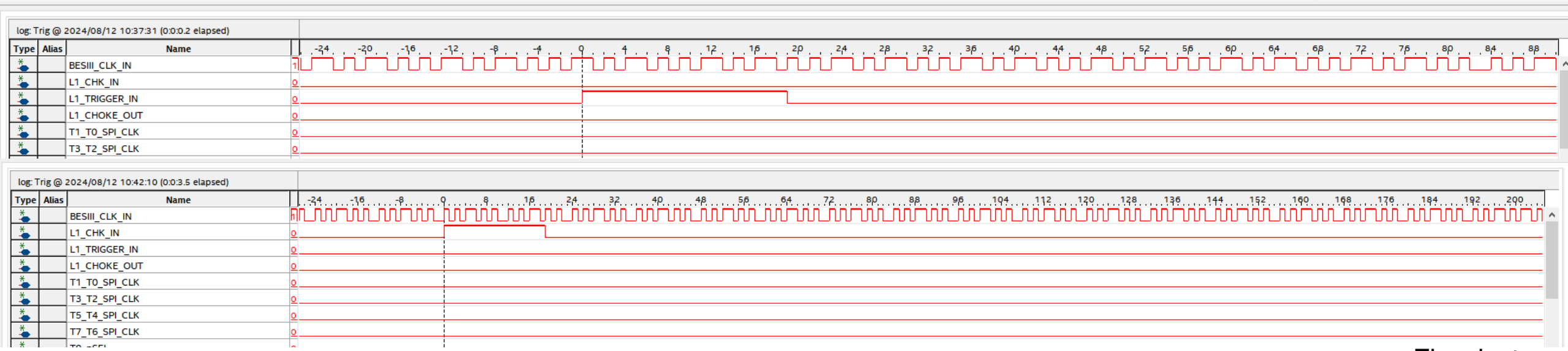



Thanks to
Angelo
Jingzhou
Li
Tingxuan

✓ **Output signals seen @ oscilloscope**

Check CLK, TRG, L1 CHECK signals ~~**in progress**~~
**DONE! Shortly after the meeting**

# ✓ DAQ : trigger signal test/ first phase




✓ **CLK, L1TRG, L1 CHK Signals acquired with SignalTAP using the Fanout MODULE that we use for Cosmic rays data acquisition**

Thanks to Angelo

The spare FANOUT module used until August 12th morning has a malfunction of the JTAG interface.
We will retrieve the spare FANOUT module for the second phase but we need some time because we have to do an HW replacement.

In the meantime, Tingxuan can perform real data acquisition tests (noise data) in 106 : for these tests we can change the TRIGGER rate. I emphasise that only noise data can be also collected in the experiment hall during the second phase of testing, which will follow as soon as we can retrieve the spare FANOUT module.